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DEALING WITH HIGH-RADIATION ENVIRONMENTS

Radiation-tolerant circuits incorporate special processes, circuitry, packaging, and coatings to protect them from the effects of radiation.

Courtesy of NASA

Executive Summary

Today's aerospace systems, space satellites, and nuclear reactors rely heavily on semiconductor technology to control, calculate, communicate, and drive various systems. However, the harsh radiation environment of space, high-altitude flights, and nuclear reactors rules out the use of most commercial- and industrial-grade integrated circuits (ICs) and power semiconductors.

To better match the circuits and systems to the effects of radiation, several different grades of radiation endurance have been defined to ensure proper operation based on the expected exposure to radiation.

The three main classifications include:

- Radiation tolerant for the lightest exposure
- Radiation hardened for moderate-to-heavy exposure
- Space hardened for the most extreme exposure

The three basic classifications of radiation endurance are defined by the amount of radiation that the circuits can tolerate before they stop operating properly. Radiation is specified in terms of total ionizing dose (TID) and single-event upsets (SEUs). TID is a measure of how much radiation will cause the circuit to stop functioning and is specified in kilorads (Si), while SEUs are a measure of how many times radiation causes a bit to change state (see Table 1).

Radiation Tolerance Level	Single-Event Upsets	Total Ionizing Dose	Single-Event Latch-Up
Terrestrial (sub 150k feet)	>50 MeVcm^2/mg		>100
Near Earth Orbit (10 to 1,500 miles)			>100
Deep Space Qualified (beyond 1,500 miles)	37 MeVcm^2/mg	300 krad (Si)	>120

Table 1: Radiation-Hardening Levels

However, at different distances from the earth, the electronic systems are exposed to different types of radiation, and the differing radiation types will affect the various error rates. Thus, knowing the distance of the orbit will determine the level of radiation exposure the circuits can tolerate.

For example, for low-earth orbiting systems (500 to 2,000 km) exposure is dominated by protons and some heavy ions, and exposures of 60 MeV-cm2 /mg can be tolerated. Geosynchronous satellites, orbiting at distances of 35,000 km, can typically tolerate levels of 75-80 MeV-cm2 /mg and SEU levels of 80 to 100 krads(Si). Deep-space probes will be exposed to the most radiation and are often specified to withstand doses of 1 Mrads(Si) and over 80 MeV-cm2 /mg.

The function the satellite/probe performs can also determine the level of radiation protection. For example, a weather satellite or other system that captures images can probably withstand some pixel errors in the images they capture and, therefore, may have a lower level of radiation tolerance. A communications satellite, on the other hand, cannot tolerate errors in the data streams and would have to incorporate higher levels of radiation tolerance.

There are many types of errors that radiation can cause. Some errors are caused by radiation that accumulates in the circuits while other errors are caused by single radiation strikes. This white paper examines a range of radiation protection strategies.

Radiation Protection Goes Beyond the Chip

In addition to protecting the semiconductors from radiation, circuit design techniques at the board level can protect systems from radiation effects such as flipped bits (ones turned to zeros or vice-versa), also referred to as "soft errors." Design techniques and packaging can also mitigate more serious effects such as stuck-at faults and gate punch through.

One approach employs triple redundant circuit paths and use of a voting scheme to determine the correct state (two of the three paths must agree). Additional approaches could just restart the current operation if the redundant paths don't correlate.

As defined in JEDEC publication 133C, a single-event effect (SEE) is any measurable or observable change in state or performance of a microelectronic device, component, subsystem, or system (digital or analog) resulting from the passage of a single energetic-particle. SEEs include single-event upset (SEU), single-bit upset (SBU), multiple-bit SEU (MBU), multiple-cell upset (MCU), single-event functional interrupt (SEFI), single-event latch-up (SEL), single-event hard error (SHE), single-event transient (SET), single-event burnout (SEB), and single-event gate rupture (SEGR).

The most common problem encountered, an SEU, is a temporary change of state that is the result of the free charge created by ionization, in or close to an important node of a logic element (e.g., memory "bit"). The SEU can be cleared if the circuit is reset/restarted, or in the case of a memory device, an error-checking and correction (ECC) circuit can "scrub" the memory.

In memory blocks, the addition of one or more parity bits for each word allows systems to run parity checks or perform ECC. However, the extra bits increase the size of the memory array, and that might limit the overall memory capacity.

The SEU does not permanently damage the functionality of the transistor or circuit. In addition to ECC circuits to correct soft errors, special shielding can be added to minimize the number of radiation particles that impact the circuitry. For high-reliability applications, ECC is a must. Shielding should also be used,

but in many aerospace applications, weight and physical space are trade-off considerations since shielding would add weight and could "bulk up" the system.

Radiation in the form of charged particles and gamma rays creates ionization when they impact a semiconductor. The ionization, in turn, can alter the device performance. The ionization is quantified in terms of the TID and is specified in rad, an absorbed energy of 100 ergs on a gram of material (about a decade ago the rad was replaced by a different unit of measurement—the gray: 1 rad = 0.01 Gy). The energy loss per unit of mass varies from one material to another; thus, the material the dose enters is always included in the unit of measurement [for example rad (Si) or rad (GaAs)].

There are other radiation SEE effects that can inflict permanent damage—SEL, in which the latched circuit will draw a large current and potentially burn out part of the circuit unless countermeasures are included during the circuit design phase; SEGR, in which the radiation causes the transistor's gate to short to the silicon, thus rendering the transistor inoperable; and SEB, which causes the device to fail.

Radiation Tolerance vs. Radiation Hardness

The different levels of radiation resistance provide designers with some guidelines as to which level to use in their particular application. For example, high-altitude aircraft—heights of 25,000 ft to 150,000 ft—and shielded reactors can typically use radiation-tolerant circuits. Such circuits are often specially tested versions of industrial/military-grade components with special coatings and packaging, although some may incorporate special circuit enhancements to further protect them from the radiation. Unfortunately, radiation-hardened technology has been trailing further and further behind state-of-the-art silicon technology in recent years.

The harsher space environment above 150,000 ft (low earth orbit) demands many more "tricks" to ensure the circuits work in the higher radiation environment. Radiation hardening tackles the challenge by modifying both the process used to manufacture the devices, and in many cases, changes to the circuitry, transistor structures, and system architecture to ensure the systems work as desired. The same is true for the deep space applications (from hundreds of miles to billions of miles and beyond), where even more attention has to be paid to internal circuit designs and transistor structures.

Process and Circuit Tricks to Protect Chips

When crafting a custom chip, designers can leverage one of the rad-hard foundries that offer specially developed and dedicated process lines to fabricate rad-hard devices. Their radiation-hardening methodology, rad-hard-by-process (RHBP), employs modified manufacturing processes to improve their ability to withstand radiation.

However, as transistor feature sizes continue to shrink, the cost of developing new RHBP technology nodes became prohibitively expensive. As a result, there are no RHBP technologies available today that are only one or two generations behind state-of-the-art 22-nm commercial technologies. The last “true” RHBP technology node is the 0.15-µm technology offered by Honeywell SSEC and BAE Systems.

Today, the primary radiation-hardening methodology for technology nodes below 0.15 µm is referred to as rad-hard-by-design (RHBD). The RHBD approach leverages an existing foundry process and comprises a collection of radiation-hardening design techniques. Each technique is able to mitigate a certain aspect of radiation effects.

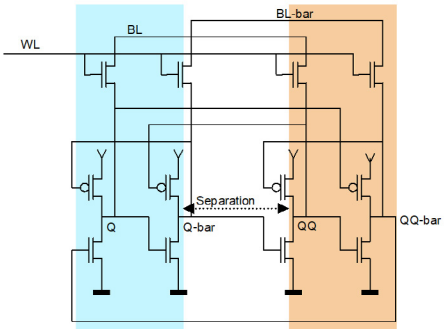


Figure 2: The dual-node 12-transistor memory cell developed by Xilinx for its Virtex 5VQ rad-hard FPGAs uses a physical separation of the two six-transistor nodes to provide better SEU immunity.

These techniques typically depend on specific technology node and the target application and carry certain performance, power, and density penalties. As a result, most RHBD components are typically "quasi" radiation-hardened (rad-tolerant), depending on how many radiation-hardening techniques are applied.

A practical example of the RHBD approach can be seen in the Virtex-5QV family of field-programmable gate arrays (FPGAs) developed by Xilinx. The FPGAs, based on a 65-nm process with copper metallization, use RHBD techniques to lower SEU susceptibility on key memory elements. In particular, the dual-node configuration memory cells require a minimum charge collection at two intentionally widely spaced nodes—that achieves about 1,000x improvement over the earlier space-grade Virtex-4QV series FPGAs.

The use of a 12-transistor dual-node static memory cell rather than the typical 6-T static RAM cell in the configuration memory array eliminates the main source of errors previously seen in the various architectural blocks. Thus, the SEU rate is a low 3.80E-10 upsets/bit/day for a system in geosynchronous orbit at a distance of 36,000 km from earth. The FPGAs can also withstand SELs and TIDs of over 1 Mrads(Si).

Symbol	Description	Min	Typical	Max	Units
TID	Total Ionizing dose, Method 1019, dose rate 300 rad (Si)/sec	1	–	–	Mrad (Si)
SEL	Single-event latch-up immunity: heavy ion linear energy transfer (LET) threshold	100	–	–	LET (Mev-cm^2/mg)
SEFI	Single-event functional interrupt GEO 36,000 km typical day	–	2.76E-07	–	Upset/device/day
SEU_{CFG}	Single-event upset in configuartion memory; GEO 36,000 km typical day. TOtal bits: 35 M	–	3.80E-10	–	Upsets/bit/day

Table 2: Xilinx Virtex-5QV Radiation Tolerances

To protect data stored in memory, Xilinx designers also incorporated an enhanced ECC block. The ECC circuit includes an optional, automatic, write-back feature so that upsets are corrected even when only reading the (corrected) data. Hamming-code-based ECC is well known to be an effective way to prevent system errors in the presence of a few random upsets. The write-back feature makes it easier to prevent upset accumulation, which would eventually overwhelm

the ECC. Additional hardening against SEU and SET incidents was added to the configuration and JTAG control logic by employing triple module redundancy; control registers have independent and redundant error detection and correction circuits for autonomous state correction.

In the past, the design of radiation-tolerant/hardened semiconductor devices often limited the complexity of the circuits that could be implemented due to larger process nodes and transistor structures to prevent radiation upsets and additional circuitry to catch errors caused by radiation. Advances in process technology, as well as the use of isolation technologies such as silicon on insulator (SOI) and trench isolation, allow designers to implement more complex chips and much more functionality on the system boards they craft.

One example of a radiation-hardened technology is the CMOS7 process developed by Sandia National Laboratories. The process, based on an SOI structure formed by a buried oxide layer and five levels of metal interconnect, allows designers to craft custom, high-reliability, application-specific ICs (ASICs) that include digital, analog, or mixed-signal functions.

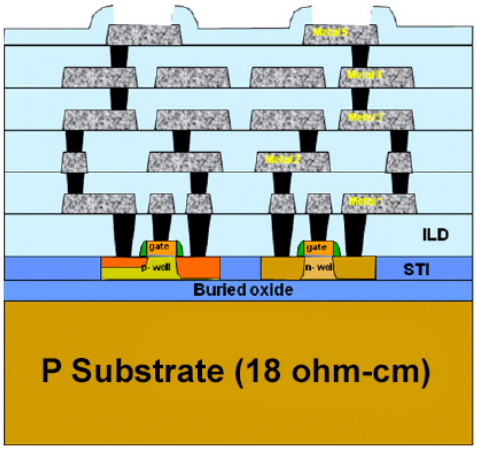
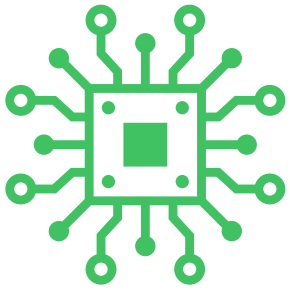


Figure 3: The CMOS7 radiation-hardened process from Sandia National Laboratories employs a five-metal layer, 350-nm process that uses a buried-oxide layer to isolate the circuitry from the substrate.

Employing 350 nm geometry, the process doesn't offer the highest density or performance, but the larger geometries allow better device matching for analog functions, higher supply voltages, and broader signal dynamic range vs. smaller geometry processes. Additionally, shallow-trench isolation allows



critical circuit sections to avoid interference from adjacent circuits. Sandia also offers two structured ASICs that consist of prefabricated silicon but are metal-layer configurable, the Eiger ViArray for digital systems and the Whistler ViArray for mixed-signal applications.

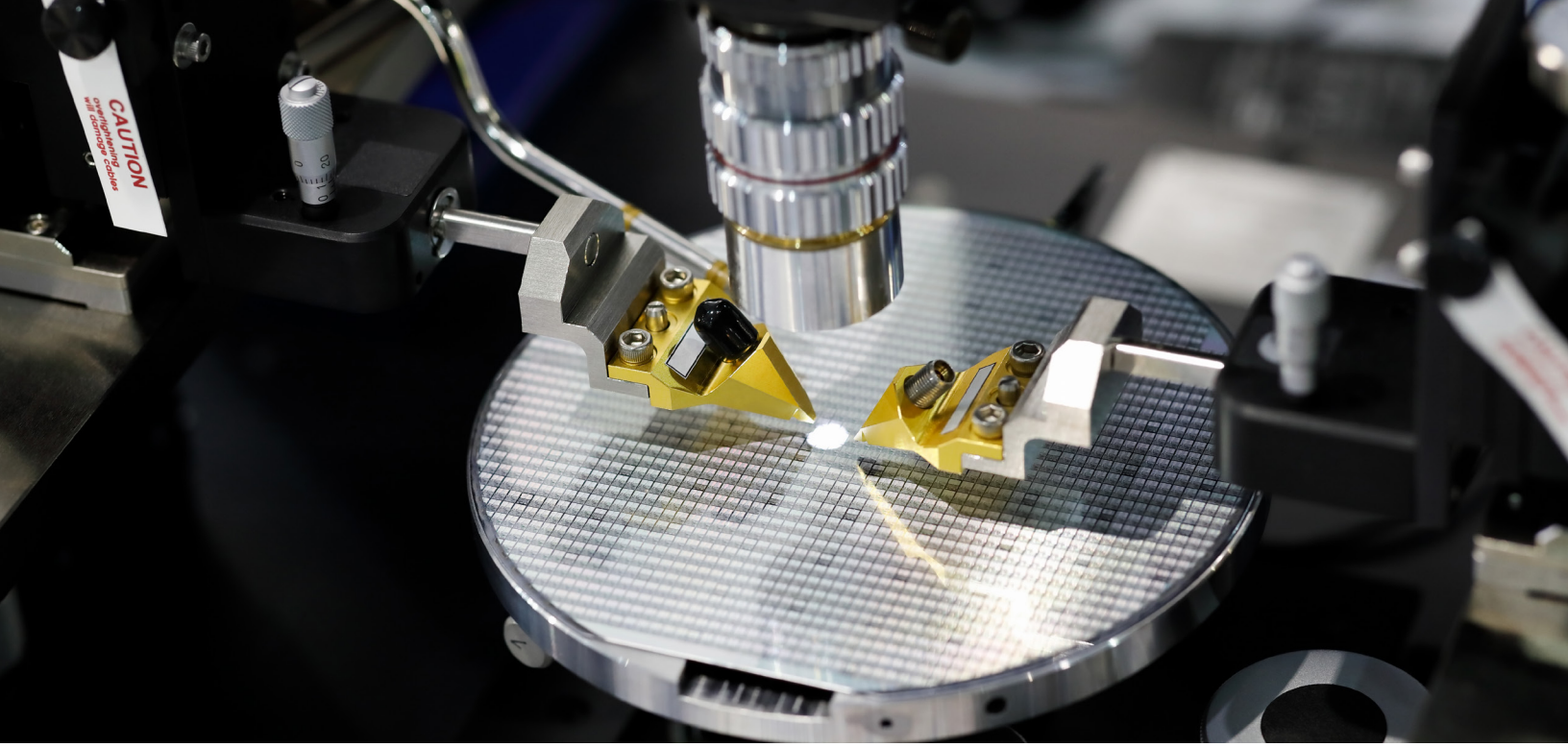
Both bulk and SOI CMOS are subject to the effects described above. SOI is often employed as a specifically radiation-hard technology because of its resistance to transient radiation effects, primarily latch-up due to photocurrents developed at high intensity bursts of radiation (>106 -107 rad/s) typical of nuclear detonations. In some applications, an epitaxial layer deposited on top of the bulk silicon can also be used to prevent latch-up. However, the addition of the epi layer increases the wafer cost.

Although SOI can provide superior device speed because of reduced stray capacitance, this technology is not inherently more resistant to radiation in many applications. If anything, the additional oxide interfaces tend to complicate matters. At this time, most radiation-resistant CMOS processes are on bulk silicon.

Silicon wafers are typically fabricated such that the surface layer is n-type silicon. If the epi layer is not added to the wafer, isolation structures are required to prevent unwanted cross-coupling between devices.

There are three basic techniques that designers can use to prevent the cross-coupling:

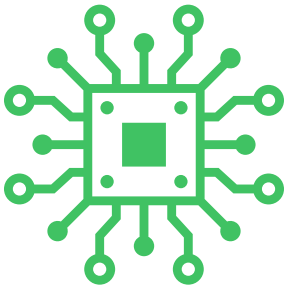
1. Junction isolation, where reverse-biased pn junctions provide both ohmic and capacitive isolation;
2. Lateral oxide isolation, where oxide layers with carefully controlled interface properties deplete the adjacent silicon of mobile charge, thus isolating the devices on either side of the oxide; and
3. Buried oxide isolation, which creates an SOI structure to isolate the devices in the layer of the silicon above the oxide layer. This is often accompanied by shallow trench isolation, which uses trenches etched in the silicon above the oxide layer to isolate the circuitry formed in the silicon layer.



These three techniques have been used for many years. They do, however, have some trade-offs associated with their use. For instance, they add extra steps in the process flow and occupy additional area. The additional area consumed by the isolation techniques limits the complexity of the circuits; therefore, less complex functions could be integrated.

Often, system designs will incorporate multichip modules (MCMs)—also referred to as system in modules, or SIMs—to achieve higher levels of integration and improve performance. However, in a high-radiation environment, there are several concerns that should be addressed:

- The chips or other components used for the circuits can come from a variety of suppliers ranging from qualified sources of radiation-hardened ICs or discrete devices, where the radiation response of the devices is specified, to high-volume commercial suppliers that provide no guarantees concerning device hardness. Therefore, a careful selection of the components must be done.
- The radiation response of an MCM/hybrid must be addressed as a subsystem rather than as just a group of components. It is possible that even though a component operates within its radiation specifications, radiation response of a die can cause the malfunctioning of the entire MCM/hybrid due to the interaction of the interconnected components.



- In very high dose rate environments, the actual MCM/hybrid structure (lands, grooves, etc.) can become a source of radiation-induced current, further impacting individual die response.
- The actual hybrid/MCM construction methods should also be considered (e.g., ground connections, die attach, etc.) since they can influence the overall package and individual die response.

Depending on the expected life of the product launched into space, designers may be able to opt for the lower-cost radiation tolerant products if the expected life is several months to several years. Deep-space applications, though, often last for decades and would require the fully hardened space-qualified products.

Space-qualified and radiation-tolerant chips from vendors such as Amphenol, Xilinx, ITT Cannon, TE Connectivity, Renesas, Vishay, Samtec, and many other suppliers provide a range of circuit functionality—FPGAs, microprocessors/microcontrollers, switches, A-D converters, operational amplifiers, memories, and still other functions. Board and system suppliers also provide many functions such as single-board computers, I/O cards, communication subsystems, and still other subsystem products.

The higher levels of integration at the chip level translate into higher complexity system boards that provide more functionality while consuming the same or less power and delivering higher performance. Distributors such as Avnet and others also offer off-the-shelf radiation-hard/tolerant components and boards that can meet the demands of most high-reliability systems.

Rakesh Trivedi and Usha S. Mehta, "A Survey of Radiation Hardening by Design (RHBD) Techniques for Electronic Systems for Space Application," *International Journal of Electronics and Communication Engineering & Technology*, Vol. 7, No. 1, Jan-Feb. 2016, pp.75-86.