Integrated Absolute Pressure Sensor (IAPS) with SPI Interface E524.71

PRODUCT PREVIEW – July 11, 2017

RoHS compliant

Features

- Fully integrated and compensated pressure sensor
- Measurement range of absolute pressure: 40 … 115 kPa
- Full thermal compensation to accuracy ±1.0 kPa
- Digital SPI data interface provides measurement, diagnostic, controls, and ID-data:
  - pressure output, 16-bit resolution
  - temperature output (int. sensor), 16-bit resolution
  - sensor diagnostics (state-of-health)
  - power-down control: Sleep Mode selected via SPI
  - unique device ID
- Two 16-bit ADCs for acquisition of pressure and temperature inputs; pressure acquired @ 20 kS/s
- Diagnosis of sensor, sensor supply and wiring, and NVM check-sum supervision at power-on
- Sleep-mode with low current consumption
- Supply voltage 3.3V or 5V in the same device
- Large temperature range -40 ... + 125°C

Applications

- Automotive applications
- Industrial applications
- Medical applications

General Description

The E524.71 is an integrated absolute pressure sensor (IAPS) for barometric air pressure measurement (BAP). It includes a piezo-resistive pressure bridge and a signal processing IC, which performs amplification and thermal compensation of the pressure sensor output to provide a linear, thermally stable signal output.
The sensor delivers calibrated output data (pressure and temperature) at an SPI interface.
The calibrated transfer characteristic maps the nominal input pressure range linear to a defined fraction of the positive digital number range. Also the temperature from an on-chip sensor or diagnosis data can be read via SPI.

Sensor specific calibration data, configuration and product ID are stored in an embedded NVM.

Ordering Information

Ordering Code	*Pressure Range*	*Package*
E524.71A53D232	40 - 115 kPa	SO8n *

* cover with pressure inlet opening (see below)

Typical Operating Circuit

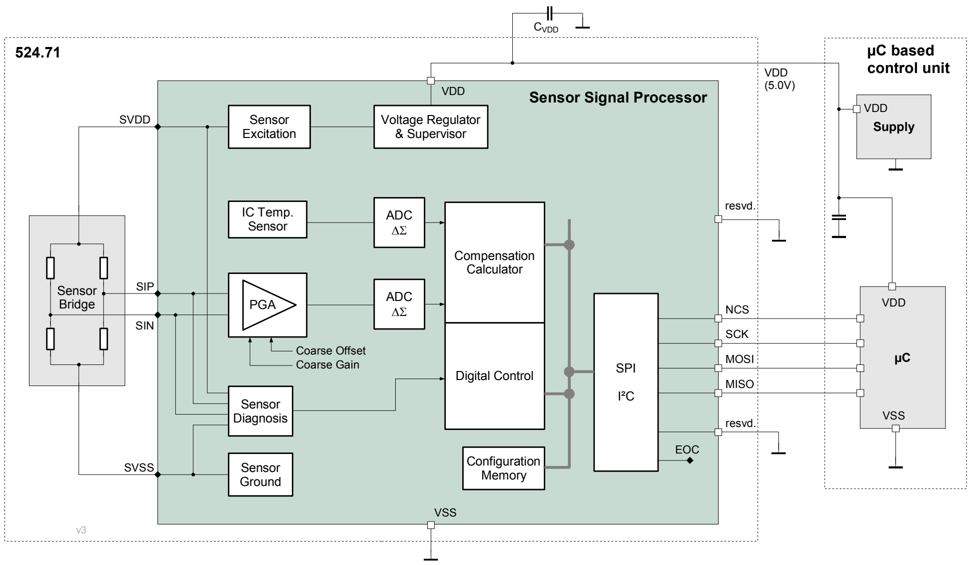

Figure 1: Typical application circuit

This document contains information on a product under development. Elmos Semiconductor AG reserves the right to change or discontinue this product without notice.

Functional Diagram

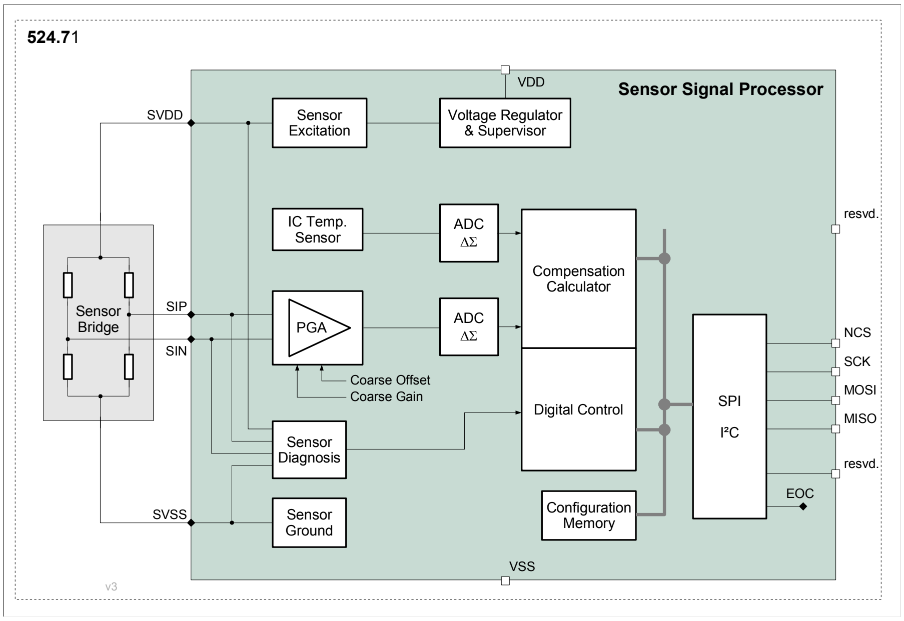

Figure 1: Functional Diagram

Pin Configuration

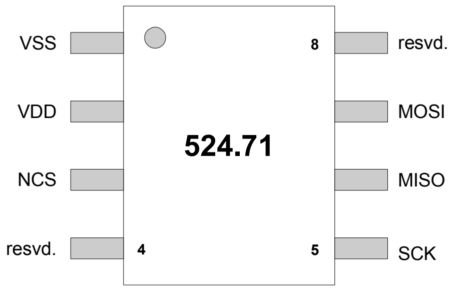

Figure 1: Pin Configuration

Pin Description

No.	Name	Type	Description
1	VSS	S	Ground (Negative device supply)
2	VDD	S	Supply voltage
3	NCS	D_I	SPI chip select (active low)
4	resvd.	-	reserved, connect to VSS (on PCB)
5	SCK	D_I	SPI clock input
6	MISO	D_O	SPI data output
7	MOSI	D_I	SPI data input
8	resvd.	-	reserved, connect to VSS (on PCB)

Note: A = Analog, D = Digital, S = Supply, I = Input, O = Output, B = Bidirectional, NC - not connected

1 Absolute Maximum Ratings

Stresses beyond these absolute maximum ratings listed below may cause permanent damage to the device. **These are stress ratings only; operation of the device at these or any other conditions beyond those listed in the operational sections of this document is not implied.** Exposure to absolute maximum rated conditions for extended periods may affect device reliability. All voltages referred to VSS. Currents flowing into terminals are positive, those drawn out of a terminal are negative.

Table 1-1: Absolute Maximum Ratings

No.	Description	Condition	Symbol	Min	Max	Unit
1	Supply Voltage		VDD	-0.3	6	V
2	Digital IO voltage		$V_{IO,DIG}$	-0.3	VDD+0.3	V
3	Max. digital IO current (DC)		$I_{IO,DIG}$	-10	+10	mA
4	Ambient pressure		p_A	1	600	kPa
5	Junction Temperature		T_J	-40	130	°C
6	Storage temperature		T_{STG}	-40	125	°C
7	Power dissipation	$T_A \leq 125°C$	P_{el}		33	mW

2 ESD

Table 2-1: ESD ratings

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	ESD HBM Protection at all Pins	AEC Q100-002 (HBM) chip level test	$V_{ESD(HBM)}$	-2		-2	kV
2	ESD CDM Protection at all Pins	AEC Q100-011 (CDM) chip level test	$V_{ESD(CDM)}$	-500		-500	V
3	ESD CDM Protection at Corner Pins	AEC Q100-011 (CDM) chip level test	$V_{ESD(CDM), C}$	-750		-750	V

3 Recommended Operating Conditions

The recommended operating conditions must not be exceeded in order to ensure proper functionality of the device. All parameters specified in the following sections refer to these recommended operating conditions unless stated otherwise.

Table 3-1: Recommended Operating Conditions

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Supply voltage		V_{VDD}	3.0	-	5.5	V
2	Low level input voltage at SPI pins NCS, SCK, MOSI		$V_{IN,SPI,lo}$	-0.3		0.9	V
3	High level input voltage at SPI pins NCS, SCK, MOSI		$V_{IN,SPI,hi}$	0.8 * V_{VDD}		V_{VDD} +0.3	V
4	Operating Pressure Range		p_A	40		115	kPa
5	Operating Temperature	ambient	T_A	-40		125	°C

4 External Components

Table 4-1: External Components

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Supply bypass capacitor*)		C_{VDD}		100		nF

*) Not tested in production

5 Electrical Characteristics

(V_{DD} = 3.0V to 5.5V, T_A=-40°C to + 125°C, unless otherwise noted. Typical values are at V_{DD} = 5.0V and T_A=+25°C. Positive currents flow into the device pins.)

5.1 Global Sensor Parameters

Table 5.1-1: Sensor Accuracy Parameters

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Accuracy pressure measurement mid temperature range	T_{MID} = 0 ...85°C, 40 ... 115kPa	ΔP_{TMID}	-1.0		+1.0	kPa
2	Accuracy pressure measurement low temperature range	T_{LOW} = -40°C, 40 ... 115kPa	ΔP_{TLOW}	-2.0		+2.0	kPa
3	Accuracy pressure measurement high temperature range	T_{HIGH} = 125°C, 40 ... 115kPa	ΔP_{THIGH}	-2.0		+2.0	kPa
4	Accuracy temperature measurement	-40°C ... +125°C, referred to ambient T	ΔT	-5		+5	°C

1) For a graphical description of the tolerance band see 6.2.3-1

Table 5.1-2: Sensor Timing Parameters

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Power-up time*)	from supply VDD > 3.0V to output settled to 90% of final value	t_{UP}			5	ms
2	Step response time*)	pressure step response; output rising from 10% to 90% of final value	t_{RESP}			1	ms
3	Step response settling time*)	pressure step response; output settling to full accuracy	t_{SETTLE}			10	ms

*) Not tested in production

5.2 Voltage Supply

Table 5.2-1: Supply Parameters

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Current consumption	continuous operation	I_{VDD}	-	4.5	6.0	mA
2	Current consumption, sleep-mode[1]	Pin 4 connected to VSS	$I_{VDD,SM}$		10	20	µA
3	Power OK reset threshold VDD, rising edge		$V_{VDD,TH}$	2.1	2.35	2.6	V
4	Power OK reset threshold VDD, falling edge		$V_{VDD,TL}$	1.8	2.05	2.3	V

[1] Device set to sleep mode by digital control command.

5.3 SPI Interface

Table 5.3-1: SPI electrical characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	MISO output low voltage	I_{MISO} = 4 mA, VDD = 4.5 ... 5.5 V	$V_{MISO,L,5}$	0		0.1	VDD
2		I_{MISO} = 1.5 mA, VDD = 3.0 ... 3.6 V	$V_{MISO,L,3}$	0		0.1	VDD
3	MISO output high voltage	I_{MISO} = -4 mA, VDD = 4.5 ... 5.5 V	$V_{MISO,H,5}$	0.85		1.0	VDD
4		I_{MISO} = -1.5 mA, VDD = 3.0 ... 3.6 V	$V_{MISO,H,3}$	0.85		1.0	VDD

Table 5.3-2: SPI timing parameters

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	SPI clock frequency*)		f_{SCK}			10	MHz
2	SPI clock low time*)		t_{SCKL}	35			ns
3	SPI clock high time*)		t_{SCKH}	35			ns
4	Time between two SPI frames*)		t_{NCSW}	1000			ns
5	MOSI setup time*)		t_S	10			ns
6	MOSI hold time*)		t_H	10			ns
7	NCS to MISO drive*)		t_{EN}			40	ns
8	NCS to MISO high-Z*)		t_{DIS}			40	ns
9	SCKL to MISO time*)		t_{SA}			40	ns
10	SCK setup time vs. falling edge of NCS*)		t_{FS}	40			ns
11	SCK hold time vs. falling edge of NCS*)		t_{FH}	40			ns
12	SCK setup time vs. rising edge of NCS*)		t_{RS}	40			ns
13	SCK hold time vs. rising edge of NCS*)		t_{RH}	40			ns

*) Not tested in production

See 6.6-1 for the corresponding timing diagram

6 Functional Description

6.1 Overview

The E524.71 is a high precision, factory calibrated absolute pressure sensor for barometric air pressure (BAP) measurement. Pressure output data are available at a digital data interface (SPI).
Also temperature measurement data from an integrated temperature sensor and information on the sensor integrity are accessible via this digital interface.

6.2 Global Sensor Parameters

6.2.1 Digital Pressure Transfer Function

In general digital output data are available with a word length of 16 bit. The numeric representation is always as 2's complement, which results in a range of:

0 ... +32767 LSB (positive range, or 0000h ... 7FFFh)
-32768 ... -1 LSB (negative range, or 8000h ... FFFFh)

For representation of absolute pressure output only the positive range of values is used. In case of under pressure with pressure falling below the lower definition range, the MSB of the output data can be used as an under-range indicator (showing negative pressure data).

The pressure sensor device is calibrated in Elmos end-of-line production test. The linear pressure transfer function is described by the following equation:

$$D_p = a_1 * P_A + a_0$$

Sensitivity a_1 and offset a_0 are trimmed during the calibration process to exhibit as low as possible sensitivity to external conditions (temperature).

See 6.2.2-1 depicting the pressure transfer characteristic.

6.2.2 P-range: 40 - 115 kPa

Table 6.2.2-1: Pressure transfer function parameters, digital output

Pressure		***Digital Output***		***Sensitivity / Offset***		
Symbol	**Pressure [kPa]**	**Symbol**	**Value [LSB_{16}]**	**Symbol**	**Value**	**Unit**
$P_{A,1}$	40	$D_{P,1}$	0	a_1	400	LSB_{16}/kPa
$P_{A,2}$	115	$D_{P,2}$	30000	a_0	-16000	LSB_{16}

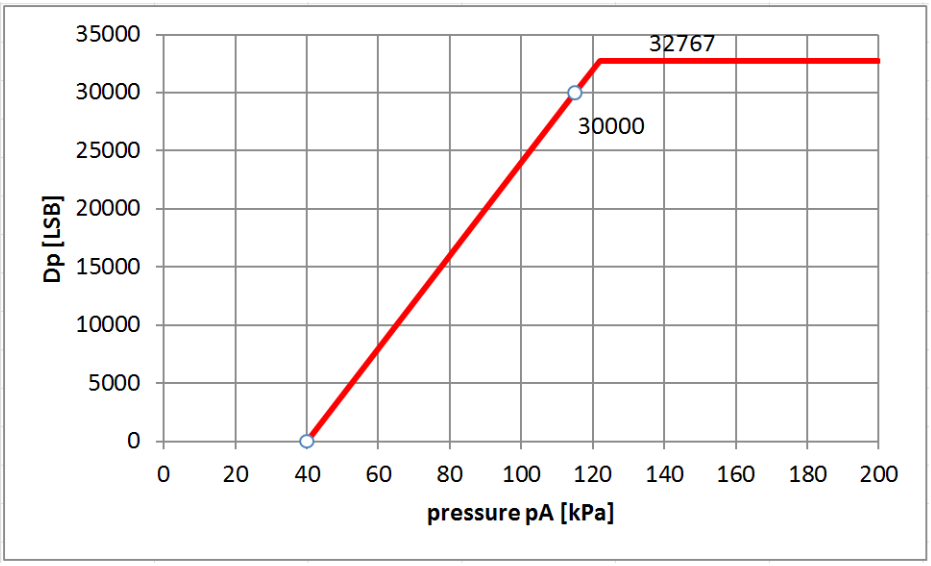

Figure 6.2.2-1: Digital Pressure Transfer Characteristic

The positive number range is exploited for regular pressure output data up to the maximum +32767.
If the MSB of the 16-bit data word is 1, this indicates negative numbers, which can be used as an indicator for under pressure (pressure below minimum value $P_{A,1}$.

6.2.3 Pressure Accuracy

The accuracy of the measured pressure output is given in medium temperature range T_{MID} = 0 ... 85°C, low temperature range T_{LOW} = -40°C ... 0°C, and high temperature range T_{HIGH} = 85°C ... 125°C, respectively. Best accuracy is achieved in the medium temperature range.

The detailed accuracy data are given in 5.1-1.
The accuracy bands are enlarged linearly towards minimum and maximum temperatures as depicted in 6.2.3-1.

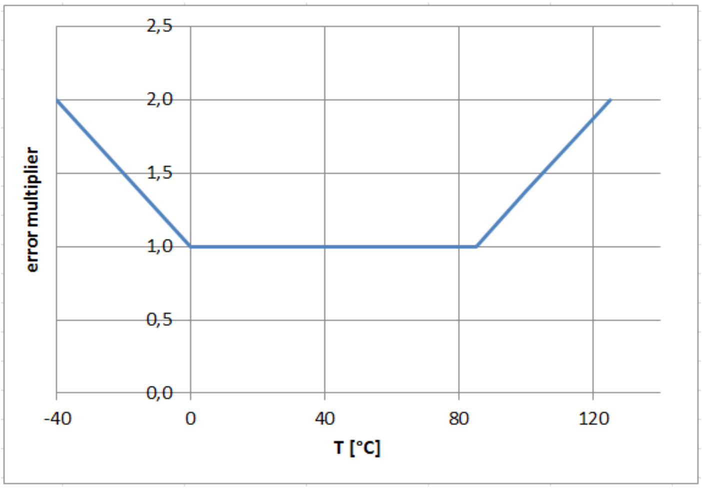

Figure 6.2.3-1: Temperature Dependent Error Multiplier of Pressure Accuracy

6.2.4 Digital Temperature Transfer Function

An internal temperature sensor measures the chip temperature. The temperature output which can be read via the digital interface is calibrated in Elmos' functional test. The temperature characteristic is linear and is described by the following equation:

$$D_T = b_1 * T_A + b_0$$

Sensitivity b_1 and offset b_0 are trimmed during the end-of-line calibration at Elmos.

Table 6.2.4-1: Temperature transfer function parameters

Pressure		***Digital Output***		***Sensitivity / Offset***		
Symbol	**Temperature [°C]**	**Symbol**	**Value [LSB_{16}]**	**Symbol**	**Value**	**Unit**
$T_{A,1}$	-50	$D_{T,OUT,1}$	0	b_1	150	LSB_{16}/°C
$T_{A,2}$	150	$D_{T,OUT,2}$	30000	b_0	7500	LSB_{16}

The positive number range are exploited up to the maximum +32767. When the MSB is 1, this indicates negative numbers and it can be used as an indicator for temperature below -50 °C (typical).

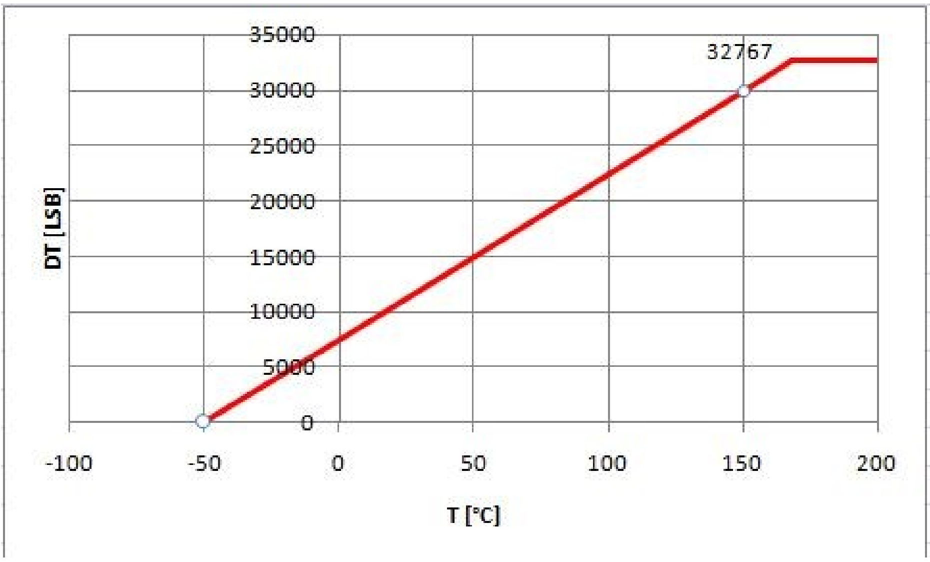

Figure 6.2.4-1: Digital Temperature Transfer Characteristic

6.3 Voltage Supply

The sensor device is supplied from pin VDD (typical 5.0 or 3.3V). From this supply input several internal voltage regulators are generating stabilized voltage levels for analog and digital circuit sections. The different internal voltages are supervised by power-OK comparator structures.
Also a stabilized voltage for the resistive pressure sensor cell is derived from VDD.
The digital data interface allows to set it into *Sleep Mode* using a specific command (*Enter Sleep Mode*), which ensures very low consumption $I_{VDD,SM}$. Of course, in *Sleep Mode* no pressure data are acquired.

For the SPI command to send the sensor into *Sleep Mode* see 6.6.2. To wake-up the sensor to normal operation, the clock input SCK shall be toggled while NCS is pulled low.

6.4 Pressure Signal Path

The signal from a resistive pressure sensor bridge is processed in the analog front-end (AFE) of the integrated sensor signal conditioner as depicted in 6.4-1.

Here, the differential voltage input is amplified in a two stage programmable gain amplifier (PGA1, PGA2). This allows to optimize the gain setting to the full-scale input from the resistive bridge. Additionally, an offset correction network in the analog front-end (after the first amplifier stage PGA1) supports coarse offset trimming by a voltage injected from a DAC. The output from the 2nd amplifier stage is fed to a high resolution ADC. A digital low-pass filter is used to adjust the response time and overall noise performance of the sensor IC.
The complete signal pre-processing in the analog front-end is fully ratiometric to an on-chip voltage reference, i.e. the bridge supply, offset-DAC and the ADC reference are related to the same reference. By this any variations of the reference voltage will be cancelled in the digitized output of the ADC, resulting in negligible temperature variation of the acquired pressure signal and an excellent power supply rejection.

All trimming parameters are adjusted to achieve optimum performance for the resistive sensor bridge used inside this pressure sensor device.

The resistive bridge type pressure sensor cell connected at pins SIP, SIN, SVDD, and SVSS, respectively, is supervised by the sensor bridge diagnostic as described in chapter 6.5.1.

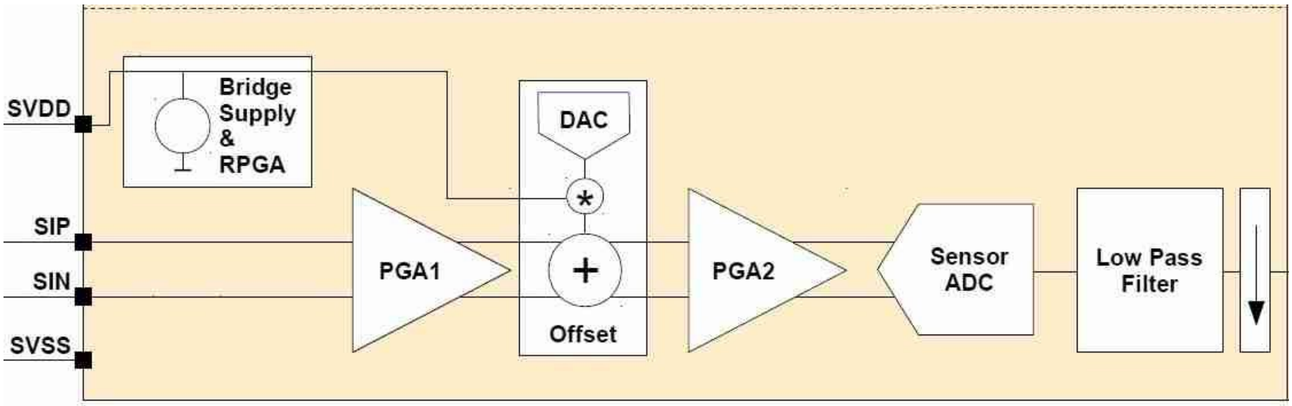

Figure 6.4-1: Pressure Signal Path (AFE)

6.5 Diagnosis Functions

6.5.1 Sensor Bridge Diagnostics

Internal errors of the pressure sensor shall be detected and indicated at the signal output of the component.

Bridge Diagnostics
An integrated bridge diagnostic circuit supervises the resistive pressure sensor cell to detect any of the faults as follows:

- *Sensor faults*:
  - Short of any of the four bridge resistors of the pressure cell
  - Interruption of any of the four of bridge resistors

- *Wiring faults*:
  - Open connection of any of the bridge supply or signal inputs SVDD, SVSS, SIP, or SIN
  - Wrong connection of any sensor bridge terminal SIP or SIN to either SVDD or SVSS

For bridge diagnostics the signal input path pins SIP and SIN are pulled to ground with two matched low current sinks, which are active permanently (true background diagnostics). The voltage levels of the two signal path inputs (SIP and SIN) are monitored by two window comparators with detection thresholds of the low and high comparators at 25% SVDD and 75% SVDD, respectively.
The comparator outputs are combined in a logic (OR) and fed to a debouncing low pass filter. In case of an error the bridge check fail event is indicated by setting the bit **bc_fail** in the internal STATUS register.

Bridge Supply Diagnostics
Another comparator function checks if the supply to the sensor bridge is in its specified range. Here, in case of a supply error the bit **bs_fail** in the STATUS register will be set.

Error indication
The diagnosis bits **bc_fail** and **bs_fail** in the STATUS register (see 6.7) can be read via the digital SPI interface.

6.5.2 Configuration Memory Check

The integrity of data stored in the embedded NVM used as the configuration memory (calibration parameters, device configuration, device ID, etc.) is checked at power-up of the component by calculation of a check sum (CRC). If a check sum error is detected no reliable pressure calculation is possible.
Therefore, the sensor remains in idle state, i.e. no pressure data transferred to the output registers DSP_T and DSP_S. In this case the bits **STATUS.dsp_s_up** and **dsp_t_up** will never be set.

In case of a failed CRC of the configuration memory (NVM) will not allow any communication via SPI with the device. Additionally, the data output MISO will remain at hi-Z.

6.6 SPI Interface

The E524.71 features an SPI slave interface. This interface provides direct access to registers of the memory of the IAP sensor. An external SPI master (e.g. a µC) can read and write memory addresses (registers) of the device using the following commands:

- **Random write**: Writes data to consecutive memory addresses of the device starting at the specified memory address.
- **Random read**: Reads data from consecutive memory addresses of the device starting at the specified memory address.

All read/writes must start at **word aligned addresses** (i.e. LSB of memory address equals 0) and read/write an **even number of bytes**.

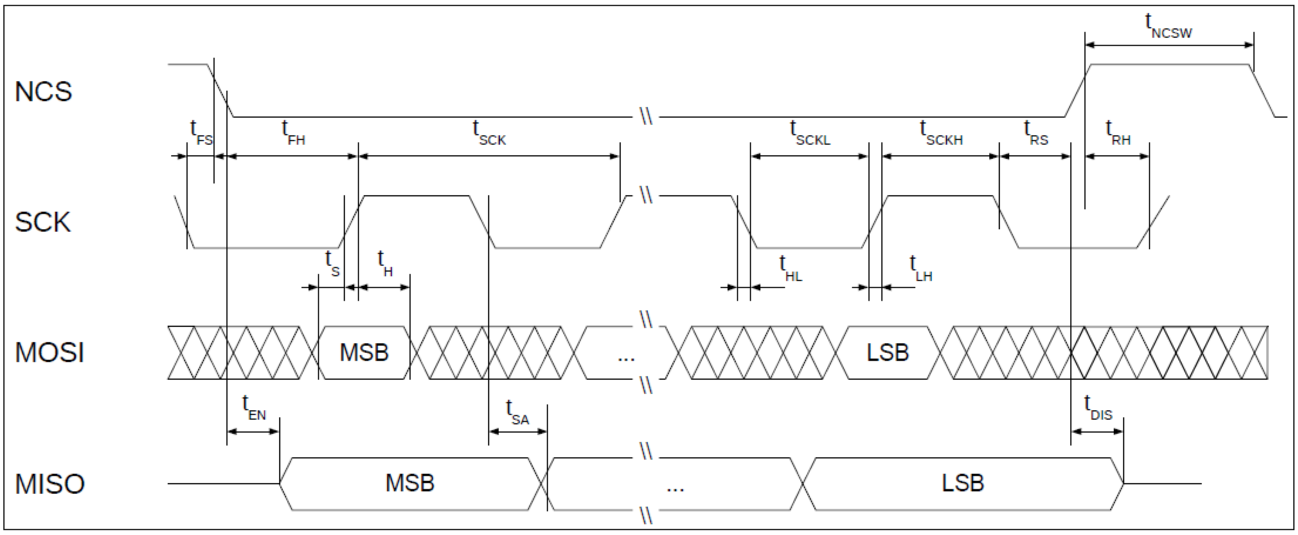

Figure 6.6-1: SPI Interface Timing Diagram

6.6.1 SPI Command Format

The SPI interface supports two command formats, without (6.6.1-1) and with CRC protection (6.6.1-2), respectively.

The **NCS** frames every command, i.e. the frame starts when NCS is reset (= 0) and the frame ends when NCS is disabled (= 1).

The **memory address** field sets the byte address of the first memory location to be read or written. Only 16-bit word aligned read / writes commands are supported, accordingly the LSB of the memory address field is not part of the frame. The LSB of the first byte is used to indicate read or write.
The **read / write data** is transferred MSB first, high byte before low byte.

The MSB (bit[7]) of the second byte sent by the master specifies if the transmitted data are in a frame without CRC (bit[7] = 0) or with CRC (bit[7] = 1).
The length field (bits[6:4]) specifies the number of 16 bit data words to transfer decremented by 1, i.e. a value of *0001* corresponds two 16 bit words. All frames must transfer an even number of bytes. Maximum length for CRC protected read/write frames is 16/4 bytes; for unprotected frames the length is unlimited.

The CRC4 and CRC8 for redundancy checks are computed in the same bit and byte order as the transmission over the bus. The polynomials utilized are:

- CRC4 polynomial: 0x03 ; initialization value: 0x0F
- CRC8 polynomial: 0xD5 ; initialization value: 0xFF

If a CRC error occurs, then the event bit **com_crc_error** in the STATUS register will be set

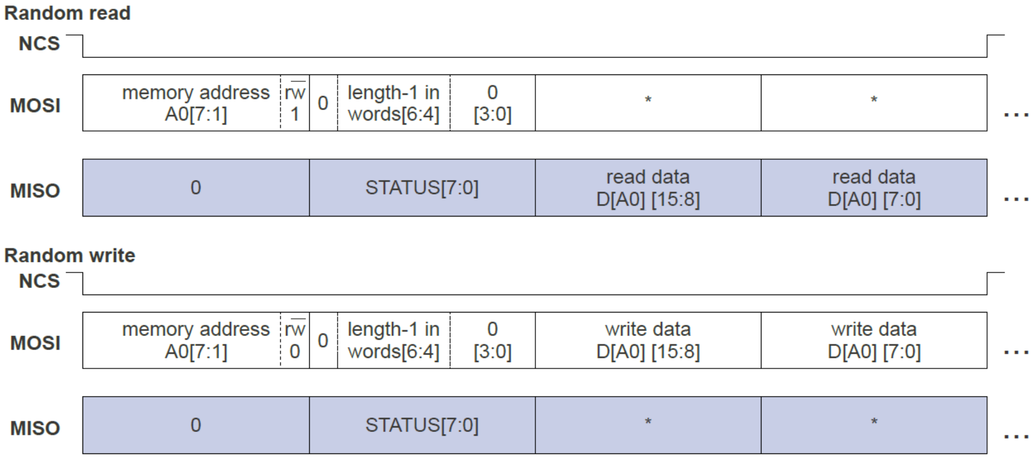

Figure 6.6.1-1: Read / Write without CRC

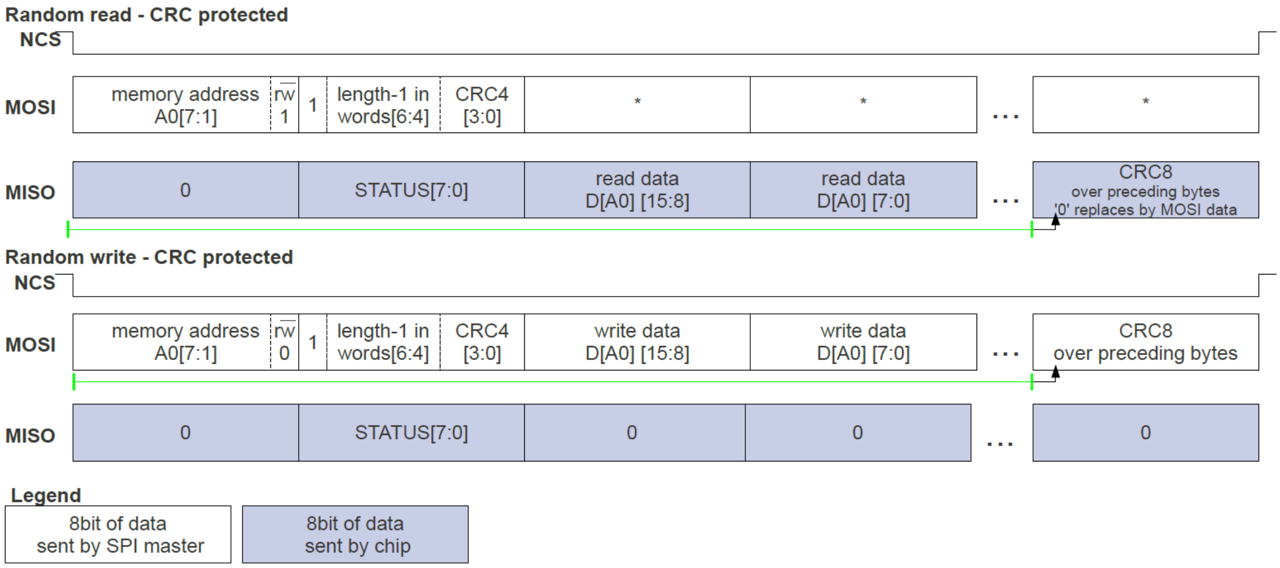

Figure 6.6.1-2: Read / Write with CRC

6.6.2 SPI Command Examples

The following examples of SPI Read and Write sequences are referring to the protocols without and with CRC protection as described in the section above and the register definitions in 6.7. Exemplary C-code is available for all commands.

The next command sequence describes an unprotected *Read* command (without CRC) of 3 subsequent 16-bit words starting at memory address 0x2E. This will read the corrected IC temperature, corrected pressure signal, and (synchronized) status bits of the sensor.

Table 6.6.2-1: Random Read

Byte #	***0***	***1***	***2***	***3***	***4***	***5***	***6***	***7***
MOSI	0x2F	0x20	*dc: don't care*	*dc*	*dc*	*dc*	*dc*	*dc*
MOSI comment	= memory addr. 2E + 1 with LSB = 1 for *Read*	[b7:b0] = 00100000 MSB=0: without CRC [b6:b4] = length-1 → 3 data words [b3:b0]: must be 0	*dc*: ignored by device					
MISO	0x00	0x1E	0x7D	0xF2	0x82	0xEA	0x00	0x1E
MISO comment		STATUS_ SYNC [b7:b0]	DSP_T [b15:b8] (ad. 0x2E)	DSP_T [b7:b0]	DSP_S [b15:b8] (ad. 0x30)	DSP_S [b7:b0]	STATUS_ SYNC [b15:b8] (ad. 0x32)	STATUS_ SYNC [b7:b0]

The following sequence writes one 16-bit word to address 0x22. This will copy 0x6C32 into the command register CMD to move the component to Sleep Mode.

Table 6.6.2-2: Random Write

Byte #	***0***	***1***	***2***	***3***
MOSI	0x22	0x00	0x6C	0x32
MOSI comment	memory address with LSB = 0 for *Write*	[b7:b0] = 00000000 MSB=0: without CRC [b6:b4] = length-1 → 1 data word [b3:b0]: must be 0	written to CMD[15:8]	written to CMD[7:0]
MISO	0x00	0x1E	*dc: don't care*	*dc*
MISO comment		STATUS_ SYNC [b7:b0]	*dc*: ignored by device	

The following command sequence describes a CRC protected *Read* command of 3 subsequent 16-bit words starting at memory address 0x2E to read the corrected IC temperature, corrected pressure signal, and (synchronized) status bits of the sensor.

Table 6.6.2-3: Random Read - protected by CRC

Byte #	*0*	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*
MOSI	0x2F	0xAC	*dc: don't care*	*dc*	*dc*	*dc*	*dc*	*dc*	*dc*
MOSI comment	= memory addr. 2E + 1 with LSB = 1 for *Read*	[b7:b0] = 10101100 MSB=1: with CRC [b6:b4] = length-1 → 3 data words [b3:b0]: CRC4	*dc*: ignored by device						
MISO	0x00	0x1E	0x7D	0xF2	0x82	0xEA	0x00	0x1E	0x28
MISO comment		STATUS_SYNC [b7:b0]	DSP_T [b15:b8] (ad. 0x2E)	DSP_T [b7:b0]	DSP_S [b15:b8] (ad. 0x30)	DSP_S [b7:b0]	STATUS_SYNC [b15:b8] (ad. 0x32)	STATUS_SYNC [b7:b0]	CRC8 (calc'd)

The next example describes a *Write* of one 16-bit word (contents 0xCF9E) with CRC protection to address 0x36 to clear events in the STATUS register.

Table 6.6.2-4: Random Write - protected with CRC

Byte #	*0*	*1*	*2*	*3*	*4*
MOSI	0x36	0x8E	0xCF	0x9E	0x3E
MOSI comment	memory address with LSB = 0 for *Write*	[b7:b0] = 10001110 MSB=1: with CRC [b6:b4] = length-1 → 1 data word [b3:b0]: CRC4	written to STATUS[15:8] (after CRC8)	written to STATUS[7:0] (after CRC8)	CRC8 (calc'd)
MISO	0x00	0x1E	*dc: don't care*	*dc*	*dc*
MISO comment		STATUS_SYNC [b7:b0]	*dc*: ignored by device		

6.7 Register Descriptions

Register *Read* or *Write* are performed via the digital communication interface. After power-up of the IC all registers except STATUS and CMD are write protected.

Table 6.7-1: *Command* register

0x22		***CMD***		
bits	**name**	**default**	**rw**	**description**
15:0	cmd	0	w	Writing to this register controls the state of the IAPS device. 0x6C32: *SLEEP Mode* Initiate the power state *SLEEP*, powering down the ASIC 0xB169: *RESET* Performs a reset. After reset the power-up sequence will be executed, i.e. the registers are loaded with data from the configura-tion memory, also a CRC check is performed.

Table 6.7-2: *Temperature* register

0x2E		***DSP_T***		
bits	**name**	**default**	**rw**	**description**
15:0	dsp_t		r	corrected temperature measurement value of the sensor. Whenever this register is updated with a new measurement the STATUS.dsp_t_up event bit is set.

Table 6.7-3: *Pressure* register

0x30		***DSP_S***		
bits	**name**	**default**	**rw**	**description**
15:0	dsp_s		r	corrected pressure measurement value of the sensor. Whenever this register is updated with a new measurement the STATUS.dsp_s_up event bit is set.

The registers DSP_T and DSP_S contain invalid data after power-up until the first temperature and pressure values have been measured by the device and transferred to these registers. In case a NVM CRC error occurred, the DSP_T and DSP_S registers would never be updated. Thus, after power up it is necessary to wait until the STATUS.dsp_s_up and dsp_t_up bits have been set at least once before using the temperature or pressure data. It is not sufficient to wait just for a fixed time delay.

Table 6.7-4: *Status* register - synchronized

0x32		***STATUS_ SYNC***			
bits	**name**	**default**	**rw**	**type**	**description**
0	idle	0	rw	status	STATUS.idle
1	- reserved -	0	rw	event	reserved
2	- reserved -	0	rw	event	reserved
3	dsp_s_up	0	rw	event	when DSP_S is read STATUS.dsp_s_up is copied here
4	dsp_t_up	0	rw	event	when DSP_T is read STATUS.dsp_t_up is copied here
5	- reserved -	0	rw	status	reserved
6	- reserved -	0	rw	status	reserved
7	bs_fail	0	rw	event	STATUS.bs_fail
8	bc_fail	0	rw	event	STATUS.bc_fail
9	- reserved -	0	rw	event	reserved
10	dsp_sat	0	rw	status	STATUS.dsp_sat
11	com_crc_error	0	rw	event	STATUS.com_crc_error
12	- reserved -	0	rw	status	reserved
13	- reserved -	0	rw	status	reserved
14	dsp_s_missed	0	rw	event	STATUS.dsp_s_missed
15	dsp_t_missed	0	rw	event	STATUS.dsp_t_missed

The bits STATUS_SYNC[15:5,0] are identical to the bits STATUS[15:5,0].
The bits STATUS_SYNC[4:3] are copied from the STATUS register when the corresponding DSP registers are read. First reading the DSP registers and then STATUS_SYNC ensures that both values are consistent to each other.
The synchronized status STATUS_SYNC register can be used to continuously poll the pressure, temperature and status of the device with a single read command by reading three 16 bit words starting at address 0x2E. By evaluating STATUS_SYNC.dsp_t_up and STATUS_SYNC.dsp_s_up it can be determined if the values in DSP_T and DSP_S acquired during the same read contain recently updated temperature or pressure values.

Table 6.7-5: *Status* register

0x36		***STATUS***			
bits	**name**	**default**	**rw**	**type** [1)]	**description**
0	idle	0	rw	status	0: chip in busy state 1: chip in idle state
1	- reserved -	0	rw	event	reserved
2	- reserved -	0	rw	event	reserved
3	dsp_s_up	0	rw	event	1: DSP_S register has been updated. Cleared when DSP_S is read
4	dsp_t_up	0	rw	event	1: DSP_T register has been updated. Cleared when DSP_T is read.
5	- reserved -	0	rw	status	reserved
6	- reserved -	0	rw	status	reserved
7	bs_fail	0	rw	event	1: bridge supply failure occurred
8	bc_fail	0	rw	event	1: sensor bridge check failure occurred
9	- reserved -	0	rw	event	reserved

0x36		***STATUS***			
10	dsp_sat	0	rw	event	1: a DSP computation leading to the current DSP_T or DSP_S values was saturated to prevent overflow
11	com_crc_error	0	rw	event	1: communication CRC error
12	- reserved -	0	rw	status	reserved
13	- reserved -	0	rw	status	reserved
14	dsp_s_missed	0	rw	event	1: dsp_s_up was 1 when DSP_S updated
15	dsp_t_missed	0	rw	event	1: dsp_t_up was 1 when DSP_T updated

1)

- "Event" type flags remain set until cleared by writing '1' to the respective bit position in STATUS register (not STATUS_SYNC). Writing 0xFFFF to the STATUS register will clear all event bits.
- "Status" type flag represents a condition of a hardware module of the IC and persists until the condition has disappeared.

Table 6.7-6: *Serial Number* register 0

0x50		***SER0***		
bits	**name**	**default**	**rw**	**description**
15:0	ser0		r	serial number of the IC, Lo-Word

Table 6.7-7: *Serial Number* register 1

0x52		***SER1***		
bits	**name**	**default**	**rw**	**description**
15:0	ser1		r	serial number of the IC, Hi-Word

"

7 Package Reference

The E524.71 is available in a Pb free, RoHs compliant, 8-pin SO plastic package with footprint according to JEDEC MO-012-F, variant AA. The pressure port is realized by two redundant inlet holes on top of the housing. The package is classified to Moisture Sensitivity Level 3 (MSL 3) according to JEDEC J-STD-020E with a soldering peak temperature of 260°C.

Note: Thermal resistance junction to ambient $R_{th,ja}$ is 160 °C/W, based on JEDEC standard JESD-51.

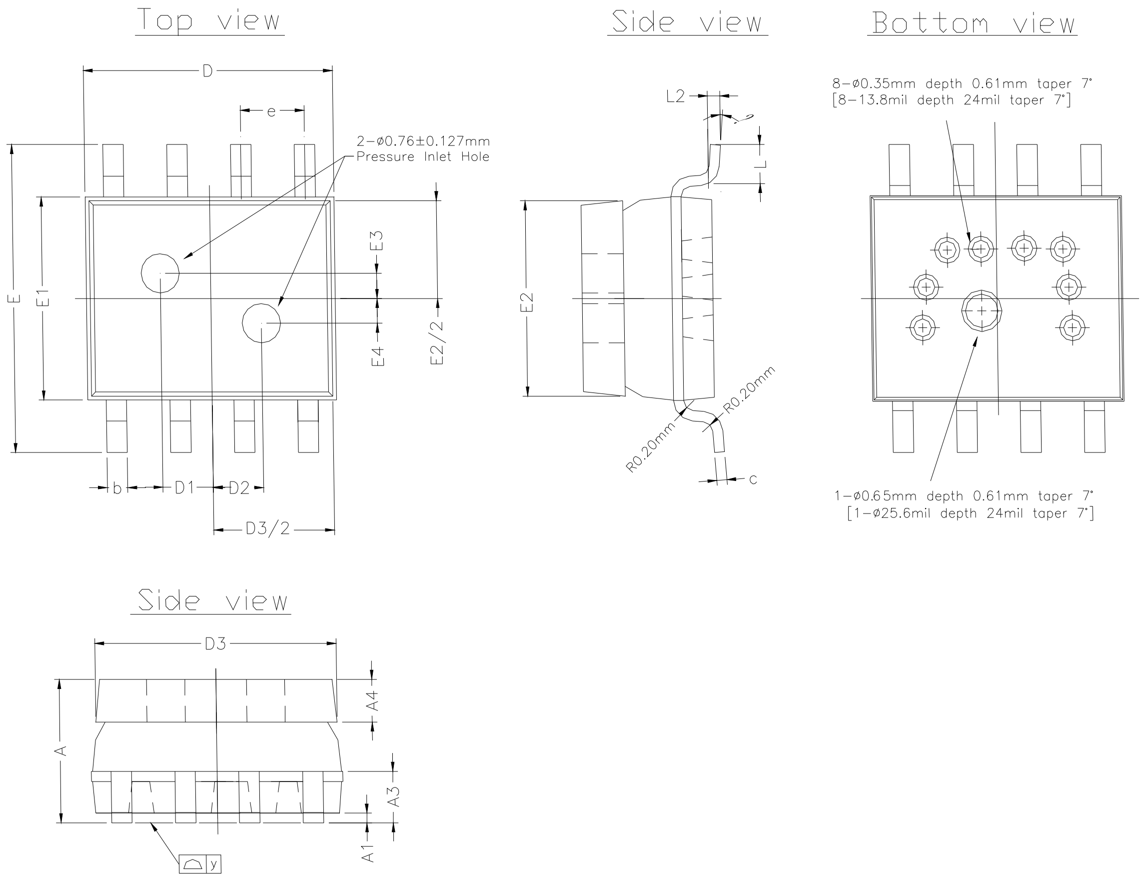

Figure 7-1: Package Outline

Note: Contact factory for specific location and type of pin 1 identification.

Table 7-1: Package Characteristics

Description	***Symbol***		***mm***	
		min	**typ**	**max**
Package height	A		2.81	
Stand off	A1		0.19	
Width of terminal leads	b		0.41	
Thickness of terminal leads	c		0.20 Ref	
Length of terminal for soldering to substrate	L		0.76	
Angle of lead mounting area	Θ [°]	0	-	8
Lead pitch	e		1.27 BSC	
Package length	D		4.95	

Description	Symbol		mm	
Package total width	E		6.00	
Package body width	E1		3.95	
Thickness of the lid	A4		0.83 Ref	
Length of lid	D3		4.80	
Width of lid	E2		3.80	
Off center position, longitudinal, inlet hole	D1 / D2		1.00	
Off center position, lateral, inlet hole	E3 / E4		0.49	

8 General

8.1 WARNING - Life Support Applications Policy

ELMOS Semiconductor AG is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing ELMOS Semiconductor AG products, to observe standards of safety, and to avoid situations in which malfunction or failure of an ELMOS Semiconductor AG Product could cause loss of human life, body injury or damage to property. In development your designs, please ensure that ELMOS Semiconductor AG products are used within specified operating ranges as set forth in the most recent product specifications.

8.2 General Disclaimer

Information furnished by ELMOS Semiconductor AG is believed to be accurate and reliable. However, no responsibility is assumed by ELMOS Semiconductor AG for its use, nor for any infringements of patents or other rights of third parties, which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of ELMOS Semiconductor AG. ELMOS Semiconductor AG reserves the right to make changes to this document or the products contained therein without prior notice, to improve performance, reliability, or manufacturability .

8.3 Application Disclaimer

Circuit diagrams may contain components not manufactured by ELMOS Semiconductor AG, which are included as means of illustrating typical applications. Consequently, complete information sufficient for construction purposes is not necessarily given. The information in the application examples has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of ELMOS Semiconductor AG or others.

9 Contact Info

Table 9-1: Contact Information

Headquarters ELMOS Semiconductor AG Heinrich-Hertz-Str. 1, D-44227 Dortmund (Germany) www.elmos.com	Phone: +49 (0) 231 / 75 49-100 Fax: +49 (0) 231 / 75 49-149 sales-germany@elmos.com
Sales and Application Support Office North America ELMOS NA. Inc. 32255 Northwestern Highway, Suite 220 Farmington Hills, MI 48334 (USA)	Phone: +1 (0) 248 / 8 65 32 00 Fax: +1 (0) 248 / 8 65 32 03 sales-usa@elmos.com
Sales and Application Support Office Korea and Japan ELMOS Korea C-301, Innovalley, 253, Pangyo-ro, Bundang-gu, Sungnam-si, Gyeonggi-do, 13486 Republic of Korea	Phone: +82 (0) 31 / 7 14 11 31 Fax: +82 (0) 31 / 8018-0790 sales-korea@elmos.com
Sales and Application Support Office China Elmos Semiconductor Technology (Shanghai) Co., Ltd. Unit 16B, 16F Zhao Feng World Trade Building, No. 369 Jiang Su Road, Chang Ning District, Shanghai, 200050 P.R. China	Phone: +86 21 6210 0908 Fax: +86 21 6219 7502 sales-china@elmos.com
Sales and Application Support Office Singapore ELMOS Semiconductor Singapore Pte Ltd. 3A International Business Park, #09-13 ICON@IBP, Singapore 609935	Phone: (+65) 6635 1293 Fax: (+65) 6635 1140 sales-singapore@elmos.com