500 mA Sinusoidal BLDC Motor Controller E523.81

Production Data – May 15, 2018

RoHS compliant

Features

- IC for standalone PMSM applications
- Internal power bridge up to 500mA(RMS)
- selectable PWM speed and error interface or analog speed interface
- SVM (Space Vector Modulation) realizes +14% output amplitude
- Tacho output
- Current controlled start up
- Integrated configurable error handling
- Blockage detection
- Automatic restart and rotor delocking
- Speed or current control
- Windmill functions
- Safety functions for overtemperature, over-/under-voltage, overcurrent and short circuit

General Description

This IC integrates all components to control and drive a small BLDC fan or pump in a standalone application with minimum external component effort.

Ordering Information

Ordering-No.:	*J_{Temp} Range*	*Package*
E52381B62C	-40°C to +170°C	QFN20L5

Applications

- Small PMSM / BLDC FANs
- Small PMSM / BLDC pumps

Typical Operating Circuit

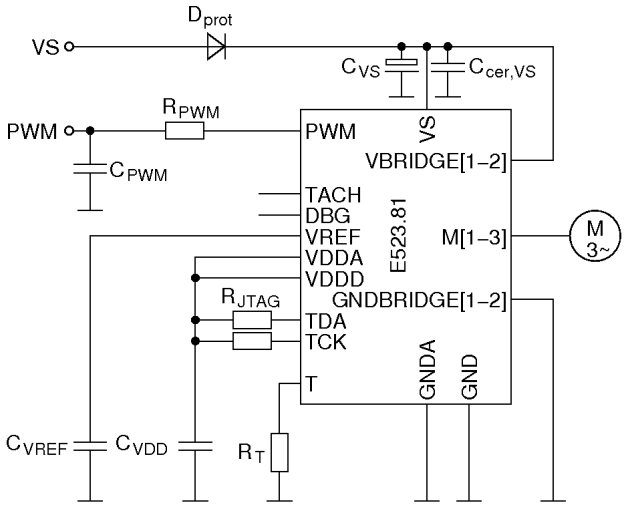

Figure 1: Block diagram on L0

The device is designed for directly driving a motor on the same PCB. If longer wiring between IC and motor is applied, additional components for system level EMC & ESD compliance of the IC at pins M1..M3 may be required.

Functional Diagram

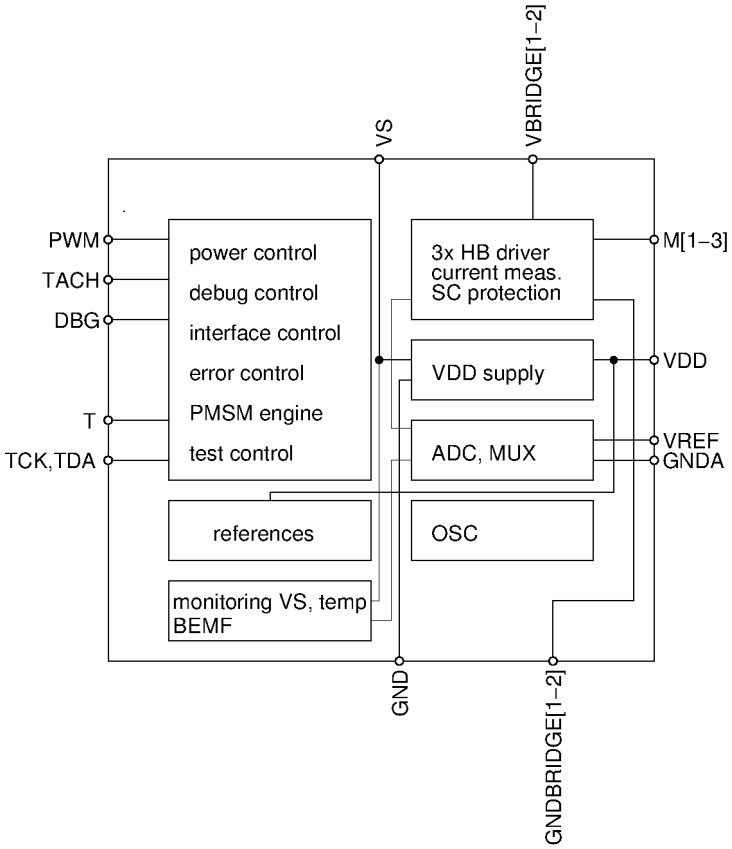

Figure 1: Block diagram on L1 (IC, functional blocks)

Pin Configuration

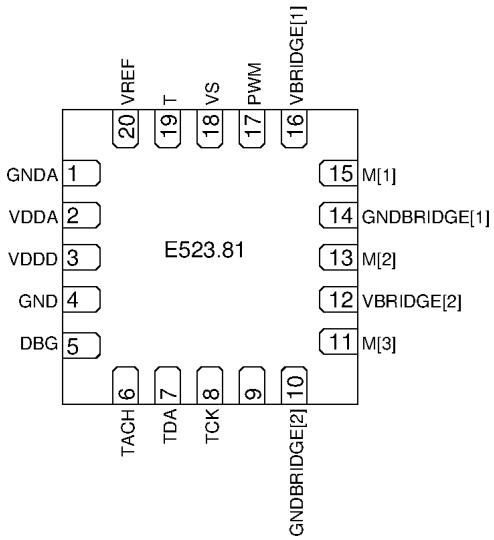

Figure 1: Pin Configuration

Pin Description

No	Name	Type	Description
1	GNDA	HV_S	ADC reference ground ground
2	VDDA	S	unconnected VDD supply output; connection of external capacitor
3	VDDD	S	internal VDD interface supply voltage
4	GND		ground
5	DBG	D_IO AD_IO	wave output; digital I/O pin special output for system configuration in the lab
6	TACH	D_IO	tachometer output digital I/O pin
7	TDA	D_IO	test interface; digital I/O pin JTAG bidirectional signal. shared signal for TMS, TDI and TDO
8	TCK	D_IO D_I	test interface; digital I/O pin JTAG clock input
9	n.c.		unconnected
10	GNDBRIDGE[2]	S	bridge ground pin bridge ground
11	M[3]	HV_A_IO	motor pin motor
12	VBRIDGE[2]	HV_S	bridge supply pin bridge supply voltage
13	M[2]	HV_A_IO	motor pin motor
14	GNDBRIDGE[1]	S	bridge ground pin bridge ground
15	M[1]	HV_A_IO	motor pin motor
16	VBRIDGE[1]	HV_S	bridge supply pin bridge supply voltage
17	PWM	HV_D_I	PWM I/O goal speed input
18	VS	HV_S	supply supply input
19	T	HV_D_I	test mode activation test activation input
20	VREF		ADC reference voltage
EP	EP		exposed die paddle, connect to GND

Note: A = Analog, D = Digital, S = Supply, I = Input, O = Output, B = Bidirectional, HV = High Voltage

1 Absolute Maximum Ratings

Stresses beyond these absolute maximum ratings listed below may cause permanent damage to the device. **These are stress ratings only; operation of the device at these or any other conditions beyond those listed in the operational sections of this document is not implied.** Exposure to absolute maximum rated conditions for extended periods may affect device reliability. All voltages referred to GND. Currents flowing into terminals are positive, those drawn out of a terminal are negative.

Table 1-1: AbsMaxRatingsTable

No.	*Description*	*Condition*	*Symbol*	*Min*	*Max*	*Unit*
1	170°C retention time		$T_{QJ,170}$		300	h
2	160°C retention time		$T_{QJ,160}$		1000	h
3	150°C retention time		$T_{QJ,150}$		2000	h
4	85°C retention time		$T_{QJ,85}$		8700	h
5	PWM input voltage range		V_{PWM}	-0.3	40	V
6	digital I/O pin voltage		V_{DP}	-0.3	3.6	V
7	digital supply voltage		V_{VDDD}	-0.3	3.6	V
8	digital I/O pin current		I_{DP}	-50	50	mA
9	T pin voltage		V_T	-0.3	40	V
10	VS voltage		V_{VS}	-0.3	40	V
11	VDD pin forced voltage		V_{VDDA}	-0.3	3.6	V
12	VDD pin forced current		I_{VDDA}	-20	2	mA
13	VBRIDGE voltage		$V_{VBRIDGE}$	-0.3	40	V
14	ground bounce		$V_{GNDBRIDGE}$	-0.3	0.3	V
15	M current	T_J=35°C	I_M	-700	700	mA
16	M current		I_M	-500	500	mA

2 ESD

Table 2-1: ESD Protection

Description	*Condition*	*Symbol*	*Min*	*Max*	*Unit*
ESD HBM protection at pin PWM	1)	$V_{ESD(HBM),PWM}$	-4	4	kV
ESD HBM protection at all other pins	1)	$V_{ESD(HBM)}$	-2	2	kV
ESD CDM protection at all pins	2)	$V_{ESD(CDM)}$	-500	500	V

1) According to AEC-Q100-002 (HBM) chip level test
2) According to AEC-Q100-011 (CDM) chip level test

3 Recommended Operating Conditions

Table 3-1: Recommended Operating Conditions

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	PWM input frequency range		f_{PWM}	100		2200	Hz
2	goal speed input low level		$V_{L,PWM}$	0		2.5	V
3	goal speed input high level		$V_{H,PWM}$	4V		V_{VS}	
4	goal speed input voltage range when using analog goal value instead of input PWM		$V_{VM,PWM}$	0		2.5	V
5	DP input high level		$V_{IH,DP}$	0.8			V_{VDDD}
6	DP input low level		$V_{IL,DP}$			0.2	V_{VDDD}
7	DP output load current, high state		$I_{H,DP}$	-2		2	mA
8	DP output load current, low state		$I_{L,DP}$	-2		2	mA
9	low input voltage		$V_{L,T}$	0		0.4	V
10	high level for customer configuration mode activation		$V_{H,lab}$	2.5		3.5	V
11	VS voltage		V_{VS}	5		29	V
12	VS storage capacitance		C_{VS}	10	47		uF
13	ceramic capacitance at VS		$C_{cer,VS}$	80	100		nF
14	external load current at pin VDD	IC in active mode	$-I_{VDDA,ext}$	0		5	mA
15	capacitance at pin VDD (ceramic capacitor)		C_{VDD}	1	4.7	10	µF
16	ESR of VDD capacitor		$R_{ESR,C,VDDA}$			0.5	Ohm
17	VBRIDGE voltage		$V_{VBRIDGE}$	6	13	29	V
18	M current		I_M	-500	-	500	mA
19	VREF capacitance		C_{VREF}	8		12	nF

4 Electrical Characteristics

(V_{VS} = 8V to 29V, T_{amb}=-40°C to + 150°C, unless otherwise noted. Typical values are at V_{VS}=13.5V and T_{amb}=+35°C. Positive currents flow into the device pins.)

4.1 Clock System

Table 4.1-1: Clock system electrical parameters

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	clock frequency		f_{clk}		14.35		MHz

4.2 I/O Peripherals

4.2.1 PWM Speed Input

Table 4.2.1-1: PWM speed input electrical parameters

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	goal speed input LH threshold		$V_{LH,PWM}$			4	V
2	goal speed input HL threshold		$V_{HL,PWM}$	2.5			V
3	pull up current		$I_{pu,PWM}$	3			mA
4	pull down current		$I_{pd,PWM}$	4.3			mA

4.2.2 Low Voltage Digital I/O Pins

Table 4.2.2-1: Low voltage digital I/O pins electrical parameters

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	output high level	I_{DP}>-2mA.	$V_{HO,DP}$	0.8			V_{VDDD}
2	output low level	I_{DP}<2mA	$V_{LO,DP}$			0.2	V_{VDDD}

4.3 PMSM Motion Control Unit

4.3.1 Speed Control

Table 4.3.1-1: Speed controller parameters

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	speed controller update time[1)]		$t_{c,speed}$		10		ms
2	resolution of rpm setpoint[*)]		resolution			±0.4	%
3	thermal & lifetime drift of rpm setpoint[*)]		drift			±4.6	%

[*)] Not tested in production
[1)] SCAN tested

4.4 System Control

4.4.1 Error Detection and Behaviour

4.4.1.1 High Temperature Speed Reduction and Shut Down

Table 4.4.1.1-1: Temperature shut down values

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	[1)]		T_{off}-T_{normal}		30		K
2	[1)]		T_{off}-T_{reduce}		20		K
3	[1)]		T_{off}-$T_{restart}$		10		K
4	speed reduction delay[1)]		t_{reduce}		300		s

[1)] SCAN tested

4.4.1.2 Low Load Detection

Table 4.4.1.2-1: Low load detection parameters

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	low load detection delay time[1)]		t_{low_load}		3		s

[1)] SCAN tested

4.5 Power Supply

4.5.1 VDD Supply

Table 4.5.1-1: VDD supply electrical parameters

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	VDDA output voltage	0 > $I_{VDDA,ext}$ > -15 mA	V_{VDDA}	3.15		3.45	V
2	output current limitation (short circuit)	V_{VDDA} =0V, V_{VS}=13.5V	$-I_{lim,VDDA}$			220	mA

4.6 Integrated Motor Bridge

4.6.1 "Small" Bridge Parametrical Description

Table 4.6.1-1: Electrical parameters

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	on resistance to VBRIDGE[*)]	V_{VS},$V_{VBRIDGE}$=13.5V, T_J=35°C	$r_{on,h,rt}$		675	825	mΩ
2	on resistance to VBRIDGE[*)]	V_{VS},$V_{VBRIDGE}$=13.5V, T_J=150°C	$r_{on,h,ht}$		975	1125	mΩ
3	on resistance to VBRIDGE	V_{VS},$V_{VBRIDGE}$=6V, T_J=35°C	$r_{on,h,rt,lv}$		875	1050	mΩ
4	on resistance to VBRIDGE	V_{VS},$V_{VBRIDGE}$=6V, T_J=150°C	$r_{on,h,ht,lv}$		1200	1375	mΩ
5	on resistance to GNDBRIDGE[*)]	V_{VS},$V_{VBRIDGE}$=13.5V, T_J=35°C	$r_{on,l,rt}$		825	1100	mΩ
6	on resistance to GNDBRIDGE[*)]	V_{VS},$V_{VBRIDGE}$=13.5V, T_J=150°C	$r_{on,l,ht}$		1425	1575	mΩ
7	on resistance to GNDBRIDGE	V_{VS},$V_{VBRIDGE}$=6V, T_J=35°C	$r_{on,l,rt,lv}$		1050	1225	mΩ
8	on resistance to GNDBRIDGE	V_{VS},$V_{VBRIDGE}$=6V, T_J=150°C	$r_{on,l,ht,lv}$		1700	1875	mΩ
9	short circuit threshold		$I_{th.SC}$			4	A
10	short current detection time[1)]		$t_{d,SC}$		5		µs

[*)] Not tested in production
[1)] Scan tested

4.7 Monitoring and Measurements

4.7.1 Temperature Monitoring

Table 4.7.1-1: Temperature monitoring parameters

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	temperature measurement accuracy of the trimmed IC*)	T_J > 125°C	$D_{T,IC}$	-6		6	K

*) Not tested in production

4.7.2 VS Measurement

Table 4.7.2-1: VS measurement electrical parameters

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	VS overvoltage high activation threshold[1)]		$V_{LH,OV,HI,VS}$			31	V
2	VS overvoltage low activation threshold[1)]		$V_{LH,OV,LO,VS}$			22	V
3	overvoltage and undervoltage reaction delay[2)]		t_{deb,VS_shut_down}		100		µs

1) SCAN tested and tested by divider ratio
2) SCAN tested

5 Functional Description

5.1 Overview

This IC integrates all components to control and drive a small BLDC fan or pump in a standalone application with minimum external component effort.

5.2 Block Diagrams

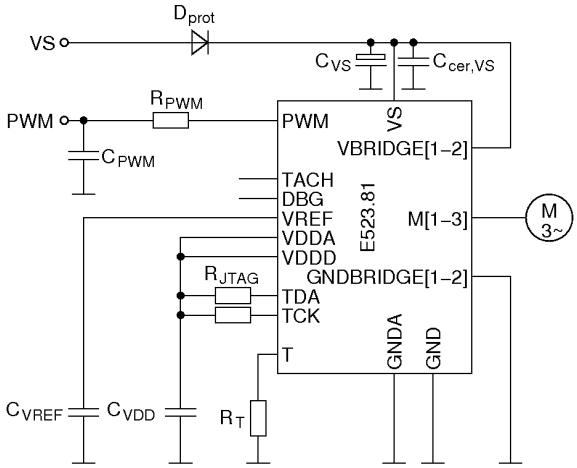

Figure 5.2-1: Block diagram on L0

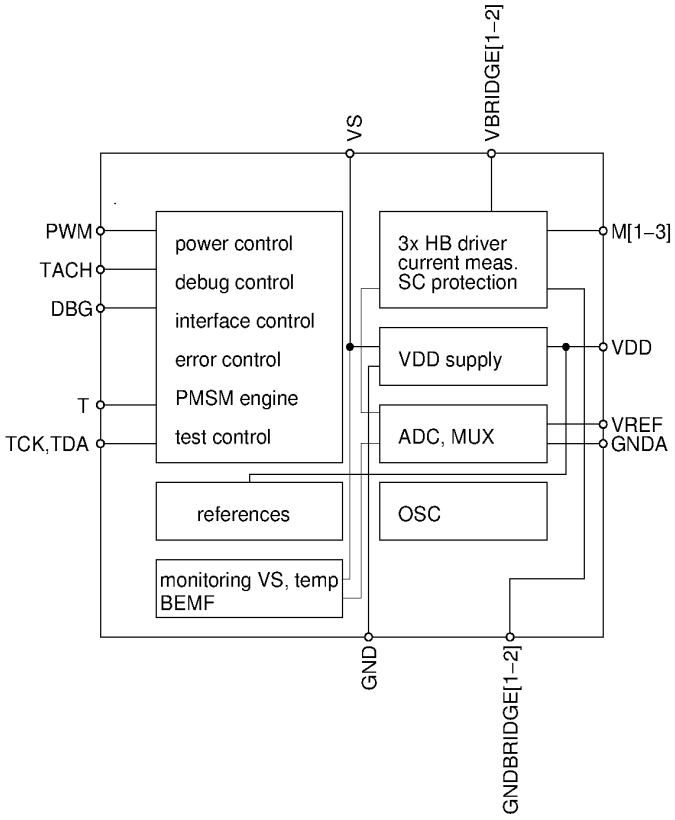

Figure 5.2-2: Block diagram on L1 (IC, functional blocks)

5.3 System Level Motor Interface and Error Interface

5.3.1 Motor Interface

5.3.1.1 Goal Speed Input

The goal speed can be controlled by the duty ratio of a rectangular input signal at the pin PWM.
5.3.1.1-1 shows the electrical field frequency and the resulting target speed versus input duty ratio. t_period,min, t_period,max and t_period,emergency can be set up with registers T_PERIOD_MIN_EXP, T_PERIOD_MAX_EXP and T_PERIOD_EMERGENCY_EXP.
Entering into the emergency mode is delayed by 4s. Entering from emergency mode into the normal mode is done as soon as the IC detects 4 subsequent valid PWM pulses with a duty ratio between 5% and 86%.
The control behaviour can also be set up to current control instead of speed control using register T_PERIOD_MODE_CTRL. If the behaviour is set up to current control T_PERIOD_MIN_EXP, T_PERIOD_MAX_EXP and T_PERIOD_EMERGENCY_EXP are used to set up the corresponding currents instead of the electrical field frequency.

The input behaviour can be set up to use an analog voltage instead of a duty ratio. The activation of this behaviour is done by register T_PERIOD_MODE_CTRL. When activated:

- the control behaviour changes to that of 5.3.1.1-2
- no emergency behaviour is available
- the pull up and pull down current sources at the PWM pin are switched off. In the analog mode the selection between current control and speed control is possible.

The electrical target field speed is

$$f_{period} = \frac{f_{clk}}{256 \cdot PLL\_CNT\_MAX \cdot 2^{\text{PLL\_PRESCALER}}} \quad ,$$

where f_{clk} is the system clock frequency. The adjusted field speeds are

$$f_{period,max} = \frac{f_{clk}}{256 \cdot T\_PERIOD\_MIN\_MANT[7:0] \cdot 16 \cdot 2^{\text{T\_PERIOD\_MIN\_EXP}}} \quad ,$$

$$f_{period,min} = \frac{f_{clk}}{256 \cdot T\_PERIOD\_MAX\_MANT[7:4] \cdot 256 \cdot 2^{\text{T\_PERIOD\_MAX\_EXP}}} \quad \text{and}$$

$$f_{period,emergency} = \frac{f_{clk}}{256 \cdot T\_PERIOD\_EMERGENCY\_MANT[7:4] \cdot 256 \cdot 2^{\text{T\_PERIOD\_EMERGENCY\_EXP}}} \quad .$$

Note $T\_PERIOD\_xxx\_EXP$ is written in 2th complement with $-7 \le T\_PERIOD\_xxx\_EXP \le 7$.

The interface allows to limit the slope of the internal target value when transfering from one target speed to another. This feature can be used to smooth the transition behaviour of the interface.
The slope limitation is configured by T_TARGET_PERIOD_CHANGE_LIMIT.

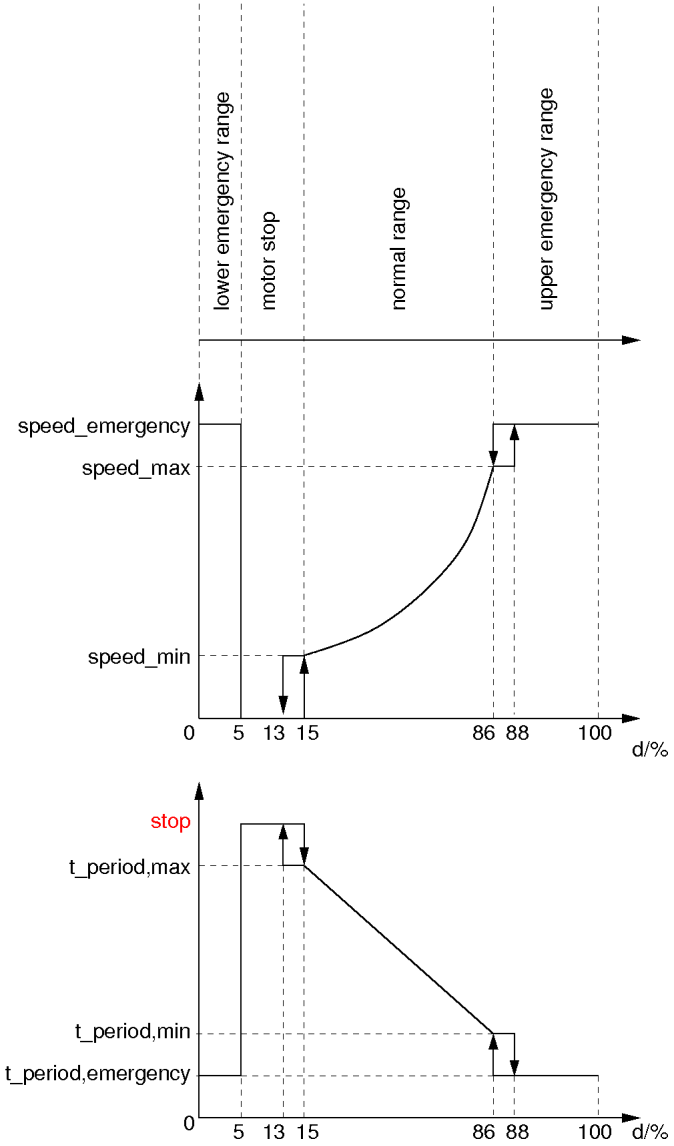

Figure 5.3.1.1-1: Goal speed vs. input duty ratio

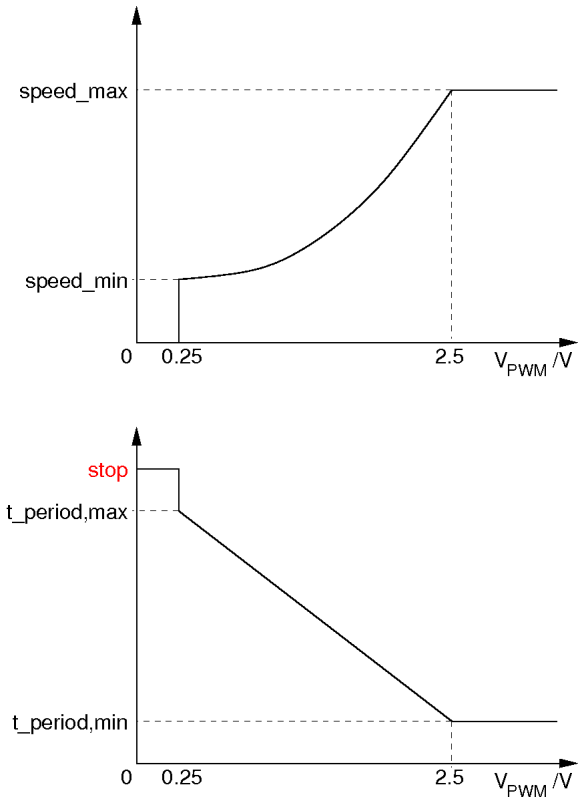

Figure 5.3.1.1-2: Goal speed vs. input voltage

Table 5.3.1.1-1: Goal speed setup registers

Register Name	*Address*	*Description*
T_PERIOD_MIN_MANT	0xDE	min electrical field period mantissa
T_PERIOD_MIN_EXP	0xDF	minimum electrical field period exponent[1)]
T_PERIOD_MAX_MANT	0xE0	maximum electrical field period, normal run mantissa
T_PERIOD_MAX_EXP	0xE1	maximum electrical field period, normal run exponent[1)]
T_PERIOD_EMERGENCY_MANT	0xE2	emergency electrical field period mantissa
T_PERIOD_EMERGENCY_EXP	0xE3	emergency electrical field period exponent[1)]
T_PERIOD_MODE_CTRL	0xE4	set field frequency control or current control
T_TARGET_PERIOD_CHANGE_LIMIT	0xCC	target period change slope limitation

[1)] 2th complement, range -8...7

Table 5.3.1.1-2: Register **T_PERIOD_MIN_MANT** (0xDE) min electrical field period mantissa

	MSB							*LSB*
Content	MIN_MANT[7:0]							
Reset value	0							
Access	R/W							
Bit Description								

Table 5.3.1.1-3: Register **T_PERIOD_MIN_EXP** (0xDF) minimum electrical field period exponent[1)]

	MSB				***LSB***
Content	MIN_EXP[3:0]				
Reset value	0				
Access	R/W				
Bit Description					

[1)] 2th complement, range -8...7

Table 5.3.1.1-4: Register **T_PERIOD_MAX_MANT** (0xE0) maximum electrical field period, normal run mantissa

	MSB							***LSB***
Content	MAX_MANT[7:4]				-	-	-	-
Reset value	0				0	0	0	0
Access	R/W				R	R	R	R
Bit Description								

Table 5.3.1.1-5: Register **T_PERIOD_MAX_EXP** (0xE1) maximum electrical field period, normal run exponent[1)]

	MSB				***LSB***
Content	MAX_EXP[3:0]				
Reset value	0				
Access	R/W				
Bit Description					

[1)] 2th complement, range -8...7

Table 5.3.1.1-6: Register **T_PERIOD_EMERGENCY_MANT** (0xE2) emergency electrical field period mantissa

	MSB							***LSB***
Content	EMERGENCY_MANT[7:4]				-	-	-	-
Reset value	0				0	0	0	0
Access	R/W				R	R	R	R
Bit Description								

Table 5.3.1.1-7: Register **T_PERIOD_EMERGENCY_EXP** (0xE3) emergency electrical field period exponent[1)]

	MSB				***LSB***
Content	EM_EXP[3:0]				
Reset value	0				
Access	R/W				
Bit Description					

[1)] 2th complement, range -8...7

Table 5.3.1.1-8: Register **T_PERIOD_MODE_CTRL** (0xE4) set field frequency control or current control

	MSB							***LSB***
Content	-	-	-	-	-	-	VM	CTRL
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R/W	R/W
Bit Description	**VM** : 0: PWM mode, 1: voltage mode **CTRL** : 0: speed control, 1: current control							

Table 5.3.1.1-9: Register **T_TARGET_PERIOD_CHANGE_LIMIT** (0xCC) target period change slope limitation

	MSB				***LSB***
Content	ACT	EXP[3:0]			
Reset value	0	0			
Access	R/W	R/W			
Bit Description	**ACT** : 0: off, 1: on **EXP[3:0]** : 2'complement exponent				

Table 5.3.1.1-10: Speed control registers

Register Name	***Address***	***Description***
FEATURE_CONTROL	0xD4	disable/enable speed-control features
DC_STATE_LAST	0xD5	duty-cycle-state 5: DC_LOWER_EMERGENCY 4: DC_UPPER_EMERGENCY 3: DC_NOK_HIGH 2: DC_OK 1: DC_NOK_LOW 0: DC_OFF

Table 5.3.1.1-11: Register **FEATURE_CONTROL** (0xD4) disable/enable speed-control features

	MSB						***LSB***
Content	MIN_VOLT_SCALER[2:0]	PID_VS_SCALED	RESET_INTEGRATOR	TEMP_CUR_DIS	D_TERM_DIS	I_TERM_DIS	
Reset value	0	0	0	0	0	0	
Access	R/W	R/W	R/W	R/W	R/W	R/W	
Bit Description	**MIN_VOLT_SCALER[2:0]** : PID_VS_SCALED=0: $\hat{v}_M = 0.54V \cdot MIN\_VOLT\_SCALER$ PID_VS_SCALED=1:fsm_scaler_min={2'b00,MIN_VOLT_SCALER,3'b000} **PID_VS_SCALED** : 0: speed controller output is VS based 1: speed controller output is fsm_voltage_scaler based **RESET_INTEGRATOR** : disable I reset if P limited **TEMP_CUR_DIS** : disable high temperature current reduction **D_TERM_DIS** : disable d-term of pid control **I_TERM_DIS** : disable i-term of pid control						

Table 5.3.1.1-12: Register **DC_STATE_LAST** (0xD5) duty-cycle-state5: DC_LOWER_EMERGENCY4: DC_UPPER_EMERGENCY3: DC_NOK_HIGH2: DC_OK1: DC_NOK_LOW0: DC_OFF

	MSB							***LSB***
Content						DC_STATE[2:0]		
Reset value	0	0	0	0	0	0		
Access	R	R	R	R	R	R		
Bit Description								

The pwm input is measured by a hardware with an accuracy of

0.8 % at an input frequency of 80 Hz to 1000 Hz

2.0 % at an input frequency of 1000 Hz to 2500 Hz

Table 5.3.1.1-13: PWM_CTRL Register

Register Name	*Address*	*Description*
PWMCTRL	0x52	PWM control

Table 5.3.1.1-14: Register **PWMCTRL** (0x52) PWM control

	MSB							*LSB*
Content	-	-	-	-	-	PWM_PD	PWM_PU	PWM_EN
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit Description	**PWM_PD** : enable PWM pull down source **PWM_PU** : enable PWM pull up source **PWM_EN** : enable PWM block							

5.3.2 Error Interface

The interface has an "ok" message when no error occurred, a "not ok" message when an internal error or over-voltage/undervoltage error occurs and 4 different error messages for motor and temperature errors. The messages are send by pulling down the PWM input for a certain time.
5.3.2-1 depicts an ok message. During the time t_2 the PWM pin is pulled down by the IC. For the rest of the time the PWM input is not pulled down and the IC observes the input PWM signal.
If an internal error occurs t_2=0 ("not ok" message).
5.3.2-2 depicts an error message. The 4 possible error messages are different in their times t_1, t_2 and the number of repeats of each message.
5.3.2-1 summarizes the different timings.
If multiple errors occur only the one with the highest priority is sent. If an error occurs or ends during a message the message first is finished before the interface starts to transmit the new message.

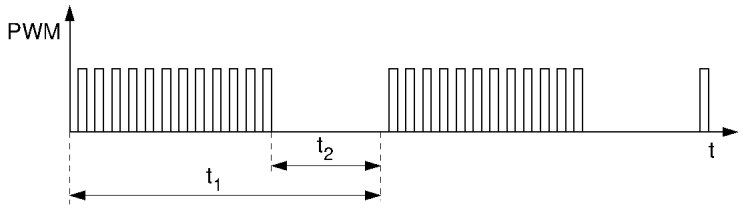

Figure 5.3.2-1: Ok message

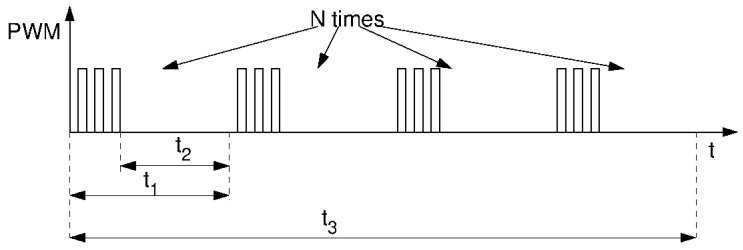

Figure 5.3.2-2: Error message

Table 5.3.2-1: Message timing parameters

message	*errors*	*t_2/s*	*t_1/s*	*N*	*t_3/s*	*priority*
not ok	V_{DS} desaturation, under voltage, over voltage	0	10	1	10	highest
1	low load	1	2	10	20	
2	rotor blocked	1.5	2.5	8	20	
3	over temperature	2	3	6	18	
4 [1)]	goal speed not achieved	2.5	3.5	5	17.5	
ok	no errors	0.5	10	1	10	lowest

[1)] This error message is delayed by one more ok message to give the motor at least 10s time to achieve the goal speed.

5.3.3 TACHO Output

This function outputs a rectangular logic level signal. Its frequency equals the fundamental frequency of the electrical motor speed. 5.3.3-1 depicts the output signal in closed loop (angle controller is active). In this case the signal is generated by push-pull output of the pin.
The behaviour in open loop can be configured by register -. If set to 0 in open loop the output is driven to GND. If set to 1 in open loop the output also toggles like shown in 5.3.3-1.
If any error occurs (see section 5.3.2) the TACHO output is actively driven high.

If the T pin is pulled to V_{VDD} the tacho pin output changes to high level. For outputting different signals at TACHO the register TACH_CFG needs to be written to the corresponding value.

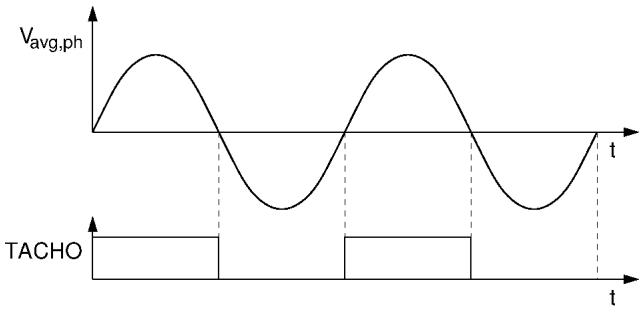

Figure 5.3.3-1: TACHO output signal

5.4 Clock System

The IC has an internal oscillator. It generates the base clock for all digital blocks. Depending on the mode of operation either all digital timing is generated from this frequency or this clock is used as base clock for synchronising to a PWM input frequency.

5.5 I/O Peripherals

5.5.1 PWM Speed Input

5.5.1-1 shows the pin structure. A comparator compares the input voltage with a threshold. The output of the comparator is connected to the pwm detection unit.
A pull up current source is connected to the supply. It pulls the pin voltage to V_{VS} when the wire breaks. This feature can also be used to detect a wire break by the ECU.
A switched pull down current source to GND is used to send an error message to the ECU.

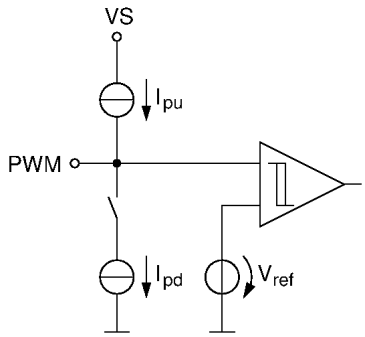

Figure 5.5.1-1: PWM speed input structure

5.5.2 Three Level Test Pin

The test pin is used to activate different lab and test modes. Apply the voltage VH,lab to activate the lab setup mode.

5.6 PMSM Motion Control Unit

5.6.1 PMSM Control Principle

The PMSM motion control unit autonomously controls the PMSM. It applies three sinusoidal voltages to the motor and controls the angle between current and voltage. The control principle in startup differs from the control in closed loop mode.

5.6.1.1 Startup

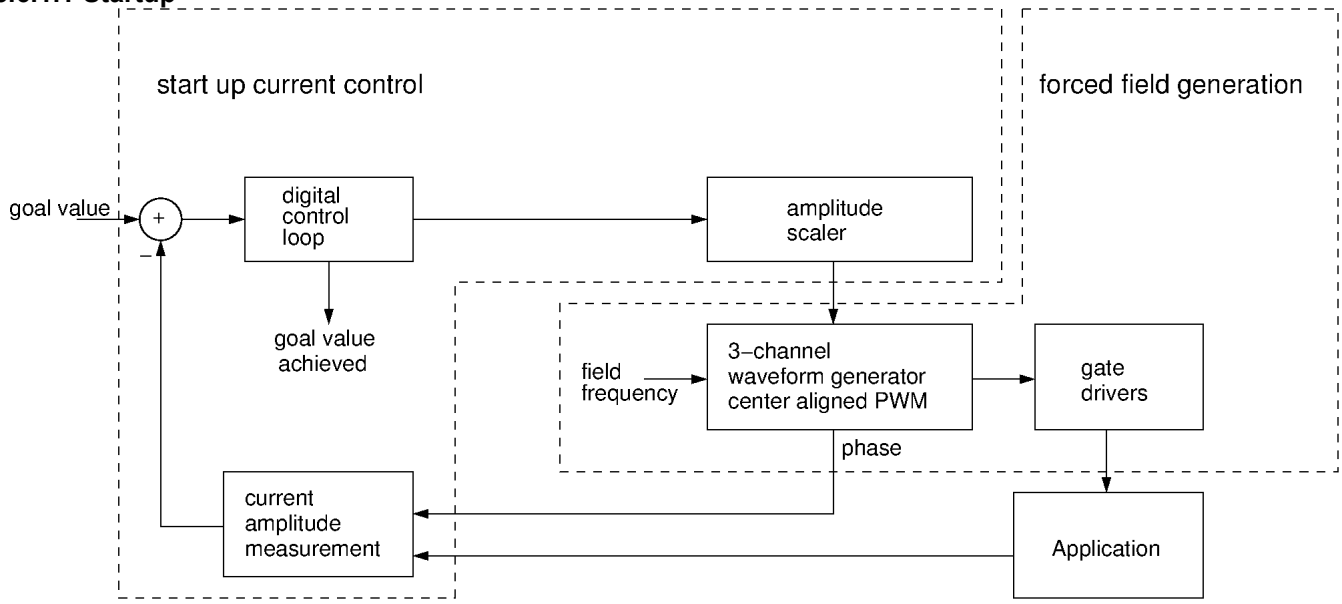

Figure 5.6.1.1-1: Start up current control

5.6.1.1-1 shows the startup current control. During the startup no angle control is active but a current control loop controls the motor current amplitude.

5.6.1.2 Closed Loop Control

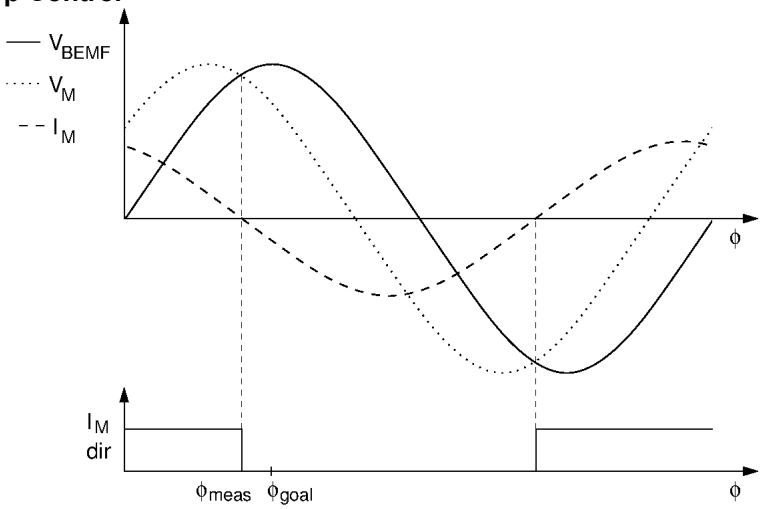

Figure 5.6.1.2-1: Closed loop control principle

The control principle is depicted in 5.6.1.2-1. The current is controlled to have a goal shift Φ_{goal} to the phase voltage. The goal of the closed loop control is explained on a single phase equivalent circuit of the motor and its averaged input voltage.
5.6.1.2-2 shows the equivalent circuit.

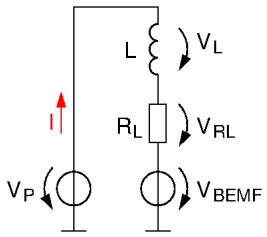

Figure 5.6.1.2-2: Single phase equivalent circuit

5.6.1.2-3 shows the corresponding voltage and current phasors in the goal state.

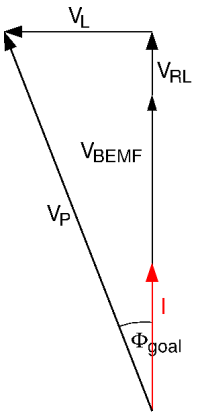

Figure 5.6.1.2-3: Phasor diagram of voltages and current of 5.6.1.2-2

The goal is to bring the motor current in phase with the BEMF voltage. To achieve this the angle Φ_{goal} needs to be adjusted depending on motor current and speed.

5.6.2 State Machine

5.6.2-1 shows the state diagram including the corresponding state transfers. The state transition from OFF state, closed loop state and failure state is set outside this state machine. The behaviour in the states is explained in the following subsections.

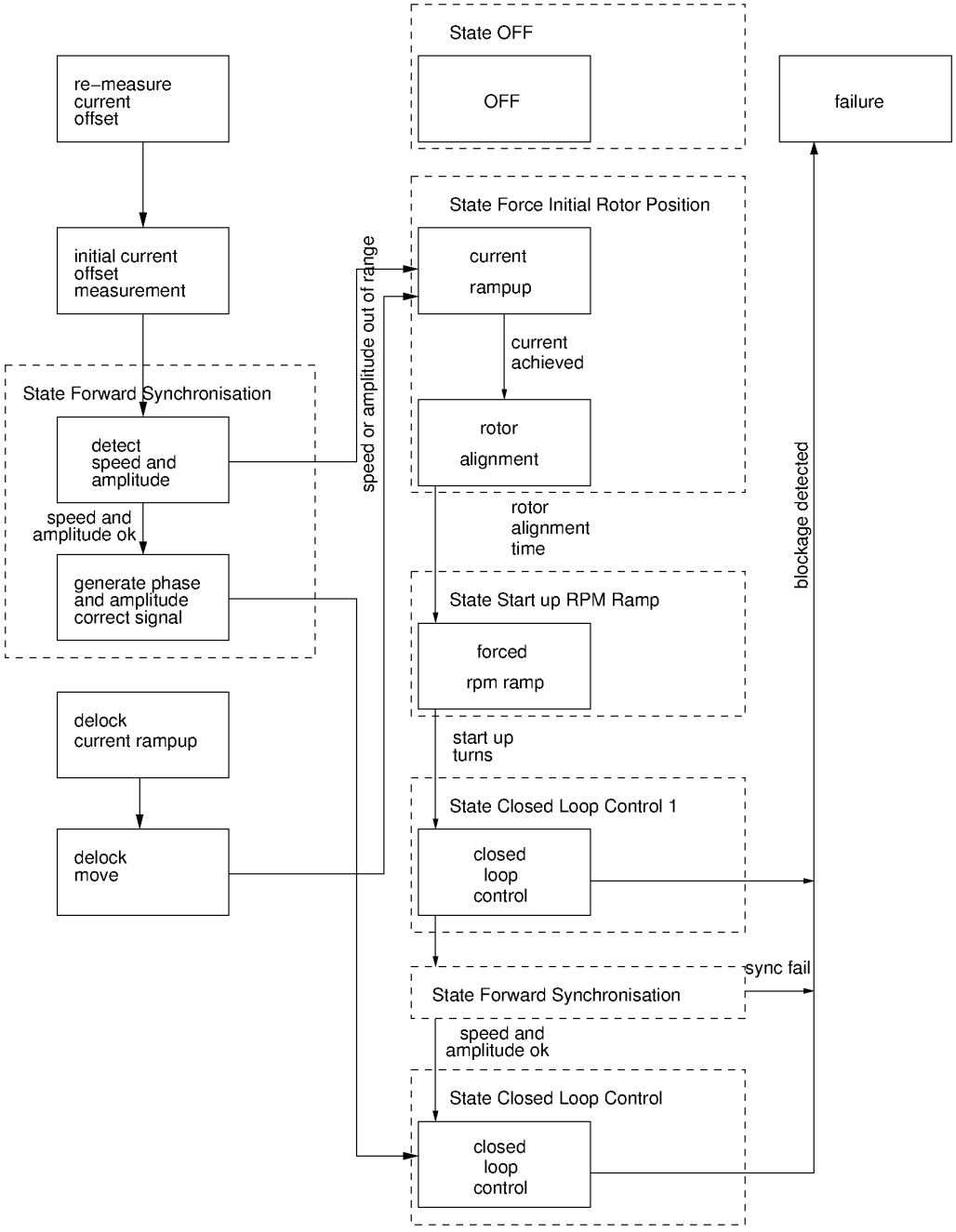

Figure 5.6.2-1: State diagram, no initial position detection

Table 5.6.2-1: State machine registers

Register Name	*Address*	*Description*
FSM_STATE	0x92	PMSM state
DIRECTION	0x25	rotation direction
EN	0x90	enable the PMSM MCU

Table 5.6.2-2: Register **FSM_STATE** (0x92) PMSM state

	MSB			*LSB*
Content	state[3:0]			
Reset value	0			
Access	R/W			
Bit Description	**state[3:0]** : PMSM state			

Table 5.6.2-3: Register **DIRECTION** (0x25) rotation direction

	MSB
Content	DIR
Reset value	0
Access	R/W
Bit Description	**DIR** : select rotation direction

Table 5.6.2-4: Register **EN** (0x90) enable the PMSM MCU

	MSB
Content	EN
Reset value	0
Access	R/W
Bit Description	**EN** : enable the MCU

5.6.2.1 State Off

In this state:

- The power bridge is at high impedance.
- All motor position measurement functions are off.

There is no automatic state transfer from this state to any other state.
A state transfer can only be initialised by setting the fsm state from outside.

5.6.2.2 State Forward Synchronisation

In this state:

- The bridges are off.
- The motor synchronisation is activated. It measures the initial fundamental frequency and amplitude. Details and parameters of the detection are described in section 5.6.10.
- The fundamental frequency base generation, section 5.6.4.6, is activated to allow the fundamental frequency measurement.
- The BEMF measurement, section 5.6.5.2, is activated to allow the fundamental amplitude measurement.
- Speed control, stall detection, current control, current direction detection and angle controller are off.

When a valid fundamental frequency and amplitude is detected the phase voltage generation, section 5.6.4, is initialised to these values. The voltage angle is initialised to have a 10 degree enhance. A state transfer to state closed loop control, section 5.6.2.8, is initialised.

When no valid fundamental frequency and/or amplitude is detected a state transfer to state current rampup is initialised.

5.6.2.3 State Current Rampup

In this state:

- The speed control is switched off.
- PWM generation, section 5.6.4.1 and averaged voltage generation, section 5.6.4.2, are on to allow a motor current to flow.
- Look up table address generation, section 5.6.4.3, is set up to a fixed value.
- Fundamental frequency base generation, section 5.6.4.6, is off to force a fixed phase voltage angle.
- Current control is on.
- CC_CURRENT_GOAL and CC_NUM_EVENTS_RUN are applied to the current control to force the start current.
- Stall detection, current direction detection, its reference, angle controller and motor synchronisation are off.
- The current ramps to its goal value CC_CURRENT_GOAL.

Details on the current control and how the inputs act on the goal current are described in section 5.6.6. When the current achieved its goal value the fsm transfers to state rotor settling, section 5.6.2.4.

Table 5.6.2.3-1: Start current control registers

Register Name	*Address*	*Description*
CC_CURRENT_GOAL	0x21	start current mantissa & exponent
CC_NUM_EVENTS_RUN	0x23	start current control speed

Table 5.6.2.3-2: Register **CC_CURRENT_GOAL** (0x21) start current mantissa & exponent

	MSB							*LSB*
Content	MANT[3:0]				EXP[3:0]			
Reset value	0				0			
Access	R/W				R/W			
Bit Description								

Table 5.6.2.3-3: Register **CC_NUM_EVENTS_RUN** (0x23) start current control speed

	MSB		*LSB*
Content	NUM[2:0]		
Reset value	0		
Access	R/W		
Bit Description			

5.6.2.4 Rotor Settling

In this state:

- The speed control is switched off.
- PWM generation, section 5.6.4.1 and averaged voltage generation, section 5.6.4.2, are on to allow a motor current to flow.
- Look up table address generation, section 5.6.4.3, is set to a fixed value.
- Fundamental frequency base generation, section 5.6.4.6, is off to force a fixed phase voltage angle.
- Current control is on.
- CC_CURRENT_GOAL and CC_NUM_EVENTS_RUN are applied to the current control to force the start current.
- Stall detection, current direction detection, its reference, angle controller and motor synchronisation are off.
- A counter is started to measure the time.

When the time achieves the value $t_{settle} \cdot 10\,ms$ where $t_{settle} = T\_SETTLE\_ROTOR\_MANT \cdot 2^{T\_SETTLE\_ROTOR\_EXP}$ can be set up with T_SETTLE_ROTOR, the state changes to start up RPM ramp, section 5.6.2.5.

Table 5.6.2.4-1: Rotor settling set up registers

Register Name	*Address*	*Description*
T_SETTLE_ROTOR	0x26	rotor settling time

Table 5.6.2.4-2: Register **T_SETTLE_ROTOR** (0x26) rotor settling time

	MSB				*LSB*
Content	MANT[1:0]		EXP[2:0]		
Reset value	0		0		
Access	R/W		R/W		
Bit Description	**MANT[1:0]** : Mant **EXP[2:0]** : Exp				

5.6.2.5 State Startup RPM Ramp

In this state:

- The speed control is off.
- The phase voltage generation is on.
- The configuration data PLL_PRESCALER_SU and PLL_INC_SCAL_MAX is input to the fundamental frequency base generation to set initial speed and speed ramp.
- The current limitation is active.
- The configuration data CC_CURRENT_GOAL and CC_NUM_EVENTS_RUN is input to the current limitation to set its value and speed.
- The stall detection is off.
- The current direction detection and its reference are on.
- The angle controller is off.
- The motor synchronisation is off.

A counter counts the number of electrical turns in start up. When its value equals start_up_turns the state changes to closed loop control.

The start up speed is:

$$f_{period,start} = \frac{f_{clk}}{256 \cdot 2048 \cdot 2^{PLL\_PRESCALER\_SU}} \quad \text{where} \quad -7 \le PLL\_PRESCALER\_SU \le 7 \quad .$$

Note the prescaler is adjusted using sign and absolute value notation.
Please refer to section 5.6.4.4 for details on the speed ramp generation.

Table 5.6.2.5-1: Start up ramp configuration registers

Register Name	*Address*	*Description*
PLL_PRESCALER_SU	0x27	start up prescaler
START_UP_TURNS	0x29	number of el. turns in the speed ramp state
PLL_INC_SCAL_MAX	0x28	speed ramp parameter

Table 5.6.2.5-2: Register **PLL_PRESCALER_SU** (0x27) start up prescaler

	MSB				***LSB***
Content	sign	su[3:0]			
Reset value	0	0			
Access	R/W	R/W			
Bit Description	**sign** : 0: positive, 1: negative				

Table 5.6.2.5-3: Register **START_UP_TURNS** (0x29) number of el. turns in the speed ramp state

	MSB				***LSB***
Content	TURNS[4:0]				
Reset value	0				
Access	R/W				
Bit Description	**TURNS[4:0]** : number of speed ramp electrical turns				

Table 5.6.2.5-4: Register **PLL_INC_SCAL_MAX** (0x28) speed ramp parameter

	MSB			***LSB***
Content	SCAL[3:0]			
Reset value	0			
Access	R/W			
Bit Description	**SCAL[3:0]** : speed ramp slope			

5.6.2.6 State Closed Loop Control 1

This state is an intermediate state before a re-synchronisation is initiated. The behaviour in this state is exactly the same as described in section 5.6.2.8.
For details on the re-synchronisation and parametrisation refer to sections 5.6.7.4 and 5.6.10.

5.6.2.7 State Forward Synchronisation

This state allows the detection of a rotor blockage after start up as described in section 5.6.7.4. The synchronisation behaviour is the same as described in sections 5.6.2.2 and 5.6.10.
When the re-synchronisation was successfully state closed loop control is activated. When not the fsm transfers to state off.

5.6.2.8 State Closed Loop Control

In this state:

- The speed control is on.
- The phase voltage generation is on completely.
- The current limitation is on.
- The configuration data CC_CURRENT_GOAL_CLOSED and CC_NUM_EVENTS_RUN_CLOSED is input to the current limitation.
- The stall detection is on.
- The current direction detection and its reference are on.
- The angle controller is on.
- The motor synchronisation is off.

If the stall detection detects a stall the state is changed to OFF.

Table 5.6.2.8-1: Closed loop current control registers

Register Name	*Address*	*Description*
CC_CURRENT_GOAL_CLOSED	0x22	current limitation value
CC_NUM_EVENTS_RUN_CLOSED	0x24	current limitation speed
CC_CURRENT_GOAL_CLOSED_INITIAL	0xD9	current limitation value when the speed controller is activated

Table 5.6.2.8-2: Register **CC_CURRENT_GOAL_CLOSED** (0x22) current limitation value

	MSB							*LSB*
Content	MANT[3:0]				EXP[3:0]			
Reset value	0				0			
Access	R/W				R/W			
Bit Description	**MANT[3:0]** : mantissa **EXP[3:0]** : exponent							

Table 5.6.2.8-3: Register **CC_NUM_EVENTS_RUN_CLOSED** (0x24) current limitation speed

	MSB		*LSB*
Content	NUM[2:0]		
Reset value	0		
Access	R/W		
Bit Description			

Table 5.6.2.8-4: Register **CC_CURRENT_GOAL_CLOSED_INITIAL** (0xD9) current limitation value when the speed controller is activated

	MSB							*LSB*
Content	MANT[3:0]				EXP[3:0]			
Reset value	0				0			
Access	R/W				R/W			
Bit Description								

5.6.3 Speed Control

The motor speed is controlled by a PID controller. 5.6.3-1 shows the topology. The controller measures the time difference t_{diff} between an electrical turn and an electrical turn at target speed. The measured difference $n_{diff} = t_{diff} f_{clk}$ is used to periodically calculate a new control value. The new control value is

$$ctrl_{new} = \mathrm{sum}_{n_{diff}} \cdot 2^{\mathrm{T\_PERIOD\_CONTROL\_KI\_EXP}} + n_{diff} \cdot 2^{\mathrm{T\_PERIOD\_CONROL\_KP\_EXP}} + (n_{diff} - n_{diff,last}) \cdot 2^{\mathrm{T\_PERIOD\_CONTROL\_KD\_EX}}$$

with $\mathrm{sum}_{n_{diff}} = \mathrm{sum}_{n_{diff}} + n_{diff}$ and $n_{diff,last} = n_{diff}$.
The period for the calculation is tc,speed.
Note the control always refers to the electrical field period. If the motor has more than one pole pair the electrical target period setup should consider the number of pole pairs.

The control value can be set up to be either the voltage scaler FSM_VOLTAGE_SCALER or a voltage amplitude V_M .
We recommend to use the voltage amplitude V_M as then VS variations are cancelled out better.
The control value is selected by FEATURE_CONTROL.

An anti windup feature is also included and can be activated by FEATURE_CONTROL.

When the voltage amplitude V_M is selected as control value the minimum control value can be selected by FEATURE_CONTROL and the maximum control value can be selected by MAX_VA_VOLTAGE.

When the voltage scaler FSM_VOLTAGE_SCALER is selected as control value only the minimum control value can be selected by FEATURE_CONTROL.

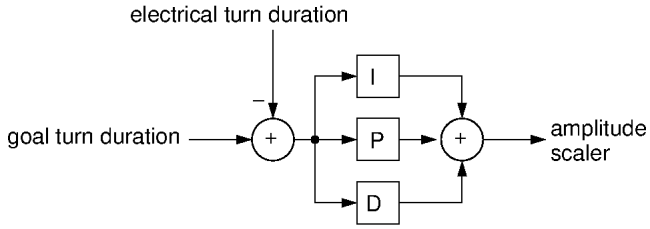

Figure 5.6.3-1: Speed controller topology

Table 5.6.3-1: Speed controller registers

Register Name	*Address*	*Description*
T_PERIOD_CONTROL_KP_EXP	0xE5	exponent of p term of the speed controller
T_PERIOD_CONTROL_KI_EXP	0xE6	exponent of i term of the speed controller
T_PERIOD_CONTROL_KD_EXP	0xE7	exponent of d term of the speed controller
MAX_VA_VOLTAGE	0xC8	upper voltage amplitude limitation of the speed controller

Table 5.6.3-2: Register **T_PERIOD_CONTROL_KP_EXP** (0xE5) exponent of p term of the speed controller

	MSB			*LSB*
Content	KP[3:0]			
Reset value	0			
Access	R/W			
Bit Description				

Table 5.6.3-3: Register **T_PERIOD_CONTROL_KI_EXP** (0xE6) exponent of i term of the speed controller

	MSB			*LSB*
Content	KI[3:0]			
Reset value	0			
Access	R/W			
Bit Description				

Table 5.6.3-4: Register **T_PERIOD_CONTROL_KD_EXP** (0xE7) exponent of d term of the speed controller

	MSB			*LSB*
Content	KD[3:0]			
Reset value	0			
Access	R/W			
Bit Description				

Table 5.6.3-5: Register **MAX_VA_VOLTAGE** (0xC8) upper voltage amplitude limitation of the speed controller

	MSB							***LSB***
Content	MAX_VA[7:0]							
Reset value	0							
Access	R/W							
Bit Description								

5.6.4 Phase Voltage Generation

The phase voltage generation consists of the blocks PWM generation, averaged voltage generation, look up table address generation and fundamental frequency base generation. 5.6.4-1 shows the principle.

- The fundamental frequency base generation generates a scalable wide range time base for the fundamental output frequency

$$f_{fund,b} = \frac{f_{clk} \cdot pll\_increment}{pll\_cnt\_max \cdot 2^{pll\_prescaler-1}}$$

- The look up table address generation is triggered with the variable frequency and generates an address for the look up table
- The averaged voltage generation takes the address and generates the scaled averaged sine signals
- The PWM generation transforms the scaled averaged signals into PWM modulated output signals. The trigger signals for the current direction measurement and current measurement are generated in this block, too. The fundamental frequency of the averaged motor voltage is $f_{fund} = \frac{f_{fund,b}}{tab\_length}$, where tab_length is the address range of the look up table. The following sections describe these four functions more in detail.

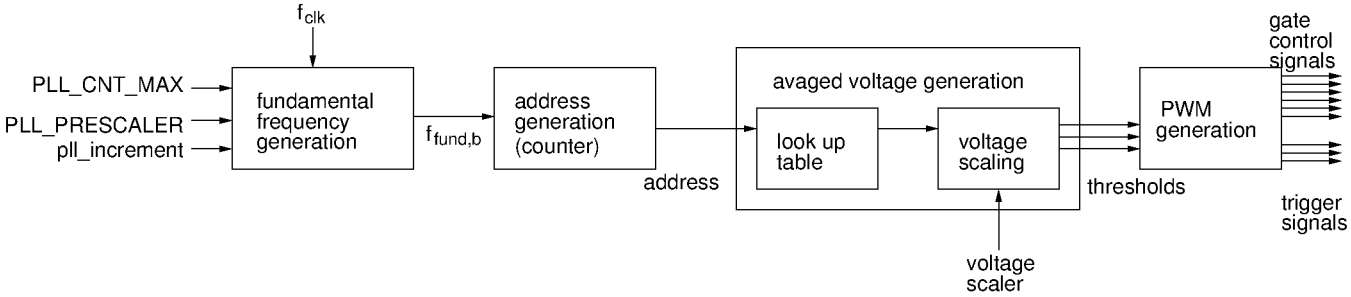

Figure 5.6.4-1: Phase voltage generation principle

Table 5.6.4-1: Phase voltage generation registers

Register Name	***Address***	***Description***
FSM_VOLTAGE_SCALER	0x93	output voltage relative amplitude
PLL_PRESCALER	0x38	period exponent
PLL_CNT_MAX_H	0x39	period mantissa
PLL_CNT_MAX_L	0x3A	period mantissa

Table 5.6.4-2: Register **FSM_VOLTAGE_SCALER** (0x93) output voltage relative amplitude

	MSB							***LSB***
Content	scaler[7:0]							
Reset value	0							
Access	R/W							
Bit Description								

Table 5.6.4-3: Register **PLL_PRESCALER** (0x38) period exponent

	MSB				***LSB***
Content	SIGN	EXP[3:0]			
Reset value	0	0			
Access	R/W	R/W			
Bit Description	**SIGN** : prescaler sign **EXP[3:0]** : exponent				

Table 5.6.4-4: Register **PLL_CNT_MAX_H** (0x39) period mantissa

	MSB						***LSB***
Content	CNT[14:8]						
Reset value	0						
Access	R/W						
Bit Description	**CNT[14:8]** : filtered period mantissa						

Table 5.6.4-5: Register **PLL_CNT_MAX_L** (0x3A) period mantissa

	MSB							***LSB***
Content	CNT[7:0]							
Reset value	0							
Access	R/W							
Bit Description	**CNT[7:0]** : filtered period mantissa							

5.6.4.1 PWM Generation

Table 5.6.4.1-1: PWM generation parameters

parameter	***value***
pwm_max	358

5.6.4.1.1 Principle

5.6.4.1.1-1 shows the principle of the center aligned PWM generation.
An up/down counter counts up and down between a fixed value pwm_max and 0. Every time the counter reaches one of these two values it changes its direction.
The counter base frequency is the system clock frequency f_{clk} . The resulting PWM output frequency is

$$f_{PWM} = \frac{f_{clk}}{pwm\_\max+1} \quad .$$

The three input signals pwm_th_1, pwm_th_2 and pwm_th3 are the scaled averaged signals from the averaged voltage generation. The high side bridge gate control signals are toggled when the counter achieves the corresponding threshold.

The thresholds for the low side gate control signals are derived from pwm_th_1, pwm_th_2 and pwm_th3 by adding the value pwm_t_dead to them. It can be configured using register pwm_t_dead. When a low side gate threshold is equal to or larger than pwm_max the corresponding gate control signal will stay at low.

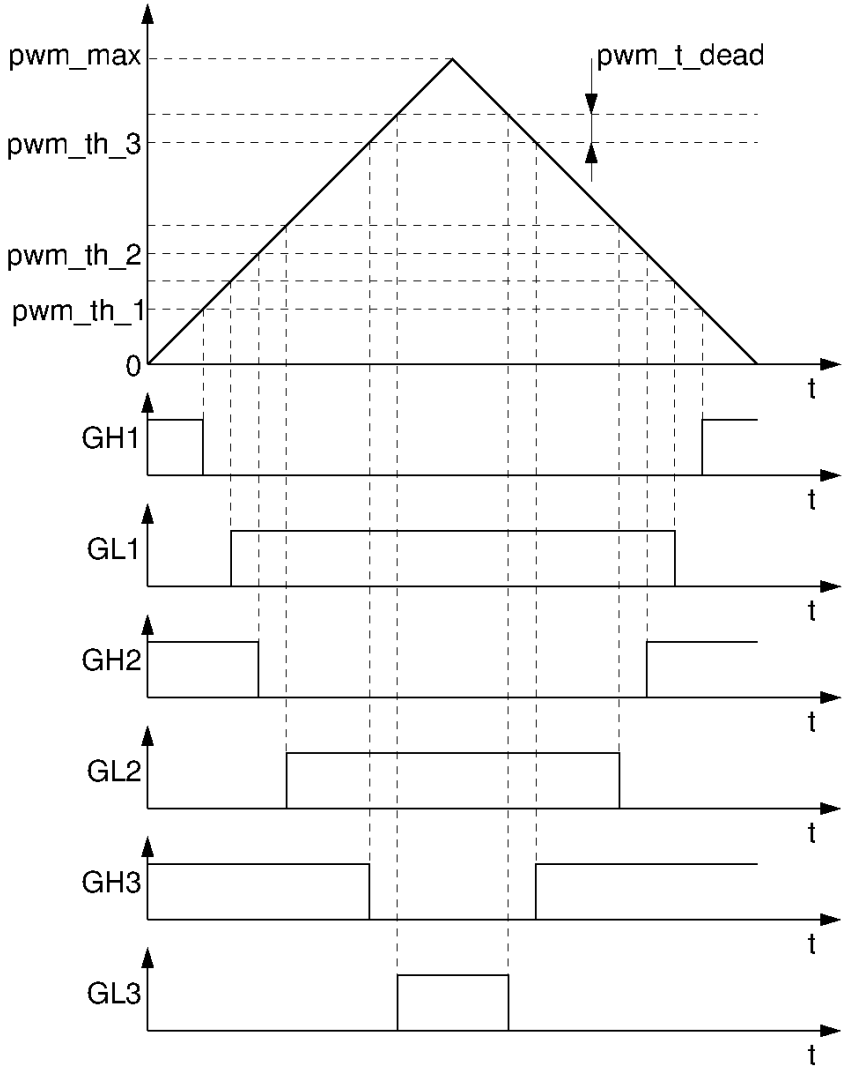

Figure 5.6.4.1.1-1: Center aligned PWM principle

5.6.4.1.2 Current Measurement Trigger Generation

During each PWM cycle three current measurement triggers are generated, 5.6.4.1.2-1.
This section only describes the trigger generation. The current measurements and calculations are described more in detail in section 5.6.6.

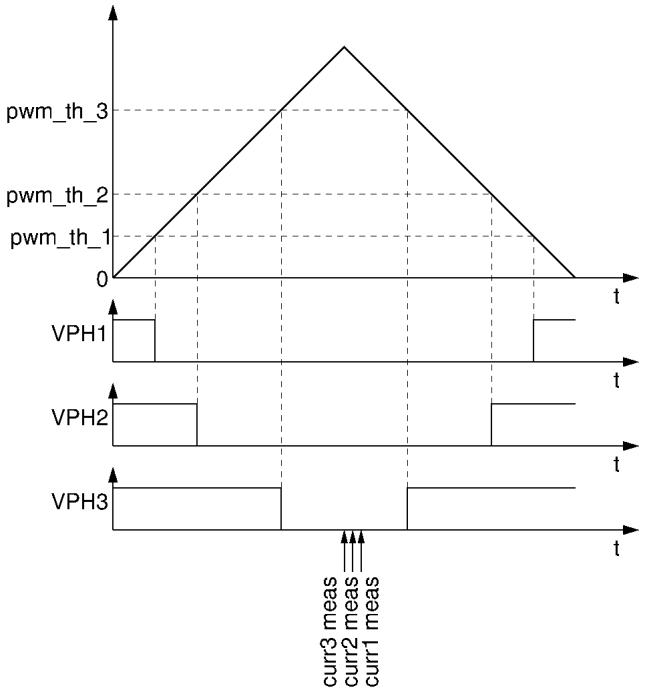

Figure 5.6.4.1.2-1: Current measurement events

5.6.4.2 Averaged Voltage Generation

This block gets the input address_i from the look up table address generation, section 5.6.4.3. From the address three addresses with 120 degree phase shift are calculated.
The addresses are fed to a look up table, section 5.6.4.2.1. The three output signals of table are scaled using the voltage scaler input scaler_i.
The scaled results are output to the PWM generation.
The thresholds are calculated by

$$val\_x\_0 = (tab\_value - 179) \cdot \frac{FSM\_VOLTAGE\_SCALER}{256} + 179 \quad ,$$

where tab_value is the value read from the look up table.

5.6.4.2.1 Look up Table

The loop up table has a length of 256 elements. It stores a sinusoidal signal with 9 bit resolution.

5.6.4.3 Look up Table Address Generation

The address generation is a counter. It is clocked with the overflow signal of the fundamental frequency base generation. The max. angle resolution of the system is
360°/256=1.4°.

5.6.4.4 Speed Ramp Generator

This block is used to generate the speed ramp during open loop operation. It operates as follows:
at each timer tick (overflow) of the fundamental frequency base generation a counter is increased.
When this counter reaches the value inc_ovf_num_i the value pll_cnt_max is re-calculated by

$$PLL\_CNT\_MAX\ (new) = PLL\_CNT\_MAX\ (old) \cdot (1 - 2^{INC\_SCAL\_MAX})$$

5.6.4.5 Pll Prescaler Adjust Unit

This block automatically adjusts the prescaler of the fundamental frequency base generation in a way that the MSB is always zero and MSB-1 is always one. This assures a maximum frequency resolution.

5.6.4.6 Fundamental Frequency Base Generation

This block generates a widely variable output base frequency for the look up table. The output frequency is

$$f_{fund,b} = \frac{f_{clk}}{\text{PLL\_CNT\_MAX} \cdot 2^{\text{PLL\_PRESCALER-1}}} \quad .$$

The prescaler can be positive or negative.

5.6.5 ADC Calculations

This section describes the motor specific calculations that are made from the ADC results.

5.6.5.1 ADC Current Measurement

The IC measures the three phase currents.
5.6.5.1-1 shows the measurement sequence. During each PWM cycle for every phase a current measurement is done.
From the current measurements the motor current amplitude is calculated and stored in MOTOR_CURRENT_H:MOTOR_CURRENT_L.

Table 5.6.5.1-1: Current measurement registers

Register Name	*Address*	*Description*
MOTOR_CURRENT_H	0x3B	calculated motor current amplitude
MOTOR_CURRENT_L	0x3C	calculated motor current amplitude
CUR_MEAS_OFFSET_CTRL	0x58	

Table 5.6.5.1-2: Register **MOTOR_CURRENT_H** (0x3B) calculated motor current amplitude

	MSB			*LSB*
Content	CURRENT[11:8]			
Reset value	0			
Access	R			
Bit Description	**CURRENT[11:8]** : higher bits			

Table 5.6.5.1-3: Register **MOTOR_CURRENT_L** (0x3C) calculated motor current amplitude

	MSB							*LSB*
Content	CURRENT[7:0]							
Reset value	0							
Access	R							
Bit Description	**CURRENT[7:0]** : lower bits							

Table 5.6.5.1-4: Register **CUR_MEAS_OFFSET_CTRL** (0x58)

	MSB	*LSB*
Content	INC_OFFS	EN_OFFS
Reset value	0	1
Access	R/W	R/W
Bit Description	**INC_OFFS** : increase forced current measurement offset **EN_OFFS** : enable forced current measurement offset	

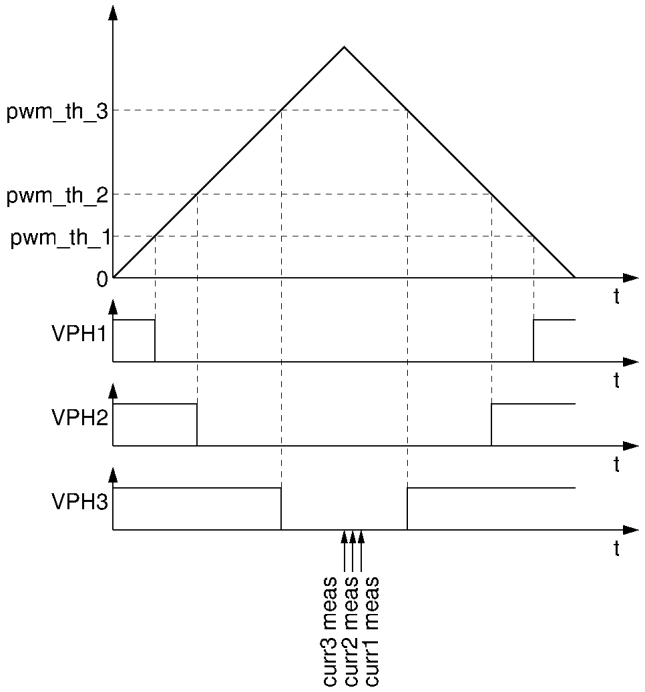

Figure 5.6.5.1-1: Current measurement principle

5.6.5.1.1 Current Filter

The current amplitude is filtered with a IIR filter with the function

$$f_{filtered} = f_{filtered} - (I - I_{filtered}) \cdot 2^{-\text{ADC\_CURR\_FILT\_FACTOR}}$$,

where $I_{filtered}$ is the filtered output current and I is the unfiltered input current.

The filter funtion is calculated each time the address of the look up table, section 5.6.4.3 changes. Hence the filter response is rotor frequency dependent and the "averaging" is done over a constant angle interval independent from the motor speed.

All current based functions (e.g. high speed stall detection, current control, angle control) use the filtered current $f_{filtered}$.

Table 5.6.5.1.1-1: Current filter registers

Register Name	*Address*	*Description*
ADC_CURR_FILT_FACTOR	0x20	current filter parameter

Table 5.6.5.1.1-2: Register **ADC_CURR_FILT_FACTOR** (0x20) current filter parameter

	MSB			*LSB*
Content	FACTOR[3:0]			
Reset value	0			
Access	R/W			
Bit Description				

5.6.5.2 BEMF Measurement and Calculation

5.6.5.2.1 Phase Voltage Measurement

The three phase voltages $V_{M[1]}$, $V_{M[2]}$ and $V_{M[3]}$ are measured only during motor synchronisation. They are used to calculate the three BEMF voltages during synchronisation. In this case the ADC periodically measures the three phase voltages without any additional synchronisation mechanism.

5.6.5.2.2 BEMF Calculation

The three BEMF voltages are calculated from the phase voltages by

$$\text{bemf\_1} = V_{M[1]} - \frac{V_{M[1]} + V_{M[2]} + V_{M[3]}}{3} \quad .$$

$$\text{bemf\_2} = V_{M[2]} - \frac{V_{M[1]} + V_{M[2]} + V_{M[3]}}{3} \quad .$$

$$\text{bemf\_3} = V_{M[3]} - \frac{V_{M[1]} + V_{M[2]} + V_{M[3]}}{3} \quad .$$

They are used during synchronisation, section 5.6.10.

5.6.6 Current Control/Limitation

The current control/limitation is a ramp control. Its principle is shown in 5.6.6-1. Each time the control loop is executed the voltage scaler is increased or decreased by 1 depending on the current and the motor/generator mode.

The trigger of the control loop is as follows. An event with the motor speed dependent frequency $f_{fund,b}$, see section 5.6.4.6, triggers a counter. The counter counts from zero to $2^{\text{CC\_NUM\_EVENTS\_RUN}}$. When the counter achieves this value the counter is reset and the current control loop is executed one time. Hence for large values CC_NUM_EVENTS_RUN the current control loop is slowed down.

CC_NUM_EVENTS_RUN can be adjusted separately for motor start with register CC_NUM_EVENTS_RUN and for closed loop with register CC_NUM_EVENTS_RUN_CLOSED.

The value current_max is also adjusted separately with register CC_CURRENT_GOAL for motor start up and with CC_CURRENT_GOAL_CLOSED for closed loop control.

The value scaler comes from the speed control.

Typically the current control operates as a control during start up and as a limitation during closed loop operation.

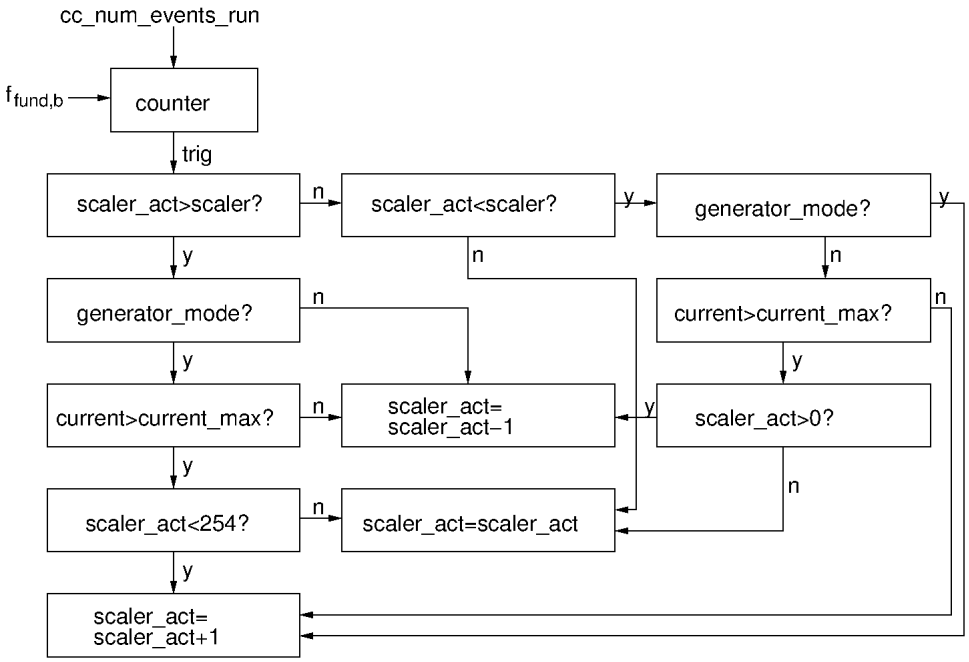

Figure 5.6.6-1: Current control principle

5.6.7 Stall Detection

Table 5.6.7-1: Stall detection registers

Register Name	*Address*	*Description*
STALL_DETECTION_CFG	0x36	enable/disable the different stall detection mechanisms
STALL_DET_STAT	0x3D	detected stalls

Table 5.6.7-2: Register **STALL_DETECTION_CFG** (0x36) enable/disable the different stall detection mechanisms

	MSB			*LSB*
Content	stall_sync_en	stall_cm_en	stall_curr_en	stall_speed_en
Reset value	0	0	0	0
Access	R/W	R/W	R/W	R/W
Bit Description	**stall_sync_en** : enable re-synchronisation after start up **stall_cm_en** : enable motor constant based stall detection **stall_curr_en** : enable current slope based stall detection **stall_speed_en** : enable field speed based stall detection			

Table 5.6.7-3: Register **STALL_DET_STAT** (0x3D) detected stalls

	MSB			LSB
Content	stall_sync	stall_cm	stall_curr	stall_speed
Reset value	0	0	0	0
Access	R/W	R/W	R/W	R/W
Bit Description	**stall_sync** : re-synchronisation after start up failed **stall_cm** : motor constant based stall detection triggered **stall_curr** : current slope based stall detection triggered **stall_speed** : field speed based stall detection triggered			

5.6.7.1 Current Slope Based Stall Detection

The high speed stall detection stores the measured current amplitudes in a ring buffer for one complete electrical turn. After the buffer is filled the detection unit continuously measures the actual current amplitude I_{ADC} , compares it with the corresponding value in the buffer $I_{ADC,last,turn}$ and updates the buffer.
When $|I_{ADC} - I_{ADC,last,tur}| > I_{stall}$ a motor stall is detected. I_{stall} is adjusted with register stall_det_threshold.
The high speed stall detection requires a minimum motor speed to be able to detect the current slope during one electrical turn. For low speed a different principle is used.

Table 5.6.7.1-1: Current slope based stall detection registers

Register Name	Address	Description
STALL_DET_THRSHLD	0x32	Stall Detection Limit

Table 5.6.7.1-2: Register **STALL_DET_THRSHLD** (0x32) Stall Detection Limit

	MSB							LSB
Content	MANT[3:0]				EXP[3:0]			
Reset value	0				0			
Access	R/W				R/W			
Bit Description								

5.6.7.2 Field Speed Based Stall Detection

When the rotor is blocked typically a too big angle between current and voltage is measured. As a result the angle controller will increase the field speed to the maximum possible value.
The stall detection uses this effect. When the speed exceeds a certain limit a stall is detected.
The max. speed is adjusted according to section 5.6.4.6.
The stall detection uses the min. prescaler of section 5.6.10 as max. speed configuration.

Additionally a stall is detected when the speed falls below a lower limit configured with PLL_PRESCAL_MAX_STALL.
The configuration of the lower limit is done equivalent to 5.3.1.1.

Table 5.6.7.2-1: Field speed based stall detection registers

Register Name	Address	Description
PLL_PRESCAL_MAX_STALL	0x37	prescaler stall detection

Table 5.6.7.2-2: Register **PLL_PRESCAL_MAX_STALL** (0x37) prescaler stall detection

	MSB			***LSB***
Content	PRESCAL[3:0]			
Reset value	0			
Access	R/W			
Bit Description	**PRESCAL[3:0]** : prescaler in 2 complement			

5.6.7.3 Motor Constant Based Stall Detection

This block verifies the applied voltage amplitude with $c_m \cdot f_{el}$. If the difference between these two values exceeds a limit the applied voltage does not fit to the motor speed. This results in a detected stall. 5.6.7.3-1 shows the operation principle of this kind of stall detection

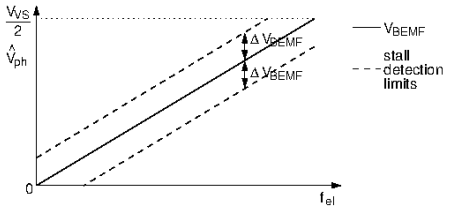

Figure 5.6.7.3-1: Motor constant based stall detection principle

The block is parametrised as follows:

$$c_m = \frac{c_m \cdot f_{clk} \cdot \sqrt{2}}{4 \cdot 1.14 \cdot \mathrm{div}_V \cdot V_{ref,ADC}} \quad ,$$

where $c_m = \frac{V_{pp} \cdot T_{el}}{2 \cdot \sqrt{6}}$ is the field speed based motor constant, f_{clk} is the system clock, N_{ADC} is the ADC resolution, div_V is the BEMF divider ratio and $V_{ref,ADC}$ is the ADC reference voltage.
cm is set up using fractional writing $c_m = \mathrm{CM\_MANT} \cdot 2^{\mathrm{CM\_EXP}}$.

The max. deviation from the from $c_m \cdot f_{el}$ is parametrised by

$$\mathrm{SVM\_VOLTAGE\_SCALER\_OFFSET}[7:0] = \frac{\Delta V_{BEMF} \cdot 32 \cdot 2^{\mathrm{N\_ADC}}}{\mathrm{div}_V \cdot V_{ref,ADC}} \quad ,$$

where ΔV_{BEMF} is the max. allowed deviation between the generated phase voltage amplitude and $c_m \cdot f_{el}$.

Table 5.6.7.3-1: Motor constant based stall detection registers

Register Name	***Address***	***Description***
CM	0x33	Motor constant
SVM_VOLTAGE_SCALER_OFFSET	0x34	Voltage scaler offset

Table 5.6.7.3-2: Register **CM** (0x33) Motor constant

	MSB							***LSB***
Content	CM_MANT[3:0]				CM_EXP[3:0]			
Reset value	0				0			
Access	R/W				R/W			
Bit Description								

Table 5.6.7.3-3: Register **SVM_VOLTAGE_SCALER_OFFSET** (0x34) Voltage scaler offset

	MSB							***LSB***
Content	OFFSET[7:0]							
Reset value	0							
Access	R/W							
Bit Description	**OFFSET[7:0]** : SVM voltage scaler offset							

5.6.7.4 Synchronisation Based Stall Detection

This principle is used to detect a rotor blockage after start up. 5.6.7.4-1 depicts the principle.
After the forced speed ramp the closed loop state 1 is entered for an adjustable time. This state is introduced to allow further acceleration after the forced speed ramp. In closed loop state 1 the behaviour is exactly the same as in the closed loop control. After the adjustable time the motor phases are switched to high impedance and a synchronisation procedure according to section 5.6.10 is started. It uses the same parameters as described in section 5.6.10.
If the synchronisation procedure was successful the closed loop state is entered. If the procedure was not detected a rotor blockage is detected and the motor is stopped.

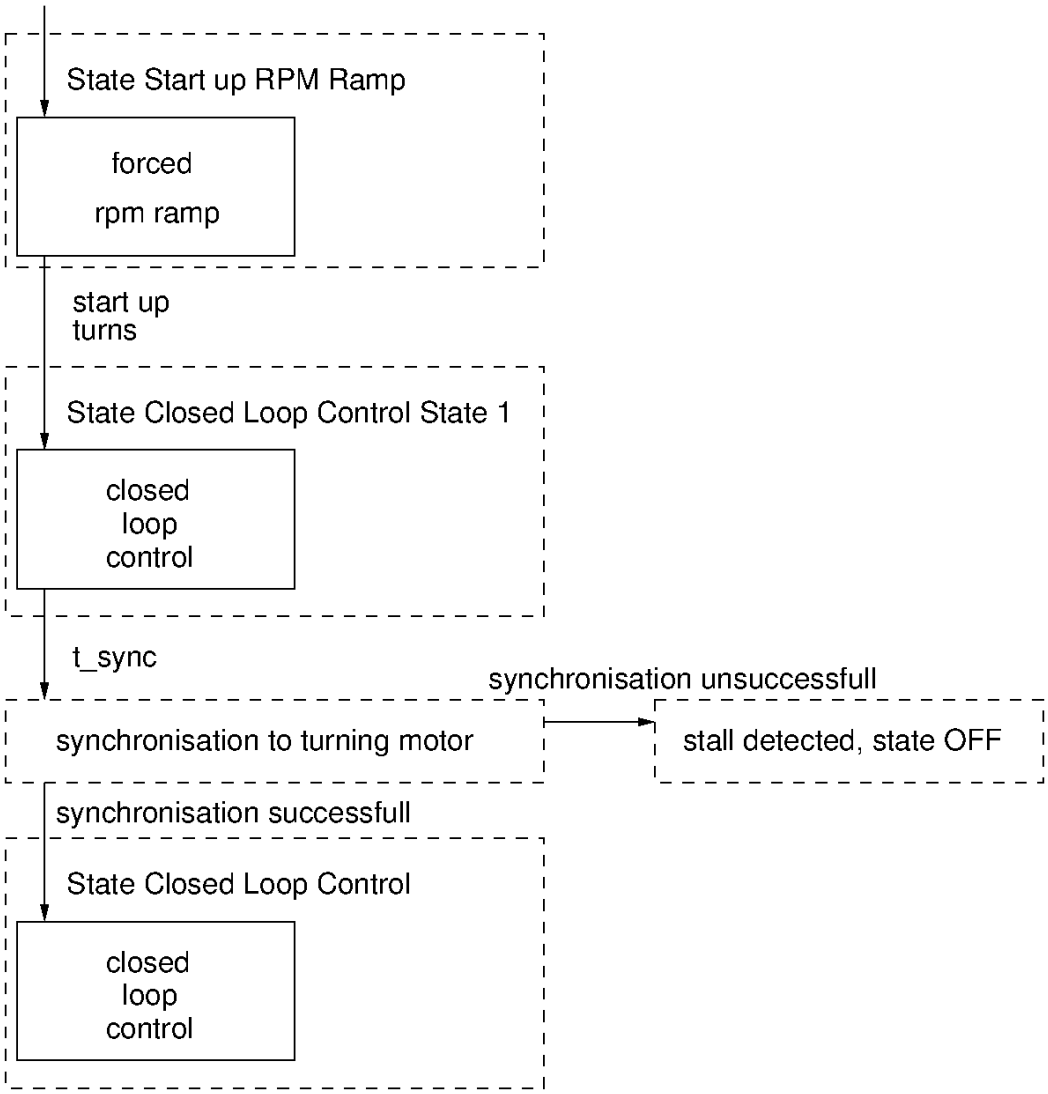

Figure 5.6.7.4-1: Synchronisation based stall detection principle

The duration of the closed loop state 1 is:

$$t_{\text{closed\_loop\_state\_1}} = 2^{\text{T\_SYNC\_CHECK}} \cdot 80\,ms \quad .$$

5.6.7.5 Current Zero Crossing Observation

This block counts the number of electrical turns in which no valid current zero crossing has been detected. At the beginning of each electrical turn a counter counts up by one. When a valid current zero crossing has been detected the counter is reset to zero.

When the counter value achieves a threshold NUM_{MAX} defined by NUM_TURNS_ZERO_CURRENT the motor is stopped and fsm state is set to 0xf.

The threshold is calculated by NUM_{MAX}=2^NUM_TURNS_ZERO_CURRENT with 1<=NUM_TURNS_ZERO_CURRENT<=6. The mechanism can be disabled by setting NUM_TURNS_ZERO_CURRENT to 7.

Table 5.6.7.5-1: Current Zero Crossing Observation Registers

Register Name	*Address*	*Description*
NUM_TURNS_ZERO_CURRENT	0x9E	

Table 5.6.7.5-2: Register **NUM_TURNS_ZERO_CURRENT** (0x9E)

	MSB		*LSB*
Content	NUM[2:0]		
Reset value	0		
Access	R/W		
Bit Description	**NUM[2:0]** : max. number of electrical turns without valid crossing detection		

5.6.8 Current Direction Detection

The current direction detection consists of an automatic window generation and a current direction sampling block. The current direction is measured at each motor phase.

The current direction at each phase is extracted from the phase current measurements at each output PWM cycle.

5.6.9 Angle Controller

5.6.9-1 shows the principle of the angle controller. The control loop is executed each time a measurement window is closed.

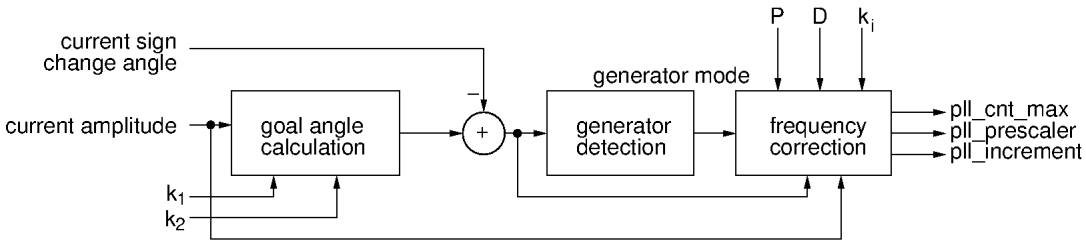

Figure 5.6.9-1: Angle controller principle

5.6.9.1 Goal Angle Calculation

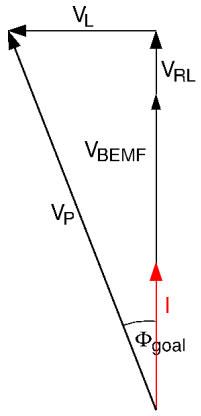

Figure 5.6.9.1-1: Goal angle dependency

5.6.9.1-1 repeats the control goal of the angle controller. The goal is to bring the current in phase with the BEMF. To achieve this a current and speed dependent angle Φ_{goal} is calculated by

$$\Phi_{goal} = \arctan\left(\frac{\omega \cdot L \cdot I}{I \cdot R_L + \omega \cdot c_M}\right) \quad ,$$

where ω is the electrical field frequency, L the motor inductance, R_L the motor resistance and c_M the motor BEMF constant normalised to the electrical field frequency ω.

The block calculates the angle Φ_{goal} using the formula

$$\Phi_{goal} = \arctan\left(\frac{1}{\frac{k_1 pll\_cnt\_max \cdot 2^{pll\_prescal}}{k_i} + \frac{k_j}{k_2 I_{ADC}}}\right) ,$$

where I_{ADC} is the ADC value of the current amplitude and k_i and k_j are fix constants.

k_1 and k_2 can be adjusted and are stored using the fractional notation $k_1 = \text{k\_1\_mant} \cdot 2^{\text{k\_1\_exp}}$ and $k_2 = \text{k\_2\_mant} \cdot 2^{\text{k\_2\_exp}}$.

These constants are parametrised as follows:

$$k_1 = \frac{R \cdot 2^{31} \cdot 25}{L \cdot \pi \cdot f_{clk}} \quad ,$$

$$k_2 = \frac{2^{23} \cdot L \cdot V_{ref,ADC}}{25 \cdot c_M \cdot 2^{10} \cdot R_i \cdot \sqrt{2}} \quad ,$$

where

- R is the phase resistance,
- L is the phase inductance,
- $c_M = \frac{V_{BEMF}}{2 \cdot \pi \cdot f_{el}}$ is the field speed based motor constant,
- f_{clk} is the system clock,
- $V_{ref,ADC}$ is the ADC reference voltage,
- N_{ADC} is the ADC resolution in bits and
- R_i is the transconductance of the current measurement network.

Table 5.6.9.1-1: Goal angle configuration registers

Register Name	*Address*	*Description*
k1	0x2a	k1
k2	0x2b	k2

Table 5.6.9.1-2: Register **k1** (0x2a) k1

	MSB							*LSB*
Content	MANT[2:0]			EXP[4:0]				
Reset value	0			0				
Access	R/W			R/W				
Bit Description								

Table 5.6.9.1-3: Register **k2** (0x2b) k2

	MSB							*LSB*
Content	MANT[3:0]				EXP[3:0]			
Reset value	0				0			
Access	R/W				R/W			
Bit Description								

5.6.9.2 Angle Difference Calculation
This unit calculates the difference between the actual current angle and the current goal angle.

5.6.9.3 Generator Detection
The generator detector compares the angle difference with fixed limits. If the angle difference is within the interval [-90°,+90°] the motor mode is detected. Otherwise the generator mode is detected.

5.6.9.4 Frequency Correction
This control is triggered every time a current sign change is detected. 5.6.9.4-1 shows the signals that are calculated at each such trigger event. The controller structure is a PD controller with the angle difference as input and a frequency correction value as output.

angle_difference, current amplitude, pll_cnt_max and pll_prescaler are varying inputs.
p_part is a parameter for the P term of the frequency correction and can be adjusted with GSCC_AMP_FACTOR[7:4]. d_part is a parameter for the D term of the frequency correction and can be adjusted with GSCC_AMP_FACTOR[3:0].
The multiplication of the angle difference with $2^{\text{pll\_prescaler}}$ is used to compensate the motor speed dependent frequency of control loop activation.

A special feature is the current dependency of the controller. The internal correction value is amplified with a scaled value of the current amplitude. This increases the speed of load step responses while it damps the reactions for low motor load cases. The current scaling gscc_curr_amp can be set up with GSCC_MOT_CURR_MULT.
The output value correction is limited.

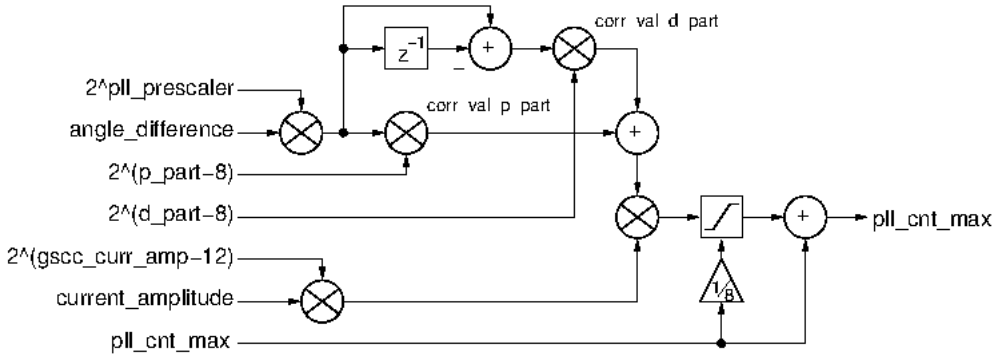

Figure 5.6.9.4-1: Frequency correction calculation

Table 5.6.9.4-1: Frequency correction registers

Register Name	*Address*	*Description*
GSCC_AMP_FACTOR	0x2c	exponents of p and d parts of the angle controller
GSCC_MOT_CURR_MULT	0x2d	exponent of current dependency of the angle controller

Table 5.6.9.4-2: Register **GSCC_AMP_FACTOR** (0x2c) exponents of p and d parts of the angle controller

	MSB							***LSB***
Content	P[3:0]				D[3:0]			
Reset value	0				0			
Access	R/W				R/W			
Bit Description								

Table 5.6.9.4-3: Register **GSCC_MOT_CURR_MULT** (0x2d) exponent of current dependency of the angle controller

	MSB			***LSB***
Content	MULT[3:0]			
Reset value	0			
Access	R/W			
Bit Description				

5.6.10 Motor Synchronisation

5.6.10-1 shows the synchronisation sequence. First the duration and amplitude for a complete electrical turn is measured. Then a plausibility check is done on these values. If the check is passed the phase voltage generation is synchronised to the frequency and amplitude. The result of the plausibility check is considered at the sync_failed output.

The parameters pll_prescal_min, pll_cnt_min, pll_prescal_max and bemf_ampl_min of the plausability check can be adjusted by the registers PLL_PRESCAL_MIN, PLL_CNT_DEBOUNCE, PLL_PRESCAL_MAX and BEMF_AMPLITUDE_MIN correspondingly.

When the plausability check has been passed successfully the amplitude scaler is calculated by

$$scaler = \frac{128 \cdot \mathrm{BEMF\_ampl}}{VSUP} \quad .$$

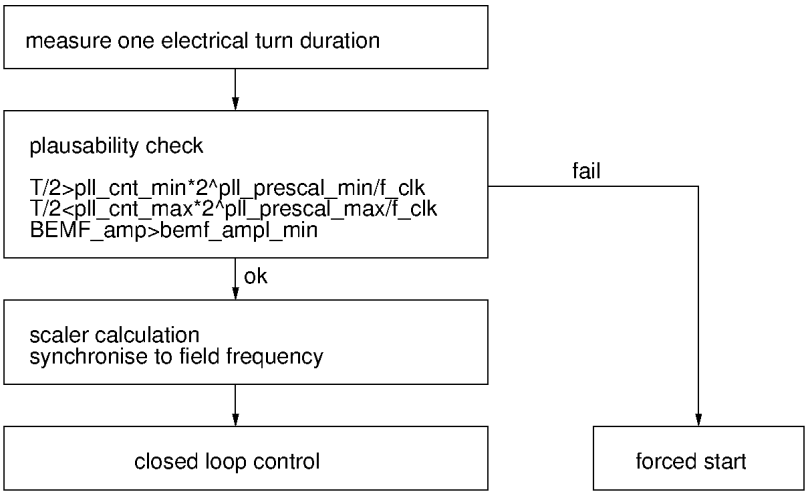

Figure 5.6.10-1: Synchronisation sequence

The min. and max. allowed el. field frequency are defined by:

$$f_{el,max} = \frac{f_{clk}}{256 \cdot 256 \cdot 2 \cdot \text{PLL\_CNT\_DEBOUNCE} \cdot 2^{\text{PLL\_PRESCAL\_MIN}}}$$ and

$$f_{el,min} = \frac{f_{clk}}{256 \cdot 2 \cdot 2048 \cdot 2^{\text{PLL\_PRESCAL\_MAX}}}$$.

The min. allowed BEMF amplitude is defined by:

$$V_{\text{BEMF,min}} = \frac{\text{BEMF\_AMPLITUDE\_MIN} \cdot 64 \cdot V_{ref,ADC} \cdot \text{div}_V}{2048}$$,

where $V_{\text{ref,ADC}}$ is the ADC reference voltage and div_V is the BEMF voltage divider ratio.

Table 5.6.10-1: Motor synchronisation registers

Register Name	*Address*	*Description*
BEMF_AMPLITUDE_MIN	0x2e	minimum BEMF amplitude allowed for synchronisation
PLL_CNT_DEBOUNCE	0x31	max. allowed el. field frequency[1)]
PLL_PRESCAL_MIN	0x30	max. allowed el. field frequency[1)]
PLL_PRESCAL_MAX	0x2f	min. allowed el. field frequency[1)]

[1)] notation is sign and absolute value

Table 5.6.10-2: Register **BEMF_AMPLITUDE_MIN** (0x2e) minimum BEMF amplitude allowed for synchronisation

	MSB			*LSB*
Content	MIN[3:0]			
Reset value	0			
Access	R/W			
Bit Description				

Table 5.6.10-3: Register **PLL_CNT_DEBOUNCE** (0x31) max. allowed el. field frequency[1)]

	MSB			*LSB*
Content	DEB[3:0]			
Reset value	0			
Access	R/W			
Bit Description				

[1)] notation is sign and absolute value

Table 5.6.10-4: Register **PLL_PRESCAL_MIN** (0x30) max. allowed el. field frequency[1)]

	MSB				*LSB*
Content	SIGN	MIN[3:0]			
Reset value	0	0			
Access	R/W	R/W			
Bit Description					

[1)] notation is sign and absolute value

Table 5.6.10-5: Register **PLL_PRESCAL_MAX** (0x2f) min. allowed el. field frequency[1)]

	MSB				***LSB***
Content	SIGN	MAX[3:0]			
Reset value	0	0			
Access	R/W	R/W			
Bit Description					

[1)] notation is sign and absolute value

5.7 System Control

5.7.1 Power up Behaviour

At power up the IC immediately goes into normal operation as soon as V_{VDD} is stable.

5.7.2 Error Detection and Behaviour

Table 5.7.2-1: Register Table

Register Name	***Address***	***Description***
BRIDGE_STAT	0x53	Bridge Status: set '1' by internal logic and reset by writing 0x00 to the register

Table 5.7.2-2: Register **BRIDGE_STAT** (0x53) Bridge Status: set '1' by internal logic and reset by writing 0x00 to the register

	MSB							***LSB***
Content	-	-	-	VS_UV	VS_OV	DS_DET_3	DS_DET_2	DS_DET_1
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit Description	**VS_UV** : VS undervoltage **VS_OV** : VS overvoltage **DS_DET_3** : Drain source desaturation phase 3 **DS_DET_2** : Drain source desaturation phase 2 **DS_DET_1** : Drain source desaturation phase 1							

5.7.2.1 High Temperature Speed Reduction and Shut Down

The IC has a speed reduction and temperature shut down function. 5.7.2.1-1 shows the behaviour. If the temperature is in its normal range the output speed is between the min. and max. value. If the temperature exceeds T_{reduce} after t_{reduce} the speed is limited to 50% of the max. value. Also the emergency speed is limited to this value. When the temperature falls below T_{normal} immediately the speed range is increased up to the max. value again.
When the temperature exceeds T_{off} the IC shuts down immediately. Then no message is sent anymore. The IC restarts when the temperature falls below $T_{restart}$.
A high temperature indication is output at the error interface as soon as the IC temperature exceeds T_{normal}.
T_{off} can be configured using register T_OT_CFG. 5.7.2.1-3 shows the possible configurations. All other temperatures depend on this value, see 4.4.1.1-1.

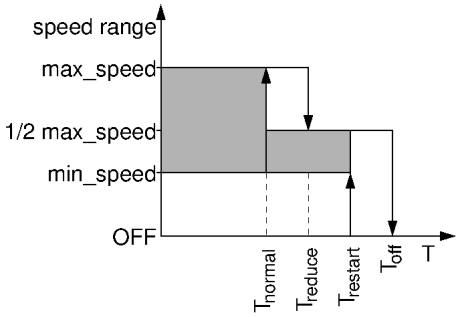

Figure 5.7.2.1-1: Temperature speed reduction and shutdown behaviour

Table 5.7.2.1-1: Temperature behaviour configuration registers

Register Name	*Address*	*Description*
T_OT_CFG	0xE8	

Table 5.7.2.1-2: Register **T_OT_CFG** (0xE8)

	MSB		*LSB*
Content	OT_CFG[2:0]		
Reset value	0		
Access	R/W		
Bit Description			

Table 5.7.2.1-3: Temperature shut down configurations

T_OT_CFG[2:0]	*T_{OFF}/°C*
0	120
1	130
2	140
3	150
4	160
5	170
6	no OT behaviour
7	no OT behaviour

5.7.2.2 High Temperature Current Reduction

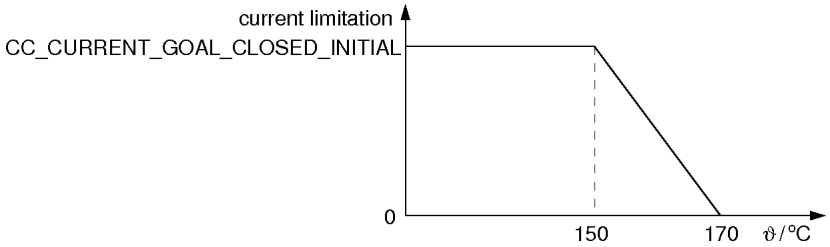

Figure 5.7.2.2-1: High temperature current reduction

The IC has a high temperature current reduction function. It reduces the current limitation when the junction temperature exceeds 150°C. The transfer function is shown in 5.7.2.2-1.

5.7.2.3 Low Load Detection

The IC has a low load detection. It operates when the goal speed or current is above 80% of its maximum value. The detection principle is different for speed control and current control.

Speed Control

When this mode is active LOW_LOAD_TH acts as a current threshold: When the speed is above 80% of its max. value and the motor current amplitude is smaller than LOW_LOAD_TH a low load condition is detected after t_low_load.

Current Control

When this mode is active LOW_LOAD_TH acts as a speed threshold: when the speed achieves LOW_LOAD_TH a low load condition is detected after t_low_load.

Behaviour

When a low load condition is detected depending on the control mode either the speed (speed control) or the control current (current control) is limited to LOW_LOAD_CTRL. When the low load condition vanishes the limitation is removed.

Table 5.7.2.3-1: Low load detection registers

Register Name	*Address*	*Description*
LOW_LOAD_TH_MANT	0xE9	threshold to detect low load condition mantissa
LOW_LOAD_TH_EXP	0xEA	threshold to detect low load condition exponent
LOW_LOAD_CTRL_MANT	0xEB	control value in case of low load, mantissa
LOW_LOAD_CTRL_EXP	0xEC	control value in case of low load, exponent

Table 5.7.2.3-2: Register **LOW_LOAD_TH_MANT** (0xE9) threshold to detect low load condition mantissa

	MSB			*LSB*
Content	MANT[3:0]			
Reset value	0			
Access	R/W			
Bit Description				

Table 5.7.2.3-3: Register **LOW_LOAD_TH_EXP** (0xEA) threshold to detect low load condition exponent

	MSB			*LSB*
Content	EXP[3:0]			
Reset value	0			
Access	R/W			
Bit Description				

Table 5.7.2.3-4: Register **LOW_LOAD_CTRL_MANT** (0xEB) control value in case of low load, mantissa

	MSB			***LSB***
Content	MANT[3:0]			
Reset value	0			
Access	R/W			
Bit Description				

Table 5.7.2.3-5: Register **LOW_LOAD_CTRL_EXP** (0xEC) control value in case of low load, exponent

	MSB			***LSB***
Content	EXP[3:0]			
Reset value	0			
Access	R/W			
Bit Description				

5.7.2.4 Rotor Blockage Detection and Reaction

Table 5.7.2.4-1: Rotor blockage registers

Register Name	***Address***	***Description***
STALL_STAT	0xD8	stall status bits

Table 5.7.2.4-2: Register **STALL_STAT** (0xD8) stall status bits

	MSB								***LSB***
Content	MOTOR_STARTED	STALL_STATE[6:4]			RESTART_COUNT[3:0]				
Reset value	0	0			0				
Access	R	R			R				
Bit Description	**MOTOR_STARTED** : this flag indicates running motor (motor FSM passed state SPEED_RAMP) **STALL_STATE[6:4]** : current blockage reaction FSM state **RESTART_COUNT[3:0]** : current motor restart count (how often the motor was restarted before unblock sequence)								

5.7.2.4.1 Detection

The rotor blockage detection uses the stall detection methods to detect if the motor is running or not. The stall detection methods are described in section 5.6.7.

5.7.2.4.2 Reaction

If a blockage is detected the IC stops the motor immediately and tries to restart after configurable delay. This is repeated 4 times. If all 4 starts fail the IC starts an unblock procedure. During the unblock procedure the IC does 8 alternating start ups backwards and forwards at a 50% increased current amplitude. Then the IC again starts a normal start up procedure and repeats this loop indefinitely. The restart delay is configured by register T_RESTART_BLOCK.
A blockage message is started when the unblock procedure starts. This message ends 5s after a motor start was successfully.

Table 5.7.2.4.2-1: Blockage reaction control

Register Name	*Address*	*Description*
T_RESTART_BLOCK	0xED	

Table 5.7.2.4.2-2: Register **T_RESTART_BLOCK** (0xED)

	MSB
Content	T_BLK
Reset value	0
Access	R/W
Bit Description	**T_BLK** : 0: $T_{RESTART}$=1s, 1: $T_{RESTART}$=10s

5.7.2.5 Short Circuit Reaction

If a short circuit or overcurrent is detected the motor is switched off immediately. After 10s the IC tries to restart the motor until the next error occurs. This sequence is repeated indefinite times.

5.8 System Configuration

5.8.1 Debugging and Configuration Interface

The IC has special functions that help to set up configuration data in the lab. These functions consist of

- disabling some functions to improve the observability of special configurations
- configuring the I/O interface to observe special internal signals at the interface

The following sections describe these functions.

5.8.1.1 Control and State Machine Disabling Functions

These functions are configured in FSM_DEBUG[3:0].

dis_fsm_transfers allows to disable all fsm transfers. It can be used for example to adjust the start up motor current without doing a motor start.

dis_speed_ramp disables the start up speed ramp. It can be used to set up the initial motor speed and observing the behaviour.

dis_cc disables the current control loop/limitation. It can be used to adjust different parameters, e.g. angle or speed controller parameters when the current limitation prevents clean observation of these control loops.

dis_angle_c allows to disable the angle controller. When observing some effects and being unsure about the reason this configuration may help to indicate some sources of trouble.

5.8.1.2 Observing Special Internal Signals

view_1 allows to output IC internal signals. By setting it to different values,

- trigger events of current direction detection
- ADC current measurement and zero current trigger events
- measured current direction
- sync signals to synchronise to the beginning of the electrical turn
- information about the calculated goal angle
- averaged phase output voltage
- calculated current amplitude

can be observed on the TACHO and DBG output pins. Below tables show the possible observation configurations.

Table 5.8.1.2-1: Observation registers

Register Name	*Address*	*Description*
TACH_CFG	0x81	select which signal is output at the TACHO output. Can only be set and activated in customer test mode.
DBG_CFG	0x83	select which signal is output at the DBG output. Can only be set and activated in customer test mode.
DBG_CTRL	0x82	configure the DGB output behaviour

Table 5.8.1.2-2: Register **TACH_CFG** (0x81) select which signal is output at the TACHO output.Can only be set and activated in customer test mode.

	MSB				*LSB*
Content	TACH_CFG[3:0]				
Reset value	0				
Access	R/W				
Bit Description	**TACH_CFG[3:0]** : Tacho configuration in customer test mode				

Table 5.8.1.2-3: Register **DBG_CFG** (0x83) select which signal is output at the DBG output.Can only be set and activated in customer test mode.

	MSB							*LSB*
Content	DBG_CFG[7:0]							
Reset value	0							
Access	R/W							
Bit Description	**DBG_CFG[7:0]** : DBG configuration in customer test mode							

Table 5.8.1.2-4: Register **DBG_CTRL** (0x82) configure the DGB output behaviour

	MSB							***LSB***
Content	MPX[3:0]				MPX_BYPASS	DAC_OE	DOUT	OE
Reset value	0				0	0	0	0
Access	R/W				R/W	R/W	R/W	R/W
Bit Description	**MPX[3:0]** : MPX[3:0] 0001 : clk/28 0010 : reset_n 0011 : pwm 0100 : desat_hs[0] 0101 : desat_hs[1] 0110 : desat_hs[2] 0111 : desat_ls[0] 1000 : desat_ls[1] 1001 : desat_ls[2] 1010 : hsg_on[0] 1011 : hsg_on[1] 1100 : hsg_on[2] 1101 : lsg_on[0] 1110 : lsg_on[1] 1111 : lsg_on[2] **MPX_BYPASS** : 0: application 1: digital MPX to output, can only set in elmos test mode **DAC_OE** : 0: DAC disabled -> ATB 1: select in customer tm analog src from DBG_CFG **DOUT** : 0: driver disable 1: driver enable **OE** : 0: digital output disable 1: digital output enable							

Table 5.8.1.2-5: Tacho output configurations

TACHO_CFG	***tacho output signal***	***description***
0	tacho	as described in section 5.3.3
1	trig_turn	trigger at phase 1 voltage zero crossing
2	trig_target_crossing	trigger at target phase 1 current zero crossing event
3	frw	phase 1 current direction
4	gscc_window	window within which the current direction is filtered
5	bemf_1_sign	detected phase 1 BEMF sign, can be used to observe the synchronisation behaviour
6	bemf_2_sign	detected phase 2 BEMF sign, can be used to observe the synchronisation behaviour
7	bemf_3_sign	detected phase 3 BEMF sign, can be used to observe the synchronisation behaviour
8	stall_det_mot_const_based	motor constant based stall detection signal
9	stall_det_current_slope	current slope based stall detection signal
10	stall_det_speed_based	speed based stall detection signal
11	sync_failed	use to configure motor re-synchronisation
15	generator_mode	motor is generating energy

Table 5.8.1.2-6: DBG output configurations

DBG_CFG	*DBG output*	*description*
0	-	
1	pwm_th1	analog averaged phase 1 output voltage
2	pwm_th2-pwm_th1	
3	current_amplitude	calculated motor current amplitude
4	motor_amp	output voltage amplitude
5	output_voltage_angle	
129	trig_turn	trigger at phase 1 voltage zero crossing
130	trig_target_crossing	trigger at target phase 1 current zero crossing event
131	frw	phase 1 current direction
132	gscc_window	window within which the current direction is filtered
133	bemf_1_sign	detected phase 1 BEMF sign, can be used to observe the synchronisation behaviour
134	bemf_2_sign	detected phase 2 BEMF sign, can be used to observe the synchronisation behaviour
135	bemf_3_sign	detected phase 3 BEMF sign, can be used to observe the synchronisation behaviour
136	stall_det_mot_const_based	motor constant based stall detection signal
137	stall_det_speed_based	speed based stall detection signal
138	stall_det_current_slope	current slope based stall detection signal
139	sync_failed	use to configure motor re-synchronisation
143	generator_mode	motor is generating energy

5.9 Power Supply

5.9.1 Supply Overview IC Supply Only

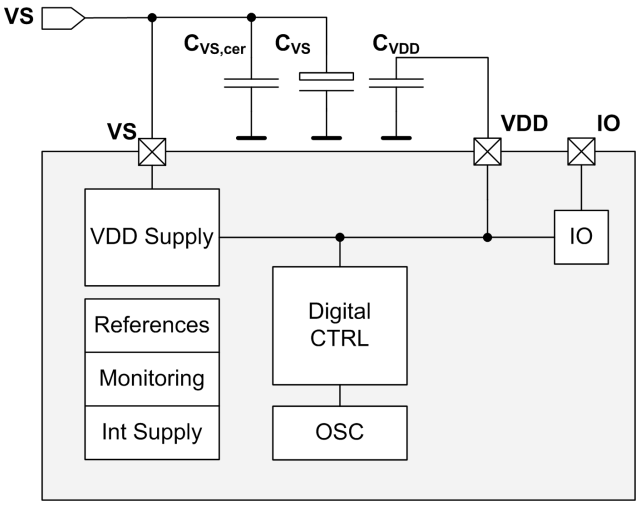

Figure 5.9.1-1: Power supply principle

5.9.2 VDD Supply

The VDDA supply contains the following components:

- The linear voltage regulator VREG delivers 3.3 V nominal supply voltage to the external storage capacitor at pin VDDA. The maximum recommended external load current at the VDDA pin is -IVDDA,ext.
- The power on reset block (POR) starts and resets the power supply control.
- The VDDA-Monitor resets the digital control unit.

5.9.3 References

5.10 Integrated Motor Bridge

The motor bridge contains three independent half bridges with over current and short circuit detection.

Attention:

As the supply monitoring only observes the chip supply pin, the bridge supply pins and the chip supply pin must always be connected to the same rail. Otherwise the undervoltage shut down of the bridge does not operate correctly which may lead to erroneous behaviour and bridge destruction in the undervoltage case.

Any supply state where the bridge is supplied and the chip supply pin is not supplied is strongly forbidden.

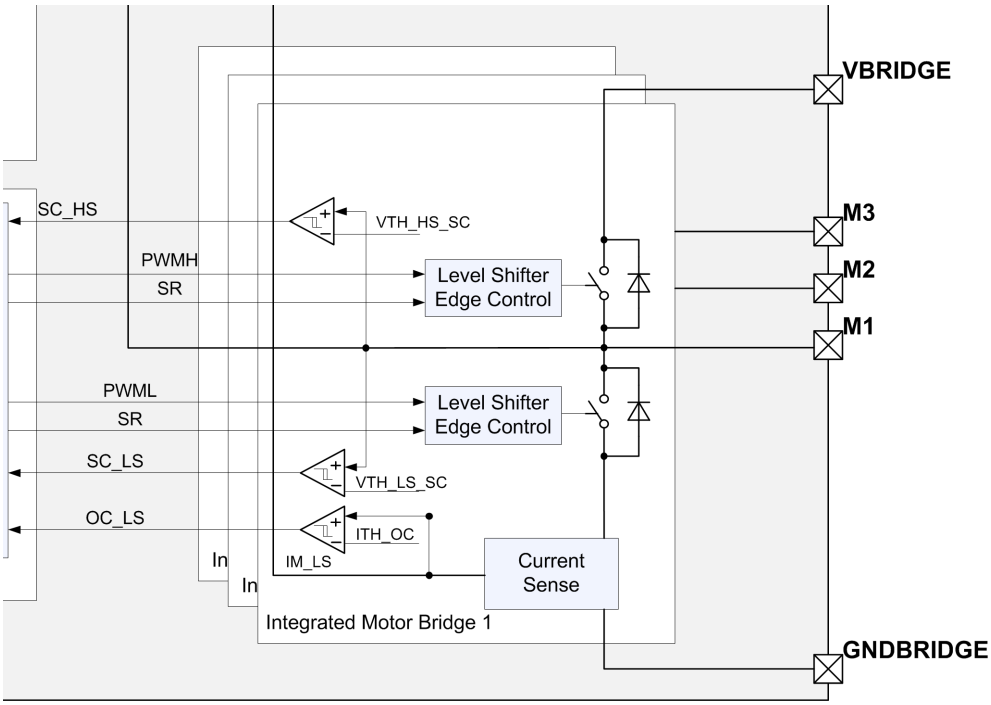

Figure 5.10-1: Half bridge block diagram

The motor phase currents are monitored by the IC. A short circuit causes immediate shut down of the bridge. The system reaction is equal to a blockage reaction.

5.11 Monitoring and Measurements

5.11.1 Monitoring Principle

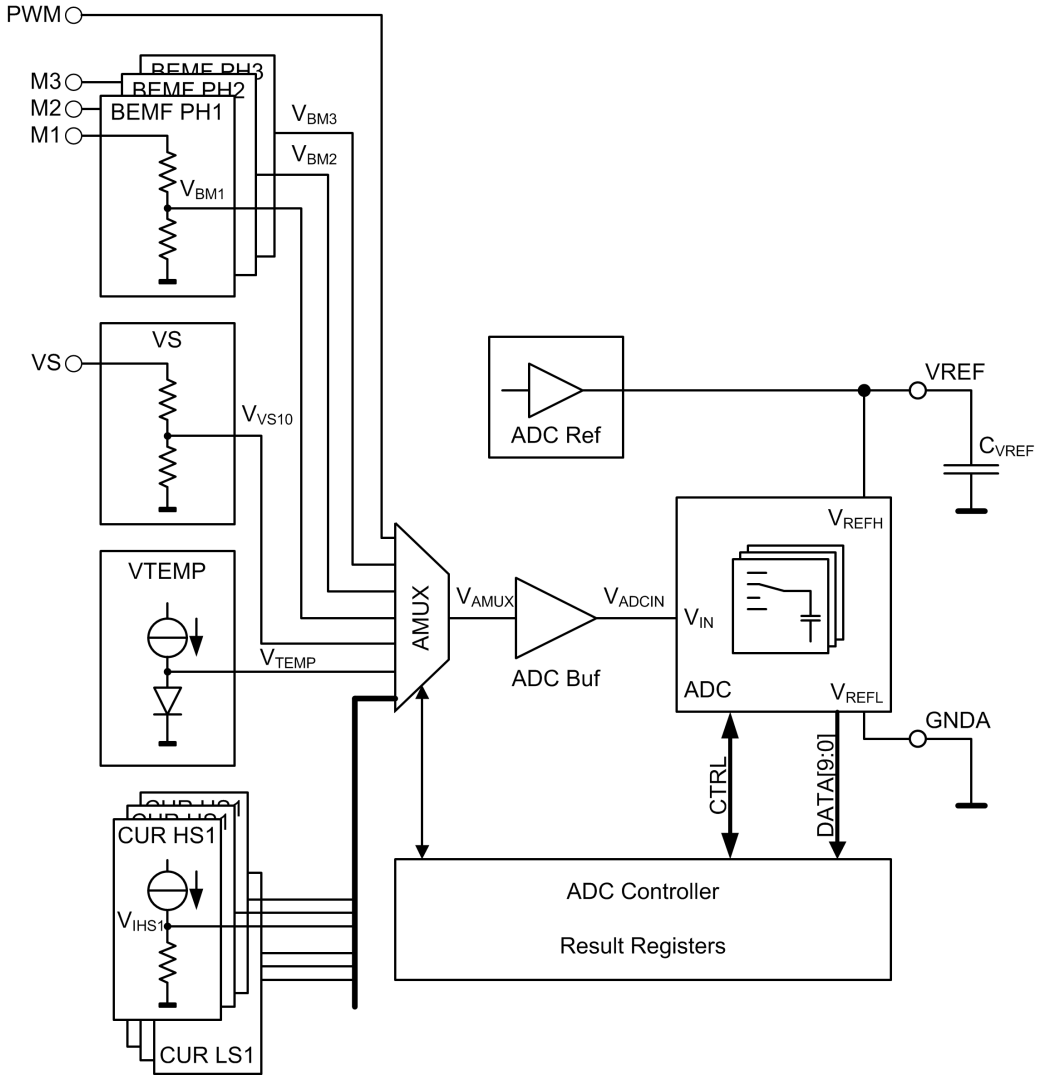

Figure 5.11.1-1: Analog Monitoring Principle (Internal Bridge)

5.11.2 Temperature Monitoring

The IC has an internal temperature monitoring. It measures the junction temperature. The system reaction at high temperatures is described in section 5.7.2.1.

5.11.3 VS Measurement

The supply voltage is continuously measured by the IC. The measured supply voltage is used
- to generate over voltage and under voltage signals
- for synchronisation to a turning motor.

The IC has a selectable over voltage shut down. The selection is done by register CONF_VS_OV_UV. With this register the threshold can be chosen between VS_OV_HI and VS_OV_LO.

If V_{VS} exceeds VS_OV the IC is shut down. The IC restarts when V_{VS} becomes lower than the reactivation threshold.
If V_{VS} becomes lower than $V_{LH,SD,BRIDGE,VS}$ the internal bridge and the IC are shut down. It restarts when V_{VS} exceeds $V_{HL,SD,BRIDGE,VS}$.

5.11.4 BEMF Measurement

The phase voltage is measured to synchronise to a turning motor. It is measured only during the synchronisation process.

5.11.5 ADC Reference

The voltage reference at pin VREF is used for A-to-D conversion. The nominal voltage is 2.5 V.

5.12 OTP

Table 5.12-1: Fuses Customer

Register Name	*Address*	*Description*
FUSE_REG_CUS[7:0]	0xA0	
FUSE_REG_CUS[15:8]	0xA1	
FUSE_REG_CUS[23:16]	0xA2	
FUSE_REG_CUS[31:24]	0xA3	
FUSE_REG_CUS[39:32]	0xA4	
FUSE_REG_CUS[47:40]	0xA5	
FUSE_REG_CUS[55:48]	0xA6	
FUSE_REG_CUS[63:56]	0xA7	
FUSE_REG_CUS[71:64]	0xA8	
FUSE_REG_CUS[79:72]	0xA9	
FUSE_REG_CUS[87:80]	0xAA	
FUSE_REG_CUS[95:88]	0xAB	
FUSE_REG_CUS[103:96]	0xAC	
FUSE_REG_CUS[111:104]	0xAD	
FUSE_REG_CUS[119:112]	0xAE	
FUSE_REG_CUS[127:120]	0xAF	
FUSE_REG_CUS[135:128]	0xB0	
FUSE_REG_CUS[143:136]	0xB1	
FUSE_REG_CUS[151:144]	0xB2	
FUSE_REG_CUS[159:152]	0xB3	
FUSE_REG_CUS[167:160]	0xB4	
FUSE_REG_CUS[175:168]	0xB5	
FUSE_REG_CUS[183:176]	0xB6	
FUSE_REG_CUS[191:184]	0xB7	
FUSE_REG_CUS[199:192]	0xB8	
FUSE_REG_CUS[207:200]	0xB9	
FUSE_REG_CUS[215:208]	0xBA	
FUSE_REG_CUS[223:216]	0xBB	
FUSE_REG_CUS[231:224]	0xBC	
FUSE_REG_CUS[239:232]	0xBD	

Table 5.12-2: Register **FUSE_REG_CUS[7:0]** (0xA0)

	MSB							***LSB***
Content	-	-	-	TSC_LIMIT_MANT	TSC_LIMIT_EXP[3:0]			
Delivery state	0	0	0	0	0			
Access	R	R	R	R	R			
Bit Description	**TSC_LIMIT_MANT** : target speed change limitiation mant **TSC_LIMIT_EXP[3:0]** : target speed change limitation exp							

Table 5.12-3: Register **FUSE_REG_CUS[15:8]** (0xA1)

	MSB							***LSB***
Content	FEATURE_DIS[7:0]							
Delivery state	0							
Access	R							
Bit Description	**FEATURE_DIS[7:0]** : feature disable							

Table 5.12-4: Register **FUSE_REG_CUS[23:16]** (0xA2)

	MSB							***LSB***
Content	CONF_VS_OV_UV	TACH_CONF	-	-	NUM_TZC[3:0]			
Delivery state	0	0	0	0	0			
Access	R	R	R	R	R			
Bit Description	**CONF_VS_OV_UV** : vs over voltage thershold **TACH_CONF** : set Tacho to low in FSM mode 4 and 5 **NUM_TZC[3:0]** : number of turns with zero current							

Table 5.12-5: Register **FUSE_REG_CUS[31:24]** (0xA3)

	MSB							***LSB***
Content	LOW_LOAD_C_MANT[3:0]				LOW_LOAD_C_EXP[3:0]			
Delivery state	0				0			
Access	R				R			
Bit Description	**LOW_LOAD_C_MANT[3:0]** : Low load ctrl mant **LOW_LOAD_C_EXP[3:0]** : Low load ctrl exp							

Table 5.12-6: Register **FUSE_REG_CUS[39:32]** (0xA4)

	MSB							***LSB***
Content	LOW_LOAD_TH_MAN[3:0]				LOW_LOAD_TH_EXP[3:0]			
Delivery state	0				0			
Access	R				R			
Bit Description	**LOW_LOAD_TH_MAN[3:0]** : Low load threshold mant **LOW_LOAD_TH_EXP[3:0]** : Low load threshold exp							

Table 5.12-7: Register **FUSE_REG_CUS[47:40]** (0xA5)

	MSB							***LSB***
Content	T_EL_KD_EXP[3:0]				T_RESTART_BLK	T_OT_CFG[2:0]		
Delivery state	0				0	0		
Access	R				R	R		
Bit Description	**T_EL_KD_EXP[3:0]** : D part of speed control exp **T_RESTART_BLK** : Restart Block **T_OT_CFG[2:0]** : Shut down threshold over voltage							

Table 5.12-8: Register **FUSE_REG_CUS[55:48]** (0xA6)

	MSB							***LSB***
Content	T_EL_KP_EXP[3:0]				T_EL_KI_EXP[3:0]			
Delivery state	0				0			
Access	R				R			
Bit Description	**T_EL_KP_EXP[3:0]** : P part of speed control exp **T_EL_KI_EXP[3:0]** : I part of speed control exp							

Table 5.12-9: Register **FUSE_REG_CUS[63:56]** (0xA7)

	MSB							***LSB***
Content	T_EL_EMGY_EXP[3:0]				SPEED_CTRL[1:0]		CUR_MEAS_OFF-SET_CTRL[1:0]	
Delivery state	0				0		0	
Access	R				R		R	
Bit Description	**T_EL_EMGY_EXP[3:0]** : Target period of emergency mode exp **SPEED_CTRL[1:0]** : Mode control							

Table 5.12-10: Register **FUSE_REG_CUS[71:64]** (0xA8)

	MSB							***LSB***
Content	T_EL_MIN_EXP[3:0]				T_EL_EMGY_MANT[3:0]			
Delivery state	0				0			
Access	R				R			
Bit Description	**T_EL_MIN_EXP[3:0]** : Min Target period exp **T_EL_EMGY_MANT[3:0]** : Target period of emergency mode mant							

Table 5.12-11: Register **FUSE_REG_CUS[79:72]** (0xA9)

	MSB							***LSB***
Content	T_EL_MIN_MANT[7:0]							
Delivery state	0							
Access	R							
Bit Description	**T_EL_MIN_MANT[7:0]** : Min target period mant							

Table 5.12-12: Register **FUSE_REG_CUS[87:80]** (0xAA)

	MSB							***LSB***
Content	T_EL_MAX_MANT[3:0]				T_EL_MAX_EXP[3:0]			
Delivery state	0				0			
Access	R				R			
Bit Description	**T_EL_MAX_MANT[3:0]** : Max target period mant **T_EL_MAX_EXP[3:0]** : Max target period exp							

Table 5.12-13: Register **FUSE_REG_CUS[95:88]** (0xAB)

	MSB							***LSB***
Content	T_SETTLE_ROTOR[4:0]					T_SYNC_CHK[2:0]		
Delivery state	0					0		
Access	R					R		
Bit Description	**T_SETTLE_ROTOR[4:0]** : Settle rotor **T_SYNC_CHK[2:0]** : Sync check							

Table 5.12-14: Register **FUSE_REG_CUS[103:96]** (0xAC)

	MSB							***LSB***
Content	VOLT_SCAL_OFFS[7:0]							
Delivery state	0							
Access	R							
Bit Description	**VOLT_SCAL_OFFS[7:0]** : Svm voltage scaler offset							

Table 5.12-15: Register **FUSE_REG_CUS[111:104]** (0xAD)

	MSB							***LSB***
Content	STALL_SYNC_EN	STALL_DET_BEMF	STALL_DET_HIGH_SPEED	STALL_SPEED_LIMIT	PRES_MAX_STALL[3:0]			
Delivery state	0	0	0	0	0			
Access	R	R	R	R	R			
Bit Description	**STALL_SYNC_EN** : Stall sync enable **STALL_DET_BEMF** : Stall detection BEMF based **STALL_DET_HIGH_SPEED** : Stall detection high speed **STALL_SPEED_LIMIT** : Stall detection speed limit **PRES_MAX_STALL[3:0]** : Pll prescal max stall							

Table 5.12-16: Register **FUSE_REG_CUS[119:112]** (0xAE)

	MSB							***LSB***
Content	STALL_DET_THRSH[7:0]							
Delivery state	0							
Access	R							
Bit Description	**STALL_DET_THRSH[7:0]** : Stall detection threshold							

Table 5.12-17: Register **FUSE_REG_CUS[127:120]** (0xAF)

	MSB							***LSB***
Content	-	-	-	PLL_PRESCAL_SU_SIGN	PLL_PRESCAL_SU[3:0]			
Delivery state	0	0	0	0	0			
Access	R	R	R	R	R			
Bit Description	**PLL_PRESCAL_SU_SIGN** : PLL prescaler su sign **PLL_PRESCAL_SU[3:0]** : PLL prescaler su							

Table 5.12-18: Register **FUSE_REG_CUS[135:128]** (0xB0)

	MSB							***LSB***
Content	-	-	-	PLL_PRESCAL_MIN_SIGN	PLL_PRESCAL_MIN[3:0]			
Delivery state	0	0	0	0	0			
Access	R	R	R	R	R			
Bit Description	**PLL_PRESCAL_MIN_SIGN** : PLL prescaler min sign **PLL_PRESCAL_MIN[3:0]** : PLL prescaler min							

Table 5.12-19: Register **FUSE_REG_CUS[143:136]** (0xB1)

	MSB							***LSB***
Content	-	-	-	PLL_PRESCAL_MAX_SIGN	PLL_PRESCAL_MAX[3:0]			
Delivery state	0	0	0	0	0			
Access	R	R	R	R	R			
Bit Description	**PLL_PRESCAL_MAX_SIGN** : PLL prescaler max sign **PLL_PRESCAL_MAX[3:0]** : PLL prescaler max							

Table 5.12-20: Register **FUSE_REG_CUS[151:144]** (0xB2)

	MSB							***LSB***
Content	PLL_CNT_DEB[3:0]				PLL_IN_SCAL_MAX[3:0]			
Delivery state	0				0			
Access	R				R			
Bit Description	**PLL_CNT_DEB[3:0]** : PLL cunter debounce **PLL_IN_SCAL_MAX[3:0]** : PLL inc scaler max							

Table 5.12-21: Register **FUSE_REG_CUS[159:152]** (0xB3)

	MSB							***LSB***
Content	K2[7:0]							
Delivery state	0							
Access	R							
Bit Description	**K2[7:0]** : K2							

Table 5.12-22: Register **FUSE_REG_CUS[167:160]** (0xB4)

	MSB							***LSB***
Content	K1[7:0]							
Delivery state	0							
Access	R							
Bit Description	**K1[7:0]** : K1							

Table 5.12-23: Register **FUSE_REG_CUS[175:168]** (0xB5)

	MSB							***LSB***
Content	GSCC_AMP_FAC[7:0]							
Delivery state	0							
Access	R							
Bit Description	**GSCC_AMP_FAC[7:0]** : gscc amp factor							

Table 5.12-24: Register **FUSE_REG_CUS[183:176]** (0xB6)

	MSB							***LSB***
Content	GSCC_M_CUR_MULT[3:0]				MAX_VA_VOLTAGE[3:0]			
Delivery state	0				0			
Access	R				R			
Bit Description	**GSCC_M_CUR_MULT[3:0]** : GSCC motor current multiplier **MAX_VA_VOLTAGE[3:0]** : upper limit of VA PID voltage							

Table 5.12-25: Register **FUSE_REG_CUS[191:184]** (0xB7)

	MSB							***LSB***
Content	CM_MANT[3:0]				CM_EXP[3:0]			
Delivery state	0				0			
Access	R				R			
Bit Description	**CM_MANT[3:0]** : Motor constant CM mant **CM_EXP[3:0]** : Motor constant CM exp							

Table 5.12-26: Register **FUSE_REG_CUS[199:192]** (0xB8)

	MSB							***LSB***
Content	-	CC_NM_EV_RUN[2:0]			-	CC_NM_EV_RUN_CL[2:0]		
Delivery state	0	0			0	0		
Access	R	R			R	R		
Bit Description	**CC_NM_EV_RUN[2:0]** : CC number events run **CC_NM_EV_RUN_CL[2:0]** : CC number events run closed							

Table 5.12-27: Register **FUSE_REG_CUS[207:200]** (0xB9)

	MSB							***LSB***
Content	CC_CUR_GOAL_CLO[7:0]							
Delivery state	0							
Access	R							
Bit Description	**CC_CUR_GOAL_CLO[7:0]** : CC current goal closed							

Table 5.12-28: Register **FUSE_REG_CUS[215:208]** (0xBA)

	MSB							***LSB***
Content	CC_CUR_GOAL[7:0]							
Delivery state	0							
Access	R							
Bit Description	**CC_CUR_GOAL[7:0]** : Current goal							

Table 5.12-29: Register **FUSE_REG_CUS[223:216]** (0xBB)

	MSB							***LSB***
Content	CURR_FILT_FAC[3:0]				BEMF_AMP_MIN[3:0]			
Delivery state	0				0			
Access	R				R			
Bit Description	**CURR_FILT_FAC[3:0]** : ADC current filter factor **BEMF_AMP_MIN[3:0]** : BEMF amplitude min							

Table 5.12-30: Register **FUSE_REG_CUS[231:224]** (0xBC)

	MSB							***LSB***
Content	ECC	-	DIRECTION	START_UP_TURNS[4:0]				
Delivery state	0	0	0	0				
Access	R	R	R	R				
Bit Description	**ECC** : ECC[0] **DIRECTION** : Motor direction **START_UP_TURNS[4:0]** : Start up turns							

Table 5.12-31: Register **FUSE_REG_CUS[239:232]** (0xBD)

	MSB							***LSB***
Content	ECC[8:1]							
Delivery state	0							
Access	R							
Bit Description	**ECC[8:1]** : ECC[8:1]							

6 Package Reference

The E523.81 is available in a Pb free, RoHs compliant QFN20L5 plastic package according to JEDEC MO-220 K, variant
VJJC-2. The package is classified to Moisture Sensitivity Level 3 (MSL 3) according to JEDEC J-STD-020 with a soldering peak temperature of (260+5)°C.
Note: Thermal resistance junction to case $R_{th,jc}$ is 5 K/W, based on JEDEC standard JESD-51-6 and JESD.

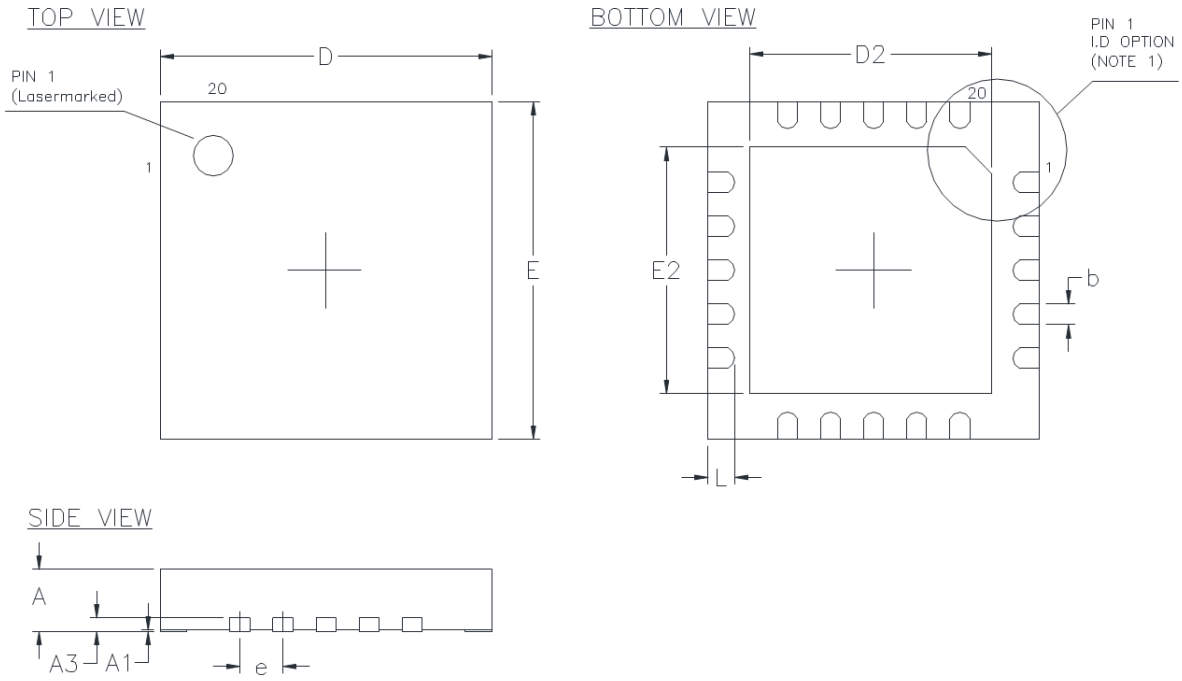

Figure 6-1: Package Outline

Table 6-1: Package Characteristics

Description	***Symbol***		***mm***			***inch***	
		min	**typ**	**max**	**min**	**typ**	**max**
Package height	A	0.80	0.90	1.00	0.031	0.035	0.039
Stand off	A1	0.00	0.02	0.05	0.000	0.00079	0.002
Thickness of terminal leads, including lead finish	A3	0.20 REF			0.0079 REF		
Width of terminal leads	b	0.25	0.30	0.35	0.010	0.012	0.014
Package length / width	D / E	5.00 BSC			0.197 BSC		
Length /width of exposed pad	D2 / E2	3.50	3.65	3.80	0.138	0.144	0.150
Lead pitch	e	0.65 BSC			0.026 BSC		
Length of terminal for soldering to substrate	L	0.35	0.40	0.45	0.014	0.016	0.018
Number of terminal positions	N	20			20		

Note: the mm values are valid, the inch values contain rounding errors

7 Typical Applications

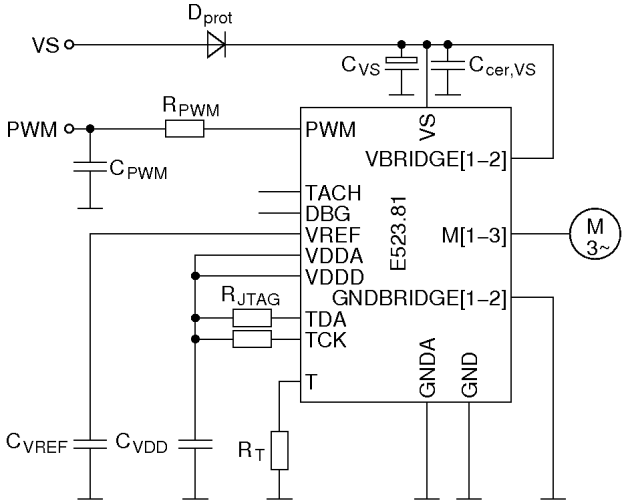

Figure 7-1: Block diagram on L0

Table 7-1: External Components

Symbol	*Value*	*Unit*	*Description*
R_{PWM}	470	Ω	PWM input series resistance
C_{PWM}	10	nF	PWM ESD protection capacitance
R_T	10	kΩ	pull-down resistance
R_{JTAG}	10	kΩ	pull-up resistance
$C_{cer,VS}$	100	nF	ceramic VS blocking capacitance
C_{VS}	>10	µF	VS blocking capacitance
C_{VDD}	1	µF	ceramic VDD blocking capacitance
C_{VREF}	10	nF	ADC reference blocking capacitance
D_{prot}			reverse polarity protection diode

Remark
The voltage at VS and at VBRIDGE must be identical. Please connect the corresponding supply rails to the same voltage. Connecting VS and VBRIDGE to different voltages results in incorrect low voltage shut down behaviour of the bridge.

8 Revision History

Table 8-1: Table of Revisions

Rev.	*Chapter*	*Description of change*	*Changed by*	*Date*
03	all	Revision for PPAP	KFH/ZOE	15.05.2018

9 General

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