# Scalable, dense and flexible PoL design for Xilinx Zynq UltraScale+ FPGAs

## Understanding the crux of FPGA PoL design while eliminating the pitfalls of a cookie-cutter design

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## About this document

### Scope and purpose

This application note describes the multi-faceted use of the Zynq UltraScale+ MPSoC and RFSoC range, from machine learning to computer vision, and from ADAS systems to video conferencing applications, Zu02 to Zu19. Whether it is the space-optimized Zynq RFSoC or the more powerful Zu21DR or Zu29DR, a scalable digital PoL architecture that meets the Zynq sequencing and performance requirements needs to be implemented. In this paper, the digital PMIC from Infineon, IRPS5401M, is shown in various applications where the core voltages range from 30 to 70 A with other dedicated rails that meets Xilinx's sequencing, efficiency and power density requirements.

### Intended audience

The intended audience is decision makers (project engineering managers and lead engineers) interested in Infineon's solutions for SoCs as well as field application engineers and sales engineers focusing on Xilinx solutions and between 10 W to 50 W of multi-rail DC-DC power.

## Table of contents

# 1 Introduction

The size of the FPGA varies with the scope of the application. Bigger applications require more horsepower, thus requiring larger FPGAs. Figure 1 shows the typical architecture of a Xilinx Zynq US FPGA. A Zynq is typically divided into the Programmable Logic (PL), processing domain (PS) and RFSoC. A typical Xilinx FPGA PL domain can operate at 0.72 V, 0.85 V and 0.9 V. Video codec core voltage on the Zynq UltraScale+ Zu04/Zu05/Zu07 "EV series" requires an extra 0.9 V supply.

The Zynq FPGAs are designed using a 16 nm process, and today most of the core voltages are 0.73 V, 0.85 V or 0.9 V. These core voltages will go below 0.7 V as the process technology moves to a 7 nm process. The larger FPGAs such as the Zu21DR and Zu29DR will have traditional programmable logic cores with added high-speed ADC processing, thus requiring more current. The PS domain operates at 0.85 V and 0.9 V. Even at lower process technologies, these processing side cores are not likely to go to lower operating voltages. For the logic sections, the core voltages can operate at lower core voltages. The PS side typically requires higher voltages. The RFSoC has the high-speed ADCs; this typically ranges from 4 to 16 ADCs. All digital controllers and digital PMICs are operated in the Infineon PowIR Center tool. Details of the PowIR Center tool will be displayed to represent the various advantages of digital power.

The common rails that require power are shown in the diagram below. Powering the rails based on the end application – space-constrained or efficiency-optimized – is the focus of this application note.

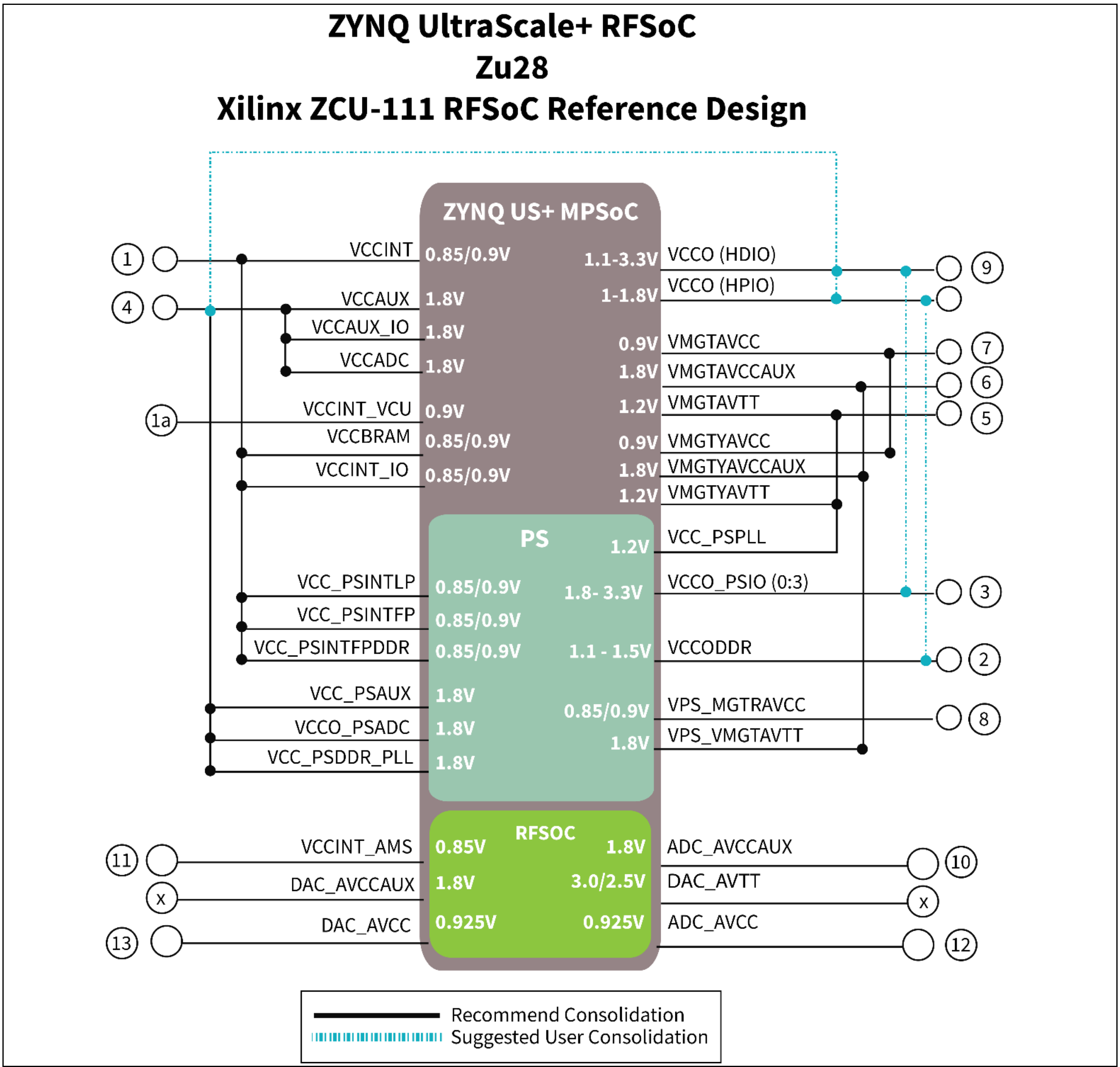


**Figure 1** Overview of the typical rails in a Xilinx Zynq US RFSoC

# 2 Space-constrained power solution

Figure 1 illustrates the power needs for a typical Zynq US FPGA. Different applications have varying power requirements on each rail. Figure 2 represents a space-optimized power solution. In the proposed solution below, various rails are consolidated. The IRPS5401 PMIC at U1 with an external power stage in switcher A will power the VCCINT, VCC_PSINTLP, VCC_PSINTFP, VCCBRAM, VCC_PSINTFPDDR, VCCINT_IO and VCCINT_AMS rails. So the core voltage could be either 0.85 V or 0.90 V. In most such applications, the current for this rail ranges from 30 to 50 A, thus either the TDA21240 µDrMOS power stage (rated at 40 A) or the TDA21470 power stage (rated at 70 A) can be used. Without the external power stage, switcher A of the IRPS5401 PMIC can support up to 2 A. None of the other rails can support an external power stage. So switcher B can support up to 2 A, while switchers C and D can supply up to 4 A each. You also have the option to combine switcher outputs C and D to deliver up to 8 A.

In the architecture below, switcher B can regulate 1.8 V at 2 A to power the VCCAUX, VCCAUX_IO, VCCADC/VCC_PSAUX, VCCO_PSADC and VCC_PSDDR_PLL rails. Switcher C can supply an additional 1.8 V rail at 2 A to power the ADC_AVCCAUX. Switcher C can handle up to 4 A of load capability. Since switcher D has the capability to deliver up to 4 A, this rail can be used to regulate 1.2 V to power the VCC_PSDDR and DDR_VDDQ rails. The LDO on U1 IRPS5401 can deliver 500 mA and can be used to power the DAC_AVCCAUX rail.

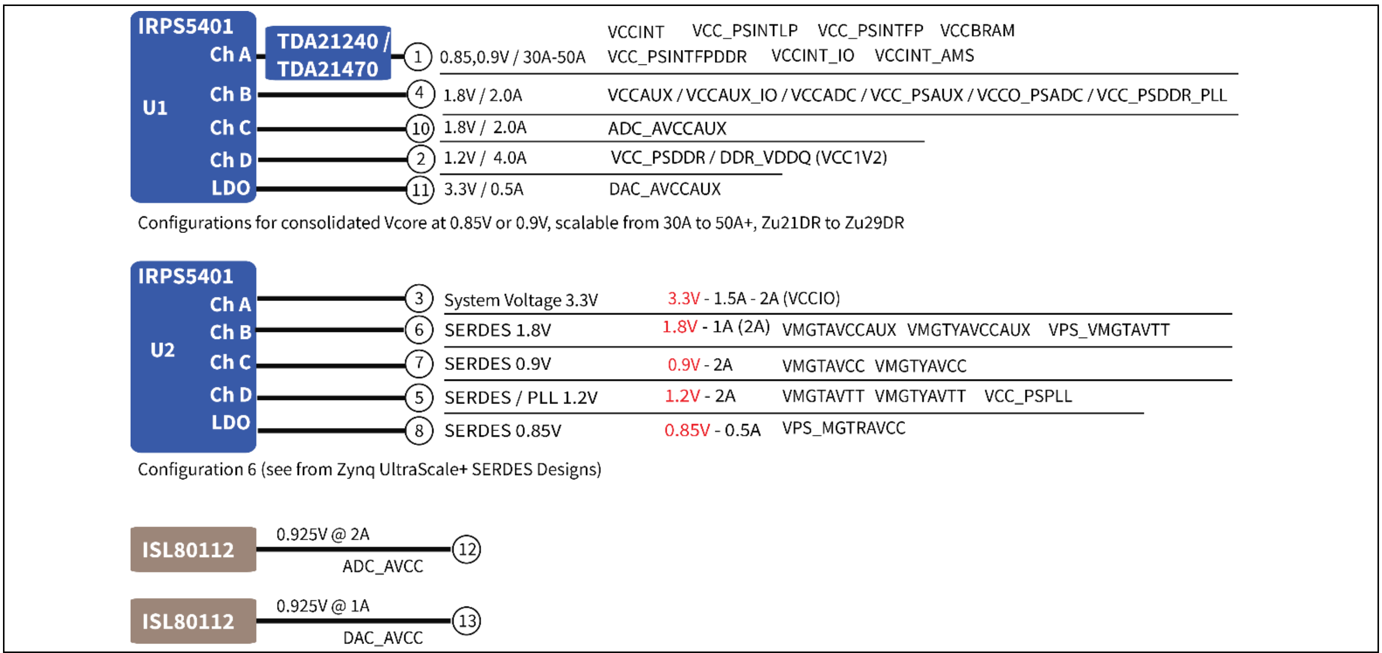


**Figure 2 Space-optimized power solution for Zynq RFSoC, Zu21DR to Zu29DR**

The IRPS5401 at U2 is dedicated to power all SERDES rails. Each SERDES rail requires dedicated power. In this instance, a system voltage of 3.3 V ranging from 1.5 to 2 A can be used to power the VCCIO rail. Switcher B can be used to power the 1.8 V rail at 2 A for the VMGTAVCCAUX, VMGTYAVCCAUX and VPS_VMGTAVTT rails. Switcher C of U2 can deliver 0.8 V at 2 A to power the VMGTAVCC and VMGTYAVCC rails. Switcher D is used to power the 1.2 V rail at 2 A to power the VMGTAVTT, VMGTAVTT and VCC_PSPLL rails. This leaves the LDO to power the SERDES 0.85 V rail VPS_MGTRAVCC.

In this proposal we are using an alternative LDO to power the ADC_AVCC and DAC_AVCC rails. Any LDO can be used to power the bias supply for the ADCs. Also in this particular proposal we are using two IR3897Ms to power the DDR4_VTT and PL_DDR4_VTT rails. Since each DDR4_VTT rail requires 3 A and requires tracking capabilities based on the 1.2 V VDDQ supply this is a good choice. Delivering power in an integrated solution is part of design, but meeting the Zynq US sequencing requirement is another requirement. The sequencing requirements are reviewed in a later section.

# 3 Efficiency-optimized solution for the Zynq RFSoC, Zu21DR and Zu29DR

A typical architecture for an efficiency-optimized design is shown in Figure 3. In such applications, larger FPGAs are used, thus requiring FPGA core supplies in the 30 to 70 A range. In this particular example, efficiency has priority. To meet this requirement, the IR35215 (multi-phase controller) with external TDA21470 OptiMOS™ power stages in 2+1 configurations is being used. TDA21470 multi-phase controllers have two control loops that can operate in N+M configuration for up to eight phases. Here, we are operating Loop 1 in two phases to power the VCCINT rail and Loop 2 to provide 0.85 or 0.9 V from 10 to 20 A. This could be used to power the VCC_PSINTFPDDR, VCCINT_IO, VCCINT_AMS, VCC_PSINTFP, VCCBRAM and VCC_PSINTLP rails.

At this point IRPS5401 at U1 can be operated without a power stage. Switcher A of U1 can be used to power the ADC_AVCC rail at 0.925 V with 2 A. Switchers B, C, D and LDO of U1 are utilized the same way as in the space-optimized solution.

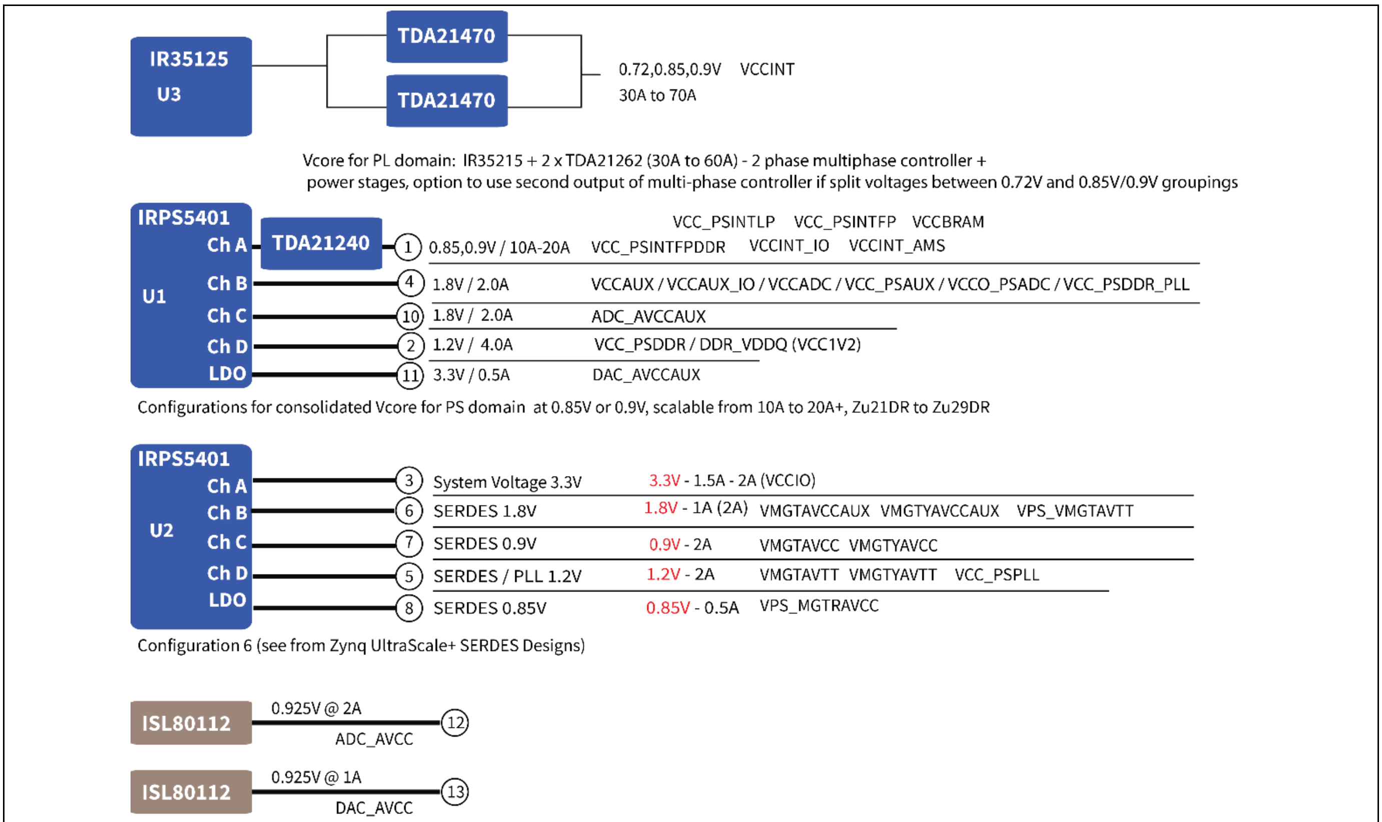


**Figure 3 Efficiency-optimized power solution for Zynq RFSoC, Zu21DR and Zu29DR**

The IRPS5401 at U2 is used to power the SERDES rails, similar to the space-optimized solution. This particular proposal eliminates the need for extra discrete LDOs. If the rails are moved around, switcher C of U1 IRPS5401 can be used to power the ADC_AVCC and DAC_AVCC rails as well. This leaves the original 1.8 V at 2 A on switcher C to be powered by switcher A. As you can see, the flexibility that comes with the IRPS5401 PMIC is an advantage. This device can be configured to operate in your system based on your requirements.

# 4 Efficiency

Efficiency is a key requirement in PoL design. Figure 4 shows the efficiency curve of the IRPS5401 PMIC with an external TDA21240 µDrMOS device. All the efficiency measurements are taken at room temperature with 0 LFM cooling and at 800 kHz switching frequency.

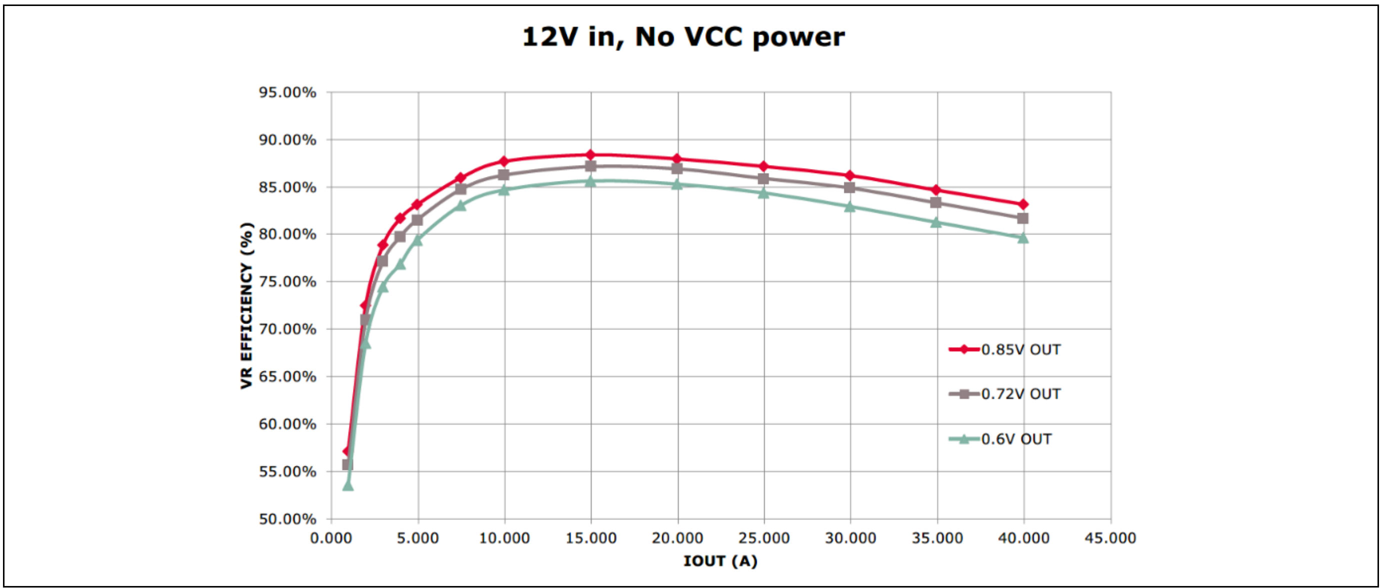


**Figure 4 Efficiency of IRPS5401 PMIC + TDA21240 µDrMOS power stage**

The IRPS5401 with the µDrMOS provides a peak efficiency of about 87 percent. The location of the peak efficiency on the efficiency curve is dictated by the output inductor value. In the above measurements, you can observe this at around 15 A.

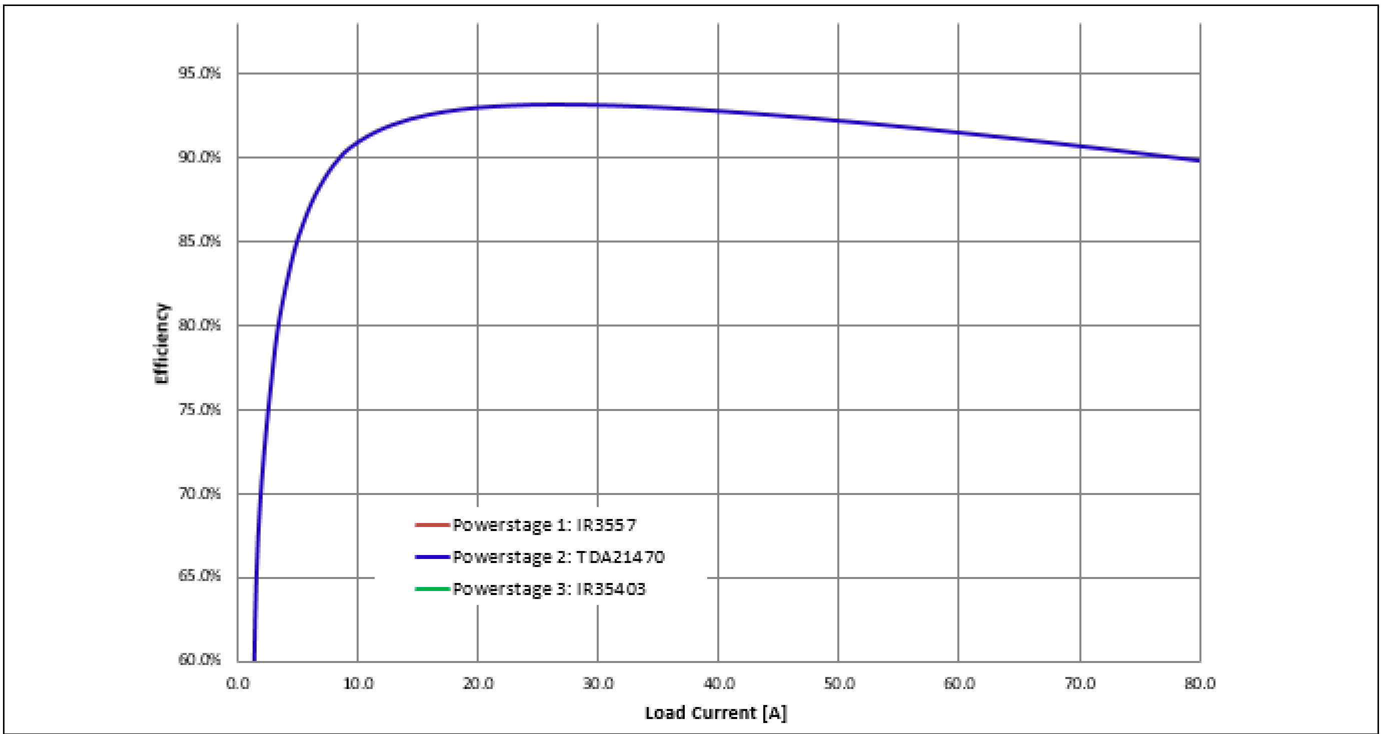


**Figure 5 Efficiency of IR35215 multi-phase controller + TDA21470 OptiMOS™ power stage in two phases for 0.85 V**

The IR35215 controller is designed for multi-phase applications, and for 70 to 90 A core power applications this is a better solution. The IR35215 controller also has features such as Diode Emulation Mode (DEM), active phase shedding and low-power states that allow a designer to boost the light-load efficiency. For efficiency-oriented designs, this is the recommended solution to power the core rails.

# 5 Sequencing

The advantage of digital PoLs is that sequencing can be programmed via the config files. This eliminates the need for external sequencers or RC timing circuits. Sequencing is a critical requirement for Zynq US FPGAs for the PL domain, and the power-on sequence is as follows:

VCCINT → VCCINT_IO/VCCBRAM → VCCAUX/VCCAUX_IO → VCCO. Following this sequence ensures there is minimum current draw and the IOs are tri-stated during power-on. The power-off sequence is the opposite of the power-on sequence. VCCAUX/ VCCAUX_IO and the VCCINT_IO/VCCBRAM have the same voltage levels, therefore they can be powered on and off at the same time. For GTY transceivers, the recommended power-on sequence is VCCINT → VMGTAVCC → VMGTAVTT or VMGTAVCC → VCCINT → VMGTAVTT. Shown below is the sequencing diagram from PowIR Center for the Xilinx ZCU-111 board.

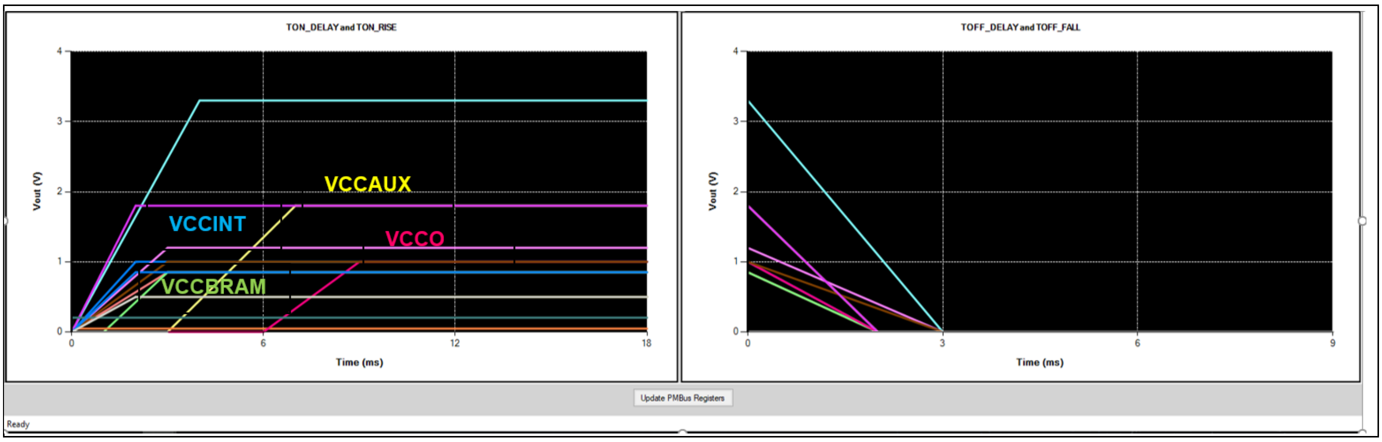


**Figure 6 High-level power sequencing on the ZCU-111 design. The rails mentioned above are highlighted in the sequencing diagram.**

Shown above is the high-level sequencing diagram for the PMBus rails of the ZCU-111 design. The rail names and their corresponding turn-on/off waveforms are shown in the above diagram.

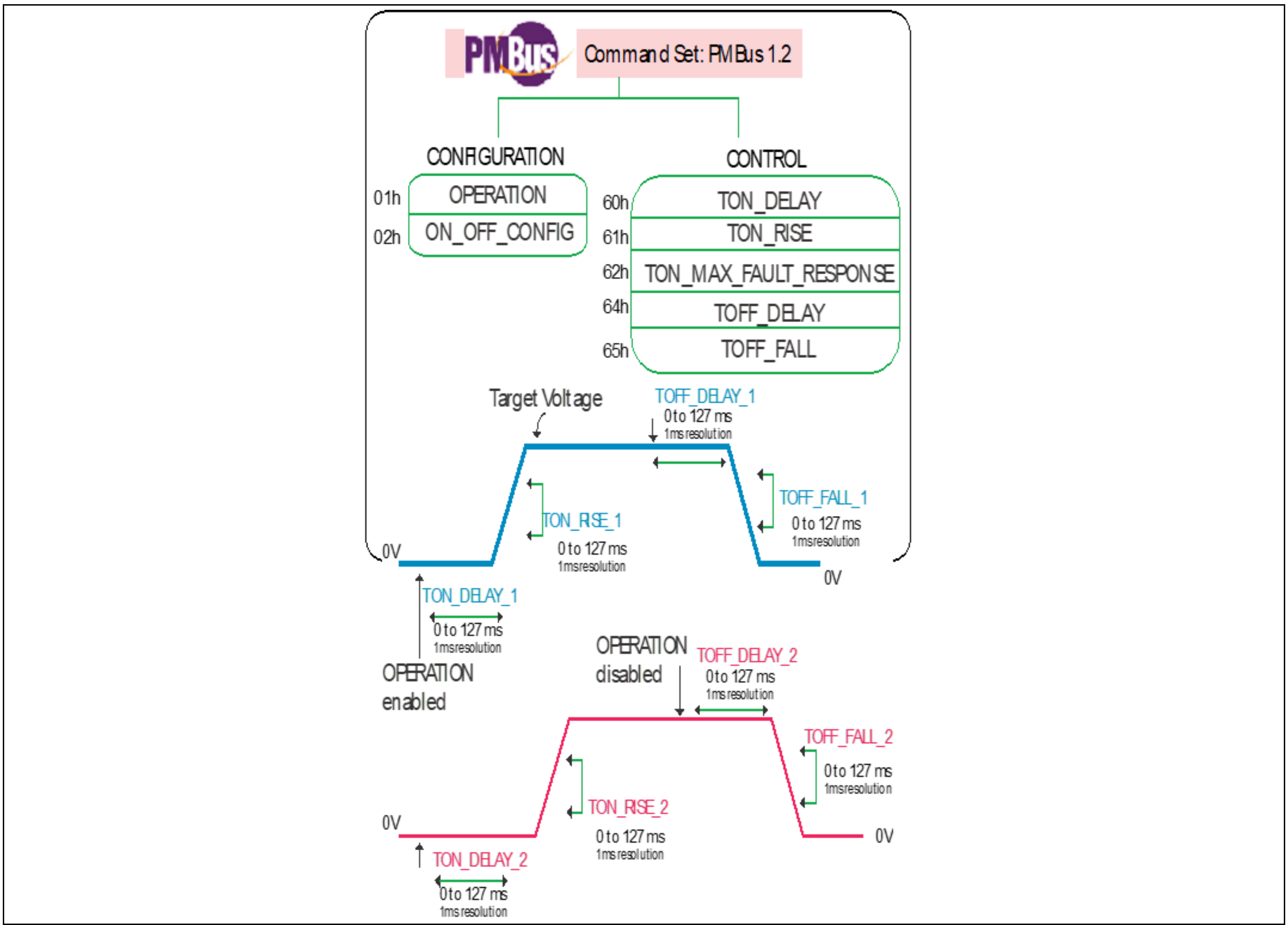


**Figure 7 Details for TON_DELAY, TOFF_DELAY, TON_RISE and TOFF_FALL**

Figure 7 shows how the sequencing commands TON_DELAY, TOFF_DELAY, TON_RISE and TOFF_FALL are specified in the PowIR Center GUI. These parameters are modified to get the sequencing diagram shown in Figure 6. Each command has a 0 to 127 ms range with 1 ms resolution. They also have PMBus command codes.

# 6 Performance

The IRPS5401 digital PMIC provides excellent transient performance for the switchers and LDO. Shown below is the transient load test for a VCCINT_IO_BRAM rail where the IRPS5401 PMIC with a µDrMOS power stage is to power a rail up to 15 A.

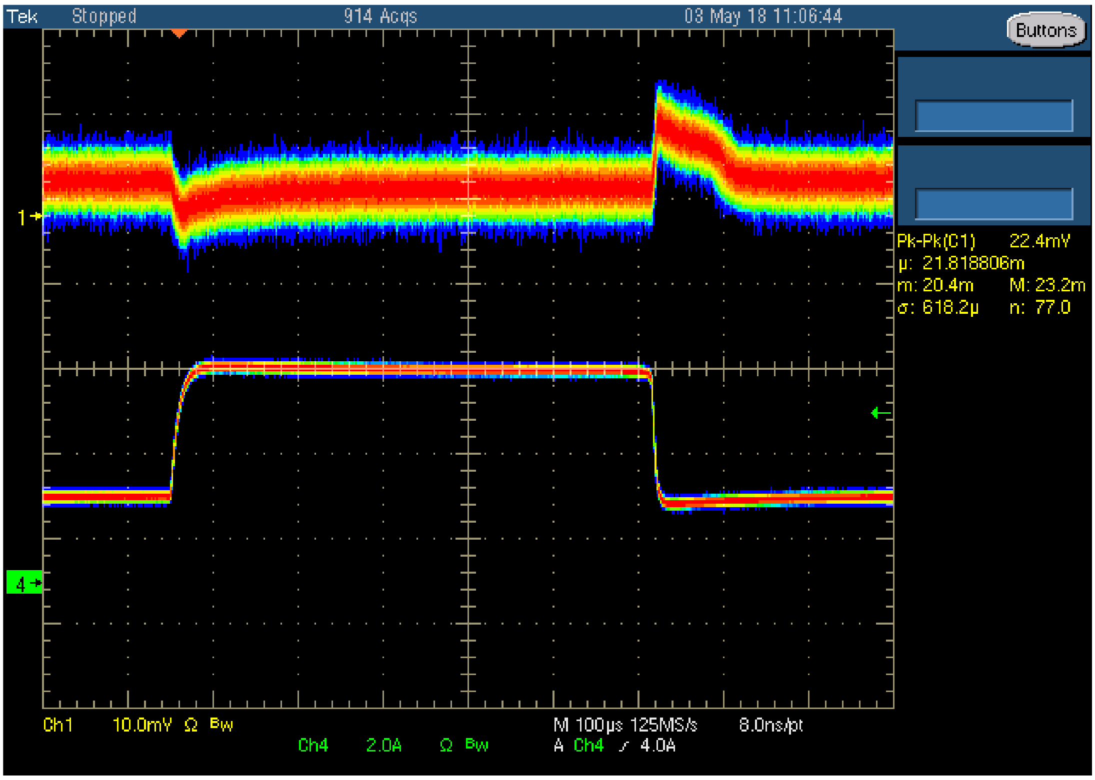


**Figure 8 VCCINT_IO_BRAM rail with 2 to 10 A load step with di/dt = 2.5 A/µs**

During a transient 2 to 10 A load step we are observing 5.4 mV $V_{out}$ excursion and during a 10 to 2 A load release, we are seeing $V_{out}$ overshoot of 9.4 mV. The transient response is well within spec of the Xilinx requirement.

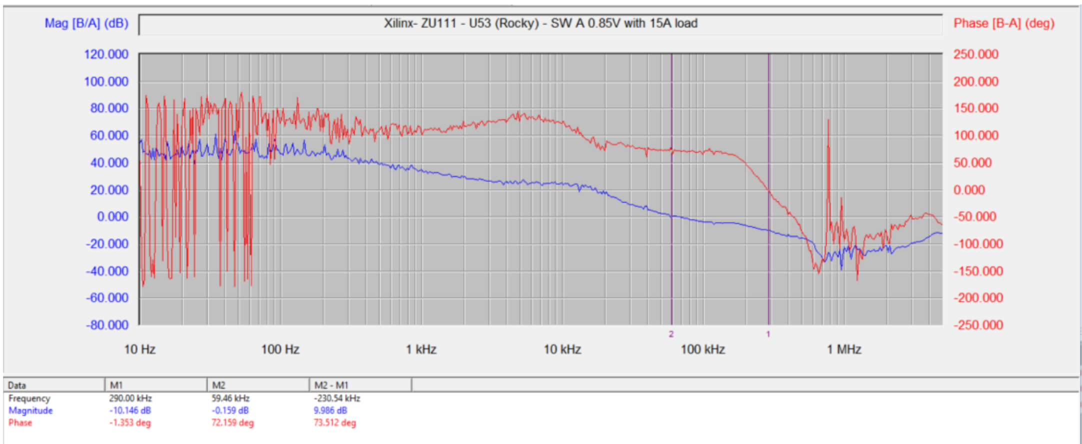


**Figure 9 Bode analysis measurements of the VCCINT_IO_BRAM rail with a 15 A constant load**

At full load of 15 A, the closed-loop bandwidth is around 60 kHz with 72 degrees of phase margin and around -10 dB of gain margin.

# 7 Telemetry

One of the primary advantages of a digital PoL is telemetry over the I²C or PMBus. The IRPS5401 PMIC and digital IPoL series (IR3806x) devices all support I²C and PMBus telemetry. Shown below is the snapshot in PowIR Center for a IRPS5401 PMIC switcher A.

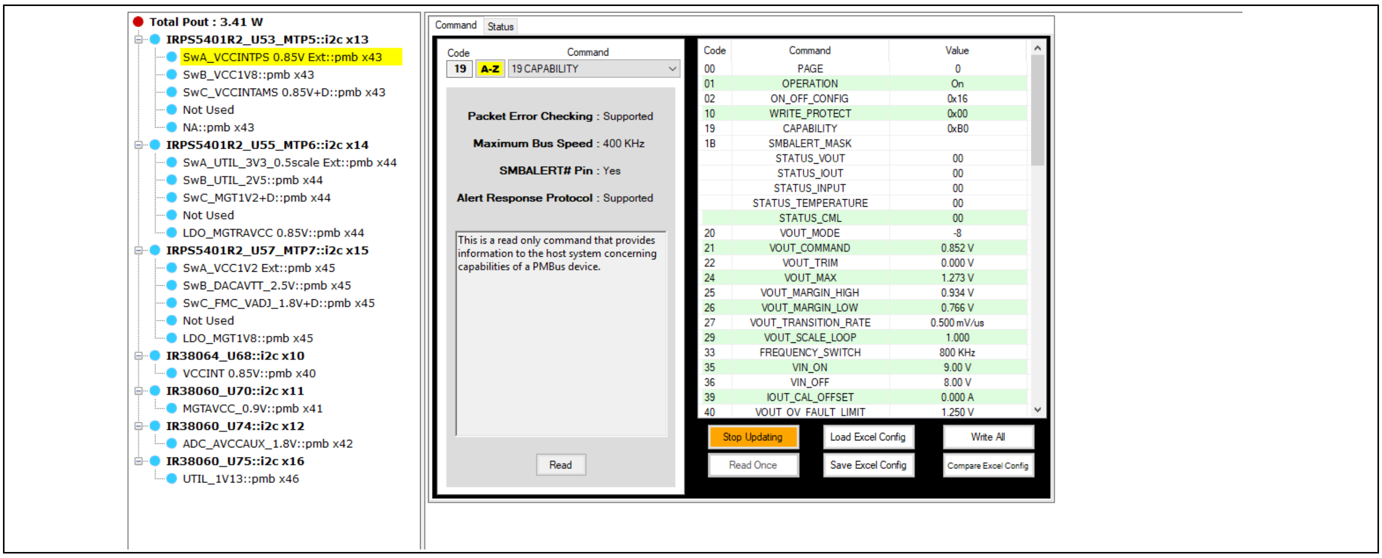


**Figure 10 PowIR Center snapshot of IRPS5401 PMIC switcher A and supported PMBus commands**

All the IRPS5401 PMICs shown in the above PowIR Center GUI are as per the ZCU-111 reference design. All devices listed here support the PMBus 1.2 spec and all supporting commands.

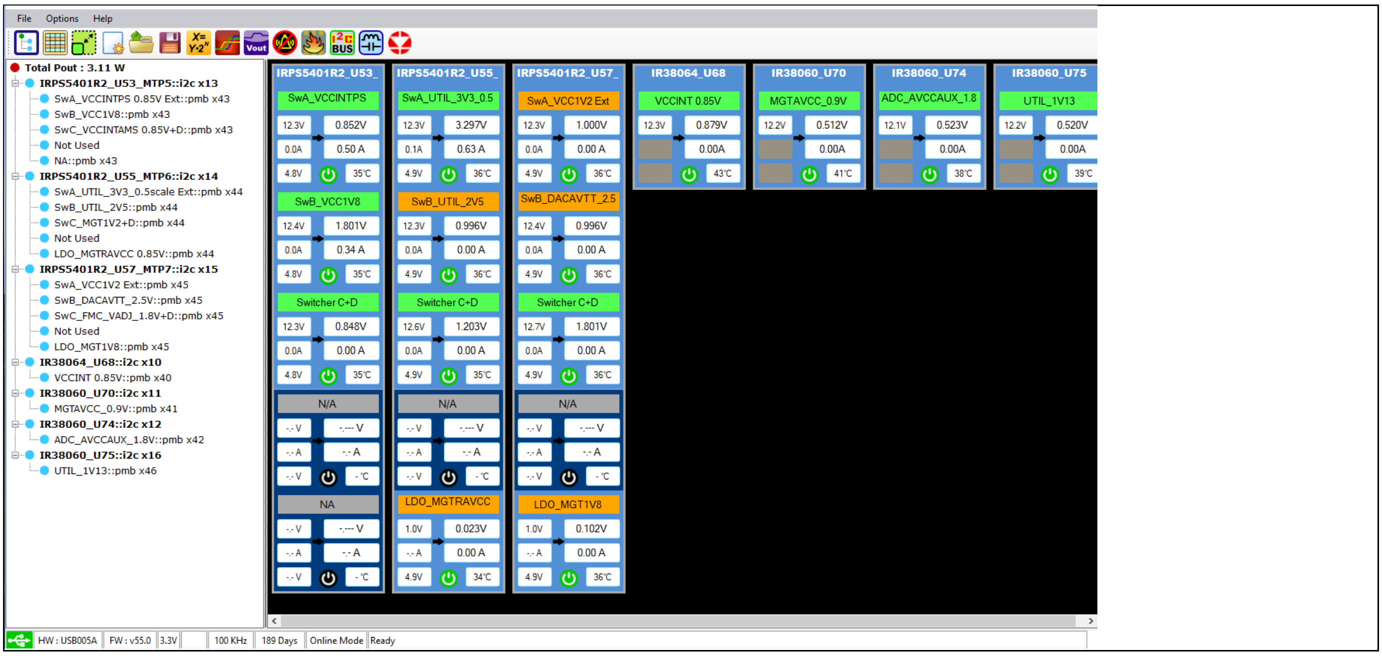


**Figure 11 The main window in PowIR Center showing the ZCU-111 reference design**

The main window shows all the main power rails on the ZCU-111. In the main window you can easily see the $V_{in}$ voltage of 12 V and the output voltage with all corresponding load current information. All other information is available in PowIR Center for further telemetry readings. The main window shows critical information about the voltage rail such as $V_{in}$, $V_{out}$, $I_{out}$, $V_{drive}$ voltage and die temperature. The green light indicates that the rail is operating as expected without problems. The orange indicator means that there is a warning flag on the rail. If there is a fault on the rail causing a shut-down, that particular rail will show up as red.

# 8 Form factor

Form factor typically varies from application to application. Shown below is a fully fledged ZCU-111 evaluation platform with various IRPS5401 PMICs and digital IPoLs (IR3806x).

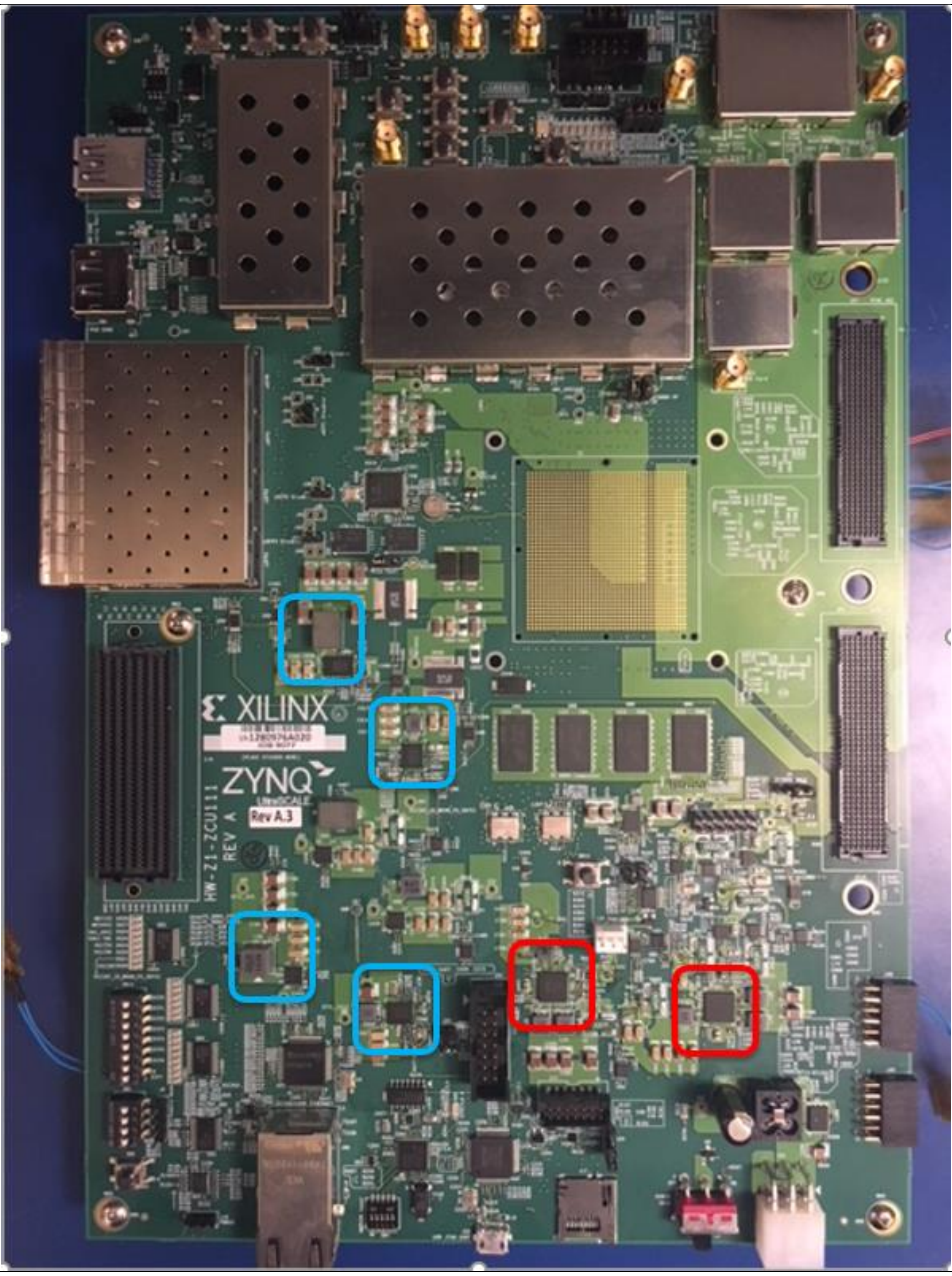


**Figure 12 Photo of the ZCU-111 reference board design. Devices highlighted in red are the two out of three IRPS5401 PMICs on this design. The third IRPS5401 PMIC is on the bottom side. The devices highlighted in blue are the four IR3806x digital IPoL devices.**

The end application could require additional power rails like the ZCU-111 design shown in Figure 12, or it could be a small form-factor design like the ones shown in Figure 13.

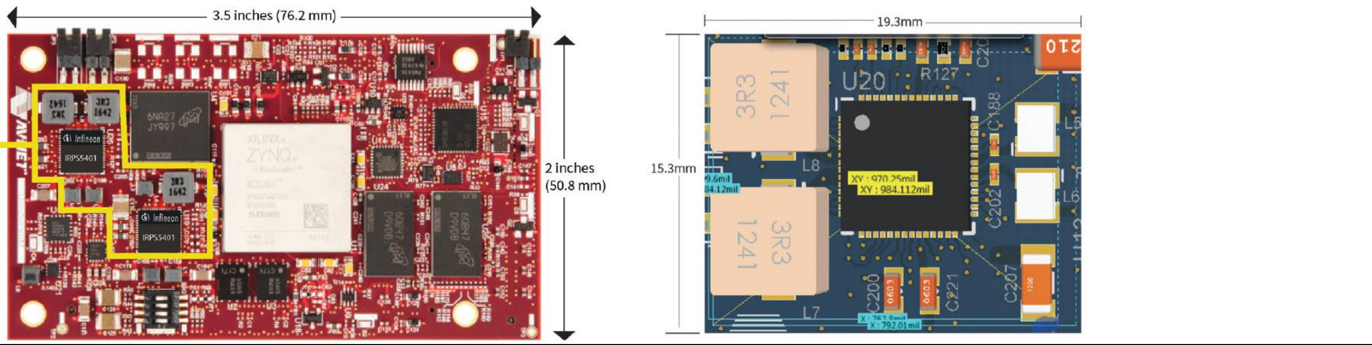


**Figure 13** **(a) Photo of a compact Zynq FPGA/SoC design (b) small form-factor design with just the IRPS5401 PMIC**

From Figures 12, 13a and 13b, it is evident that the IRPS5401 PMIC can be configured to meet various form-factor requirements. Whether it is a space-constrained design or an efficiency-optimized design, Infineon can provide an IRPS5401-based power architecture that will meet your design requirements. Figures 13a and 13b show tighter PMIC design that can meet small form-factor requirements.

# 9 Conclusion

There are limitless end applications for FPGAs today. The Zynq UltraScale+ FPGAs provide unique processing capabilities. Providing the necessary solutions to power the various SKUs of Zynq US FPGAs is critical for any Zynq design. The unique sequencing, power capabilities and performance necessary to power each rail of the Zynq US FPGA have all been discussed. The IRPS5401 PMIC is an essential recommendation in such design. Depending on the core power requirements an IRPS5401 PMIC with an external power stage or an IR35215 multi-phase controller can be utilized every other rail and can be powered with the integrated switchers and LDO on the IRPS5401 PMIC. There are various power reference designs that power different SKUs of the Zynq US FPGA. All telemetry information is provided in conformance with the PMBus spec to provide an intelligent power supply for FPGA applications.

## Revision history

| Document version | Date of release | Description of changes |
|---|---|---|
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