2019 Xilinx Security Working Group (XSWG) Munich, Germany Agenda

Hilton Airport Munich, Terminalstraße Mitte 20, 85356 München-Flughafen, Germany

Wednesday, December 4, 2019	
All Presentations in Munich I & II	
Topic	**Time**
Welcome and Introductions	8:15 - 8:30
Designing Security into Commercial Products: Challenges and Best Practices	8:30 - 9:00
What is "In the Box" and What is "Out of the Box"	9:00 - 9:30
Attacking Semiconductor Devices - Part I	9:30 - 10:00
Break	10:00 - 10:30
Attacking Semiconductor Devices - Part II	10:30 - 11:30
3rd Party Assessments of Xilinx Devices	11:30 - 12:15
Lunch	12:15 - 1:15
Securing FPGA as a Service (FaaS)	1:15 - 1:45
SmartNIC Security Considerations	1:45 - 2:15
Industrial and Healthcare IoT Security	2:15 - 3:00
Break	3:00 - 3:30
Securing the Automobile	3:30 - 4:15
Supply Chain Protections: From Xilinx to the End User	4:15 - 5:00
Day 1 wrap up / Summary Statements	5:00 - 5:15

2019 Xilinx Security Working Group (XSWG) Munich, Germany Agenda

Hilton Airport Munich, Terminalstraße Mitte 20, 85356 München-Flughafen, Germany

Thursday, December 5, 2019		
Track 1 :Munich I & II Room Topics	**Time**	**Track 2 : Chicago Room Topics**
Day 2 Welcome	8:15 - 8:30	
Versal Hardware Root of Trust (HWRoT) Secure Boot	8:30 - 9:15	**ZU+ Secure Boot**
Versal Encrypt Only Secure Boot	9:15 - 10:00	**ZU+ Security Features**
Break	10:00 - 10:30	**Break**
Versal Security Features	10:30 - 11:30	**ZU+ Trusted Execution Environment (TEE)**
Isolation and Access Controls in Versal	11:30 - 12:15	**ZU+ Embedded Software Security**
Lunch	12:15 - 1:15	**Lunch**
Versal Security Solutions Roadmap	1:15 - 2:15	**ZU+ Hardware Security Module (HSM) IP Solution**
UltraScale / UltraScale+ FPGA Security	2:15 - 3:00	**Security Monitor IP**
Break	3:00 - 3:30	**Break**
Provisioning / Secure Provisioning Service	3:30 - 4:15	**Please join presentations in Munich I & II Room**
Guidance on Essential Security Design Resources / Information	4:15 - 5:00	
XSWG 2019 Adjournment	5:00 - 5:15	