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PIC16F170X Peripheral Pin Select (PPS) Technical Brief

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INTRODUCTION

Peripheral Pin Select (PPS) enables flexible digital peripheral mapping to a wide range of external pins. Whereas in the past, a peripheral was hard-wired to a specific pin (example: PWM1 output on pin RC5). PPS allows the developer to choose from a number of output pins, creating the following advantages:

1. More drop-in sockets: With the flexibility to change pin mappings, it will sometimes be possible to switch from another microcontroller/ ASIC to a PIC® device without any board changes.
2. Board work-arounds: If a PCB has an error where the signal was not routed to the correct (intended) pin, this problem may be solved in firmware, without requiring PCBs to be scrapped/re-done.
3. Efficient layout/reduced PCB area: With the option to route signals to components placed close-by, layout can be simplified and PCB area reduced. Shorter traces also maximize signal integrity.

PIC16F170X parts offer wide-ranging PPS capability, where any digital peripheral can be connected to any standard I/O pin. This offers increased flexibility over PPS scenarios where full interconnect is not permitted.

Some Microchip customers may be familiar with PPS from the PIC24 product line. PPS for the PIC16 differs in that each PIC16 digital peripheral input signal is connected to a pin by default. This stands in contrast to PPS for the PIC24 products, where peripherals are left unconnected by default. For PIC16 PPS, peripheral output signals need to be selected before the peripheral is enabled. Peripheral input signals should be re-mapped to other pins (if desired). Then, the peripheral should be enabled after both input and output selection has been completed.

This short technical brief describes how pin selection is done for some common peripherals on the PIC16F1708. Because the PPS settings are critical to the operation of the device, the PPS registers are equipped with a LOCK mechanism. After PPS settings are completed, the PPS registers should be locked to prevent unintended changes. The PPS registers are unlocked following a Reset event.

For further protection, a PPS1WAY fuse is available which disallows an UNLOCK of the registers. If this fuse is enabled, the PPS registers can be initialized after Reset, and once the PPSLOCK is set, it cannot be cleared through software.

The PPS LOCK/UNLOCK code sequence is shown below:

EXAMPLE 1: CODE SEQUENCE TO LOCK PPS REGISTERS FROM CHANGES

```
BCF INTCON, GIE       ; DisableInterrupts:
BANKSEL PPSLOCK       ; Bank to PPSLOCK register
MOVLW 55h             ; Required sequence, next 4 instructions
MOVWF PPSLOCK
MOVLW AAh
MOVWF PPSLOCK
BSF PPSLOCK, 0        ; Set PPSLOCK bit - BCF for unlock
BSF INTCON, GIE       ; Re-enable Interrupts
```

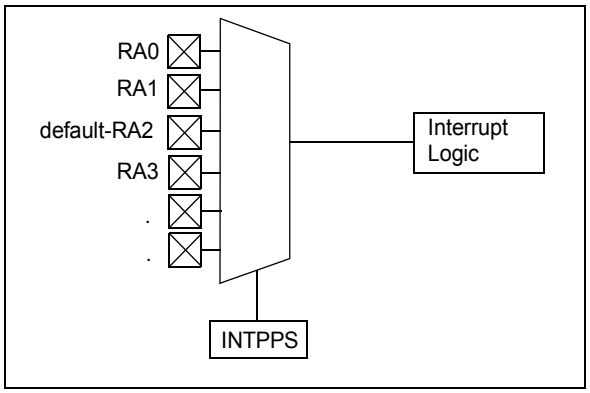
PPS is configured differently for input and output signals:

1. Input Signals: Input signals are configured in the peripheral itself. The port must be configured as an input using the associated TRIS register.
2. Output Signals: Output signals are controlled by a corresponding PPS selection register for the output pin.

PPS INPUT EXAMPLE – INTERRUPT CONNECTED TO RA3

To illustrate how an input can be reconfigured, we will look at the case of an interrupt. The interrupt block contains a register called “INTPPS”. The value in this register determines which pin is connected to the interrupt module.

FIGURE 1: INTPPS INPUT MUX



The INTPPS register has a default value of 0x02, which maps the interrupt input to the RA2 pin. The INTPPS value can be changed to map the interrupt input signal to another physical input pin according to the following table:

TABLE 1: INTPPS INPUT MUX DECODE

INTPPS value	Connected to	INTPPS value	Connected to	INTPPS value	Connected to
00000	RA0	01000	GND	10000	RC0
00001	RA1	01001	GND	10001	RC1
00010	RA2	01010	GND	10010	RC2
00011	RA3	01011	GND	10011	RC3
00100	RA4	01100	RB4	10100	RC5
00101	RA5	01101	RB5	10101	RC5
00110	GND	01110	RB6	10110	RC6
00111	GND	01111	RB7	10111	RC7

All other PPS Input Selection registers use the same values to connect to the corresponding pin. Code to connect the interrupt to RA3 would be the following:

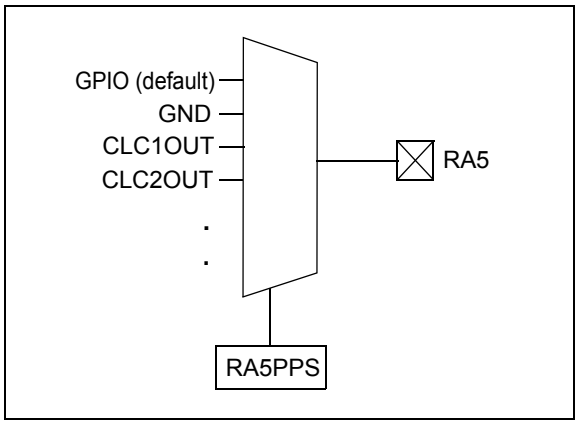
EXAMPLE 2: CODE IMPLEMENTATION CONNECTING INTERRUPT TO RA3

```
Banksel INTPPS            ; go to bank with INTPPS registers
movlw 0x03                ; move value of 3
movwf INTPPS              ; to INTPPS register
```

PPS OUTPUT EXAMPLE – CONFIGURABLE LOGIC CELL (CLC) TO RA5

To illustrate how an output can be reconfigured, we will look at the case of a CLC output signal. Physical output pins are mapped to the peripheral through a register associated with the pin. It is necessary to map the output signal to the desired physical pin through the pin's associated PPS register.

FIGURE 2: RA5PPS OUTPUT MUX



For this example, we will use the "RA5PPS" register. The RA5PPS register has a Reset value of '0', which means that the RA5 pin is General Purpose Input/Output (GPIO) and controlled with the LATA<5> and TRISA<5> registers. In order to connect the CLC1OUT signal to this pin, we need to write a value of 00100 to the RA5PPS register. The RA5 pin output function mapping is controlled according to the following table:

TABLE 2: RA5PPS OUTPUT MUX DECODE

INTPPS value	Connected to	INTPPS value	Connected to	INTPPS value	Connected to
00000	GPIO	01000	COG1A	10000	SCK/SCL
00001	GND	01001	COG1B	10001	SDA
00010	GND	01010	COG1C	10010	SDO
00011	GND	01011	COG1D	10011	ZCDOUT
00100	CLC1OUT	01100	CCP1	10100	TX/KX
00101	CLC2OUT	01101	CCP2	10101	DT
00110	CLC3OUT	01110	PWM3OUT	10110	C1OUT
00111	GND	01111	PWM4OUT	10111	C2OUT

Code to connect the CLC1OUT output signal to RA5 would be the following:

EXAMPLE 3: CODE IMPLEMENTATION CONNECTING CLC1OUT TO THE RA5 PIN

```
Banksel RA5PPS       ; go to bank with RA5PPS registers
movlw 0x04           ; move value of 4
movwf RA5PPS         ; to RA5PPS register
```

CONCLUSION

This short technical brief describes how Peripheral Pin Select (PPS) can be used. More details can be found in the product-specific data sheet (DS40001683).

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