IS31FL3713

4×3 MATRIX LED DRIVER WITH INTEGRATED BOOST

July 2026

GENERAL DESCRIPTION

The IS31FL3713 is a general purpose 4×3 LED Matrix programmed via 1MHz I2C compatible interface. Each LED can be dimmed individually with 6+4-bit PWM data and each LED can be dimmed with 8-bit DC scaling (Color Calibration) data which allowing 1024 steps of linear PWM dimming and 256 steps of DC current level adjustment.

Additionally, each LED open and short state can be detected, IS31FL3713 stores the open or short information in Open-Short Registers. The Open-Short Registers allow MCU to read out via I2C compatible interface. Inform MCU whether there are LEDs open or short and the locations of open or short LEDs.

IS31FL3713 is supplied by an integrated boost DC-DC converter. Its output voltage can be adjusted by the internal register to optimize efficiency according to the type of LEDs (their forward voltage). This reduces the power dissipation and improves overall efficiency.

Each LED of IS31FL3713 can operate in “PWM mode” or “Pattern mode” or “Current Level mode”. In “PWM mode”, the dot current is set by 1024 steps PWM and 256 steps current level registers. In “Pattern mode”, the timing characteristics for RGB dots can be individually adjusted to maintain a pre-established pattern sequence without requiring any additional MCU interaction, thus saving valuable system resources. In “Current Level mode”, the output current is set by 256 steps current level register.

IS31FL3713 is available WLCSP-12 (0.4mm ball pitch, 0.2mm ball diameter) package.

The IS31FL3713 operates from 2.2V to 5.5V and features a very low operational current over the temperature range of -40°C to +125°C.

FEATURES

- Supply voltage range: 2.2V to 5.5V
- Support 4×3 matrix configurations
- Ultra-low operational current 1.1mA (typ.)
- Accurate color rendition
  - 6-bit global current adjustment
  - 8-bit current adjust for each dot
  - 6+4-bit PWM for each dot
- 1MHz I2C-compatible interface
  - Automatic address increment function
- Auto breath function:
  - 12 patterns for auto breath.
  - Each LED can select the pattern or PWM control
  - Each pattern contains TS~TP time slope control
- Individual open and short detect function
- Synchronization for multi-device application
- 5% (Max.) at 50.7mA bit to bit matching
- 5% (Max.) at 50.7mA device to device matching
- De-ghost
- WLCSP-12 (0.4mm ball pitch, 0.2mm ball diameter) package
- RoHS & Halogen-Free Compliance
- TSCA Compliance

APPLICATIONS

- Hand-held devices for LED display
- Wireless gaming devices (Mouse, Mouse PAD etc.)
- IOT device (AI speaker etc.)

TYPICAL APPLICATION CIRCUIT

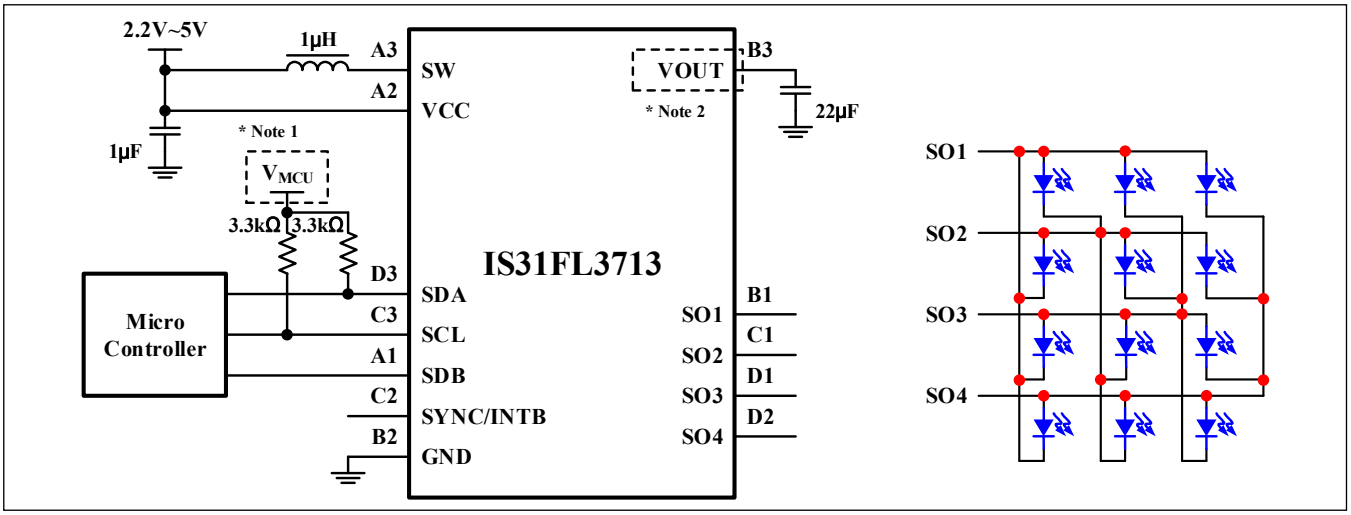


Figure 1 Typical Application Circuit: 12 Mono Color LEDs

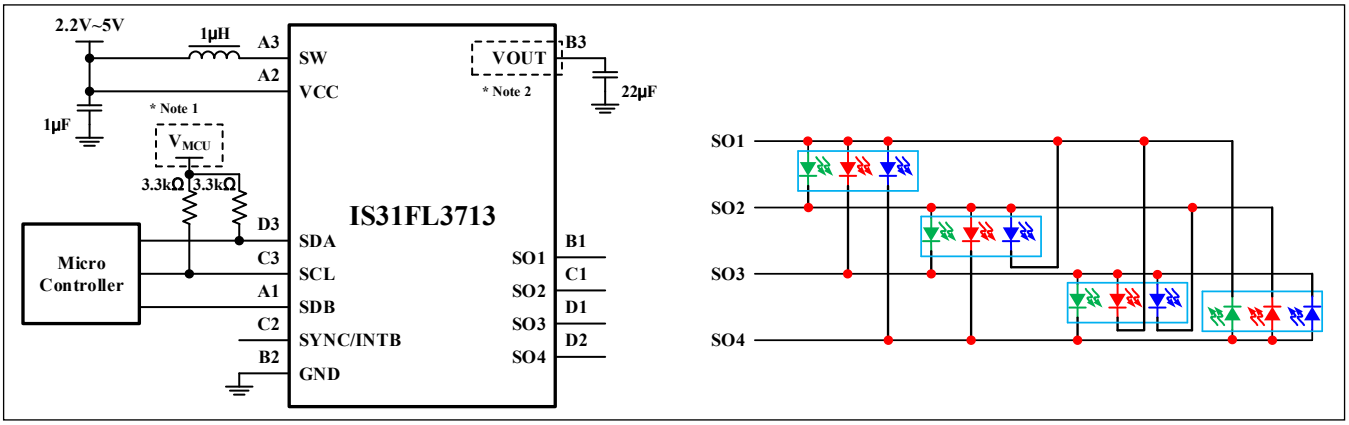


Figure 2 Typical Application Circuit: 4 RGB LEDs

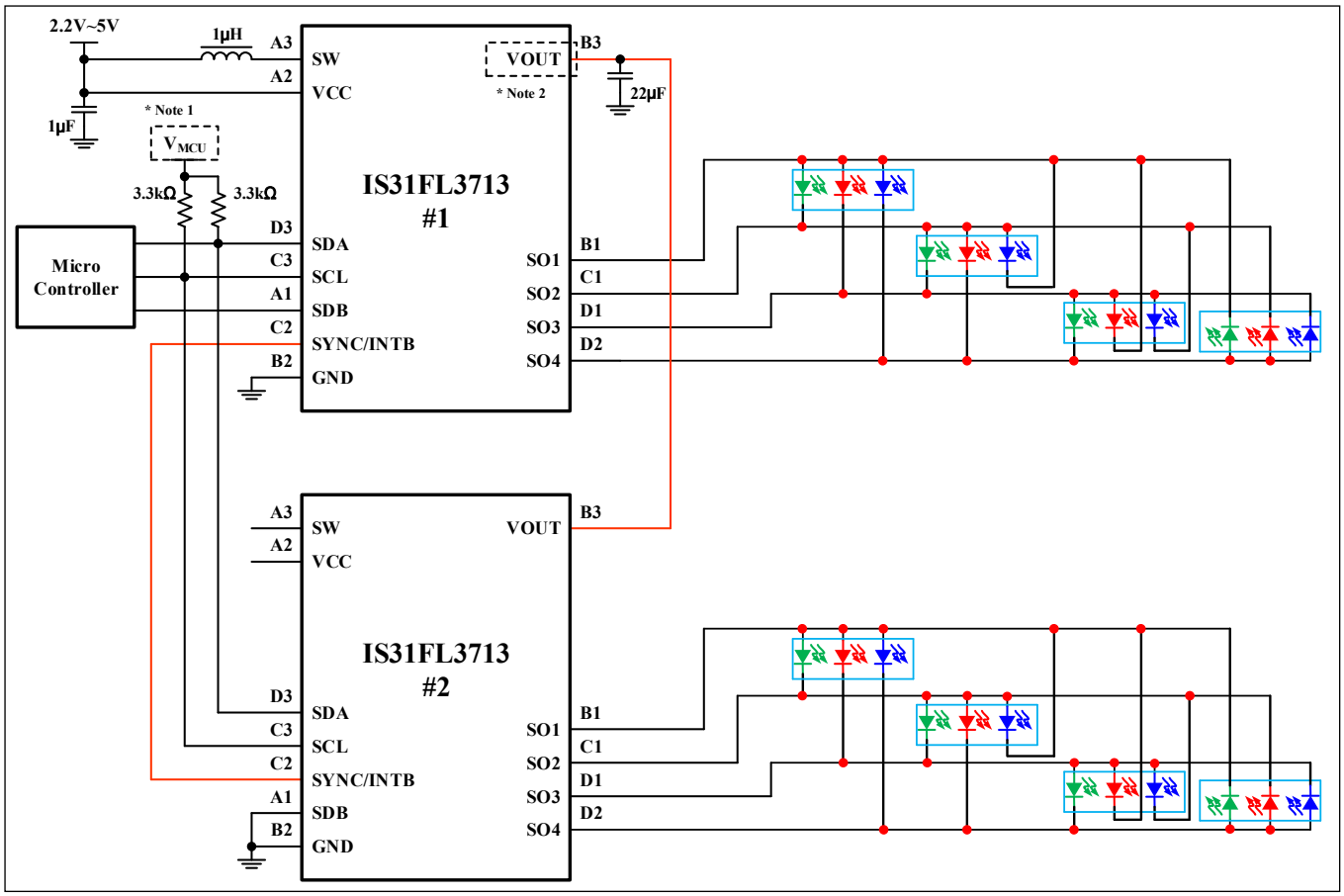
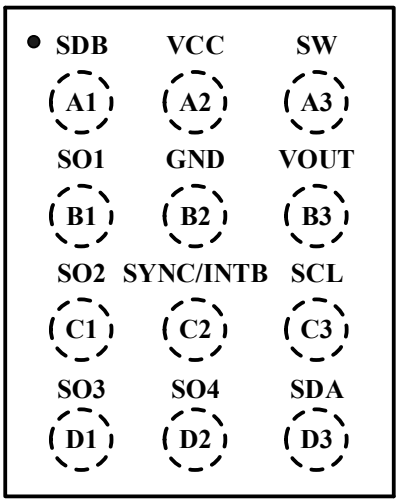


Figure 3 Typical Application Circuit: Cascade Mode

Note 1: V_{IH} is the high level voltage for IS31FL3713 I2C bus, which is usually same as VCC of Micro Controller, e.g. if VCC of Micro Controller is 3.3V, V_{IH} = 3.3V.

Note 2: V_{OUT} must be higher than V_{SOX}.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
WLCSP-12	

PIN DESCRIPTION

No.	Pin	Description
A1	SDB	Shutdown pin.
A2	VCC	Power supply.
A3	SW	Switching node of the step-up converter.
B1,C1,D1,D2	SO1~SO4	Current sink/Power SW.
B2	GND	Power ground.
B3	VOUT	Output voltage pin. Connect a 22μF capacitor from VOUT to GND.
C2	SYNC/INTB	SYNC input or output for cascade. When INTB function is enabled, this pin is INTB pin. Pull-up to V_{MCU}.
C3	SCL	I2C compatible serial clock.
D3	SDA	I2C compatible serial data.

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS31FL3713-CLS4-TR	WLCSP-12, Lead-free	3000

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a.) the risk of injury or damage has been minimized;

b.) the user assume all such risks; and

c.) potential liability of Lumissil Microsystems is adequately protected under the circumstances

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~+6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~+150°C
Operating temperature range, T_A=T_J	-40°C ~ +125°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	72.5°C/W
ESD (HBM) ESD (CDM)	±4kV ±750V

Note 3: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{CC}= 3.6V, T_A= 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	T_A= -40°C ~ +85°C	2.2		5.5	V
		T_A= -10°C ~ +85°C	1.8		5.5	V
I_{CC}	Quiescent power supply current	V_{CC}=3.6V, V_{SDB}= V_{CC}, 4×3 mode, OSC= 6MHz, PWM= 0x3FF, SL=0xFF, GCC=0x3F, B6h=0x00 (Boost pass mode)		1.2	1.29	mA
		V_{CC}=3.6V, V_{SDB}= V_{CC}, 4×3 mode, OSC= 6MHz, PWM= 0x200, SL=0xFF, GCC=0x3F, B6h=0x00 (Boost pass mode)		1.1	1.23	mA
I_{SD}	Shutdown current	V_{SDB}= 0V		0.3	1	μA
I_{STB}	Standby current	V_{SDB}= V_{CC}, A0H=0x04		0.33	0.36	mA
I_{OUT}	Peak sink current of SOx	V_{SDB}= V_{CC}, all LEDs off, 4×3 mode, OSC= 6MHz, GCC=0x3F, SL= 255/255, PWM= 0x3FF	48.17	50.7	53.24	mA
ΔI_{MAT}	Sink current between channels	PWM=0x3FF, SL=0xFF, GCC=0x3F (Note 4)	-5		5	%
ΔI_{ACC}	Sink current between device to device	PWM=0x3FF, SL=0xFF, GCC=0x3F (Note 5)	-5		5	%
ΔI_{MAT}	Sink current between channels	PWM=0x3FF, SL=0xFF, GCC=0x1A (Note 4)	-5		5	%
ΔI_{ACC}	Sink current between device to device	PWM=0x3FF, SL=0xFF, GCC=0x1A (Note 5)	-5		5	%
I_{LED}	Average current on each LED I_{LED}= $I_{OUT(PEAK)}$/Duty (Duty =1/4.363)	V_{SDB}= V_{CC}, all LEDs off, 4×3 mode, OSC= 6MHz, GCC=0x3F, SL= 255/255, PWM= 0x3FF		12.675		mA
V_{HR}	Output current headroom voltage of SOx	I_{SWITCH}= 150mA		150	200	mV
	Constant sink current headroom voltage of SOx	I_{OUT}= 50.7mA		260	350	

ELECTRICAL CHARACTERISTICS (CONTINUE)

The following specifications apply for V_{CC}= 3.6V, T_A= 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{SCAN}	Period of scanning	PFS= “000” (6MHz)		10.96		μs
t_{NOL1}	Non-overlap blanking time during scan, the SOx are all off during this time	PFS= “000” (6MHz)		0.996		μs
t_{NOL2}	Total delay time from SO2 to SO4 (Note 6)	PFS= “000” (6MHz)		83		ns
V_{OD}	OUTx pin open detect threshold	V_{CC}= 3.6V, I_{OUT}≥ 1mA, PWM on time> 1.5μs, measured at SOx	80	100		mV
V_{SD}	LED short detect threshold	V_{CC}= 3.6V, I_{OUT}≥ 1mA, PWM on time> 1.5μs, measured at (V_{OUT}-V_{SOx})		1	1.2	V
T_{SD}	LED thermal shutdown	(Note 7)		155		°C
	Boost thermal shutdown	(Note 7)		165		°C
T_{SD_HYS}	Thermal shutdown hysteresis	(Note 7)		15		°C
Logic Electrical Characteristics (SDA, SCL, SDB, SYNC/INTB)						
V_{IL}	Logic “0” input voltage	V_{OUT}= 3V~5V	GND		0.4	V
V_{IH}	Logic “1” input voltage	V_{OUT}= 3V~5V	1.4		5	V
V_{HYS}	Input Schmitt trigger hysteresis			0.2		V
I_{IL}	Logic “0” input current	V_{INPUT}= 0V (Note 7)		5		nA
I_{IH}	Logic “1” input current	V_{INPUT}= V_{CC} (Note 7)		5		nA
V_{OL_SDA}	Logic “0” output voltage	I_{LOAD}= 5mA	0		0.4	V
V_{OH}	H level SYNC pin output voltage	I_{OH}= -8mA	V_{OUT}-0.4V		V_{OUT}	V
V_{OL}	L level SYNC/INTB pin output voltage	I_{OL}= 8mA	0		0.4	V
Step-Up Converter						
I_{LIM}	Peak NMOS current limit			1.8	2.3	A
I_O	Total output current limit from VOUT	V_{CC}≥ 3V (Note 7)	400			mA
f_{SW}	Oscillator frequency			1.0		MHz
D_{MAX}	Maximum duty cycle	(Note 7)		60		%
V_{OVP}	Internal over voltage threshold of VOUT			5.2		V
R_{DS_ON}	High-side MOSFET on resistance	V_{OUT}= 5V		150		mΩ
	Low-side MOSFET on resistance	V_{OUT}= 5V		50		mΩ
t_S	soft start time	(Note 7)		<1000		μs

DIGITAL INPUT I2C SWITCHING CHARACTERISTICS (NOTE 7)

Symbol	Parameter	Fast Mode			Fast Mode Plus			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Serial-clock frequency	-		400	-		1000	kHz
t_{BUF}	Bus free time between a STOP and a START condition	1.3		-	0.5		-	μs
$t_{HD, STA}$	Hold time (repeated) START condition	0.6		-	0.26		-	μs
$t_{SU, STA}$	Repeated START condition setup time	0.6		-	0.26		-	μs
$t_{SU, STO}$	STOP condition setup time	0.6		-	0.26		-	μs
$t_{HD, DAT}$	Data hold time	-		-	-		-	μs
$t_{SU, DAT}$	Data setup time	100		-	50		-	ns
t_{LOW}	SCL clock low period	1.3		-	0.5		-	μs
t_{HIGH}	SCL clock high period	0.7		-	0.26		-	μs
t_R	Rise time of both SDA and SCL signals, receiving	-		300	-		120	ns
t_F	Fall time of both SDA and SCL signals, receiving	-		300	-		120	ns

Note 4: I_{OUT} mismatch (bit to bit) $\triangle I_{MAT}$ is calculated:

$$\Delta I_{MAT} = \pm\left(\frac{I_{OUT(MAX)} - I_{OUT(MIN)}}{\left(\frac{I_{OUT0}+I_{OUT1}+\ldots+I_{OUT4}}{4} \times 2\right)}\right) \times 100\%$$

Note 5: I_{OUT} accuracy (device to device) $\triangle I_{ACC}$ is calculated:

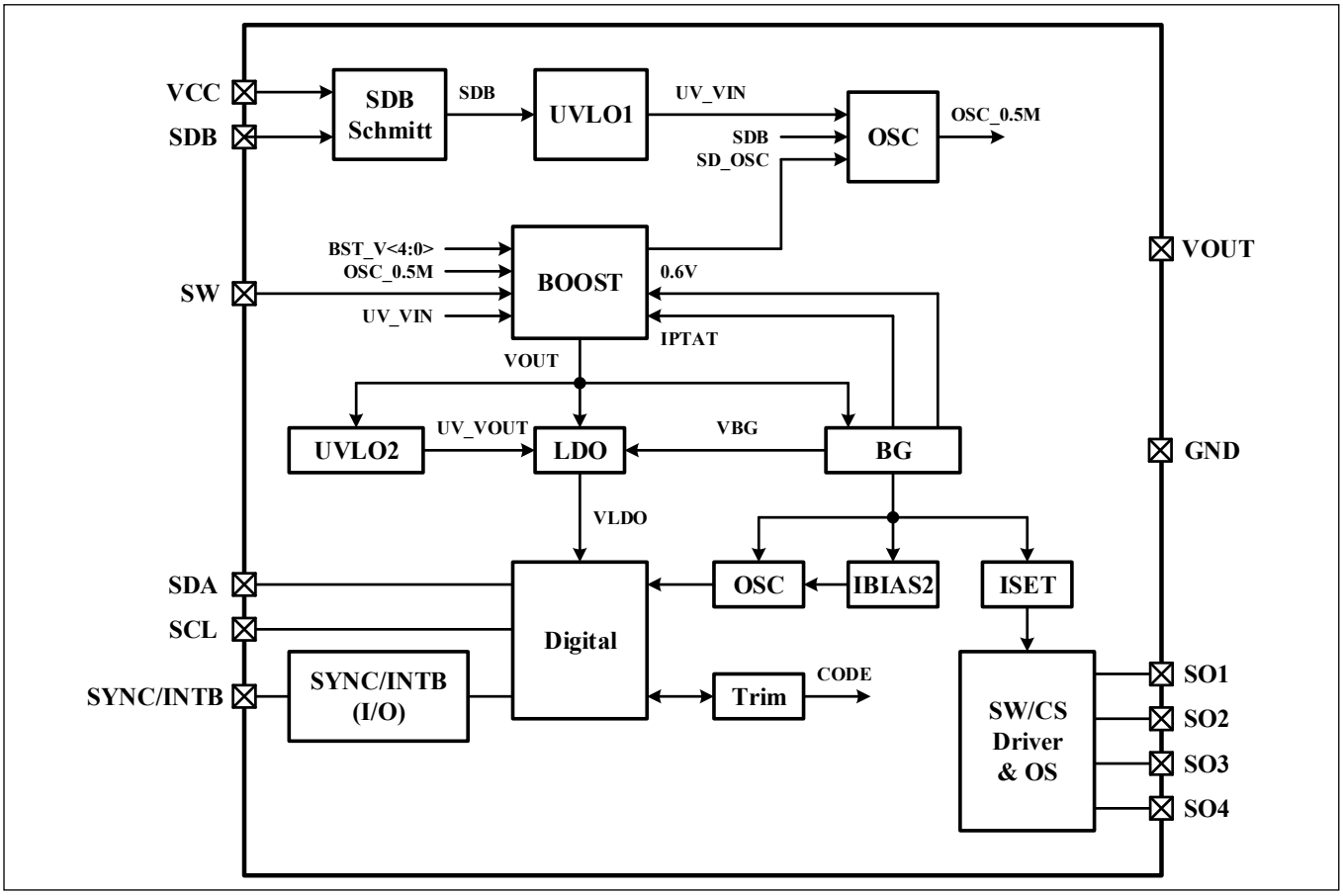
$$\Delta I_{ACC} = \pm\left(\frac{I_{OUT(AVG)} - I_{OUT(IDEAL)}}{I_{OUT(IDEAL)}}\right) \times 100\%$$

Where $I_{OUT(IDEAL)}$= 50.7mA.

Note 6: When matrix size is 4×3, only one of SOx will work as power source, and others work as constant current sinks. t_{NOL2} is the delay time of SO3/SO4. For example, when SO1 is power source, SO2 will turn on immediately, SO3/SO4 will turn on follow the time of t_{NOL2}, about 0.083μs.

Note 7: Guarantee by design.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

I2C INTERFACE

The IS31FL3713 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3713 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The complete slave address is:

Table 1 Slave Address

A7:A1	A0
0001 100	0/1

The SCL line is uni-directional. The SDA line is bi-directional (open-drain) with a pull-up resistor (typically 2kΩ). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the micro-controller and the slave is the IS31FL3713.

The timing diagram for the I2C is shown in Figure 3. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3713's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3713 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3713, the register address byte is sent, most significant bit first. IS31FL3713 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3713 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3713, load the address of the data register that the first data byte is intended for. During the IS31FL3713 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3713 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3713 (Figure 6).

READING OPERATION

Most of the registers can be read.

To read the registers, after I2C start condition, the bus master must send the IS31FL3713 device address with the R/$\overline{W}$ bit set to "0", followed by the register address, which determines which register is accessed. Then restart I2C, the bus master should send the IS31FL3713 device address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS31FL3713 to the master (Figure 7).

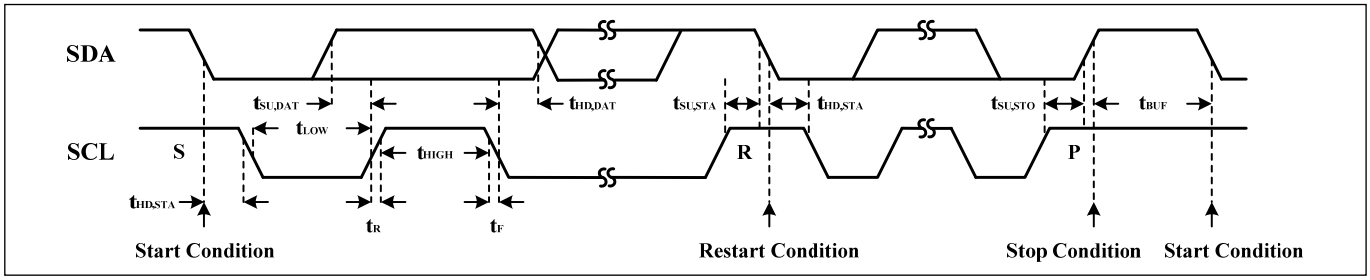


Figure 3 I2C Interface Timing

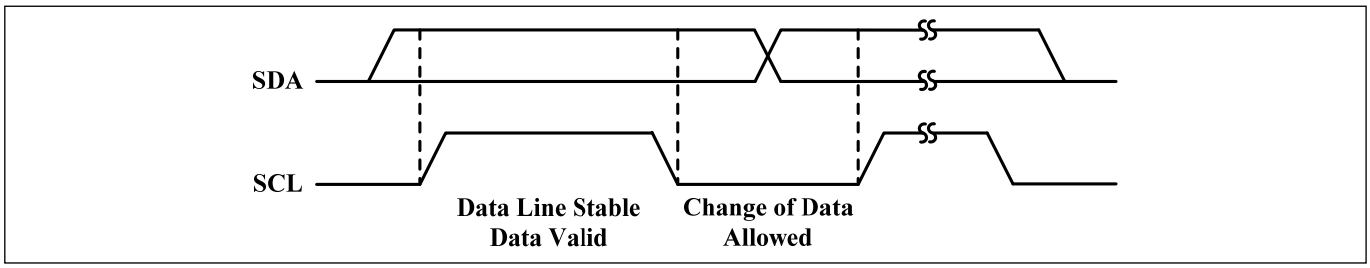


Figure 4 I2C Bit Transfer

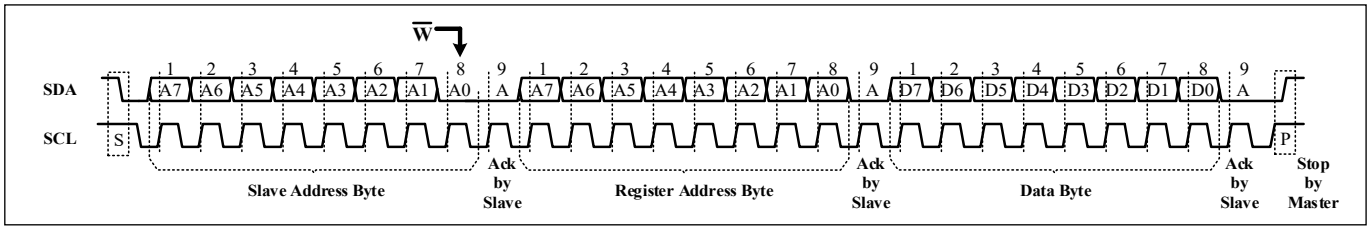


Figure 5 I2C Writing to IS31FL3713 (Typical)

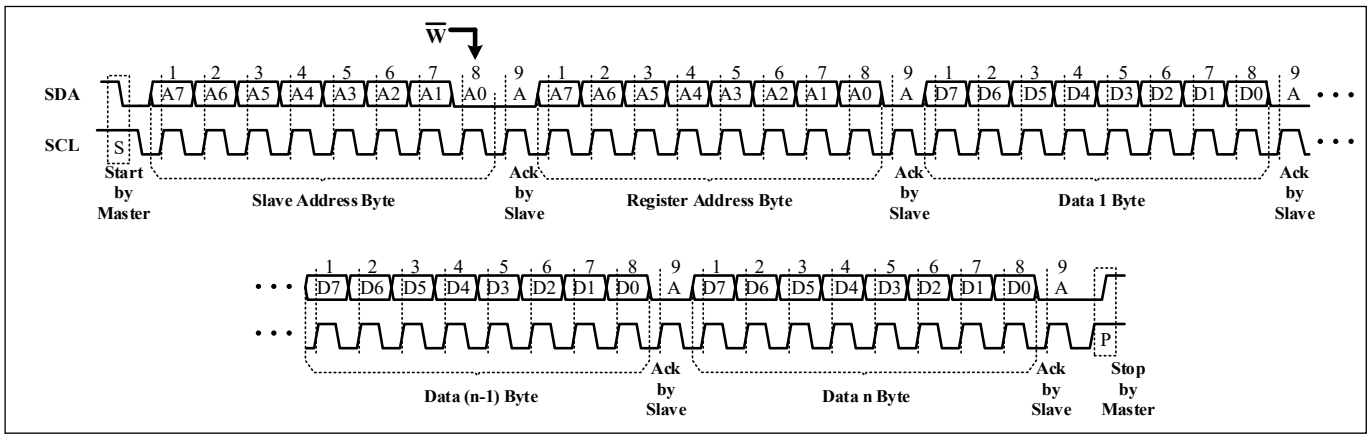


Figure 6 I2C Writing to IS31FL3713 (Automatic Address Increment)

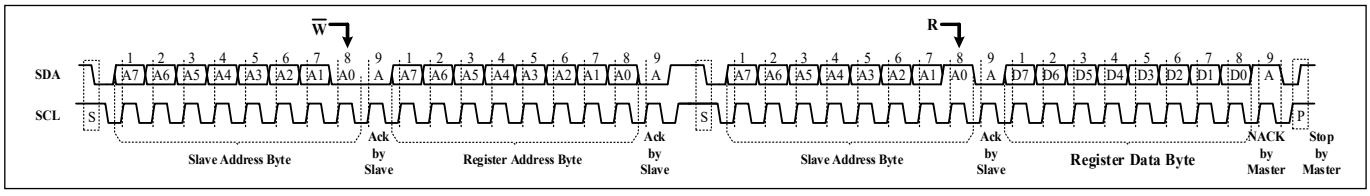


Figure 7 I2C Reading from IS31FL3713

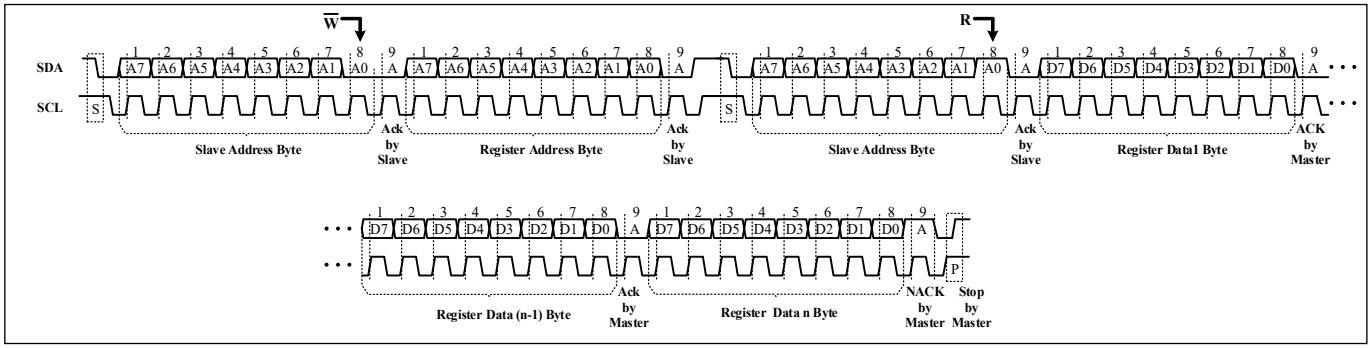


Figure 8 I2C Reading from IS31FL3713(Automatic Address Increment)

Table 2 Registers Definitions

Address	Name	Function	R/W	Table	Default
00h~01h	ON OFF Register	Enable LED	R/W	3	0111 0111
02h~19h	PWM Register	Set PWM duty for LED	R/W	4	0000 0000
1Ah~25h	Scaling Register	Set Scaling for each dot	R/W	5	0000 0000
26h~27h	Pattern Mode Enable Register	Pattern mode enable bit	R/W	7	0000 0000
28h~2Ch/31h~35h/3Ah~3Eh/ 43h~47h/4Ch~50h/55h~59h/ 5Eh~62h/67h~6Bh/70h~74h/ 79h~7Dh/82h~86h/8Bh~8Fh	Pattern Mode PWM Register	Set PWM duty for Pattern mode	R/W	8	0000 0000
2Dh/36h/3Fh/48h/51h/5Ah/ 63h/6Ch/75h/7Eh/87h/90h	Pattern TS &T1 Setting Register	Set the TS~T1 time	R/W	9	0000 0000
2Eh/37h/40h/49h/52h/5Bh/ 64h/6Dh/76h/7Fh/88h/91h	Pattern T2 &T3 Setting Register	Set the T2~T3 time	R/W	10	0000 0000
2Fh/38h/41h/4Ah/53h/5Ch/ 65h/6Eh/77h/80h/89h/92h	Pattern T4&TP Setting Register	Set the T4~TP time	R/W	11	0000 0000
30h/39h/42h/4Bh/54h/5Dh/ 66h/6Fh/78h/81h/8Ah/93h	Pattern Loop Times Register	Set the loop time of PWM1~PWM5	R/W	12	0000 0000
94h/95h/96h/97h/98h/99h	Pattern Control Register	Pattern start/stop/hold/continue	R/W	13	0000 0000
9Ah	All Pattern Start/Stop Register	Start/stop all pattern	R/W	-	0000 0000
9Bh	Current Level Mode Register	Enable current level mode	R/W	15	0000 0000
9Ch	PWM Update Register	Update PWM register	R/W	-	0000 0000
A0h	Configuration Register	Configure the operation mode	R/W	16	0000 0100
A1h	Global Current Control Register	Set the global current	R/W	18	0000 0000
A2h	PWM Frequency Register	Set the PWM Frequency	R/W	19	0000 0000
A3h	PWM Frequency Adjust Register	Adjust the PWM Frequency	R/W	20	0000 0010
A4h	Pull Down/Up Voltage Selection Register	Set the SO pin pull voltage	R/W	21	0000 1100
A6h	SYNC/INTB Select Register	SYNC or INTB enable	R/W	22	0000 0000
A7h~A8h	Interrupt Mask Register	Configure the interrupt function	R/W	23/24	0000 0000
A9h~AAh	Interrupt State Register	Show the interrupt status	R/W	25/26	0000 0000
ABh~B0h	Pattern State Register	Show the pattern status	R	27	0000 0000
B1h	Open Short Control Register	Open short setting	R/W	28	0001 0000
B2h~B3h	Open register	Store the Open information	R/W	29	0000 0000
B4h~B5h	Short register	Store the Short information	R/W	30	0000 0000
B6h	Boost Control Register	Boost function set	R/W	31	0000 0000
B7h	SO Over Current Register	Over Current enable	R/W	32	0000 0000
BFh	Reset Register	Reset the registers value to default	W	-	0000 0000

Table 3 00h~01h ON OFF Register

Bit	D7	D6:D4	D3	D2:D0
Name	-	EN	-	EN
Default	0	111	0	111

SWS=000	SO1-	SO2-	SO3-	SO4-
SO1+	-	00h_D0	00h_ D1	00h_ D2
SO2+	00h_D4	-	00h_ D5	00h_ D6
SO3+	01h_D0	01h_ D1	-	01h_ D2
SO4+	01h_D4	01h_ D5	01h_ D6	-

SWS=001	SO1-	SO2-	SO3-	SO4-
SO1+	-	00h_D0	00h_ D1	00h_ D2
SO2+	00h_D4	-	00h_ D5	00h_ D6
SO3+	01h_D0	01h_ D1	-	01h_ D2

SWS=010	SO1-	SO2-	SO3-	SO4-
SO1+	-	00h_D0	00h_ D1	00h_ D2
SO2+	00h_D4	-	00h_ D5	00h_ D6

SWS=011	SO1-	SO2-	SO3-	SO4-
SO1+	-	00h_D0	00h_ D1	00h_ D2

SWS=100	SO1-	SO2-	SO3-	SO4-
VOUT	00h_D4	00h_D0	00h_ D1	00h_ D2

SWS=101	SO1-	SO2-	SO3-	SO4-
SO1+	-	00h_D0	00h_ D1	00h_ D2
SO2+	00h_D4	-	00h_ D5	
SO3+	01h_D0	01h_ D1	-	

SWS=110	SO1-	SO2-	SO3-	SO4-
SO1+	-	00h_D0	00h_ D1	00h_ D2
SO2+	00h_D4	-	00h_ D5	

SWS=111	SO1-	SO2-	SO3-	SO4-
SO1+	-	00h_D0	00h_ D1	00h_ D2

Each dot has a bit to enable.

EN LED Enable bit
0 LED off
1 LED on

Table 4 02h~19h PWM Register

Reg	02h (04h, 06h…18h)		03h (05h, 07h…19h)
Bit	D7:D2	D1:D0	D7:D0
Name	-	PWM_H	PWM_L
Default	0000 00	00	0000 0000

SWS=000	SO1 -	SO2-	SO3-	SO4-
SO1 +	-	02h~03h	04h~05h	06h~07h
SO2+	08h~09h	-	0Ah~0Bh	0Ch~0Dh
SO3+	0Eh~0Fh	10h~11h	-	12h~13h
SO4+	14h~15h	16h~17h	18h~19h	-

SWS=001	SO1 -	SO2-	SO3-	SO4-
SO1 +	-	02h~03h	04h~05h	06h~07h
SO2+	08h~09h	-	0Ah~0Bh	0Ch~0Dh
SO3+	0Eh~0Fh	10h~11h	-	12h~13h

SWS=010	SO1 -	SO2-	SO3-	SO4-
SO1 +	-	02h~03h	04h~05h	06h~07h
SO2+	08h~09h	-	0Ah~0Bh	0Ch~0Dh

SWS=011	SO1 -	SO2-	SO3-	SO4-
SO1 +	-	02h~03h	04h~05h	06h~07h

SWS=100	SO1 -	SO2-	SO3-	SO4-
VOUT	08h~09h	02h~03h	04h~05h	06h~07h

SWS=101	SO1 -	SO2-	SO3-	SO4-
SO1 +	-	02h~03h	04h~05h	06h~07h
SO2+	08h~09h	-	0Ah~0Bh	
SO3+	0Eh~0Fh	10h~11h	-	

SWS=110	SO1 -	SO2-	SO3-	SO4-
SO1 +	-	02h~03h	04h~05h	06h~07h
SO2+	08h~09h	-	0Ah~0Bh	

SWS=111	SO1 -	SO2-	SO3-	SO4-
SO1 +	-	02h~03h	04h~05h	06h~07h

Each dot has a byte to modulate the PWM duty in 1024 steps.

PWM_H High bits of PWM Register
PWM_L Low bits of PWM Register

The value of the PWM Registers decides the average current of each LED noted I_{LED}.
I_{LED} computed by Formula (1):

$$I_{LED} = \frac{PWM}{1024} \times I_{OUT(PEAK)} \times Duty \quad (1)$$

$$PWM = \sum_{n=0}^{9} D[n] \cdot 2^n \quad (2)$$

Where Duty is the duty cycle of SOx, see SCANING TIMING section for more information.

$Duty = \frac{10.96\mu s}{(10.96+0.996)\mu s} \times \frac{1}{4} = \frac{1}{4.363}$ (2, SWS=1/4)

$Duty = \frac{10.96\mu s}{(10.96+0.996)\mu s} \times \frac{1}{3} = \frac{1}{3.272}$ (2, SWS=1/3)

$Duty = \frac{10.96\mu s}{(10.96+0.996)\mu s} \times \frac{1}{2} = \frac{1}{2.818}$ (2, SWS=1/2)

$Duty = \frac{10.96\mu s}{(10.96+0.996)\mu s} \times \frac{1}{1} = \frac{1}{1.09}$ (2, SWS=1/1)

…

I_{OUT} is the output current of SOx (x=1~4),

$$I_{OUT(PEAK)} = 50.7mA \times \frac{63}{63} \times \frac{255}{255} \quad (3)$$

GCC is the Global Current Control register (A1h, 0/63~63/63) value, SL is the Scaling Register value as Table 5. D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if PWM register D9:D0= “00 1011 0101” (0x0B5, 181), SWS= 1/4, GCC= “00111111”, SL= “11111111”:

$$I_{LED} = 50.7mA \times \frac{63}{63} \times \frac{255}{255} \times \frac{1}{4.363} \times \frac{181}{1024}$$

Table 5 1Ah~25h Scaling Register

Bit	D7:D0
Name	SL
Default	0000 0000

SWS=000	SO1-	SO2-	SO3-	SO4-
SO1+	-	1Ah	1Bh	1Ch
SO2+	1Dh	-	1Eh	1Fh
SO3+	20h	21h	-	22h
SO4+	23h	24h	25h	-

SWS=001	SO1-	SO2-	SO3-	SO4-
SO1+	-	1Ah	1Bh	1Ch
SO2+	1Dh	-	1Eh	1Fh
SO3+	20h	21h	-	22h

SWS=010	SO1-	SO2-	SO3-	SO4-
SO1+	-	1Ah	1Bh	1Ch
SO2+	1Dh	-	1Eh	1Fh

SWS=011	SO1-	SO2-	SO3-	SO4-
SO1+	-	1Ah	1Bh	1Ch

SWS=100	SO1-	SO2-	SO3-	SO4-
VOUT	1Dh	1Ah	1Bh	1Ch

SWS=101	SO1-	SO2-	SO3-	SO4-
SO1+	-	1Ah	1Bh	1Ch
SO2+	1Dh	-	1Eh	
SO3+	20h	21h	-	

SWS=110	SO1-	SO2-	SO3-	SO4-
SO1+	-	1Ah	1Bh	1Ch
SO2+	1Dh	-	1Eh	

SWS=111	SO1-	SO2-	SO3-	SO4-
SO1+	-	1Ah	1Bh	1Ch

Scaling Register (SLx) control the DC output current of each dot. Each dot has a byte to modulate the scaling in 256 steps.

SLx

0000 0000 SL=0, 0/255 DC current
0000 0001 SL=1, 1/255 DC current
0000 0010 SL=2, 2/255 DC current
….

1111 1111 SL=255, 255/255 DC current

The value of the Scaling Register decides the peak current of each LED noted $I_{OUT(PEAK)}$.

$I_{OUT(PEAK)}$ computed by Formula (3):

$$I_{OUT(PEAK)} = 50.7mA \times \frac{GCC}{63} \times \frac{SL}{255} \quad (3)$$

I_{OUT} is the output current of SOx (x=1~4), GCC is the Global Current Control Register (A1h) value.

For example: if GCC= “10 0000”, SL= “1111 1111”:

$$I_{OUT(PEAK)} = 50.7mA \times \frac{32}{63} \times \frac{255}{255}$$

Table 6 Register Map of PWM Mode

Mode	Register	SO1+			SO2+			SO3+			SO4+		
		SO2-	SO3-	SO4-	SO1-	SO3-	SO4-	SO1-	SO2-	SO4-	SO1-	SO2-	SO3-
PWM	PWM_H	02h	04h	06h	08h	0Ah	0Ch	0Eh	10h	12h	14h	16h	18h
	PWM_L	03h	05h	07h	09h	0Bh	0Dh	0Fh	11h	13h	15h	17h	19h
	SL	1Ah	1Bh	1Ch	1Dh	1Eh	1Fh	20h	21h	22h	23h	24h	25h

Table 7 26h~27h Pattern Mode Enable Register

Bit	D7	D6:D4	D3	D2:D0
Name	-	PME	-	PME
Default	0	000	0	000

SWS=000	SO1-	SO2-	SO3-	SO4-
SO1+	-	26h_D0	26h_ D1	26h_ D2
SO2+	26h_D4	-	26h_ D5	26h_ D6
SO3+	27h_D0	27h_ D1	-	27h_ D2
SO4+	27h_D4	27h_ D5	27h_ D6	-

SWS=001	SO1-	SO2-	SO3-	SO4-
SO1+	-	26h_D0	26h_ D1	26h_ D2
SO2+	26h_D4	-	26h_ D5	26h_ D6
SO3+	27h_D0	27h_ D1	-	27h_ D2

SWS=010	SO1-	SO2-	SO3-	SO4-
SO1+	-	26h_D0	26h_ D1	26h_ D2
SO2+	26h_D4	-	26h_ D5	26h_ D6

SWS=011	SO1-	SO2-	SO3-	SO4-
SO1+	-	26h_D0	26h_ D1	26h_ D2

SWS=100	SO1-	SO2-	SO3-	SO4-
VOUT	26h_D4	26h_D0	26h_ D1	26h_ D2

SWS=101	SO1-	SO2-	SO3-	SO4-
SO1+	-	26h_D0	26h_ D1	26h_ D2
SO2+	26h_D4	-	26h_ D5	
SO3+	27h_D0	27h_ D1	-	

SWS=110	SO1-	SO2-	SO3-	SO4-
SO1+	-	26h_D0	26h_ D1	26h_ D2
SO2+	26h_D4	-	26h_ D5	

SWS=111	SO1-	SO2-	SO3-	SO4-
SO1+	-	26h_D0	26h_ D1	26h_ D2

The Pattern Mode Enable Register sets operating mode of each dot. When PME is set to “1”, the LED will work at pattern mode.

PME Pattern Mode Enable bit
0 PWM mode or Current Level mode
1 Pattern Mode

Table 8 28h~2Ch/31h~35h/3Ah~3Eh/43h~47h/4Ch~50h/55h~59h/5Eh~62h/67h~6Bh/ 70h~74h/79h~7Dh/82h~86h/8Bh~8Fh Pattern PWM Register

GAM = 0, Linearity PWM 8-bit

Bit	D7:D0
Name	P_PWM1/ P_PWM2/ P_PWM3/ P_PWM4/ P_PWM5
Default	0000 0000

GAM = 1, Gamma PWM 7-bit.

Bit	D7	D6:D0
Name	-	P_PWM1/ P_PWM2/ P_PWM3/ P_PWM4/ P_PWM5
Default	0	000 0000

The IS31FL3713 provides gamma correction which can be set by GAM bit of the Configuration Register (A0h) for all patterns. When GAM bit set as 1, the gamma correction is enabled, and the 7 bits of Pattern PWM Registers (D6:D0) is for setting the PWM duty. When GAM bit set as 0, the PWM duty changes linearly, and the 8 bits of Pattern PWM Registers (D7:D0) is for setting the PWM duty.

P_PWM1/ P_PWM2/ P_PWM3/ P_PWM4/ P_PWM5 Pattern PWM duty bits

When IS31FL3713 operates in Pattern Mode, each dot can independently maintain a pre-established pattern achieving color breathing, 12 pattern settings (P1~P12) for 12 dots.

SWS=000	SO1-	SO2-	SO3-	SO4-
SO1+	-	P1	P2	P3
SO2+	P4	-	P5	P6
SO3+	P7	P8	-	P9
SO4+	P10	P11	P12	-

SWS=001	SO1-	SO2-	SO3-	SO4-
SO1+	-	P1	P2	P3
SO2+	P4	-	P5	P6
SO3+	P7	P8	-	P9

SWS=010	SO1-	SO2-	SO3-	SO4-
SO1+	-	P1	P2	P3
SO2+	P4	-	P5	P6

SWS=011	SO1-	SO2-	SO3-	SO4-
SO1+	-	P1	P2	P3

SWS=100	SO1-	SO2-	SO3-	SO4-
VOUT	P4	P1	P2	P3

SWS=101	SO1-	SO2-	SO3-	SO4-
SO1+	-	P1	P2	P3
SO2+	P4	-	P5	
SO3+	P7	P8	-	

SWS=110	SO1-	SO2-	SO3-	SO4-
SO1+	-	P1	P2	P3
SO2+	P4	-	P5	

SWS=111	SO1-	SO2-	SO3-	SO4-
SO1+	-	P1	P2	P3

The five Pattern PWM registers (P_PWM1 to P_PWM5) are configured as part of a single pattern setting, defining the dots PWM duty cycle at five time points within the pattern loop. As show in Figure 9, the PWM duty cycle transitions from one P_PWM to the next P_PWM within a period (TS, T1, T2, T3, T4, TP), with a transition step size of 256 when GAM=0 (Linear PWM) or 128/64/32 when GAM=1 (Gamma PWM).

Table 9 2Dh/36h/3Fh/48h/51h/5Ah/63h/6Ch/75h/7Eh/87h/90h Pattern TS &T1 Setting Register

Bit	D7:D3	D4:D0
Name	T1	TS
Default	0000	0000

The TS & T1 Setting Registers set the TS and T1 time in Pattern Mode.

T1	P_PWM1 Crossfade to P_PWM2 Time Selection	
0000	0ms	0x
0001	95.6ms	1x
0010	191.2ms	2x
0011	286.8ms	3x
0100	382.4ms	4x
0101	478ms	5x
0110	573.6ms	6x
0111	669.2ms	7x
1000	764.8ms	8x
1001	860.4ms	9x
1010	956ms	10x
1011	1051.6ms	11x
1100	1529.6ms	16x
1101	2103.2ms	22x
1110	3154.8ms	33x
1111	4206.4ms	44x

TS	P_PWM1 Start Hold Time Selection	
0000	0ms	0x
0001	95.6ms	1x
0010	191.2ms	2x
0011	286.8ms	3x
0100	382.4ms	4x
0101	478ms	5x
0110	573.6ms	6x
0111	669.2ms	7x
1000	764.8ms	8x
1001	860.4ms	9x
1010	956ms	10x
1011	1051.6ms	11x
1100	1529.6ms	16x
1101	2103.2ms	22x
1110	3154.8ms	33x
1111	4206.4ms	44x

Table 10 2Eh/37h/40h/49h/52h/5Bh/64h/6Dh/76h/7Fh/88h/91h Pattern T2 &T3 Setting Register

Bit	D7:D3	D4:D0
Name	T3	T2
Default	0000	0000

The T2 & T3 Setting Registers set the T2 and T3 time in Pattern Mode.

T3	P_PWM3 Crossfade to P_PWM4 Time Selection	
0000	0ms	0x
0001	95.6ms	1x
0010	191.2ms	2x
0011	286.8ms	3x
0100	382.4ms	4x
0101	478ms	5x
0110	573.6ms	6x
0111	669.2ms	7x
1000	764.8ms	8x
1001	860.4ms	9x
1010	956ms	10x
1011	1051.6ms	11x
1100	1529.6ms	16x
1101	2103.2ms	22x
1110	3154.8ms	33x
1111	4206.4ms	44x

T2	P_PWM2 Crossfade to P_PWM3 Time Selection	
0000	0ms	0x
0001	95.6ms	1x
0010	191.2ms	2x
0011	286.8ms	3x
0100	382.4ms	4x
0101	478ms	5x
0110	573.6ms	6x
0111	669.2ms	7x
1000	764.8ms	8x
1001	860.4ms	9x
1010	956ms	10x
1011	1051.6ms	11x
1100	1529.6ms	16x
1101	2103.2ms	22x
1110	3154.8ms	33x
1111	4206.4ms	44x

Table 11 2Fh/38h/41h/4Ah/53h/5Ch/65h/6Eh/77h/80h/89h/92h Pattern T4 &TP Setting Register

Bit	D7:D4	D3:D0
Name	TP	T4
Default	0000	0000

The T4 Setting Registers set the T4 time in Pattern Mode.

TP	P_PWM5 Crossfade to 0x00 Time Selection	
0000	0ms	0x
0001	95.6ms	1x
0010	191.2ms	2x
0011	286.8ms	3x
0100	382.4ms	4x
0101	478ms	5x
0110	573.6ms	6x
0111	669.2ms	7x
1000	764.8ms	8x
1001	860.4ms	9x
1010	956ms	10x
1011	1051.6ms	11x
1100	1529.6ms	16x
1101	2103.2ms	22x
1110	3154.8ms	33x
1111	4206.4ms	44x

T4	P_PWM4 Crossfade to P_PWM5 Time Selection	
0000	0ms	0x
0001	95.6ms	1x
0010	191.2ms	2x
0011	286.8ms	3x
0100	382.4ms	4x
0101	478ms	5x
0110	573.6ms	6x
0111	669.2ms	7x
1000	764.8ms	8x
1001	860.4ms	9x
1010	956ms	10x
1011	1051.6ms	11x
1100	1529.6ms	16x
1101	2103.2ms	22x
1110	3154.8ms	33x
1111	4206.4ms	44x

Table 12 30h/39h/42h/4Bh/54h/5Dh/66h/6Fh/78h/81h/8Ah/93h Pattern Loop Times Register

Bit	D7	D6:D0
Name	PLTx_H	PLTx_L
Default	0	000 0000

If PLT_H(D7)=0, PLT_L!=0

Pattern loop times:

$$Looptime = \sum_{n=0}^{6} D[n] \times 2^n \quad (4)$$

If PLT_H(D7)=0, PLT_L=0, endless

If PLT_H(D7)=1, PLT_L!=0

Pattern loop times:

$$Looptime = 16 \times \sum_{n=0}^{6} D[n] \times 2^n \quad (5)$$

If PLT_H(D7)=1, PLT_L=0, endless

Table 13 94h~99h Pattern Control Register

Bit	D7:D5	D4	D3:D1	D0
Name	PxHold (P2/P4/P6/P8/P10/P12)	PxS (P2/P4/P6/P8/P10/P12)	PxHold (P1/P3/P5/P7/P9/P11)	PxS (P1/P3/P5/P7/P9/P11)
Default	000	0	000	0

The Pattern loop can hold at 5 time points, with the PWM duty remaining as P_PWMx. PxS controls the start and stop of the Pattern loop. When the PxS bit is set to "1", the Pattern loop runs from the start of TS. When the PxS bit is set to "0", the Pattern loop stops running and proceeds to the end of TP. Writing to the PxHold bits selects the specific time point within the Pattern loop at which to hold; in this state, the PWM duty remains as P_PWMx.

PxS	Pattern Start Enable
0	Stop
1	Start

PxHold	Pattern Hold Enable
000	No Hold
001	Hold at End of TS, P_PWM1
010	Hold at End of T1, P_PWM2
011	Hold at End of T2, P_PWM3
100	Hold at End of T3, P_PWM4
101	Hold at End of T4, P_PWM5
Others	No Hold

9Ah All Pattern Start/Stop Register

A write operation of 0x55 to the start all patterns. Then PxS (94h~99h) will be changed to 1. Then automatically reset to 0x00.

A write operation of 0xA5 to the stop all patterns. Then PxS (94h~99h) will be changed to 0. Then automatically reset to 0x00.

Table 14 Register Map of Pattern Mode

Pattern x	P_PWM 1	P_PWM 2	P_PWM 3	P_PWM 4	P_PWM 5	TS &T1	T2 &T3	T4 &TP	Loop Times	12 pattern Control	All Control
P1	28h	29h	2Ah	2Bh	2Ch	2Dh	2Eh	2Fh	30h	94h	9Ah
P2	31h	32h	33h	34h	35h	36h	37h	38h	39h		
P3	3Ah	3Bh	3Ch	3Dh	3Eh	3Fh	40h	41h	42h	95h	
P4	43h	44h	45h	46h	47h	48h	49h	4Ah	4Bh		
P5	4Ch	4Dh	4Eh	4Fh	50h	51h	52h	53h	54h	96h	
P6	55h	56h	57h	58h	59h	5Ah	5Bh	5Ch	5Dh		
P7	5Eh	5Fh	60h	61h	62h	63h	64h	65h	66h	97h	
P8	67h	68h	69h	6Ah	6Bh	6Ch	6Dh	6Eh	6Fh		
P9	70h	71h	72h	73h	74h	75h	76h	77h	78h	98h	
P10	79h	7Ah	7Bh	7Ch	7Dh	7Eh	7Fh	80h	81h		
P11	82h	83h	84h	85h	86h	87h	88h	89h	8Ah	99h	
P12	8Bh	8Ch	8Dh	8Eh	8Fh	90h	91h	92h	93h		

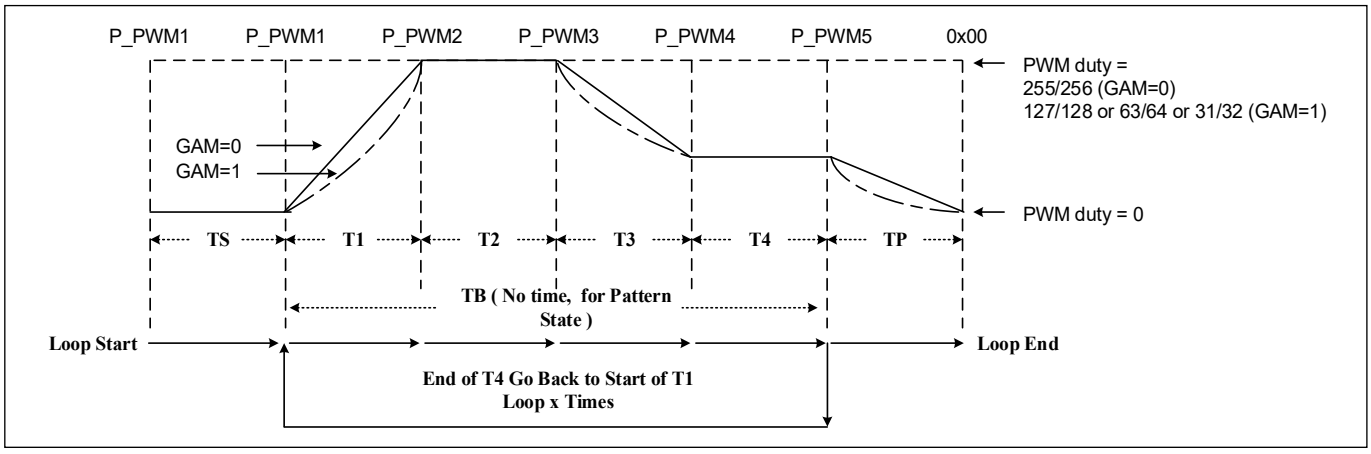


Figure 9 Pattern Loop Timing

Table 15 9Bh Current Level Mode Register

Bit	D7:D4	D3	D2	D1	D0
Name	-	DCSO4	DCSO3	DCSO2	DCSO1
Default	0000	0	0	0	0

The DCSOx (x=1~4) bits set output operation modes of IS31FL3713.

DCSOx	Current Level Mode Setting
0	PWM mode
1	Current Level Mode

The Current Level Mode configures the SOx pins as current sources, whose output levels are controlled by the Current Level Registers (1Ah~25h). The specific pins enabled depend on the SWS bits (A0h), when SWS=100, SO1, SO2, SO3, SO4 are enabled, when SWS=101, 110, 111, only SO4 is enabled.

SWS=100	**SO1-**	**SO2-**	**SO3-**	**SO4-**
VOUT	9Bh_D0	9Bh_D1	9Bh_ D2	9Bh_ D3

SWS=101	**SO1-**	**SO2-**	**SO3-**	**SO4-**
SO1+	-	-	-	9Bh_ D3
SO2+	-	-	-	
SO3+	-	-	-	

SWS=110	**SO1-**	**SO2-**	**SO3-**	**SO4-**
SO1+	-	-	-	9Bh_ D3
SO2+	-	-	-	

SWS=111	**SO1-**	**SO2-**	**SO3-**	**SO4-**
SO1+	-	-	-	9Bh_ D3

9Ch PWM Update Register

The data sent to the PWM Registers will be stored in temporary registers. A write operation of 0xD5 to the Update Register is required to update 02h~19h PWM registers. A write operation of 0x26 to Update Register is required to update A0h~B1h registers. Then it automatically reset to 0x00.

Table 16 A0h Configuration Register

Bit	D7	D6:D4	D3	D2	D1	D0
Name	-	SWS	-	GAM	-	SSD
Default	0	000	0	1	0	0

The Configuration Register sets operating mode of IS31FL3713. SWS bits control the duty cycle of the SOx, default mode is “000”, 1/4 Scan. GAM controls the gamma of pattern. When SSD is “0”, IS31FL3713 works in software shutdown mode and to normal operate the SSD bit should set to “1”.

GAM	Gamma Selection (in Pattern mode)
0	Linearity PWM (256 step)
1	Gamma PWM (128/64/32 step)

SWS	Scan Setting
000	4x3, 1/4 Scan
001	3x3, 1/3 Scan
010	2x3, 1/2 Scan
011	1x3, 1/1 Scan
100	SO1~SO4 are sink, No Scan
101	3x2, 1/3, SO4 is sink.
110	2x2, 1/2, SO4 is sink.
111	1x2, 1/1, SO4 is sink.

SSD	Software Shutdown Control
0	Software shutdown
1	Normal operation

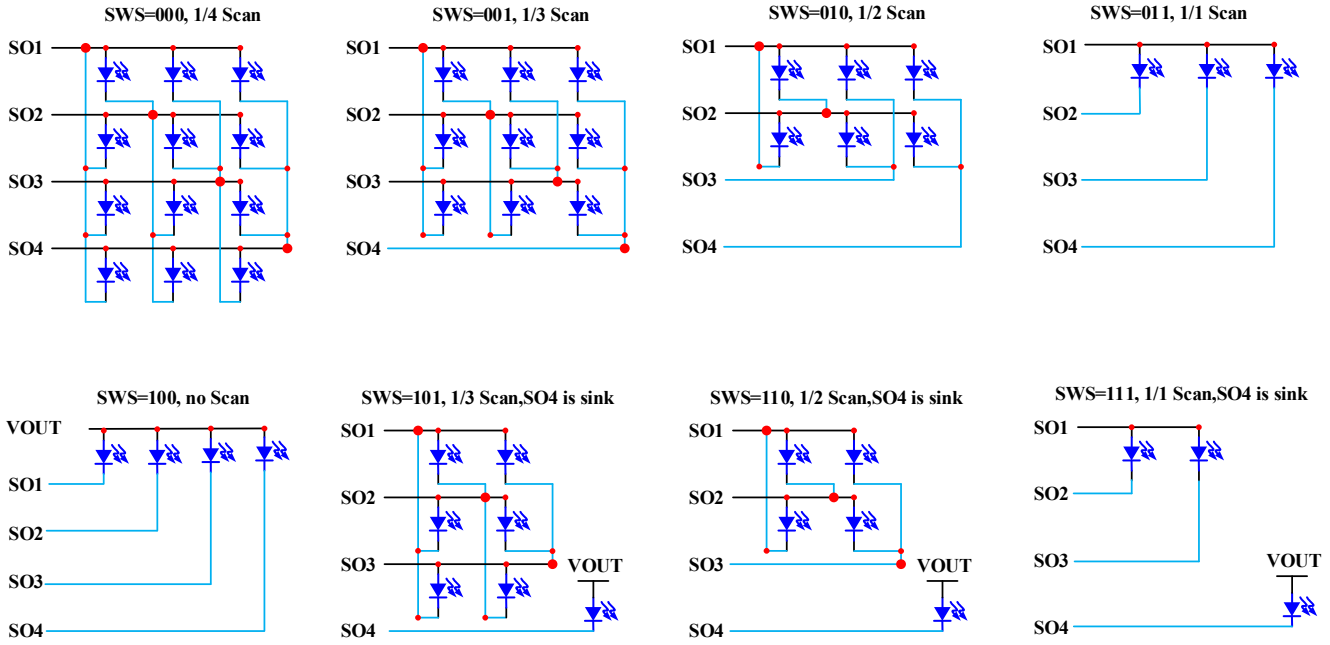


Table 17 Dot and SOx Map

SWS=000	SO1-	SO2-	SO3-	SO4-
SO1+	-	Dot1	Dot2	Dot3
SO2+	Dot4	-	Dot5	Dot6
SO3+	Dot7	Dot8	-	Dot9
SO4+	Dot10	Dot11	Dot12	-

SWS=001	SO1-	SO2-	SO3-	SO4-
SO1+	-	Dot1	Dot2	Dot3
SO2+	Dot4	-	Dot5	Dot6
SO3+	Dot7	Dot8	-	Dot9

SWS=010	SO1-	SO2-	SO3-	SO4-
SO1+	-	Dot1	Dot2	Dot3
SO2+	Dot4	-	Dot5	Dot6

SWS=011	SO1-	SO2-	SO3-	SO4-
SO1+	-	Dot1	Dot2	Dot3

SWS=100	SO1-	SO2-	SO3-	SO4-
VOUT	SO1	SO2	SO3	SO4

SWS=101	SO1-	SO2-	SO3-	SO4-
SO1+	-	Dot1	Dot2	SO4
SO2+	Dot4	-	Dot5	
SO3+	Dot7	Dot8	-	

SWS=110	SO1-	SO2-	SO3-	SO4-
SO1+	-	Dot1	Dot2	SO4
SO2+	Dot4	-	Dot5	

SWS=111	SO1-	SO2-	SO3-	SO4-
SO1+	-	Dot1	Dot2	SO4

Table 18 A1h Global Current Control Register

Bit	D7:D6	D5:D0
Name	-	GCC
Default	00	000000

The Global Current Control Register modulates all dots DC current which is noted as $I_{OUT(PEAK)}$ in 64 steps.

GCC Global current control
00 GCC=0/63
….
111111 GCC=63/63

I_{OUT} is computed by as shown in Formula (3).
If GCC=0x3F, SL=0xFF, $I_{OUT}=I_{OUT(MAX)}$

$$I_{OUT} = 50.7mA \times \frac{GCC}{63} \times \frac{SL}{255} \quad (3)$$

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (6)$$

Table 19 A2h PWM Frequency Register

Bit	D7:D4	D3:D0
Name	-	PFS
Default	0000	0000

The Configuration Register sets the PWM frequency of IS31FL3713, PWM resolution function.
The PFS bits selects a fixed oscillator frequency.

PFS PWM frequency
0000 6+4-bit: PWM frequency 83.64kHz, scan frequency 20.91kHz, TS~TP 1x =95.6ms, 128 steps
0001 6+4-bit: PWM frequency 43.64kHz, scan frequency 10.91kHz, TS~TP 1x =191.2ms, 128 steps

0010 6+4-bit: PWM frequency 22.3kHz, scan frequency 5.58kHz, TS~TP 1x =382.4ms, 128 steps
0011 6+4-bit: PWM frequency 11.28kHz, scan frequency 2.82kHz, TS~TP 1x =764.8ms, 128 steps
0100 6+4-bit: PWM frequency 5.67kHz, scan frequency 1.42kHz, TS~TP 1x =1.5296s, 128 steps
0101 6+4-bit: PWM frequency 2.84kHz, scan frequency 710.8Hz, TS~TP 1x =3.0596s, 128 steps
0110 6+4-bit: PWM frequency 1.42kHz, scan frequency 355.9Hz, TS~TP 1x =6.1184s, 128 steps
0111 6+4-bit: PWM frequency 712.13Hz, scan frequency 178.08Hz, TS~TP 1x =12.2368s, 128 steps
1000 6+4-bit: PWM frequency 43.64kHz, scan frequency 10.91kHz, TS~TP 1x =95.6ms, 64 steps
1001 6+4-bit: PWM frequency 22.3kHz, scan frequency 5.58kHz, TS~TP 1x =95.6ms, 32 steps
1010 6+4-bit: PWM frequency 22.3kHz, scan frequency 5.58kHz, TS~TP 1x =191.2ms, 64 steps

Table 20 A3h PWM Frequency Adjust Register

Bit	D7:D3	D2:D0
Name	-	PFA
Default	00000	010

The PFA bits adjust the PWM Frequency, for example, if PFA is “010”, the PWM frequency is 83.64kHz, if PFA is “000”, the PWM frequency is 97.94244kHz (+17.1%).

PFA	**PWM Frequency Adjust**
000	17.1%
001	9%
010	0%
011	-9.2%
100	-18.8%
101	-29.3%
110	-41.2%
111	-53.5%

Table 21 A4h Pull Down/Up Voltage Selection Register

Bit	D7	D6:D5	D4	D3:D1	D0
Name	-	PTS	PP	PV	PEN
Default	0	00	0	110	0

Pull Down/Up Voltage Selection Register. Set pull down/up voltage for SOx.
Please check DE-GHOST FUNCTION section for more information.

PTS	Pull time setting
00	1μs
01	1.33μs
10	1.66μs
11	2μs

PEN	Pull EN
0	Disable
1	Enable

PP	Pull period
0	only in de-ghost time
1	PWM off time

PV	Pull voltage
000	Pull to V_{OUT}-0.8V
001	Pull to V_{OUT} -1.0V
010	Pull to V_{OUT} -1.2V
011	Pull to V_{OUT} -1.4V
100	Pull to V_{OUT} -1.6V
101	Pull to V_{OUT} -2.0V
110	Pull to V_{OUT} -2.4V(default)
111	Pull to V_{OUT} -2.8V

Table 22 A6h SYNC/INTB Select Register

Bit	D7:D5	D4	D3	D2	D1:D0
Name	-	SIS	-	-	SYNC
Default	000	0	0	0	00

The SIS bit select the SYNC/INTB pin function. The SYNC bits select the SYNC mode. When SIS is set as “1”, the Interrupt Mask function enabled. When SIS is set as “0” and SYNC is set to “11”, the SYNC/INTB pin will have a clock output to support cascade connection between 2 IS31FL3713.

SIS	SYNC/INTB Function Select
0	SYNC function
1	INTB function

SYNC	SYNC Function Set
0x	Disable SYNC function, 30kOhm pull-low
10	Enable SYNC Slave, clock input
11	Enable SYNC Master, clock output

Table 23 A7h Interrupt Mask Register 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SOCE	TSE	SIE	OIE	PIE4	PIE3	PIE2	PIE1
Default	0	0	0	0	0	0	0	0

Configure the Interrupt Mask Register to generate an interrupt signal to the MCU by pulling the SYNC/INTB pin low when a specific event occurs. Set SIS bit as “1” in A6h to enable the Interrupt Mask function. SOCE bit for the overcurrent occurs on SOx, TSE bit for the thermal shutdown, SIE bit for the LED short, OIE bit for the LED open, PIEx bit for the pattern loop finished.

Note 8: The PIEx bit only takes effect in pattern mode. When using PWM mode, the PIE bit must remain 0.

Note 9: The SYNC/INTB pin needs to be connected to a pull-up resistor to VCC when the INTB function is enabled.

SOCE	SOx overcurrent Interrupt report Enable
0	Disable
1	Enable SOx overcurrent report to INTB pin

TSE	Thermal Shutdown Interrupt report Enable
0	Disable
1	Enable thermal shutdown report to INTB pin

SIE	Short Interrupt report Enable
0	Disable
1	Enable short report to INTB pin

OIE Open Interrupt report Enable
0 Disable
1 Enable open report to INTB pin

PIE1 Pattern1 Interrupt report Enable
0 Disable
1 Enable Pattern1 loop finish report to INTB pin

PIE2 Pattern2 Interrupt report Enable
0 Disable
1 Enable Pattern2 loop finish report to INTB pin

PIE3 Pattern3 Interrupt report Enable
0 Disable
1 Enable Pattern3 loop finish report to INTB pin

PIE4 Pattern4 Interrupt report Enable
0 Disable
1 Enable Pattern4 loop finish report to INTB pin

Table 24 A8h Interrupt Mask Register 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PIE12	PIE11	PIE10	PIE9	PIE8	PIE7	PIE6	PIE5
Default	0	0	0	0	0	0	0	0

Note 8: The PIE bit only takes effect in pattern mode. When using PWM mode, the PIE bit must remain 0.
Note 9: The SYNC/INTB pin needs to be connected to a pull-up resistor to VCC when the INTB function is enabled.

PIEx Patternx Interrupt report Enable
0 Disable
1 Enable Patternx loop finish report to INTB pin.

Table 25 A9h Interrupt State Register 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SOCF	TSF	SIF	OIF	PIF4	PIF3	PIF2	PIF1
Default	0	0	0	0	0	0	0	0

When the specific events occur, the corresponding status flag bit is set to 1. The MCU can poll the Interrupt State Register to retrieve the current status of the IS31FL3713. This register can only be written to '0' to clear flags, writing '1' is invalid.

SOCF SOx overcurrent Interrupt Flag
0 No happens
1 SOx overcurrent happens

TSF Thermal Shutdown Interrupt Flag
0 No happens
1 Thermal shutdown happens

SIF Short Interrupt Flag
0 No short
1 Short happens

OIF Open Interrupt Flag
0 No open
1 Open happens

PIF1 Pattern1 Interrupt Flag
0 Pattern1 loop not finish
1 Pattern1 loop finished

PIF2 Pattern2 Interrupt Flag
0 Pattern2 loop not finish
1 Pattern2 loop finished

PIF3 Pattern3 Interrupt Flag
0 Pattern3 loop not finish
1 Pattern3 loop finished

PIF4 Pattern4 Interrupt Flag
0 Pattern4 loop not finish
1 Pattern4 loop finished

Table 26 AAh Interrupt State Register 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PIF12	PIF11	PIF10	PIF9	PIF8	PIF7	PIF6	PIF5
Default	0	0	0	0	0	0	0	0

This register can only be written to '0' to clear flags, writing '1' is invalid.

PIFx Patternx Interrupt Flag
0 Patternx loop not finish
1 Patternx loop finished

Table 27 ABh~B0h Pattern State Register

Bit	D7	D6:D4	D3	D2:D0
Name	-	PxS (P2/P4/P6/P8/P10/P12)	-	PxS(P1/P3/P5/P7/P9/P11)
Default	0	000	0	000

The Pattern State Register stores the pattern loop timing status. ABh register is used for pattern 1/2, ACh for pattern 3/4, ADh for pattern 5/6, AEh for pattern 7/8, AFh for pattern 9/10, similarly B0h for pattern 11/12. Pattern State is only valid when the Pattern State Tx setting is not 0000. When the Pattern Loop enters the "0000" Tx timing period, the value read from Pattern State is invalid.

PxS Pattern State
000 TS
001 T1
010 T2
011 T3
100 T4
101 TP
110 TB
Others Error

Table 28 B1 Open Short Control Register

Bit	D7	D6	D5:D4	D3:D2	D1	D0
Name	-	OFAF	STH	-	SDE	ODE
Default	0	0	01	00	0	0

Set OFAF bit as "1" to enable the One Fail All Fail function when LED short happened, all LEDs will be shut down when any LED short. Set the STH bits to select the Short threshold voltage on SOx. When SDE is set to "1", short detection will be enabled, and the short information will be stored at B3h~B4h. When ODE is set to "1", open detection will be enabled, and the open information will be stored at B2h~B3h.

Note 10: When OFAF bit set as "1", 9Ch PWM Update Register need to write 0x26, that One Fail All Fail function will be enabled.

OFAF One Fail All Fail (When short happen)
0 Disable
1 Enable

STH Short threshold
00 V_{OUT} - 0.5V
01 V_{OUT} - 1V (default)
10/11 V_{OUT} - 1.5V

ODE Open Detection Enable
0 Disable open detection
1 Enable open detection

SDE Short Detection Enable
0 Disable short detection
1 Enable short detection

Table 29 B2h~B3h Open Register

Bit	D7	D6:D4	D3	D2:D0
Name	-	OPEN	-	OPEN
Default	0	000	0	000

SWS=000	SO1-	SO2-	SO3-	SO4-
SO1+	-	B2h_D0	B2h_ D1	B2h_ D2
SO2+	B2h_D4	-	B2h_ D5	B2h_ D6
SO3+	B3h_D0	B3h_ D1	-	B3h_ D2
SO4+	B3h_D4	B3h_ D5	B3h_ D6	-

SWS=001	SO1-	SO2-	SO3-	SO4-
SO1+	-	B2h_D0	B2h_ D1	B2h_ D2
SO2+	B2h_D4	-	B2h_ D5	B2h_ D6
SO3+	B3h_D0	B3h_ D1	-	B3h_ D2

SWS=010	SO1-	SO2-	SO3-	SO4-
SO1+	-	B2h_D0	B2h_ D1	B2h_ D2
SO2+	B2h_D4	-	B2h_ D5	B2h_ D6

SWS=011	SO1-	SO2-	SO3-	SO4-
SO1+	-	B2h_D0	B2h_ D1	B2h_ D2

SWS=100	SO1-	SO2-	SO3-	SO4-
VOUT	B2h_D4	B2h_D0	B2h_ D1	B2h_ D2

SWS=101	SO1-	SO2-	SO3-	SO4-
SO1+	-	B2h_D0	B2h_ D1	B2h_ D2
SO2+	B2h_D4	-	B2h_ D5	
SO3+	B3h_D0	B3h_ D1	-	

SWS=110	SO1-	SO2-	SO3-	SO4-
SO1+	-	B2h_D0	B2h_ D1	B2h_ D2
SO2+	B2h_D4	-	B2h_ D5	

SWS=111	SO1-	SO2-	SO3-	SO4-
SO1+	-	B2h_D0	B2h_ D1	B2h_ D2

OPEN detect function, can be enabled by configuration register(B1h),
When ODE is set to “1”, open detection will be enabled, and the open information will be stored at B2h~B3h.
Open LED will be shut down when LED open. Then write ‘0’ to clear open bit, it will be redetected.
When ODE is set to “0”, open detection will be disable, and the open information will be clean to ‘0’ at B2h~B3h.

OPEN Open Fault Flag
0 LED normal
1 LED open

Table 30 B4h~B5h Short Register

Bit	D7	D6:D4	D3	D2:D0
Name	-	SHORT	-	SHORT
Default	0	000	0	000

SWS=000	SO1-	SO2-	SO3-	SO4-
SO1+	-	B4h_D0	B4h_ D1	B4h_ D2
SO2+	B4h_D4	-	B4h_ D5	B4h_ D6
SO3+	B5h_D0	B5h_ D1	-	B5h_ D2
SO4+	B5h_D4	B5h_ D5	B5h_ D6	-

SWS=001	SO1-	SO2-	SO3-	SO4-
SO1+	-	B4h_D0	B4h_ D1	B4h_ D2
SO2+	B4h_D4	-	B4h_ D5	B4h_ D6
SO3+	B5h_D0	B5h_ D1	-	B5h_ D2

SWS=010	SO1-	SO2-	SO3-	SO4-
SO1+	-	B4h_D0	B4h_ D1	B4h_ D2
SO2+	B4h_D4	-	B4h_ D5	B4h_ D6

SWS=011	SO1-	SO2-	SO3-	SO4-
SO1+	-	B4h_D0	B4h_ D1	B4h_ D2
SWS=100	SO1-	SO2-	SO3-	SO4-
VOUT	B4h_D4	B4h_D0	B4h_ D1	B4h_ D2

SWS=101	SO1-	SO2-	SO3-	SO4-
SO1+	-	B4h_D0	B4h_ D1	B4h_ D2
SO2+	B4h_D4	-	B4h_ D5	
SO3+	B5h_D0	B5h_ D1	-	

SWS=110	SO1-	SO2-	SO3-	SO4-
SO1+	-	B4h_D0	B4h_ D1	B4h_ D2
SO2+	B4h_D4	-	B4h_ D5	
SWS=111	SO1-	SO2-	SO3-	SO4-
SO1+	-	B4h_D0	B4h_ D1	B4h_ D2

SHORT detect function, can be enabled by configuration register(B0h),
When SDE is set to “1”, short detection will be enabled, and the short information will be stored at B3h~B4h.
If ‘OFAF’ = 1, all LEDs will be shut down when any LED short. Then write ‘0’ to clear short bit, it will be redetected.
When SDE is set to “0”, short detection will be disable, and the short information will be clean to ‘0’ at B3h~B4h.

SHORT Short Fault Flag
0 LED normal
1 LED short

Table 31 B6h Boost Control Register

Bit	D7:D5	D4:D0
Name	-	VSO
Default	000	00000

The VSO bits control the boost voltage. The boost voltage can change from 3.0V to 5.0V in 20 steps, one step adds 100mV. The boost voltage will not return to the default value after writing 0xAE to the Reset Register BFh; it can only be restored to the default by setting VSO bits as 00000.

VSO boost voltage select
00000 3.0V
00001 3.1V
00010 3.2V
…..
10100 5.0V
Others 5V

Table 32 B7h SO Over Current Register

Bit	D7	D6:D0
Name	SOOC	-
Default	0	0000000

When SOOC bit is 1, SOx over current protection is enable.

SOOC SOx over current protection
0 Disable
1 Enable

BFh Reset Register

Once user writes the Reset Register with 0xAE (Other values are invalid), IS31FL3713 will reset all the IS31FL3713 registers to their default value. On initial power-up, the IS31FL3713 registers are reset to their default values for a blank display.

APPLICATION INFORMATION

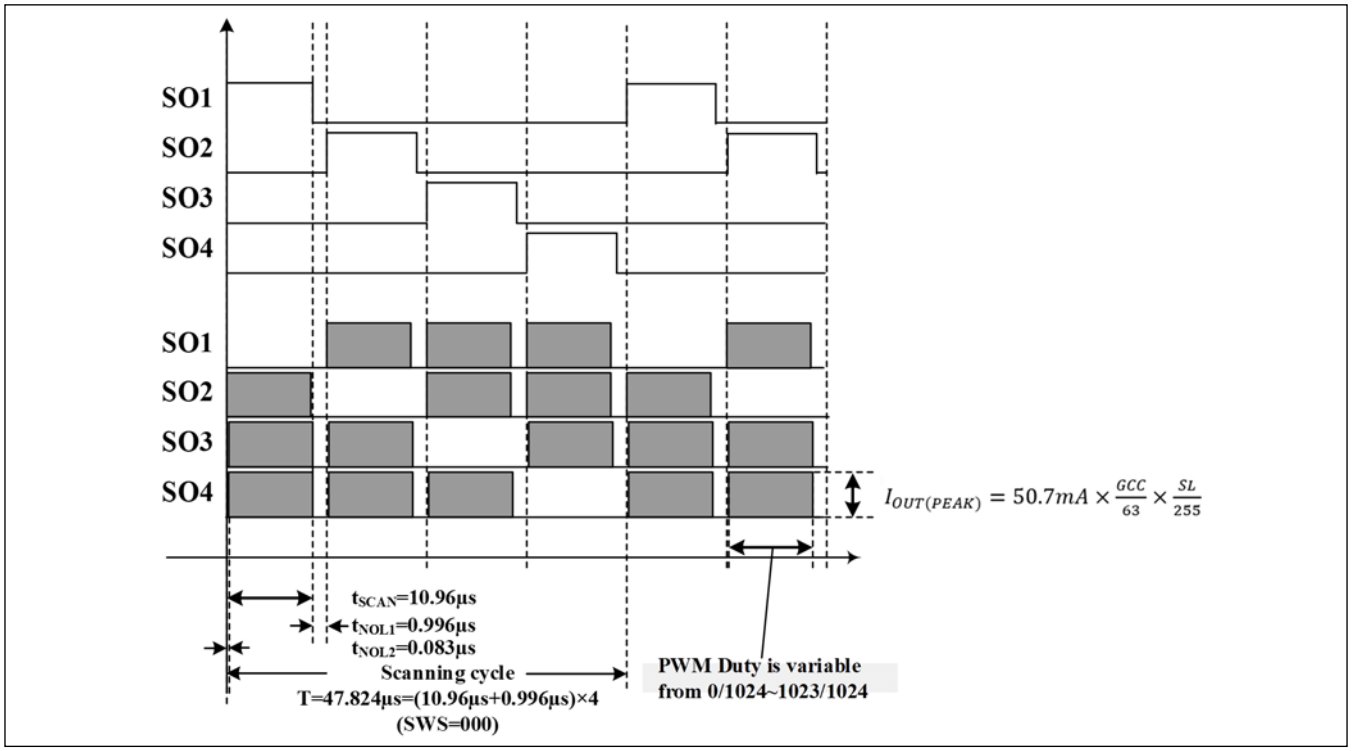


Figure 10 Scanning Timing (SWS=000)

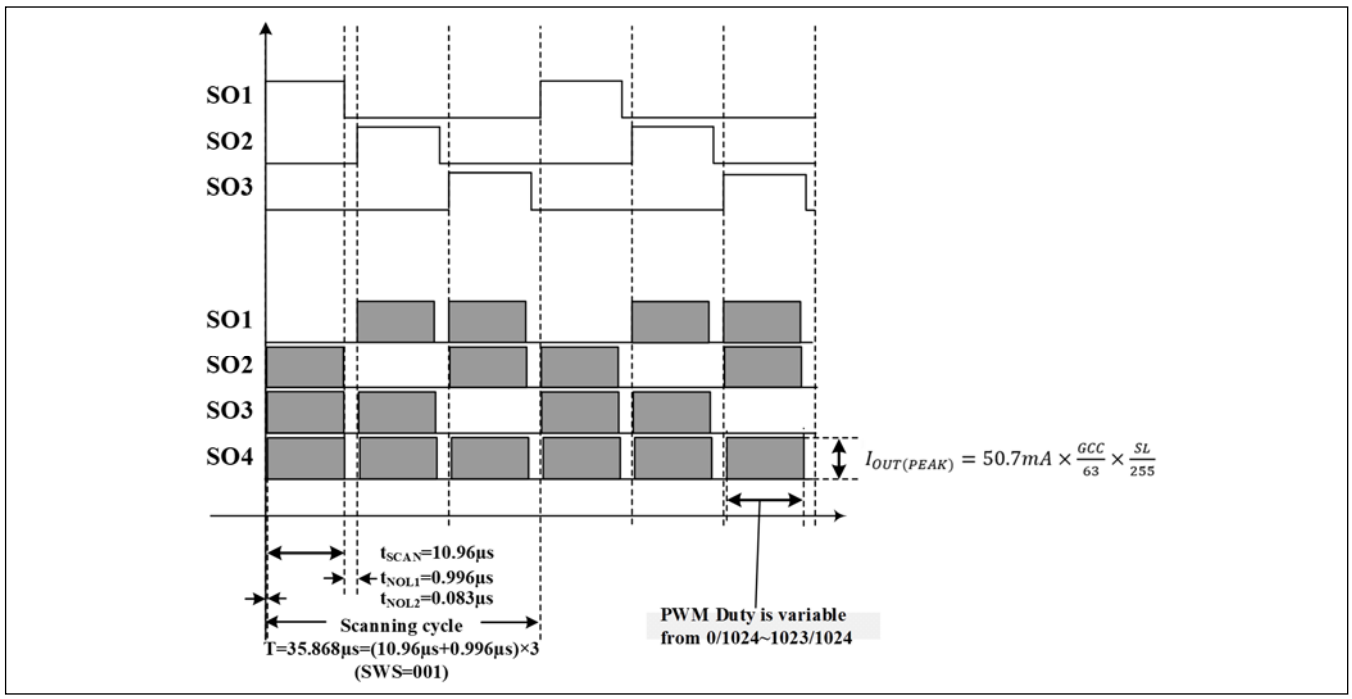


Figure 11 Scanning Timing (SWS=001)

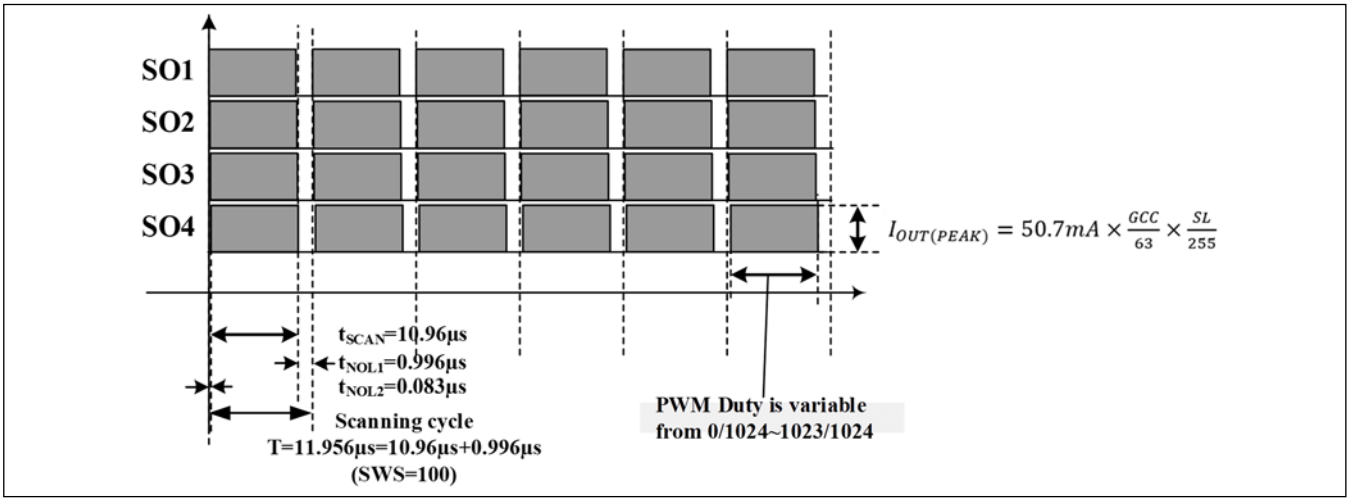


Figure 12 Scanning Timing (SWS=100)

SCANNING TIMING

As shown in Figure above, the SO1~SO4 work as power source and turned on by serial, LED is driven within the SOx (x=1~4) on time (SOx, x=1~4 is source and it is high when LED on), including the non-overlap blanking time during scan, the duty cycle of SOx (active high, x=1~4) is:

$$Duty = \frac{10.96\mu s}{(10.96+0.996)\mu s} \times \frac{1}{4} = \frac{1}{4.363} \quad (2,\ SOx=1/4)$$

Where 10.96μs is t_{SCAN}, the period of scanning and 0.9969μs is t_{NOL1}, the non-overlap time 0.083μs is the SOx delay time.

And the scan frequency is 1/n of PWM frequency, where n is scan number that can be choose by SWS of A0h register and the number of select range as = 1, 2, 3, 4. For example, when n = 2, namely SWS = 101, and the PWM frequency is 83.64kHz, the scan frequency is 1/2 of PWM frequency is 41.82kHz.; or when n = 3, the scan frequency is 1/3 of PWM frequency is 28.21kHz…

CURRENT SETTING

The maximum output current is 50.7mA. The Global Current Control register GCC (A1h) can be used to set a lower current. The 8-bit Scaling registers (1Ah~25h) control the individual currents for each of the outputs.

PWM CONTROL

The PWM Registers (02h~19h) can modulate LED brightness of each channels with 1024 steps. For example, if the data in PWM_H Register is “00” and in PWM_L Register is “0000 1000”, then the PWM is 8/1024.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

OPERATING MODE

IS31FL3713 has 3 operating modes, Current Level Mode, PWM Mode and Pattern Mode.

PWM MODE

PWM Mode When PME bits in Pattern Mode Enable Register (26h~27h) are set to “0” and DCSO bits in Current Level Mode Register (9Bh) are set to “0”, the LED will work at PWM mode. In this mode, the Scaling Registers (1Ah~25h) adjust the peak current (I_{OUT}) of the dots, the PWM Registers (02h~19h) adjust the duty cycle of the dots current, the final result is the dots average current ILED.

PWM FREQUENCY SELECT

The IS31FL3713 dots operate with a default 6+4-bit bit PWM resolution and the PWM frequency of 83.64kHz. Because all the SOx channels are synchronized, the DC power supply will experience large instantaneous current surges when the SOx channels turn ON. These current surges will generate an AC ripple on the power supply which cause stress to the decoupling capacitors. When the AC ripple is applied to a monolithic ceramic capacitor chip (MLCC) it will expand and contract causing the PCB to flex and generate audible hum in the range of between 20Hz to 20kHz, to avoid this hum, there are many countermeasures, such as selecting the capacitor type and value which will not cause the PCB to flex and contract.

An additional option for avoiding audible hum is to set the IS31FL3713’s dots PWM frequency above the audible frequency range. The PWM Frequency Register (A2h) can be used to set the switching

CURRENT LEVEL MODE

The Current Level Mode only support direct drive mode (SWS bits in A0h as 100) and MIX mode SO4 (SWS bits in A0h as 101/110/111). When the SOx work in Current Level Mode, it means the output current is controlled by Scaling Registers (1Ah~25h) and the registers can modulate LED peak current SO of each output with 256 steps independently. For example, if the data in Scaling Register is “0000 0100”, then the current level is the fourth step, with a current level of 4/256.

In Current Level Mode, a new value must be written to the Scaling registers to change the output current. Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve blinking, or any other effects that the user defines.

PATTERN MODE

By setting the PME bits of the Operating Configure Register (26h/27h) to “1”, the corresponding dot will operate in Pattern Mode. In Pattern Mode, the timing characteristics for dots current – start time (TS), changing time (T1/T2/T3/T4), and end time (TP), can be adjusted individually so that each dot can independently maintain a pre-established pattern achieving mixing color breathing or a single-color breathing without requiring any additional interface activity, 12 pattern settings (P1~P12) for 12 dots.

PATTERN PWM DUTY SETTING

In Pattern Mode, the LED color is defined by P_PWMx (x= 1, 2, 3, 4, 5) bits in Pattern PWM Registers (28h~2Ch/31h~35h/3Ah~3Eh/43h~47h/4Ch~50h/55h~59h/5Eh~62h/67h~6Bh/70h~74h/79h~7Dh/82h~86h/8Bh~8Fh). There are 4x3 RGB current combinations to generate 1 pre-defined colors for display. When PME bit is set, the P_PWMx is allowed to be displayed in current pattern.

In Pattern Mode, the 12 dots PWM duty at the 5 time points in the pattern loop is configured by the Pattern PWM Register as Table 14.

PATTERN TIME AND LOOP SETTING

User should configure the related pattern time setting registers according to actual timing requirements via I2C interface before starting pattern. The pattern time is including TS, T1~T4 and TP. And the pattern loop times need to be set. Please check the LED OPERATING MODE section for more about the time and loop setting.

PATTERN CONTROL SETTING

After configuring all other pattern registers, the pattern control register shall be used to manage pattern operation. The Pattern Control Register (94h~99h) enable independent configuration of 5 hold time points for each pattern as well as independent control over the start and stop of each pattern’s operation. The All Pattern Start/Stop Register (9Ah) supports simultaneous start and stop control for 12 patterns.

GAMMA CORRECTION

In order to perform a better visual LED breathing effect, the device integrates gamma correction to the Pattern Mode. The gamma correction causes the change in intensity to appear more linear to the human eye.

Gamma correction, also known as gamma compression or encoding, is used to encode linear luminance to match the non-linear characteristics of display. Since the IS31FL3713 can modulate the brightness of the LEDs with 128/64/32 steps in different PWM frequency, a gamma correction function can be applied when computing each subsequent LED intensity setting such that the changes in brightness matches the human eye's brightness curve.

The IS31FL3713 provides gamma corrections which can be set by GAM bit of the Configuration Register (A0h) for each pattern.

DE-GHOST FUNCTION

The “ghost” term is used to describe the behavior of an LED that should be OFF but instead glows dimly when another LED is turned ON. A ghosting effect typically can occur when multiplexing LEDs. In matrix architecture any parasitic capacitance found in the constant-current outputs or the PCB traces to the LEDs may provide sufficient current to dimly light an LED to create a ghosting effect.

To prevent this LED ghost effect, the IS31FL3713 has integrated Pull Down/Up Voltage Selection Register for each SOx (x=1~4). Select the right SOx pull down/up oltage (A4h) which eliminates the ghost LED for a particular matrix layout configuration.

Typically, selecting the SOx pull to VOUT -2.4V will be sufficient to eliminate the LED ghost phenomenon.

By selecting the pull period, the Pull Down/Up Voltage Selection Register is active when the SOx output working the OFF state, or it is active only in de-ghost time. The de-ghost time can be select.

INTERRUPT MARK FUNCTION

The Interrupt mark function serves as a signal to notify the MCU of specific events occurring on the IS31FL3713. Configure the Interrupt Mask Register (A7h/A8h) to select which events are reported to the MCU, and read the Interrupt State Register (A9h/AAh) to determine the status of these events.

When the INTB function is enabled, the SYNC/INTB pin operates as an open-drain output and requires an external pull-up resistor. Upon occurrence of a specific event, the SYNC/INTB pin generates a falling edge and remains at logic low. Once the event is cleared, the pin generates a rising edge to return to a high level.

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption.

Software Shutdown

By setting SSD bit of the Shutdown Register (A0h) to "0", the IS31FL3713 will operate in Software Shutdown mode. When the IS31FL3713 is in Software Shutdown mode, all current sources are on standby, so that the matrix is blanked. All registers can be written when the SDB pin is pulled high.

Hardware Shutdown

The chip enters Hardware Shutdown when the SDB pin is pulled low. All analog circuits are disabled during Hardware Shutdown, all registers will be reset to the default values, typical current consume is 0.3μA.

The chip enters Hardware Enable when the SDB pin is pulled high.

OPEN/SHORT DETECT FUNCTION

IS31FL3713 has open and short detect bit for each LED.

By setting the SDE/ODE bits of the Open Short Control Register (B1h) from "0" to "1" the Open Register (B2h/B3h) and the Short Register (B4h/B5h) will start to store the open/short information and the MCU can get the open/short information by reading the B2h~B5h, for those dots are turned off via Scaling registers (1Ah~25h), the open/short data will not get refreshed when setting the SDE/ODE bits of the Open Short Control Register.

To get the correct open and short information, two configurations need to set before setting the O/S bits:

1 0x0F≤ GCC≤ 0x3F
2 PWM pulse width greater than 1.5μs (Typ.)

When an LED Open/Short fault occurs, the IS31FL3713 will initiate protection actions based on the fault conditions. Upon detection of an open circuit on a single LED, the corresponding LED will be turned off, and upon detection of a short circuit on a single LED, all LEDs will be turned off. Refer to the table 31 for the activation conditions of the open/short protection actions.

Table 31 LED Open/Short Fault Action Table

Fault Type	Detection	Conditions			LED Actions	Fault Flags	FAULTB Pin	Recovery
LED open	V_{Sox} < 0.1V	PWM pulse width greater than 1.5μs (Typ.) and ODE bit= 1		OIE= 0	Faulty LED dots off	OIF bit OPEN bit	No action	V_{SOx} > 0.1V Write OPEN bit to "0"
				OIE= 1			Pull low	
LED short	(V_{OUT} - V_{Sox}) < 1V	PWM pulse width greater than 1.5μs (Typ.) and SDE bit= 1	OFAF= 0	SIE= 0	No action	SIF bit SHORT bit	No action	(V_{OUTx} - V_{SOx}) > 1V
				SIE= 1			Pull low	
			OFAF= 1	SIE= 0	All LED dots off		No action	(V_{OUTx} - V_{SOx}) > 1V Write SHORT bit to "0"
				SIE= 1			Pull low	

6+4-BIT PWM MODE

Then the dots PWM frequency is 6-bit, resolution is 10-bit. This is achieved through 6-bit PWM modulation and 4-bit dither control. For 4-bit dither, according to the 16-dither timing, each of the 16 PWM groups can add one PWM_x or no PWM_x (Where x = H or L).

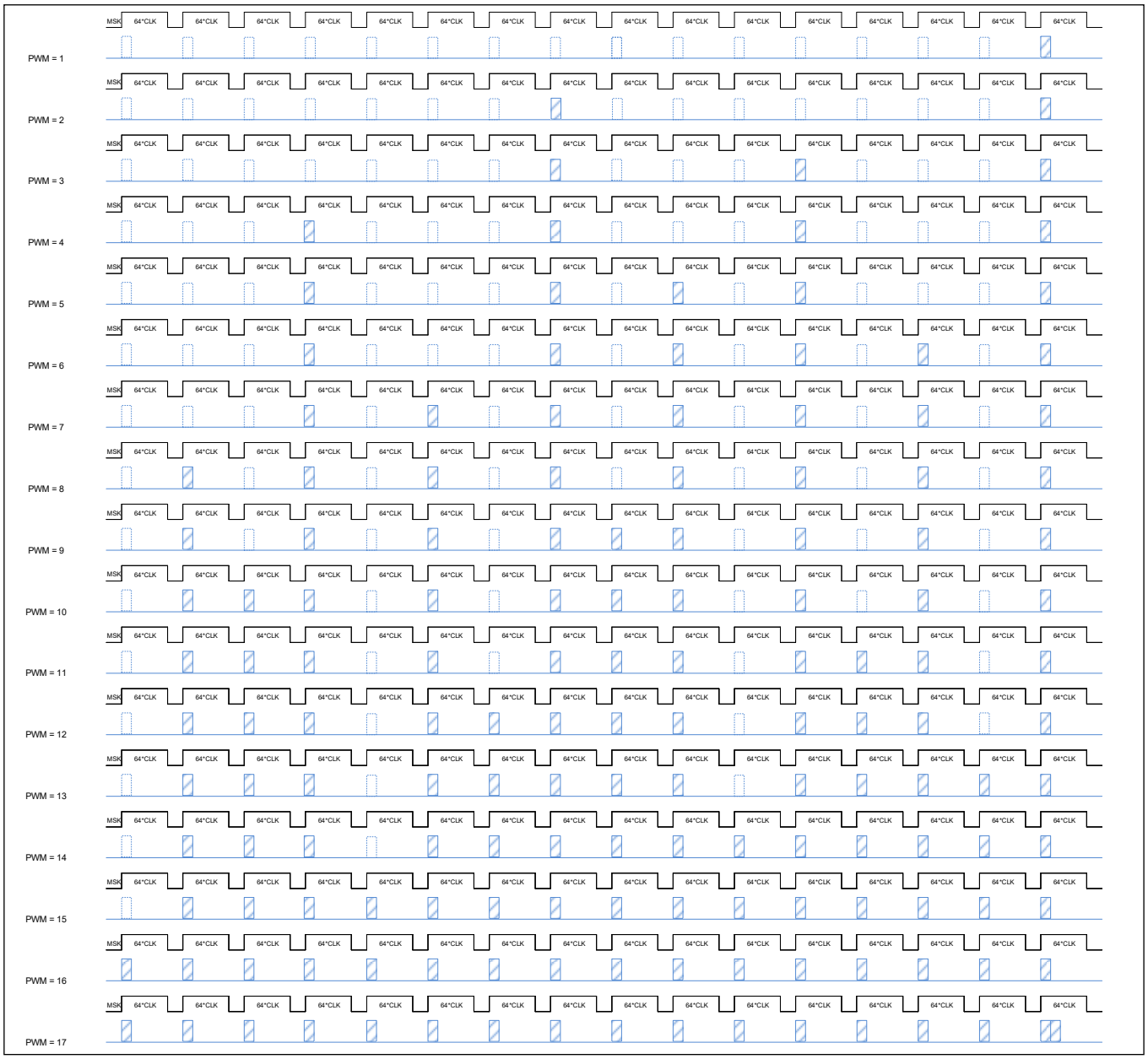


Figure 13 6+4-BIT PWM MODE

LED OPERATING MODE

12 LED dots or 4 SOx running individual. There have three operating modes which can be chosen by the SWS bits, PMEx bit and DCSOx bit.

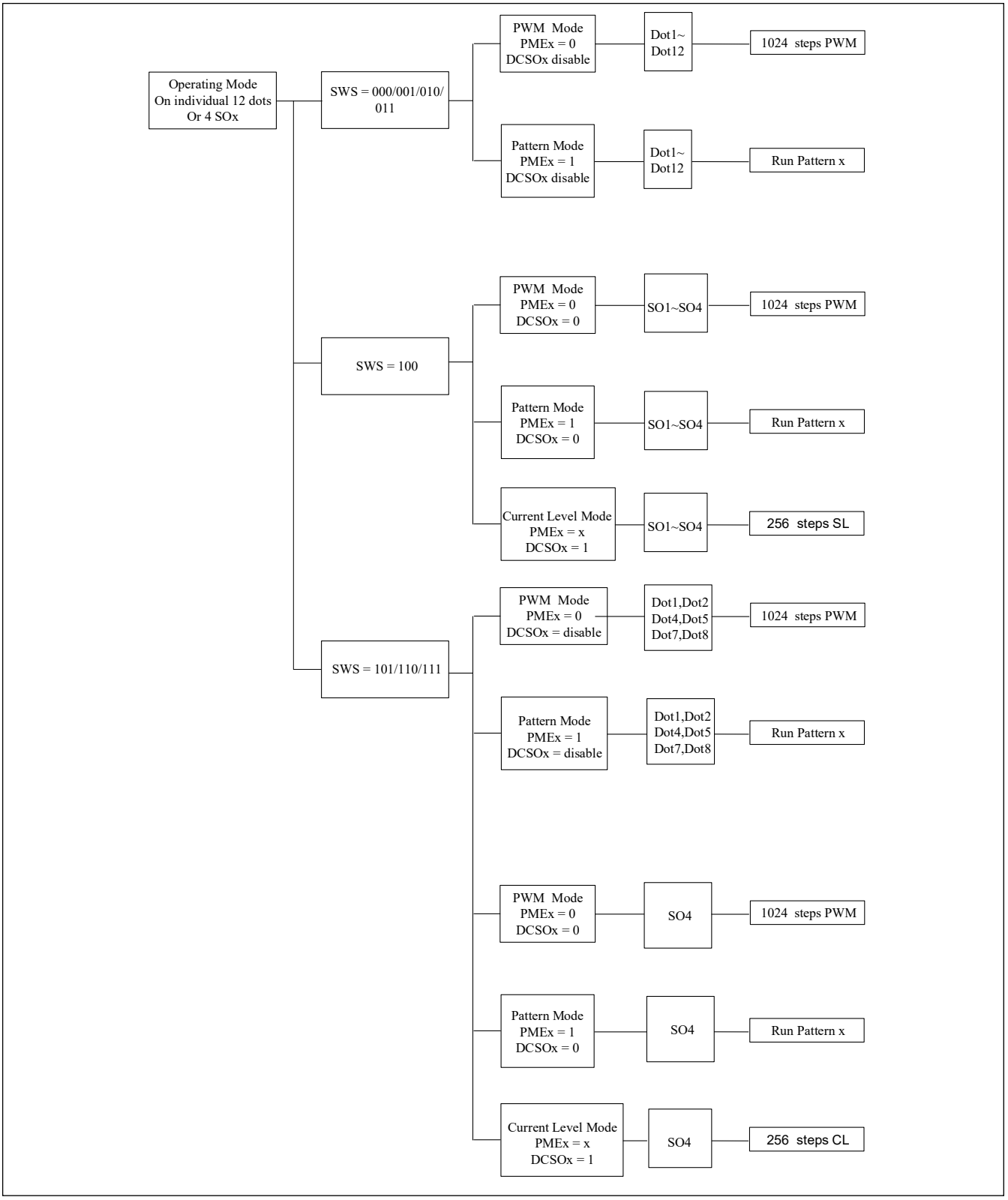


Figure 14 Operating Mode Map

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

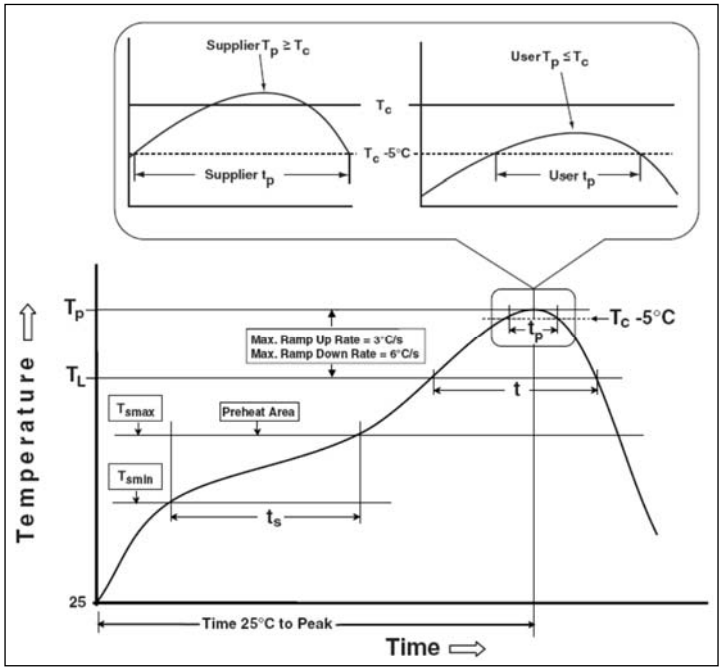
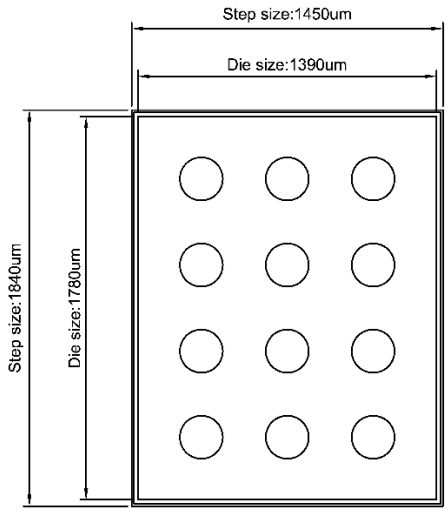


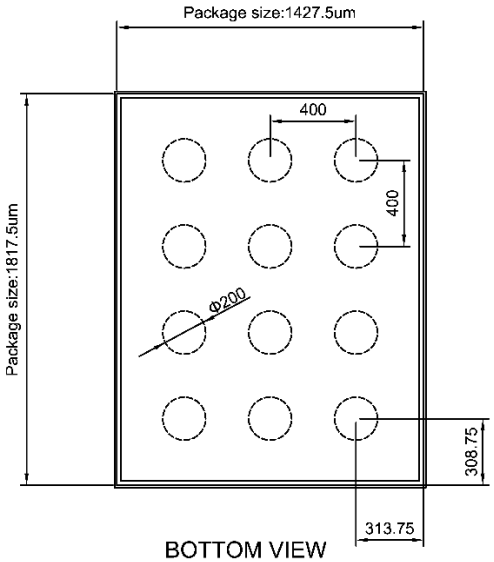
Figure 15 Classification Profile

PACKAGE INFORMATION

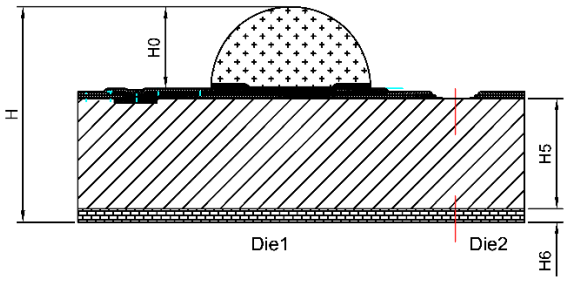
WLCSP-12



TOP VIEW



BOTTOM VIEW



CROSS SECTION

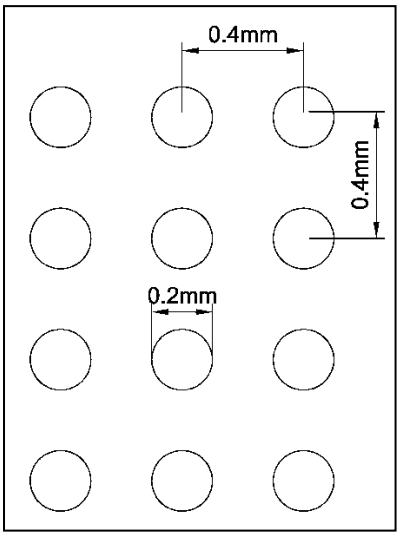
SYMBOL	ITEM	DATA(UM)
H	PACKAE HEIGHT	460±24.5
H0	BALL HEIGHT	60±6
H5	SI THICKNESS	350±10
H6	DRY FILM	25±3

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NOTE:
1. CONTROLLING DIMENSION : UM
2. THE PIN'S SHARP AND THERMAL PAD SHOWS DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

RECOMMENDED LAND PATTERN

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Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release	2026.01.04
0B	1. Update the I_{CC}/I_{STB}/ R_{DS_ON} /I_O in EC table 2. Add the description of ABh~B0h Pattern State Register 3. Add the description of Hardware Shutdown	2026.04.15
A	Release to mass production	2026.06.24