1 2 3 4 5 6

A

Zynq PicoZed 7015/7030

Avnet Engineering Services

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B

PicoZed 7015/7030

7/15/2015

2:35:34 PM

C

D

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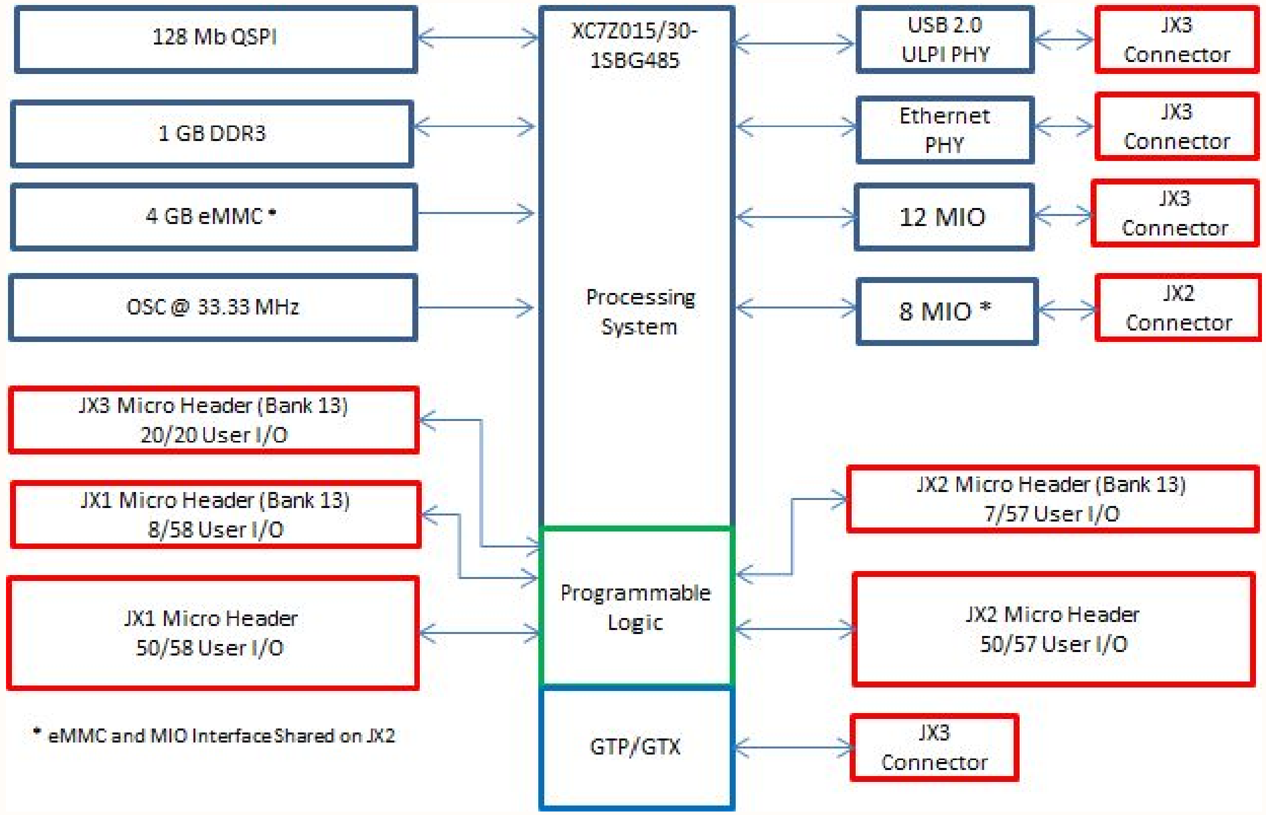
Title:	01 - Lead Sheet.SchDoc		
Size: B	Document Number: PicoZed 7015/7030		Rev: C
Date: 7/15/2015		Sheet 1 of 12	

1 2 3 4 5 6



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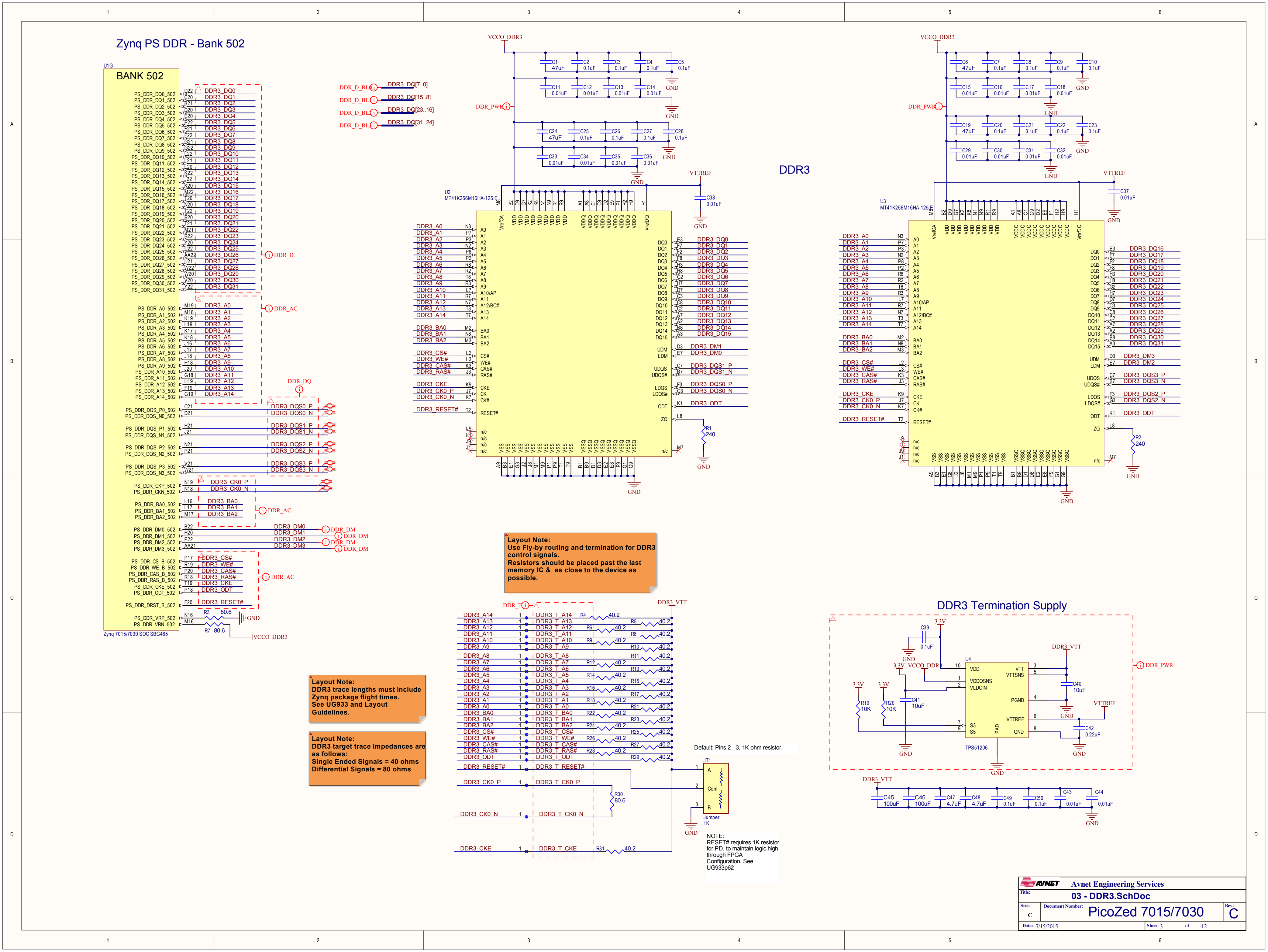
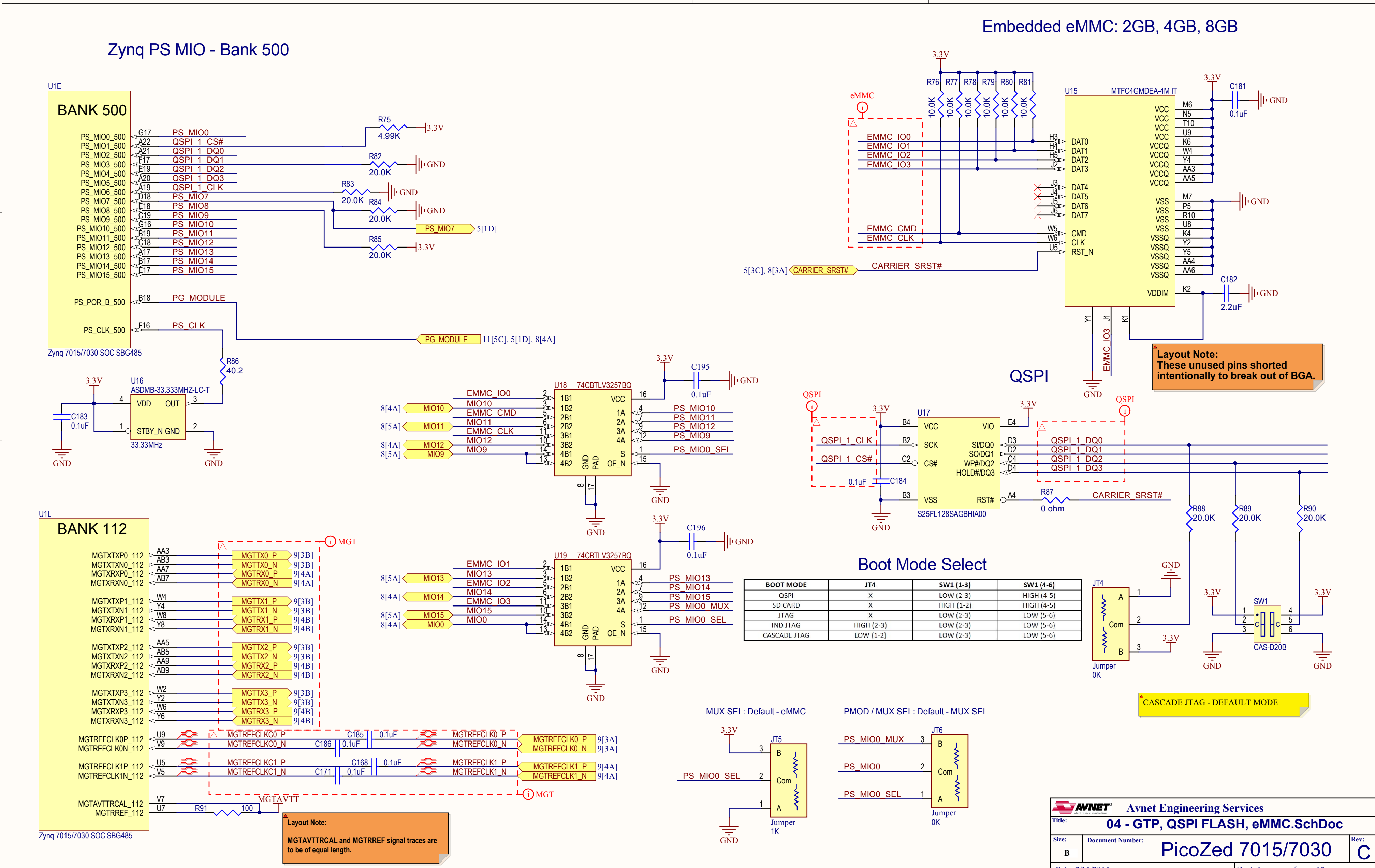
Title: 02 - Block Diagram.SchDoc

Size:	Document Number:	Rev:
B	PicoZed 7015/7030	C

Date: 7/15/2015 Sheet 2 of 12



Zynq PS DDR - Bank 502
BANK 502
U1G
Zynq 7015/7030 SOC SBG485
DDR3
U2
MT41K256M16HA-125:E
U3
MT41K256M16HA-125:E
VCCO_DDR3
VTTREF
DDR3_VTT
DDR_PWR
GND
Layout Note:
Use Fly-by routing and termination for DDR3 control signals.
Resistors should be placed past the last memory IC & as close to the device as possible.
Layout Note:
DDR3 trace lengths must include Zynq package flight times.
See UG933 and Layout Guidelines.
Layout Note:
DDR3 target trace impedances are as follows:
Single Ended Signals = 40 ohms
Differential Signals = 80 ohms
DDR3 Termination Supply
U4
TPS51206
Default: Pins 2 - 3, 1K ohm resistor.
JT1
Jumper 1K
NOTE:
RESET# requires 1K resistor for PD, to maintain logic high through FPGA Configuration. See UG933p62
AVNET
Avnet Engineering Services
Title: 03 - DDR3.SchDoc
Size: C
Document Number: PicoZed 7015/7030
Rev: C
Date: 7/15/2015
Sheet 3 of 12



Boot Mode Select

BOOT MODE	JT4	SW1 (1-3)	SW1 (4-6)
QSPI	X	LOW (2-3)	HIGH (4-5)
SD CARD	X	HIGH (1-2)	HIGH (4-5)
JTAG	X	LOW (2-3)	LOW (5-6)
IND JTAG	HIGH (2-3)	LOW (2-3)	LOW (5-6)
CASCADE JTAG	LOW (1-2)	LOW (2-3)	LOW (5-6)

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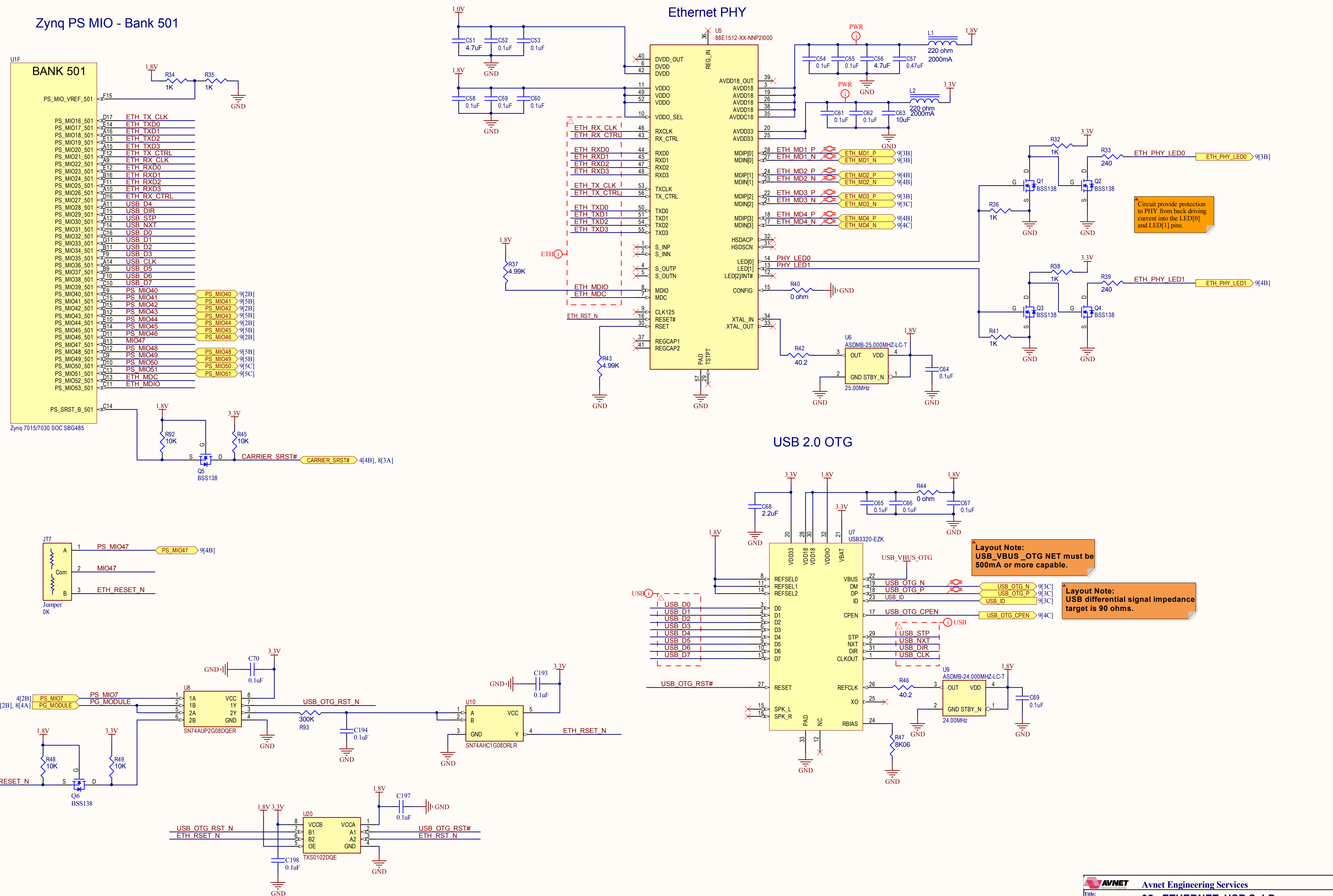
Title: 04 - GTP, QSPI FLASH, eMMC.SchDoc

Size: B | Document Number: PicoZed 7015/7030 | Rev: C

Date: 7/15/2015 | Sheet 4 of 12



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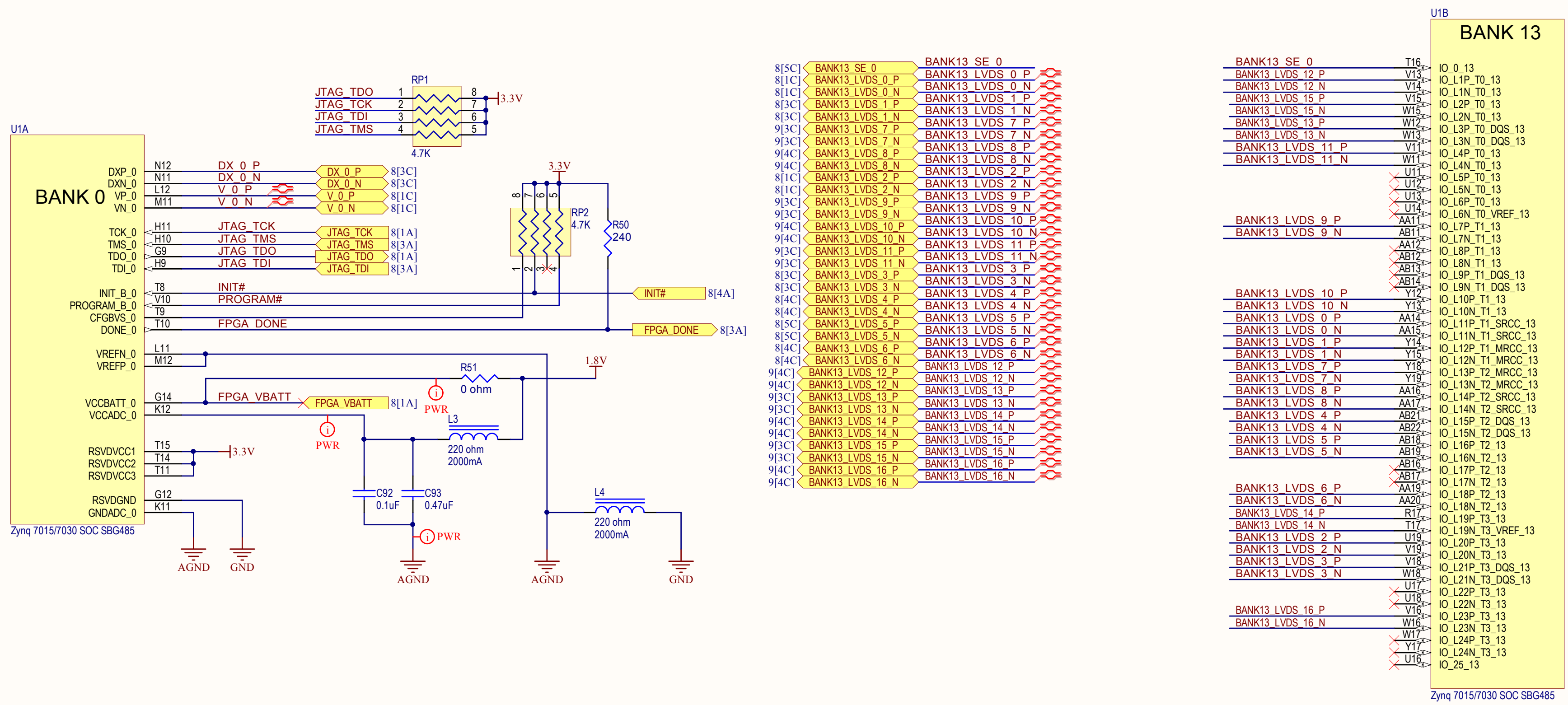
Title: 05 - ETHERNET, USB.SchDoc

Size: C | Document Number: PicoZed 7015/7030 | Rev: C

Date: 7/15/2015 | Sheet 5 of 12

WARNING!!!
Bank 34 and Bank 35 are High Performance banks (7030 only) and will only accept 1.8V level signals.
Failure to limit Bank 34 and 35 to 1.8V signals can damage the Zynq 7030 AP SoC.

AVNET	Avnet Engineering Services	
Title:	06 - BANKS 34 and 35.SchDoc	
Size: B	Document Number: PicoZed 7015/7030	Rev: C
Date: 7/15/2015	Sheet 6 of 12	



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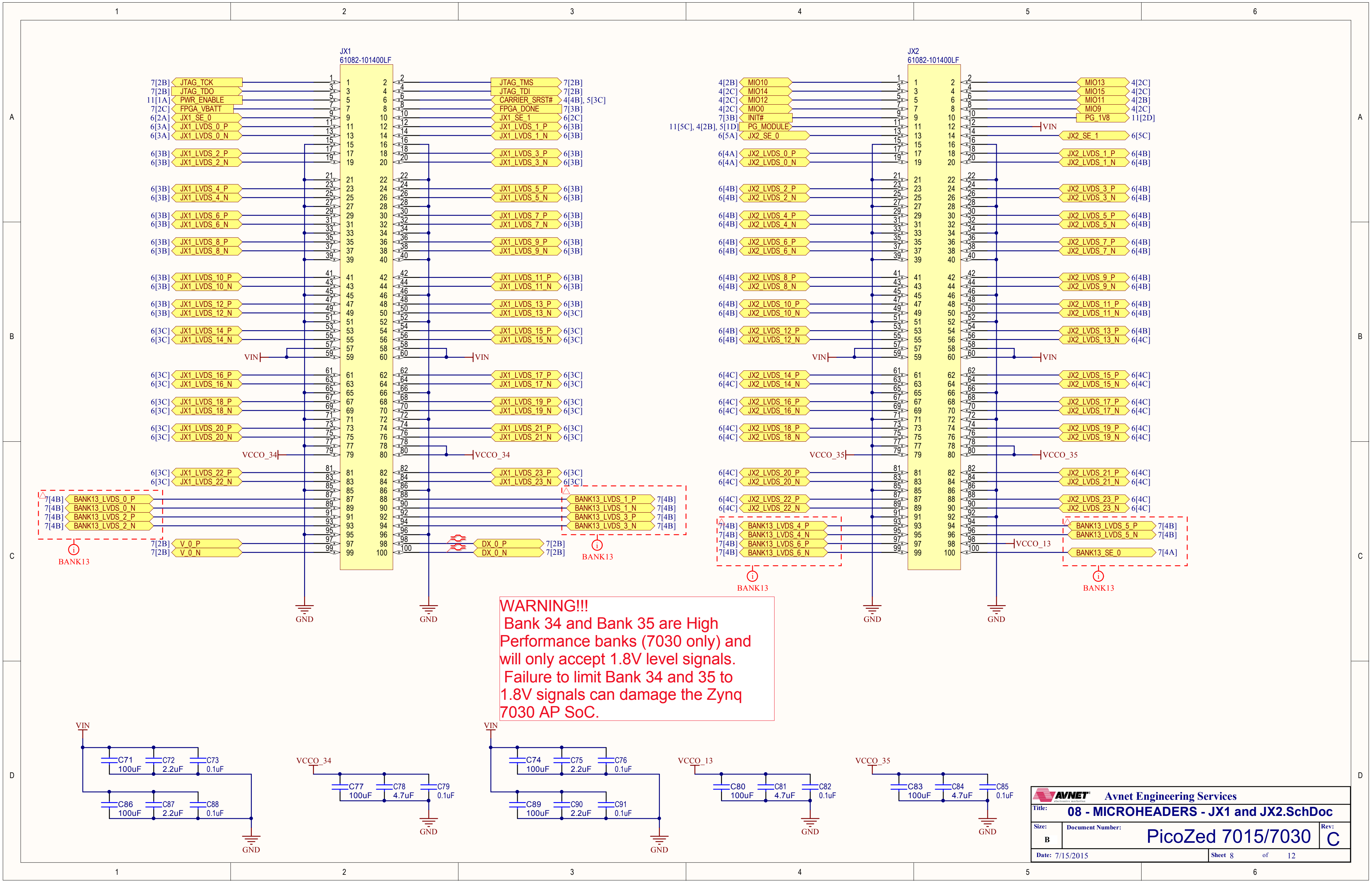
Title: 07 - BANK 0, BANK13, JTAG.SchDoc

Size:	Document Number:	Rev:
B	PicoZed 7015/7030	C

Date: 7/15/2015 Sheet 7 of 12


JX1
61082-101400LF
JX2
61082-101400LF
BANK13
VIN
VCCO_34
VCCO_35
VCCO_13
GND
WARNING!!!
Bank 34 and Bank 35 are High Performance banks (7030 only) and will only accept 1.8V level signals.
Failure to limit Bank 34 and 35 to 1.8V signals can damage the Zynq 7030 AP SoC.
C71 100uF
C72 2.2uF
C73 0.1uF
C86 100uF
C87 2.2uF
C88 0.1uF
C77 100uF
C78 4.7uF
C79 0.1uF
C74 100uF
C75 2.2uF
C76 0.1uF
C89 100uF
C90 2.2uF
C91 0.1uF
C80 100uF
C81 4.7uF
C82 0.1uF
C83 100uF
C84 4.7uF
C85 0.1uF
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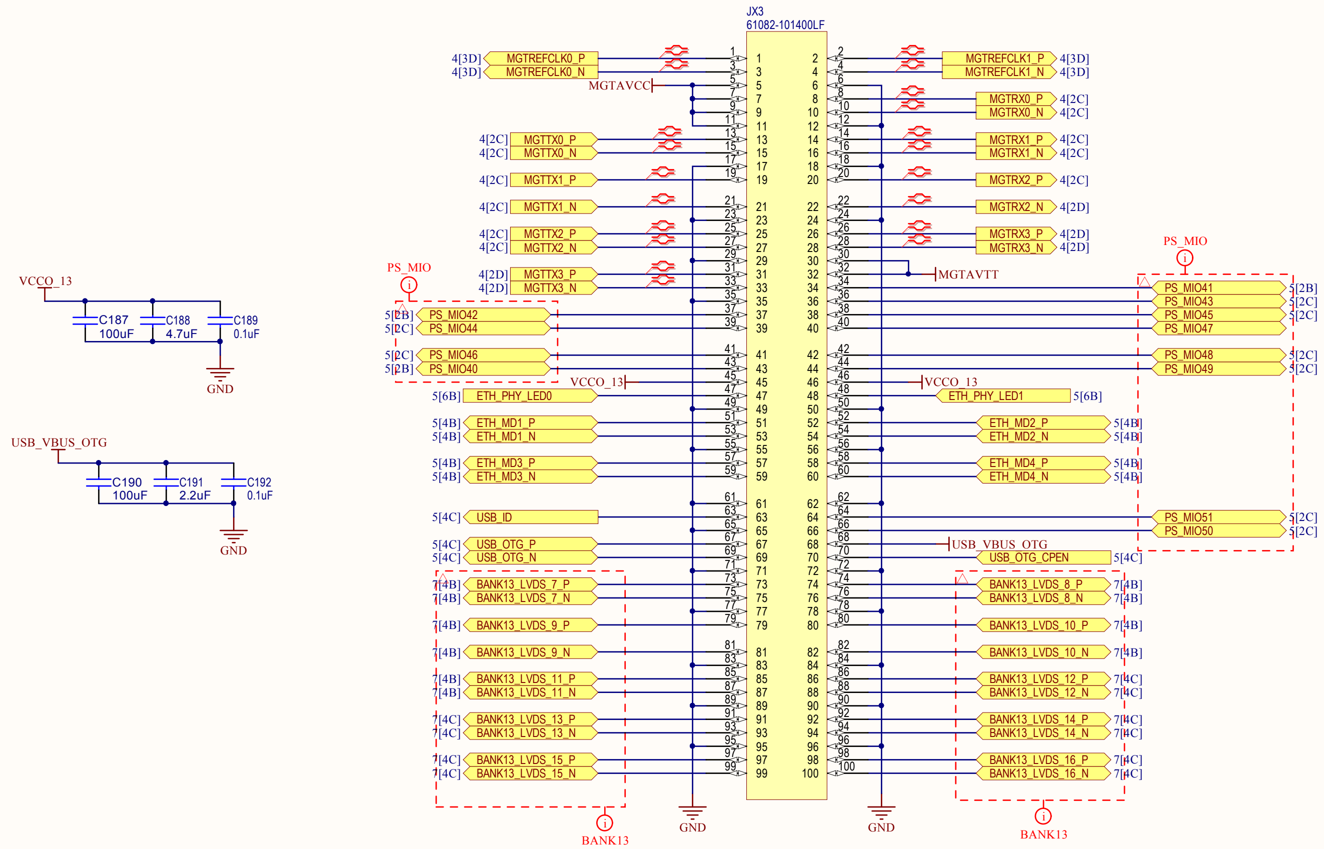
Title: 08 - MICROHEADERS - JX1 and JX2.SchDoc
Size: B
Document Number: PicoZed 7015/7030
Rev: C
Date: 7/15/2015
Sheet 8 of 12



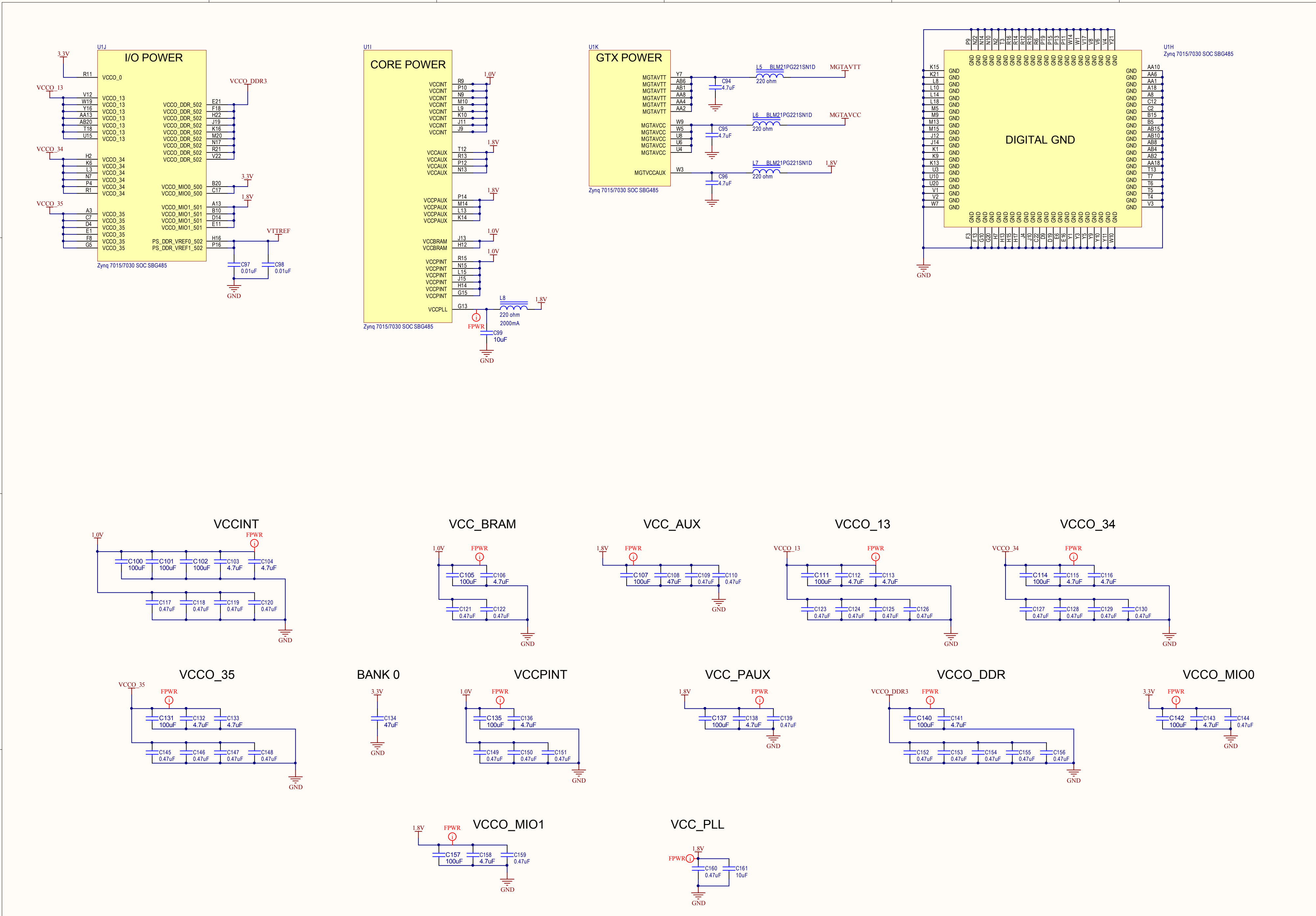
ZYNQ MIO POTENTIAL MAPPING OPTIONS:

SDIO INTERFACE
PS_MIO40 - SD_CLK through a 40.2-ohm RES
PS_MIO41 - SD_CMD
PS_MIO42 - SD_D0
PS_MIO43 - SD_D1
PS_MIO44 - SD_D2
PS_MIO45 - SD_D3
PS_MIO46 - SD_CD

UART INTERFACE
PS_MIO48 - UART_RXD (Tie to the TXD pin of a UART)
PS_MIO49 - UART TXD (Tie to the RXD pin of a UART)

USB INTERFACE
PS_MIO40 - DATA
PS_MIO41 - DIR
PS_MIO42 - STP
PS_MIO43 - NXT
PS_MIO44 - DATA
PS_MIO45 - DATA
PS_MIO46 - DATA
PS_MIO47 - DATA
PS_MIO48 - CK
PS_MIO49 - DATA
PS_MIO50 - DATA

AVNET	Avnet Engineering Services
Title:	09 - MICROHEADER - JX3.SchDoc
Size: B	Document Number: PicoZed 7015/7030 — Rev: C
Date: 7/15/2015	Sheet 9 of 12



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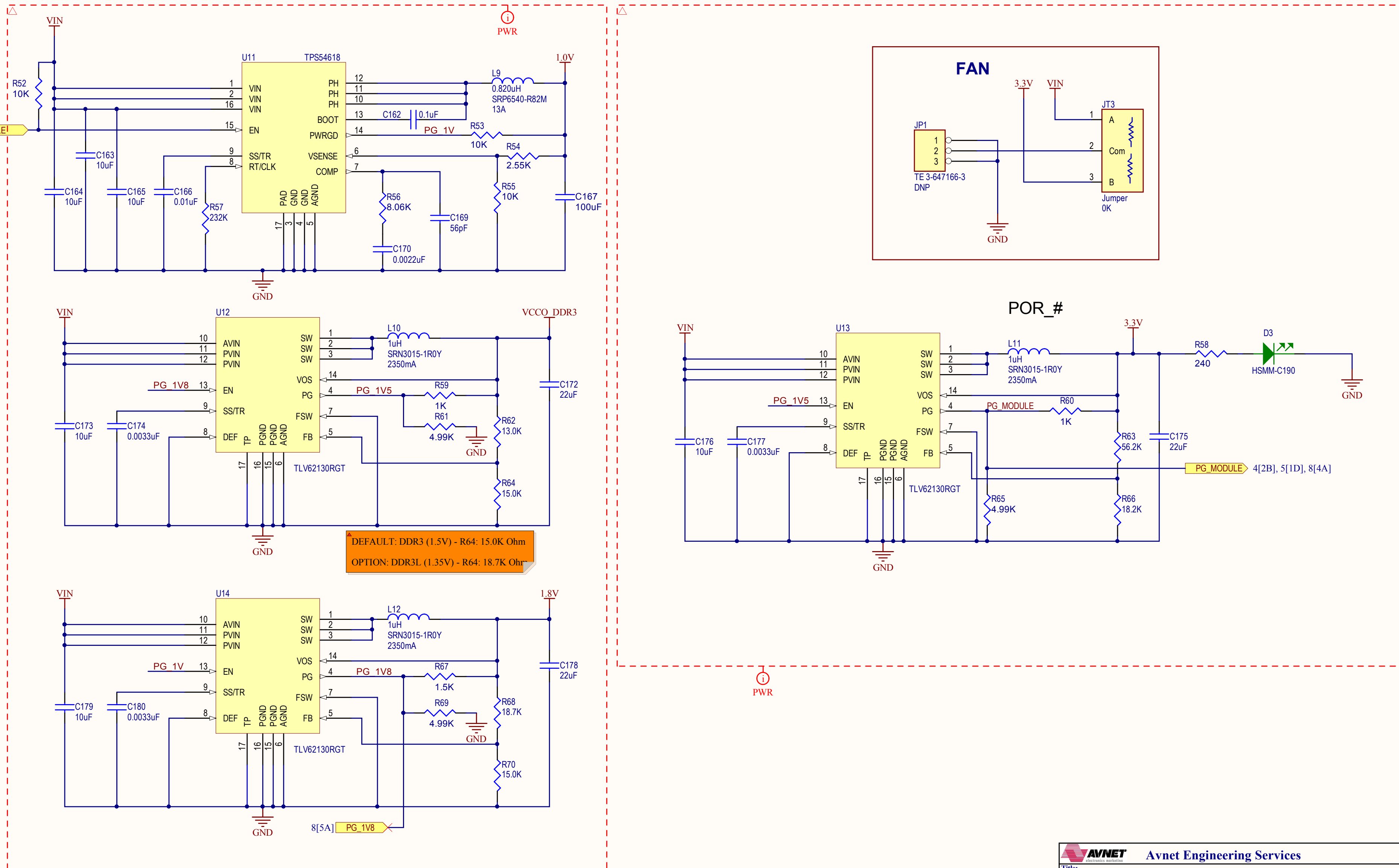
Title: 10 - DEVICE POWER.SchDoc

Size	Document Number	Rev
C	PicoZed 7015/7030	C

Date: 7/15/2015 Sheet 10 of 12



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Title: 11 - POWER, RESET.SchDoc

Size: B | Document Number: PicoZed 7015/7030 | Rev: C

Date: 7/15/2015 | Sheet 11 of 12

Revision History

Rev B

Original release

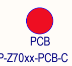
Rev C

1) Updated Block Diagram
2) Added shared circuit MIO47 to JX3 and ETHERNET RESET
3) Added RC time constant to ETHERNET RESET
4) DDR3L/DDR3 option note added
5) Renamed 1.5V and DDR3_0V75 power nets
6) Changed U4.2 connection from 1.8V to 3.3V
7) Changed JX1/JX2 connections to Zynq Bank 34/35 Clock Capable Pins

Rev C - Update

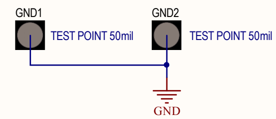
1) PUDC Default value changed to VCCO
2) C194 value changed to fix Ethernet Reset RC time constant
3) QSPI_CS resistor value changed to 4.99K

Mechanicals:



PCB Mounting Holes

GND Test Points



AVNET	Avnet Engineering Services	
Title:	12 - Back Page.SchDoc	
Size: B	Document Number: PicoZed 7015/7030	Rev: C
Date: 7/15/2015	Sheet 12 of 12	