VE2302 SOM

Hardware User Guide

Version 1.2

LIT# VE2302-SOM-UG-V1P2

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Document Control

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Version History

Version	Date	Comment
1.0	6/6/2025	Initial Release
1.1	6/30/2025	Master JX Table Correction
1.2	8/5/2025	Master JX Table Correction

1 Introduction

The Tria Technologies VE2302 SOM (System-On-Module) is a high-performance product targeted for broad use in many applications. The goal of the module is to offer a compact SOM (50mm x 50mm) solution with an AMD Versal™ AI Edge device in commercial (0C to 70C) and industrial (-40C to 85C) temperature grades for engineers to adopt in development, proof-of concept, and production designs. The features provided by the VE2302 SOM consist of:

- AMD XCVE2302-1LSESFVA784 (Pin compatible with the XCVE2202 device)
  - Pin compatible with the XCVE2102, XCVE2202, and XCVM1102
  - Primary configuration options: OSPI flash
  - Auxiliary configuration options via end user carrier card:
    - JTAG
    - microSD card
- Memory
  - LPDDR4 SDRAM (4GB, 2x32)
  - PMC OSPI Flash (Octal 256MB)
  - PMC eMMC Flash (x8 32GB)
  - I2C MAC EEPROM (2Kb)
- Interfaces
  - PMC USB 2.0 ULPI PHY (Connector required on end user carrier card)
  - Gigabit Ethernet RGMII PHY (Connector required on end user carrier card)
  - I2C 8-bit I/O Expander
  - 2-channel I2C Switch/Mux
  - 3 JX Micro-Header Connectors (3 x 160-pin)
    - 80 User XPIO Pins
    - 22 User HDIO Pins
    - 12 User LPD MIO Pins
    - 13 User PMC MIO Pins
    - 8 GTYP Transceivers
    - 4 GTYP Reference Clock Inputs
    - PMC JTAG Interface
    - PMC SYSMON interface
    - USB 2.0 Connector Interface
    - Gigabit Ethernet RJ45 Connector Interface
    - PMBus Interface
    - Carrier Card I2C Interface
    - SOM +VCC_BATT Battery Input
    - SOM Reset Input
    - Carrier Card Interrupt Input
    - Carrier Card Reset Output
    - SOM Power Good Output
    - SOM to Carrier Card Ground Pins
    - SOM Input Voltages and Output Sense Pins
  - Reference Clock
    - 33.333 MHz OSC
  - Real Time Clock (RTC)
- Power
  - On-Board Voltage Regulators
  - Custom Power Sequencer (Supports power-up and power-down sequencing)
  - Bank I/O and GTYP Transceiver Voltage Rails (Supplied via end user carrier card)
- Pertinent URLs
  - VE2302 SOM: **http://avnet.me/ve2302-som**
  - VE2302 Development Kit: **http://avnet.me/ve2302-dk**

The following table is a glossary of acronyms that will be used in description of the VE2302 SOM, and the peripherals attached to the Adaptive SoC Processing Sub-System and Programmable Logic Sub-System.

Term	Definition
PS	Adaptive SoC Processing System
PL	Adaptive SoC Programmable Logic
MIO	Multiplexed Input Output Pins
LPD	Low Power Domain
PMC	Platform Manager Controller
PLM	Platform Loader and Manager
POR	Power On Reset
APU	Application Processing Unit
RPU	Real-time Processing Unit
GPU	Graphics Processing Unit
SYSMON	System Monitor
ADC	Analog-to-Digital Converter
HDIO	High Density PL I/O Pins
XPIO	High Performance PL I/O Pins
PMBus	Power Management Bus
PDM	Power Design Manager

Table 1 – Glossary

The following figure is a high-level block diagram of the VE2302 SOM and the peripherals attached to the Adaptive SoC Processing Sub-System and Programmable Logic Sub-System.

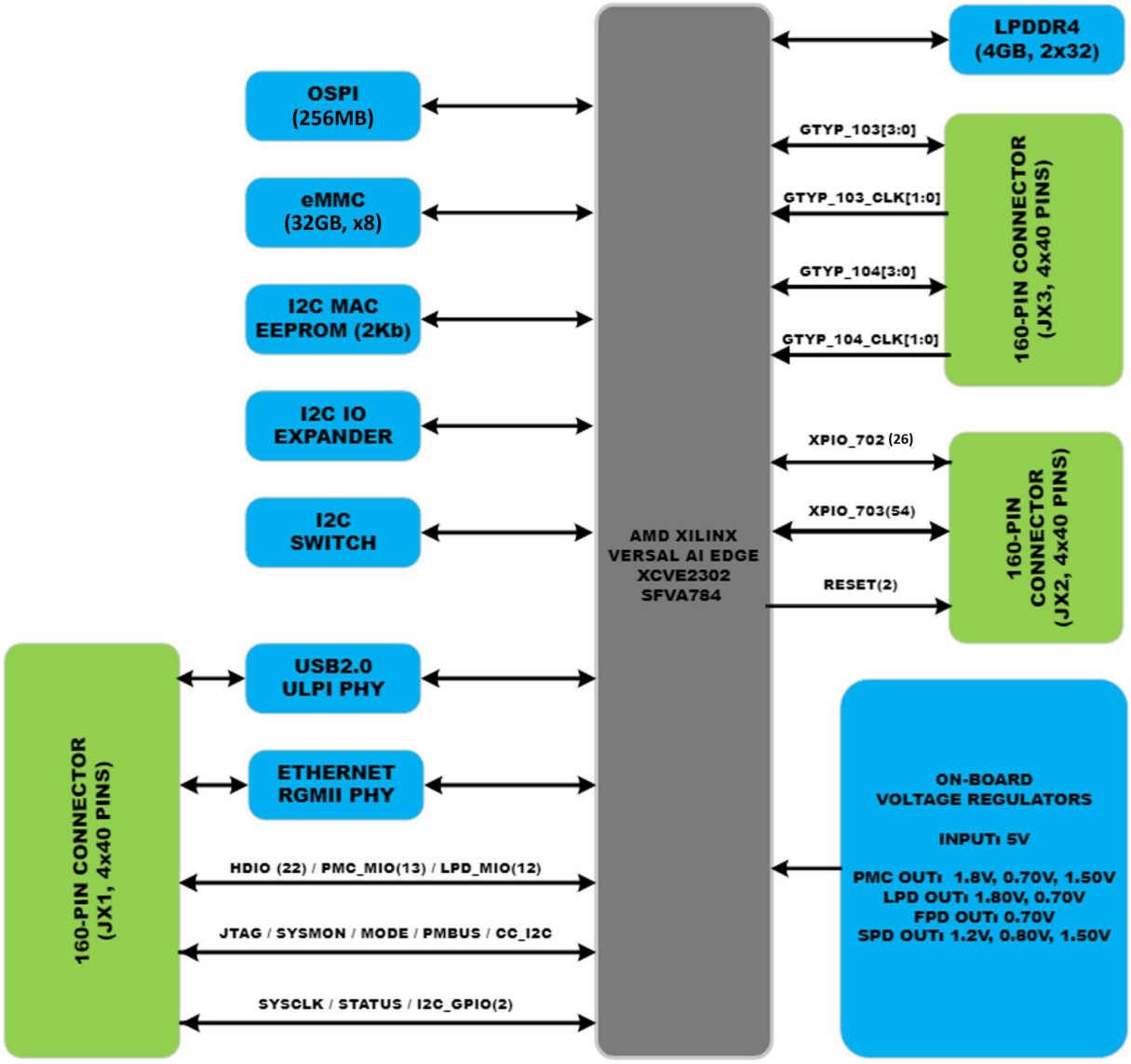

Figure 1 – VE2302 SOM Block Diagram

1.1 Additional Information

Additional information and documentation on the AMD Versal™ Adaptive SoC can be found Here:
https://www.amd.com/en/products/adaptive-socs-and-fpgas/versal.html

2 Functional Description

2.1 AMD Versal™ AI Edge

The VE2302 SOM provides the flexibility and versatility for developers to enable designs with the AMD Versal™ AI Edge series. This System-On-Module (SOM) is a small form factor and full-featured board based on the AMD Versal™ AI Edge VE2302 device featuring 328K programmable logic cells with a Dual-core Arm® Cortex®-A72 Application Processing Units and Dual-core Arm Cortex-R5F Real Time Processing Units, as well as L1 and L2 cache and 256KB on-chip memory with ECC. The SOM provides a host of features to simplify application development with a custom carrier card.

The VE2302 SOM is offered in commercial temperature grade and industrial temperature grade options. The VE2302 SOM is populated by default with a **XCVE2302-1LSESFVA784** device. Optionally, the VE2302 SOM is footprint compatible with several other AMD devices including the XCVE2102, XCVE2202, and XCVM1102.

2.2 Memory

The VE2302 SOM contains a hardened DDR memory controller that is utilized for LPDDR4-4200. The VE2302 SOM takes advantage of hardened DDR memory controller to provide system RAM as well as two different non-volatile memory sources.

2.2.1 LPDDR4

The VE2302 SOM provides 4GB of LPDDR4 memory in a 2x32 configuration using two Micron **MT53E512M32D1ZW-046 IT:B** (200-pin BGA package) x32 devices. The LPDDR4 devices are implemented in 512Mb x 32 configuration and supports up to 3733 Mbps in a -1 VE2302 device using an operating voltage of 0.80V.

The LPDDR4 devices are connected to an XPIO triplet in banks 700, 701, and 702 and are operated at +1.1V at the maximum supported bandwidth available in the **PIN EFFICIENT** implementation on the AMD Versal™ AI Edge device. The **PIN EFFICIENT** implementation results in all but four (4) signals being implemented in banks 700 and 701.

A couple of issues arise when implementing the LPDDR4 interface in this manner. First issue is that four (4) signals with a bank voltage of +1.1V exist on bank 702 which creates a potential for a mismatch with the bank voltage if you desire to utilize bank 702 for a voltage other than the memory bank voltage, such as a bank voltage like 1.2V or 1.5V. A workaround for this exists and is documented in **AMD Answer Record 35358** which helps to resolve voltage standard conflicts for pin efficient topologies.

NOTE: Link to Answer Record 35358: **Versal™ Adaptive SOC DDRMC - Change LPDDR4 RESET_N and SYS_CLK IO Standards for Pin Efficient Topologies**

The second issue that arises when implementing the LPDDR4 interface with a **PIN EFFICIENT** implementation is that some of the XPIO pins in bank 702 are dedicated to the DDRMC (DDR Memory Controller) and cannot be utilized by end-users. This results in a total of 24 pins that cannot be utilized on Bank 702 because of the **PIN EFFICIENT** implementation. The pins that are DDRMC will be identified on the JX connector pinout. Please refer to the **Expansion Headers** section of this document for the DDRMC Bank 702 pins that should not be utilized.

The implementation of LPDDR4 interface on the VE2302 SOM ensures board trace lengths are matched, compensating for the internal package flight times of the XCVE2302 SoC SFVA784 package, to meet the requirements listed in the Versal™ Adaptive SoC PCB Design User Guide (**UG863**).

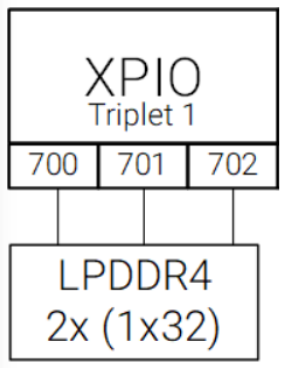

Figure 2 – LPDDR4 Block Diagram

Signal Name	Description	Bank 700 SoC Pin	LPDDR4 Pin U23
LPDDR4_CH0_DQ_A0	LPDDR4 Data Byte 0	AB21	B2
LPDDR4_CH0_DQ_A1	LPDDR4 Data Byte 0	AC20	C2
LPDDR4_CH0_DQ_A2	LPDDR4 Data Byte 0	AB15	E2
LPDDR4_CH0_DQ_A3	LPDDR4 Data Byte 0	AC16	F2
LPDDR4_CH0_DQ_A4	LPDDR4 Data Byte 0	AC13	F4
LPDDR4_CH0_DQ_A5	LPDDR4 Data Byte 0	AB14	E4
LPDDR4_CH0_DQ_A6	LPDDR4 Data Byte 0	AB20	C4
LPDDR4_CH0_DQ_A7	LPDDR4 Data Byte 0	AC22	B4
LPDDR4_CH0_DQ_A8	LPDDR4 Data Byte 1	AE22	B11
LPDDR4_CH0_DQ_A9	LPDDR4 Data Byte 1	AD22	C11
LPDDR4_CH0_DQ_A10	LPDDR4 Data Byte 1	AD21	E11
LPDDR4_CH0_DQ_A11	LPDDR4 Data Byte 1	AC14	F11
LPDDR4_CH0_DQ_A12	LPDDR4 Data Byte 1	AD14	F9
LPDDR4_CH0_DQ_A13	LPDDR4 Data Byte 1	AD17	E9
LPDDR4_CH0_DQ_A14	LPDDR4 Data Byte 1	AC17	C9
LPDDR4_CH0_DQ_A15	LPDDR4 Data Byte 1	AD20	B9
LPDDR4_CH0_DQS_T_A0	LPDDR4 Data Byte 0 Data Strobe Pair	AB18	D3
LPDDR4_CH0_DQS_C_A0	LPDDR4 Data Byte 0 Data Strobe Pair	AB17	E3
LPDDR4_CH0_DQS_T_A1	LPDDR4 Data Byte 1 Data Strobe Pair	AD12	D10
LPDDR4_CH0_DQS_C_A1	LPDDR4 Data Byte 1 Data Strobe Pair	AD11	E10
LPDDR4_CH0_DMI_A0	LPDDR4 Data Byte 0 Data Mask	AB12	C3
LPDDR4_CH0_DMI_A1	LPDDR4 Data Byte 1 Data Mask	AC19	C10
LPDDR4_CH0_DQ_B0	LPDDR4 Data Byte 2	AF13	AA2
LPDDR4_CH0_DQ_B1	LPDDR4 Data Byte 2	AG15	Y2
LPDDR4_CH0_DQ_B2	LPDDR4 Data Byte 2	AF18	V2

LPDDR4_CH0_DQ_B3	LPDDR4 Data Byte 2	AG18	U2
LPDDR4_CH0_DQ_B4	LPDDR4 Data Byte 2	AF19	U4
LPDDR4_CH0_DQ_B5	LPDDR4 Data Byte 2	AE19	V4
LPDDR4_CH0_DQ_B6	LPDDR4 Data Byte 2	AF14	Y4
LPDDR4_CH0_DQ_B7	LPDDR4 Data Byte 2	AG13	AA4
LPDDR4_CH0_DQ_B8	LPDDR4 Data Byte 3	AH22	AA11
LPDDR4_CH0_DQ_B9	LPDDR4 Data Byte 3	AG22	Y11
LPDDR4_CH0_DQ_B10	LPDDR4 Data Byte 3	AG21	V11
LPDDR4_CH0_DQ_B11	LPDDR4 Data Byte 3	AH20	U11
LPDDR4_CH0_DQ_B12	LPDDR4 Data Byte 3	AH18	U9
LPDDR4_CH0_DQ_B13	LPDDR4 Data Byte 3	AH17	V9
LPDDR4_CH0_DQ_B14	LPDDR4 Data Byte 3	AH14	Y9
LPDDR4_CH0_DQ_B15	LPDDR4 Data Byte 3	AH15	AA9
LPDDR4_CH0_DQS_T_B0	LPDDR4 Data Byte 2 Data Strobe Pair	AG17	W3
LPDDR4_CH0_DQS_C_B0	LPDDR4 Data Byte 2 Data Strobe Pair	AG16	V3
LPDDR4_CH0_DQS_T_B1	LPDDR4 Data Byte 3 Data Strobe Pair	AG20	W10
LPDDR4_CH0_DQS_C_B1	LPDDR4 Data Byte 3 Data Strobe Pair	AH19	V10
LPDDR4_CH0_DMI_B0	LPDDR4 Data Byte 2 Data Mask	AG12	Y3
LPDDR4_CH0_DMI_B1	LPDDR4 Data Byte 3 Data Mask	AH13	Y10
LPDDR4_CH0_CA_A0	LPDDR4 Address Input	AH12	H2, R2
LPDDR4_CH0_CA_A1	LPDDR4 Address Input	AE17	J2, P2
LPDDR4_CH0_CA_A2	LPDDR4 Address Input	AE14	H9, R9
LPDDR4_CH0_CA_A3	LPDDR4 Address Input	AD19	H10, R10
LPDDR4_CH0_CA_A4	LPDDR4 Address Input	AC11	H11, R11
LPDDR4_CH0_CA_A5	LPDDR4 Address Input	AE13	J11, P11
LPDDR4_CH0_CK_T_A0	LPDDR4 Clock Device 0 Pair	AD16	J8, P8
LPDDR4_CH0_CK_C_A0	LPDDR4 Clock Device 0 Pair	AD15	J9, P9
LPDDR4_CH0_CKE_A0	LPDDR4 Clock Enable Input	AE18	J4, P4
LPDDR4_CH0_CS_A0	LPDDR4 Chip Select Input	AG11	H4, R4

Table 2 – LPDDR4 U23 Connections

Signal Name	Description	Bank 701 SoC Pin	DDR4 Pin U24
LPDDR4_CH1_DQ_A0	LPDDR4 Data Byte 0	AA22	B2
LPDDR4_CH1_DQ_A1	LPDDR4 Data Byte 0	V23	C2
LPDDR4_CH1_DQ_A2	LPDDR4 Data Byte 0	V24	E2
LPDDR4_CH1_DQ_A3	LPDDR4 Data Byte 0	Y23	F2

LPDDR4_CH1_DQ_A4	LPDDR4 Data Byte 0	W25	F4
LPDDR4_CH1_DQ_A5	LPDDR4 Data Byte 0	W24	E4
LPDDR4_CH1_DQ_A6	LPDDR4 Data Byte 0	Y22	C4
LPDDR4_CH1_DQ_A7	LPDDR4 Data Byte 0	AA21	B4
LPDDR4_CH1_DQ_A8	LPDDR4 Data Byte 1	AE24	B11
LPDDR4_CH1_DQ_A9	LPDDR4 Data Byte 1	AG23	C11
LPDDR4_CH1_DQ_A10	LPDDR4 Data Byte 1	AH25	E11
LPDDR4_CH1_DQ_A11	LPDDR4 Data Byte 1	AH23	F11
LPDDR4_CH1_DQ_A12	LPDDR4 Data Byte 1	AH24	F9
LPDDR4_CH1_DQ_A13	LPDDR4 Data Byte 1	AG25	E9
LPDDR4_CH1_DQ_A14	LPDDR4 Data Byte 1	AF25	C9
LPDDR4_CH1_DQ_A15	LPDDR4 Data Byte 1	AD25	B9
LPDDR4_CH1_DQS_T_A0	LPDDR4 Data Byte 0 Data Strobe Pair	Y24	D3
LPDDR4_CH1_DQS_C_A0	LPDDR4 Data Byte 0 Data Strobe Pair	AA23	E3
LPDDR4_CH1_DQS_T_A1	LPDDR4 Data Byte 1 Data Strobe Pair	AF24	D10
LPDDR4_CH1_DQS_C_A1	LPDDR4 Data Byte 1 Data Strobe Pair	AF23	E10
LPDDR4_CH1_DMI_A0	LPDDR4 Data Byte 0 Data Mask	V22	C3
LPDDR4_CH1_DMI_A1	LPDDR4 Data Byte 1 Data Mask	AD24	C10
LPDDR4_CH1_DQ_B0	LPDDR4 Data Byte 2	AG27	AA2
LPDDR4_CH1_DQ_B1	LPDDR4 Data Byte 2	AG28	Y2
LPDDR4_CH1_DQ_B2	LPDDR4 Data Byte 2	AE27	V2
LPDDR4_CH1_DQ_B3	LPDDR4 Data Byte 2	AD26	U2
LPDDR4_CH1_DQ_B4	LPDDR4 Data Byte 2	AE26	U4
LPDDR4_CH1_DQ_B5	LPDDR4 Data Byte 2	AF26	V4
LPDDR4_CH1_DQ_B6	LPDDR4 Data Byte 2	AH27	Y4
LPDDR4_CH1_DQ_B7	LPDDR4 Data Byte 2	AG26	AA4
LPDDR4_CH1_DQ_B8	LPDDR4 Data Byte 3	AB26	AA11
LPDDR4_CH1_DQ_B9	LPDDR4 Data Byte 3	AB28	Y11
LPDDR4_CH1_DQ_B10	LPDDR4 Data Byte 3	V25	V11
LPDDR4_CH1_DQ_B11	LPDDR4 Data Byte 3	W27	U11
LPDDR4_CH1_DQ_B12	LPDDR4 Data Byte 3	W26	U9
LPDDR4_CH1_DQ_B13	LPDDR4 Data Byte 3	AA28	V9
LPDDR4_CH1_DQ_B14	LPDDR4 Data Byte 3	Y26	Y9
LPDDR4_CH1_DQ_B15	LPDDR4 Data Byte 3	AA26	AA9
LPDDR4_CH1_DQS_T_B0	LPDDR4 Data Byte 2 Data Strobe Pair	AC28	W3
LPDDR4_CH1_DQS_C_B0	LPDDR4 Data Byte 2 Data Strobe Pair	AD27	V3
LPDDR4_CH1_DQS_T_B1	LPDDR4 Data Byte 3 Data Strobe Pair	V28	W10

LPDDR4_CH1_DQS_C_B1	LPDDR4 Data Byte 3 Data Strobe Pair	V27	V10
LPDDR4_CH1_DMI_B0	LPDDR4 Data Byte 2 Data Mask	AE28	Y3
LPDDR4_CH1_DMI_B1	LPDDR4 Data Byte 3 Data Mask	Y28	Y10
LPDDR4_CH1_CA_A0	LPDDR4 Address Input	AC27	H2, R2
LPDDR4_CH1_CA_A1	LPDDR4 Address Input	AF28	J2, P2
LPDDR4_CH1_CA_A2	LPDDR4 Address Input	AE23	H9, R9
LPDDR4_CH1_CA_A3	LPDDR4 Address Input	AC25	H10, R10
LPDDR4_CH1_CA_A4	LPDDR4 Address Input	W21	H11, R11
LPDDR4_CH1_CA_A5	LPDDR4 Address Input	AC24	J11, P11
LPDDR4_CH1_CK_T_A0	LPDDR4 Clock Device 0 Pair	AB23	J8, P8
LPDDR4_CH1_CK_C_A0	LPDDR4 Clock Device 0 Pair	AC23	J9, P9
LPDDR4_CH1_CKE_A0	LPDDR4 Clock Enable Input	AB27	J4, P4
LPDDR4_CH1_CS_A0	LPDDR4 Chip Select Input	Y27	H4, R4

Table 3 – LPDDR4 U24 Connections

NOTE: The VE2302 SOM requires the end-user carrier card to provide a **SYSTEM CLOCK** that the LPDDR4 interfaces leverages. This **SYSTEM CLOCK** is provided to the LPDDR4 triplet via the JX1 connector. The **SYSTEM CLOCK** provided by the end-user carrier card should be **200MHz LVDS.** Please refer to the **Clock Sources** section of this document for implementation details of the **SYSTEM CLOCK**.

2.2.2 Octal SPI Flash

The VE2302 SOM features one 8-bit OSPI (octal-SPI) serial NOR flash device. The Micron **MT35XU512ABA1G12-0AAT** OSPI Flash device is used on the VE2302 SOM. The Multi-I/O SPI Flash memory is used to provide non-volatile boot, application code, and data storage. The OSPI Flash can be used as a Boot Device providing 256MB of overall storage and is selectable as the Primary Boot Device via setting the MODE pins appropriately.

The Octal-SPI Flash connects to the PMC OSPI interface via Bank 500. This requires connection to specific pins in MIO Bank 500 and operated at 1.8V I/O, specifically MIO[0:10] and MIO12 as outlined in the **AM011** (Versal™ Adaptive SoC Technical Reference Manual).

NOTE: The OSPI interface can be operated up to 150MHz which may be dependent on the operating mode, the performance of the OSPI controller, and the physical implementation of the design (tested with ES1 silicon). This differs from the available published maximum performance of the OSPI controller which supports performance up to 200MHz. It is important when implementing the OSPI controller interface in the AMD design tools to set the performance of the OSPI controller to 150MHz for ES1 silicon. This is expected to be resolved with production silicon. The intent is that the interface operates at 200MHz.

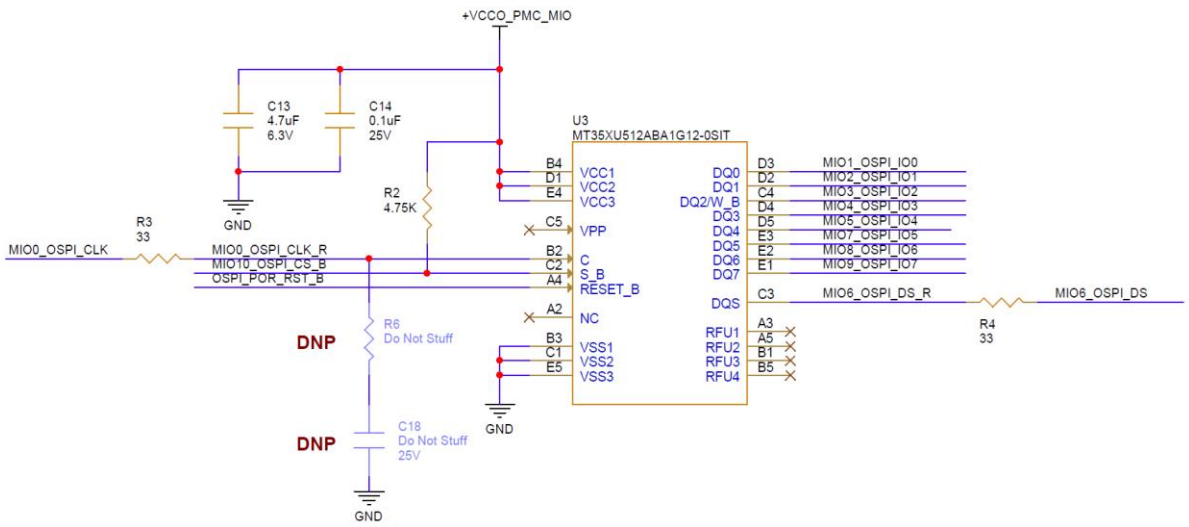

Figure 3 – OSPI Circuit

Signal Name	Description	Bank 500 SoC Pin	MIO	OSPI Pin
MIO0_OSPI_CLK	OSPI Serial Clock	AA1	MIO_0	B2
MIO1_OSPI_IO0	OSPI Data [0]	AB1	MIO_1	D3
MIO2_OSPI_IO1	OSPI Data [1]	AD1	MIO_2	D2
MIO3_OSPI_IO2	OSPI Data [2]	AE1	MIO_3	C4
MIO4_OSPI_IO3	OSPI Data [3]	AF1	MIO_4	D4
MIO5_OSPI_IO4	OSPI Data [4]	AG1	MIO_5	D5
MIO6_OSPI_DS	OSPI Data Strobe	AH2	MIO_6	C3
MIO7_OSPI_IO5	OSPI Data [5]	AG2	MIO_7	E3
MIO8_OSPI_IO6	OSPI Data [6]	AE2	MIO_8	E2
MIO9_OSPI_IO7	OSPI Data [7]	AD2	MIO_9	E1
MIO10_OSPI_CS_B	OSPI Chip Select Input	AC2	MIO_10	C2
MIO12_OSPI_RST_B	OSPI Reset Input	AA3	MIO_12	A4

Table 4 – Octal-SPI Flash Pin Assignment and Definitions

2.2.3 eMMC Flash

The VE2302 SOM provides 32GB of eMMC Flash to be used as a storage device. A single Micron **MTFC32GAZAQHD IT** (153-pin VFBGA package) device is used to implement the eMMC Flash x8 interface. The eMMC device is connected to the PMC MIO bank 501 and operated at 1.8V I/O. The eMMC I/O has direct connections to the XCVE2302 MIO through the PMC MIO[26:27] and PMC_MIO[29:36] pins.

The VE2302 SOM end-user can issue a soft reset, **P0_EMMC1_RST_B**, to the eMMC flash device via an on board two-wire serial interface. The active low reset is assigned to Port 0 of the Onsemi **FXL6408UMX** I/O expander. The I/O expander is attached to an I2C peripheral on the VE2302 device. For further

information on the I/O expander and its connections, please refer to the **I2C 8-Bit I/O Expander** section of this hardware user guide.

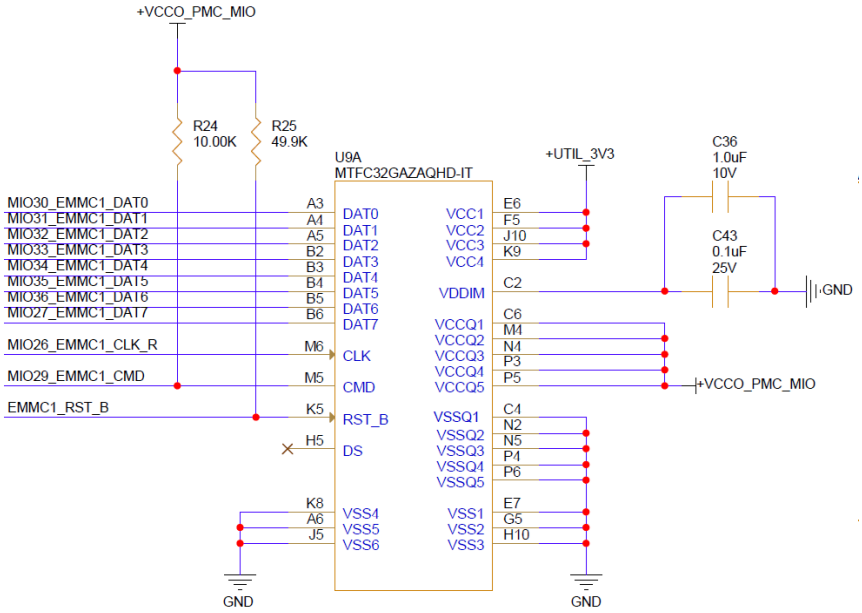

Figure 4 – eMMC Circuit

NOTE: Not shown in eMMC Circuit are pullup resistors on the data lines between the VE2302 device and the eMMC device.

Signal Name	Description	Bank 501 SoC Pin	MIO	OSPI Pin
MIO26_EMMC1_CLK	EMMC Clock	AA5	MIO_26	M6
MIO27_EMMC1_DAT7	EMMC Data IO [7]	AB5	MIO_27	B6
MIO29_EMMC1_CMD	EMMC Command	AD5	MIO_29	M5
MIO30_EMMC1_DAT0	EMMC Data IO [0]	AE6	MIO_30	A3
MIO31_EMMC1_DAT1	EMMC Data IO [1]	AD6	MIO_31	A4
MIO32_EMMC1_DAT2	EMMC Data IO [2]	AB6	MIO_32	A5
MIO33_EMMC1_DAT3	EMMC Data IO [3]	AA6	MIO_33	B2
MIO34_EMMC1_DAT4	EMMC Data IO [4]	AB7	MIO_34	B3
MIO35_EMMC1_DAT5	EMMC Data IO [5]	AC7	MIO_35	B4
MIO36_EMMC1_DAT6	EMMC Data IO [6]	AD7	MIO_36	B5

Table 5 – eMMC Pin Assignment and Definitions

2.2.4 SFVA784 Device Package Delay Compensation for Memory Interfaces

The VE2302 SOM device package delay is accommodated for in the layout of the each of the memory interfaces via adjustments in their signal trace lengths. The average of min and max values for package delay is utilized to compensate for the flight time caused by the delay associated with this package.

2.3 GTYP Transceiver Interface

The VE2302 SOM provides 8 GTYP transceivers along with 4 differential reference clocks that reside on Quad 103 and Quad 104 of the XCVE2302 device. These transceivers can be used to interface to multiple high speed interface protocols. Examples of such interfaces are SFP28 and HDMI 2.1. The listed interfaces have reference circuits provided via the Tria Technologies Versal™ AI Edge Carrier Card. The GTYP interfaces are not limited to those listed here as custom interfaces can be created on an end user carrier card.

The GTYP transceivers in the Versal™ architecture are power-efficient transceivers, supporting line rates from 1.25 Gb/s to 32.75 Gb/s depending on the device speed, temperature, and power grades. By default, the VE2302 SOM is populated with a -1LP device. Please refer to the **AM002** (Versal™ Adaptive SoC GTY and GTYP Transceivers Architecture Manual) for more information on how each GTYP transceiver can be utilized in a design.

Four (4) differential MGT reference clock inputs are available to support the GTYP transceiver lanes. The multi-gigabit transceiver lanes and their associated reference clocks are connected to the end user carrier card via the JX3 connector. The end user carrier card is responsible for sourcing the proper reference clocks to the VE2302 SOM. Please refer to the Versal™ AI Edge Series Data Sheet (**DS958**) for the requirements of these reference clocks. As an example, refer to the Versal™ AI Edge Carrier Card for a solution to providing the GTH reference clocks to the VE2302 SOM.

Each of the VE2302 SOM Quads are length tuned from the XCVE2302 device to the JX3 connector incorporating the device package delays. The device package delay report provided by AMD and the PCB net length report provided by Tria Technologies can be used to determine the required delay for each implemented interface on the end-user carrier card. If the implemented interface is wider than x4 (a single quad), it is imperative to length tune the wider implemented interface on the end user carrier card incorporating each length across the multiple Quads.

NOTE: The GTYP transceiver power rails (**+MGTYPAVCC, +MGTYPVCCAUX, and +MGTYPAVTT**) must be supplied by the carrier card via the JX2 and JX3 connectors. Please refer to the **Power Supplies** section of this document for more information.

The following figure and table show the VE2302 SOM GTYP data and GTYP reference clock input pins available on the JX3 connector.

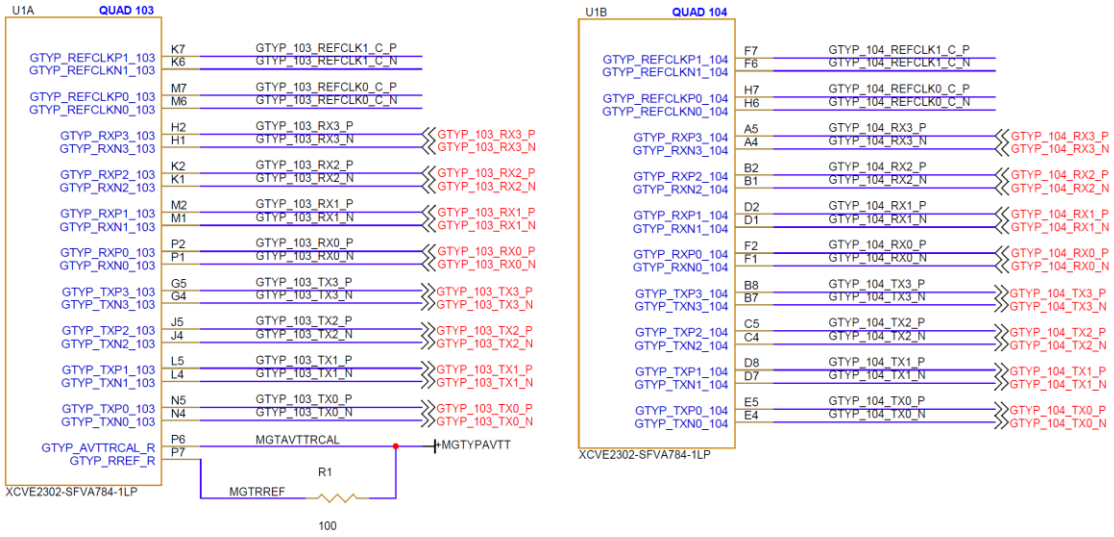

Figure 5 – GTYP Quad 103 and 104 Connections

Signal Name	Pin Number	JX3 Connector
GTYP_104_REFCLK0_P	H7	A7
GTYP_104_REFCLK0_N	H6	A8
GTYP_104_REFCLK1_P	F7	B10
GTYP_104_REFCLK1_N	F6	B11
GTYP_104_TX0_P	E5	B23
GTYP_104_TX0_N	E4	B24
GTYP_104_TX1_P	D8	A14
GTYP_104_TX1_N	D7	A15
GTYP_104_TX2_P	C5	A20
GTYP_104_TX2_N	C4	A21
GTYP_104_TX3_P	B8	B17
GTYP_104_TX3_N	B7	B18
GTYP_104_RX0_P	F2	D23
GTYP_104_RX0_N	F1	D24
GTYP_104_RX1_P	D2	C20
GTYP_104_RX1_N	D1	C21
GTYP_104_RX2_P	B2	D17
GTYP_104_RX2_N	B1	D18
GTYP_104_RX3_P	A5	C14
GTYP_104_RX3_N	A4	C15
GTYP_103_REFCLK0_P	M7	C7
GTYP_103_REFCLK0_N	M6	C8
GTYP_103_REFCLK1_P	K7	D10
GTYP_103_REFCLK1_N	K6	D11
GTYP_103_TX0_P	N5	B35
GTYP_103_TX0_N	N4	B36
GTYP_103_TX1_P	L5	A32
GTYP_103_TX1_N	L4	A33
GTYP_103_TX2_P	J5	B29
GTYP_103_TX2_N	J4	B30
GTYP_103_TX3_P	G5	A26
GTYP_103_TX3_N	G4	A27
GTYP_103_RX0_P	P2	D35
GTYP_103_RX0_N	P1	D36
GTYP_103_RX1_P	M2	C32
GTYP_103_RX1_N	M1	C33

GTYP_103_RX2_P	K2	D29
GTYP_103_RX2_N	K1	D30
GTYP_103_RX3_P	H2	C26
GTYP_103_RX3_N	H1	C27

Table 6 – Quad 103 and 104 GTYP Pin Assignments

2.3.1 SFVA784 Device Package Delay Compensation for GTYP Transceiver Interfaces

The VE2302 SOM device package delay is accommodated for in the layout of the each of the GTYP transceiver signal trace lengths. The average of min and max values for package delay is utilized to compensate for the flight time caused by the delay associated with this package.

2.4 USB 2.0 PHY

The AMD Versal™ AI Edge device contains a hardened PMC USB 2.0 controller. The VE2302 SOM takes advantage of the PMC USB 2.0 controller to provide USB 2.0 On-The-Go signaling to the JX1 connector.

An external PHY with an 8-bit ULPI interface is implemented. A Microchip **USB3321C** Standalone USB Transceiver Chip is used as the PHY. The PHY features a complete HS-USB Physical Front End supporting speeds of up to 480Mbs. VDDIO for this device can be 1.8V or 3.3V, and on the VE2302 SOM VDDIO is powered at 1.8V. The PHY is connected to PMC MIO Bank 500 which is also powered at 1.8V. This is critical since a level translator cannot be used as it would impact the ULPI timing between the PHY and the XCVE2302 SoC device.

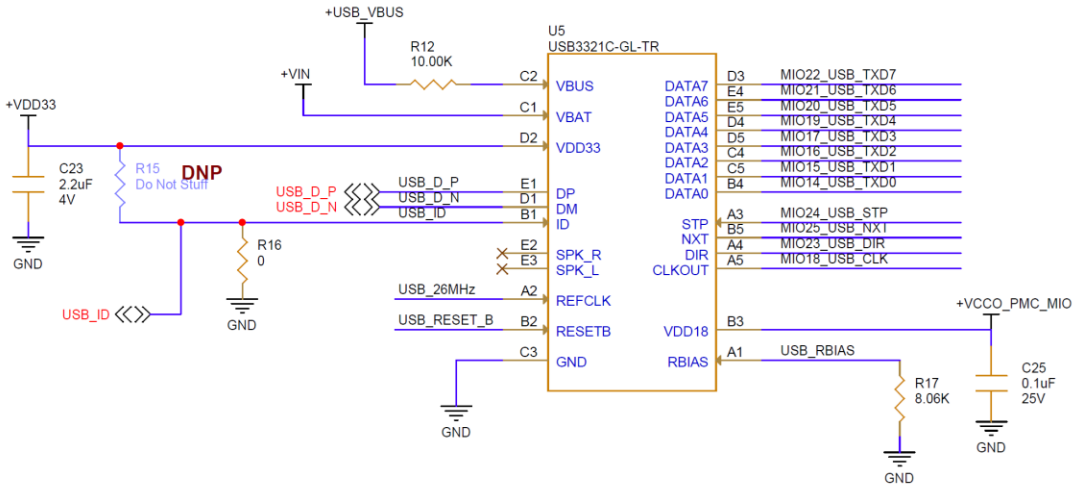

Figure 6 – USB2.0 Circuit

Additionally, the USB3321C must clock the ULPI interface which requires a 26 MHz crystal or oscillator (configured as ULPI Output Clock Mode). On the VE2302 SOM, the 26 MHz oscillator is an ECS CMOS oscillator, **ECS-2016MV-260-BN-TR**.

The physical USB connector is not populated on the VE2302 SOM. The SOM is designed to have the physical USB connector reside on the end-user carrier card. The three USB connector signals (**USB_D_P**,

USB_D_N and **USB_ID**) and **USB_VBUS** are connected to the JX1 Micro Header. The table below shows the connections of these signals at JX1.

Signal Name	JX1 Pin
USB_D_P	D29
USB_D_N	D30
USB_ID	B30
+USB_VBUS	D12

Table 7 – USB2.0 PHY JX1 Pin Assignments

The USB peripheral is connected through PMC MIO [13-25] in MIO Bank 500 and operated at 1.8V. The USB Reset signal is active-low and signal is connected to PMC MIO[13] to soft reset the USB 2.0 ULPI PHY.

Signal Name	Description	SoC Bank	MIO	OSPI Pin
DATA[7:0]	USB Data lines	MIO Bank 500	14:17,19:22	D[7:0]
CLKOUT	USB Clock	MIO Bank 500	18	A5
DIR	ULPI DIR output signal	MIO Bank 500	23	A4
STP	ULPI STP input signal	MIO Bank 500	24	A3
NXP	ULPI NXT output signal	MIO Bank 500	25	B5
DP	DP pin of USB Connector	N/C	N/C	E1
DM	DM pin of USB Connector	N/C	N/C	D1
ID	ID pin of the USB connector	N/C	N/C	B1
RESET_B	Soft Active-Low Reset	MIO Bank 500	13	B2

Table 8 – ULPI Pin Assignment and Definitions

2.4.1 SFVA784 Device Package Delay Compensation for USB2.0 Interfaces

The VE2302 SOM device package delay is accommodated for in the layout of the USB2.0 signal trace lengths. The average of min and max values for package delay is utilized to compensate for the flight time caused by the delay associated with this package.

2.5 Ethernet PHY

The VE2302 SOM provides a single Gigabit Ethernet PHY interface using the Microchip **KSZ9131RNXI** RGMII PHY device in 48-pin QFN package (in industrial temp). The VE2302 SOM takes advantage of an LPD GEM controller to provide RGMII Ethernet signaling from Bank 502 to the Gigabit Ethernet PHY. The Gigabit Ethernet PHY physical side (connected to the JX1 connector) along with an RJ45 connector located on an end-user carrier card will be used to implement the Gigabit Ethernet port.

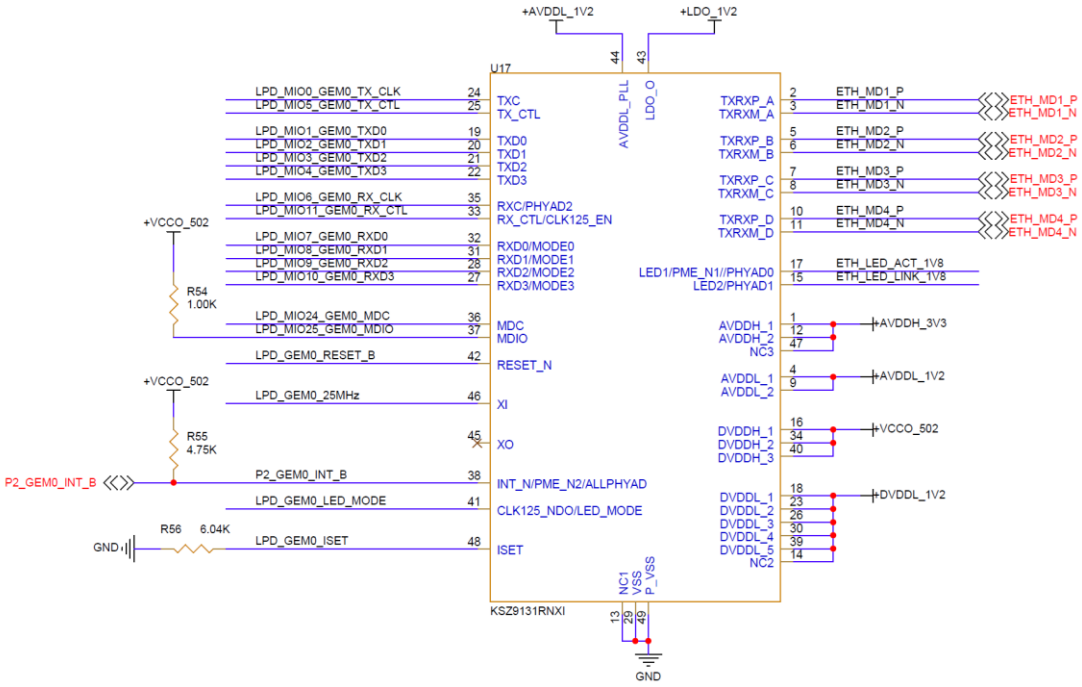

Figure 7 – Ethernet PHY Circuit

The Microchip **KSZ9131RNXI** RGMII Ethernet PHY host side I/O is connected to the LPD MIO bank 502 and operated at 1.8V on the VE2302 SOM. GPIO Port 1 of the I2C 8-bit I/O expander can be used to soft reset the Gigabit Ethernet PHY while P2 port of this I/O expander will be used for the Gigabit Ethernet PHY Interrupt (INT) output. Please refer to the **I2C 8-Bit I/O Expander** section of this document for more information.

The physical RJ45 connector and magnetics are not populated on the VE2302 SOM. The SOM is designed to have the physical RJ45 connector and magnetics reside on the end-user carrier card. The RJ45 connector signals are connected to the JX1 Micro Header. The table below shows the connections of these signals to the JX1 Micro Header:

Signal Name	JX1 Pin
ETH_MD1_P	D32
ETH_MD1_N	D33
ETH_MD2_P	C32
ETH_MD2_N	C33
ETH_MD3_P	B32
ETH_MD3_N	B33
ETH_MD4_P	A32
ETH_MD4_N	A33
ETH_ACT	A29
ETH_LINK	A30

Table 9 – Ethernet PHY JX1 Pin Assignments

On board an end-user carrier card or within the RJ45 Ethernet Jack on the end-user carrier card could be two Ethernet PHY controlled LEDs. The VE2302 SOM provides LINK SPEED and ACTIVITY signals to the on-board RJ45 Ethernet Jack through an OPEN-DRAIN circuit. When implementing these as LEDs on an end-user carrier card the signals should be pulled up to the appropriate voltage such that it will be enough to illuminate the LEDs in an RJ45 jack or other on-board LED circuitry.

The following table shows the pin assignments to Bank 502 of the XCVE2302 device for the RGMII signals.

Signal Name	SoC Pin
LPD_MIO25_GEM0_MDIO	Y9
LPD_MIO24_GEM0_MDC	Y8
LPD_MIO11_GEM0_RX_CTL	Y3
LPD_MIO10_GEM0_RXD3	V3
LPD_MIO9_GEM0_RXD2	U3
LPD_MIO8_GEM0_RXD1	T3
LPD_MIO7_GEM0_RXD0	U2
LPD_MIO6_GEM0_RX_CLK	V2
LPD_MIO5_GEM0_TX_CTL	W2
LPD_MIO4_GEM0_TXD3	Y2
LPD_MIO3_GEM0_TXD2	Y1
LPD_MIO2_GEM0_TXD1	W1
LPD_MIO1_GEM0_TXD0	U1
LPD_MIO0_GEM0_TX_CLK	T1
P1_GEM0_RST_B	N/C

Table 10 – Ethernet RGMII Pin Assignments

2.5.1 SFVA784 Device Package Delay Compensation for Ethernet Interface

The VE2302 SOM device package delay is accommodated for in the layout of the Ethernet PHY signal trace lengths. The average of min and max values for package delay is utilized to compensate for the flight time caused by the delay associated with this package.

2.6 I2C 8-Bit I/O Expander

The VE2302 SOM uses a ONSemi **FXL6408UMX** (16-pin UMLP) I2C Low-Power I/O Expander for generating various resets and control signals on the VE2302 SOM. The I2C 8-bit I/O expander device is connected to the PMC I2C bus (PMC bank 501 MIO[50:51]) and operated at 1.8V. The interrupt output (**INT_B**) of the I2C I/O expander device is connected to the PMC_MIO[11] (Bank 500). The reset input (**RST_B**) of the I2C I/O expander device has soft reset capabilities and is connected to PMC MIO[28] (Bank 501).

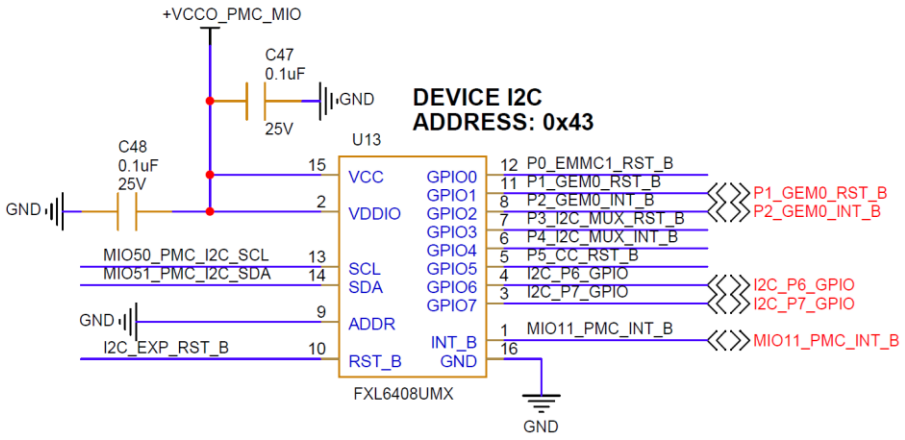

Figure 8 – I2C I/O Expander Circuit

IO Name	TRM Signal Name	Net Name
SCL	SCL_OUT	MIO50_PMC_I2C_SCL
SDA	SDA_OUT	MIO51_PMC_I2C_SDA

Table 11 – I2C TRM Pin Mapping

The following tables describes the connections and functionality of the ports of the I2C I/O Expander.

I/O Expander Name	I/O Expander Pin	Function	Net Name
INT_B	1	INTERRUPT	MIO11_PMC_INT_B
VDDIO	2	VOLTAGE REF	+VCCO_PMC_MIO
GPIO7	3	P-PORT	I2C_P7_GPIO
GPIO6	4	P-PORT	I2C_P6_GPIO
GPIO5	5	P-PORT	P5_CC_RST_B
GPIO4	6	P-PORT	P4_I2C_MUX_INT_B
GPIO3	7	P-PORT	P3_I2C_MUX_RST_B
GPIO2	8	P-PORT	P2_GEM0_INT_B
ADDR	9	ADDRESS	GND
RST_B	10	RESET	MIO28_I2C_EXP_RST_B
GPIO1	11	P-PORT	P1_GEM0_RST_B
GPIO0	12	P-PORT	P0_EMMC1_RST_B
SCL	13	SERIAL CLOCK	MIO50_PMC_I2C_SCL
SDA	14	SERIAL DATA	MIO51_PMC_I2C_SDA
VCC	15	POWER	+VCCO_PMC_MIO
GND	16	GROUND	GND

Table 12 – ONSemi FXL6408UMX Pin Mapping

NOTE: On power-up all I/O expander ports default to inputs. With the on-board pull-ups on all ports, all output reset signals shown in the following table will be in their inactive state.

IO Name	Function	Direction	Active-State	Net Name
GPIO0	eMMC soft reset	OUTPUT	LOW	P0_EMMC1_RST_B
GPIO1	Gigabit Ethernet PHY soft reset	OUTPUT	LOW	P1_GEM0_RST_B
GPIO2	Gigabit Ethernet PHY Interrupt	INPUT	LOW	P2_GEM0_INT_B
GPIO3	2-Ch I2C Switch/Mux Reset	OUTPUT	LOW	P3_I2C_MUX_RST_B
GPIO4	2-Ch I2C Switch/Mux Interrupt	INPUT	LOW	P4_I2C_MUX_INT_B
GPIO5	Carrier Card Reset	OUTPUT	LOW	P5_CC_RST_B
GPIO6	General Purpose IO – Port 6 (JX)	OUTPUT	LOW	I2C_P6_GPIO
GPIO7	General Purpose IO – Port 7 (JX)	OUTPUT	LOW	I2C_P7_GPIO

Table 13 – IO Expander Pin Functions and Definitions

The following figure describes the addressing required to access the I2C I/O Expander. Please see the appropriate device datasheet for further details regarding accessing this device for read and write transactions.

Name	ADDR Pin	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Device Address	ADDR = 0	1	0	0	0	0	1	1	WR
	ADDR = 1	1	0	0	0	1	0	0	WR

Figure 9 – I2C I/O Expander Addressing

2.6.1 Carrier Card I2C Expander GPIO Pins

The I2C I/O expander provide 2 GP (General Purpose) I/O pins for use on end-user carrier cards. These I2C driven general purpose pins are routed to the JX1 connector and can be used to implement any interface that does not demand high performance. These GPIO ports are open-drain and require pull-ups be implemented on the end-user carrier card. Please refer to the **FXL6408UMX** device datasheet for the supported voltages on the GPIO ports of the I2C I/O expander.

The following table shows the carrier card I2C expander GPIO pins available on the JX1 connector.

Signal Name	JX1 Pin Number
I2C_P6_GPIO	C18
I2C_P7_GPIO	C19

Table 14 – IO Expander GPIO PIN Assignments

2.7 2-Channel I2C Switch

The VE2302 SOM uses an NXP **PCA9543APW,118** (14-pin TSSOP) I2C Bus Switch with Interrupt connected on the PMC I2C bus (PS bank 501 MIO[50:51]). The use of this I2C switch provides isolation so that devices connected to the I2C bus on the VE2302 SOM, the I2C slave devices on an end-user carrier card, as well as end-user carrier card voltage regulators connected to the PMBus I2C are not physically placed on the same I2C bus.

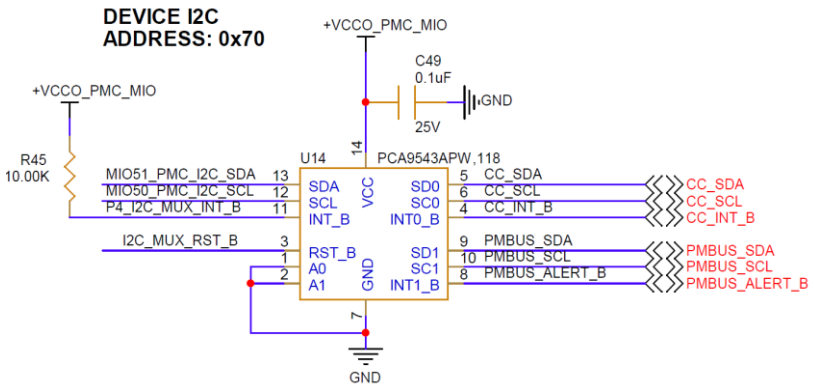

Figure 10 – 2 Channel I2C Switch Circuit

The following table shows the connections to the **PCA9543A** device.

IO Name	TRM Signal Name	Net Name
SCL	SCL_OUT	MIO50_PMC_I2C_SCL
SDA	SDA_OUT	MIO51_PMC_I2C_SDA

Table 15 – I2C TRM Pin Mapping

The **PCA9543A** may also be used for voltage translation, allowing the use of different bus voltages on each SD/SC pair such that 1.8V, 2.5V, or 3.3V devices can communicate with the 1.8V PMC I2C bus. This is achieved by using external pull-up resistors to pull the isolated bus up to the desired voltage for the master and each slave channel. To support the differing voltage levels, the **PCA9543A** VCC is connected to a 2.5V voltage rail. Please refer to the **PCA9543A** datasheet for more information.

I/O Expander Name	I/O Expander Pin	Function	Net Name
A0	1	ADDRESS	GND
A1	2	ADDRESS	GND
RST_B	3	RESET	P3_I2C_MUX_RST_B
INT0_B	4	INTERRUPT0	CC_INT_B
SD0	5	SERIAL DATA0	CC_SDA
SC0	6	SERIAL CLOCK0	CC_SCL
GND	7	GROUND	GND
INT1_B	8	INTERRUPT1	PMBUS_ALERT_B
SD1	9	SERIAL DATA1	PMBUS_SDA
SC1	10	SERIAL CLOCK1	PMBUS_SCL
INT_B	11	INTERRUPT	P4_I2C_MUX_INT_B
SCL	12	SERIAL CLOCK	MIO50_PMC_I2C_SCL
SDA	13	SERIAL DATA	MIO51_PMC_I2C_SDA
VCC	14	POWER	+UTIL_2.5V

Table 16 – ONSemi PCA9543A Pin Mapping

NOTE: GPIO3 port of the I2C 8-bit I/O expander can be used to soft reset the 2-channel I2C switch device. The following table shows how each **PCA9543A** channel will be used. SC1/SD1 should have inline jumpers implemented on an end-user carrier card to allow the PMBUS interface from the VE2302 SOM to be isolated from the circuit preventing multiple master bus contention in the case where an end-user may use an I2C dongle and third-party software to program and / or access the PMBUS regulators in-circuit. Please review the hardware user guide for the Versal™ AI Edge Carrier Card for an example implementation.

I2C Switch Channel	Usage	Note
Master Channel (SDA/SCL/INT)	This channel is connected to the PMC I2C port, MIO [51:50] and operated at 1.8V. The master **INT_N** output is connected to the P4 GPIO port of the I2C 8-bit I/O expander.	Pulled-up to 1.8V On the SOM
Slave Channel 0 (SD0/SC0/INT0)	This channel is connected to the JX1 connector (**CC_SDA**, **CC_SCL**, and **CC_INT_N** signals) to allow slave I2C devices on an end-user carrier card to be virtually placed on the same PMC I2C bus (MIO [51:50]) as the I2C devices on the VE2302 SOM so that software can use a single PMC I2C bus to communicate will I2C devices through-out the system. Please refer to the **Carrier Card I2C Interface** section of this document for more information.	Pulled-up to 1.8V, 2.5V, or 3.3V On the Carrier Card
Slave Channel 1 (SD1/SC1/INT1)	This channel is connected to JX1 connector (**PMBUS_SDA** and **PMBUS_SCL** signals) used to control all PMBus voltage regulators on end-user carrier cards. This feature allows the PMC I2C to control/monitor the PMBus voltage regulators used on end-user carrier cards for the purpose of power management and/or measurement. Please refer to the **PMBus Interface** section of this document for more information.	Pulled-up to 1.8V, 2.5V, or 3.3V On the Carrier Card

Table 17 – I2C Switch Channel Usage

The following figure describes the addressing required to access the I2C Switch. Please see the appropriate device datasheet for further details regarding accessing this device for read and write transactions.

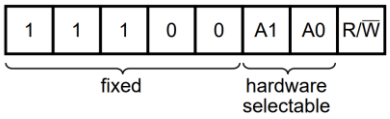

Figure 11 – I2C Switch Addressing

2.7.1 Carrier Card I2C Interface

The VE2302 SOM provides a master two-wire serial bus (**CC_SDA**, **CC_SCL**, and **CC_INT_B**) to the end-user carrier card via the JX1 connector so that software can communicate with all I2C devices on the VE2302 SOM as well as the slave I2C devices on the end-user carrier card using a single two-wire serial interface.

The end-user carrier card two-wire serial interface is connected to channel 0 of the 2-channel I2C switch. End-user carrier cards can drive the **INT0_B** of the channel 0 via **C_INT_B**, if they so desire. The **CC_INT_B** (an active low signal) is not specific to the I2C interface and can be used as a general-purpose interrupt from end-user carrier cards to the VE2302 SOM. If not used, the **CC_INT_B** signal is to be pulled up to 1.8V, 2.5V, or 3.3V on the carrier card. Since the channel 0 I2C bus is dedicated to the end-user carrier card, two-wire serial devices with any address can reside on this bus without conflicting with the I2C devices on the VE2302 SOM.

Switch Pin Name	Switch Pin	Function	Net Name	JX1 Connector
INT0_B	4	INTERRUPT0	CC_INT_B	JX1.A25
SD0	5	SERIAL DATA0	CC_SDA	JX1.C29
SC0	6	SERIAL CLOCK0	CC_SCL	JX1.B25

Table 18 – Carrier Card I2C Net Mapping

2.7.2 PMBUS Interface

A PMBus can be used with the VE2302 SOM to program/control/monitor all on-board PMBus voltage regulators on an end-user carrier card. The VE2302 SOM has access to the end-user carrier card PMBus signals via the JX1 connector (**PMBUS_SDA**, **PMBUS_SCL**, and **PMBUS_ALERT_B** signals).

After the initial programming of all PMBus voltage regulators, the VE2302 SOM can utilize the PMBus (via channel 1 and interrupt1 of the I2C switch) to control/monitor the PMBus voltage regulators on the end-user carrier card for the purpose of power management and/or measurement.

PMBUS Name	JX1 Connector
PMBUS_SDA	JX1.B28
PMBUS_SCL	JX1.C30
PMBUS_ALERT_B	JX1.A26

Table 19 – PMBUS JX1 Connector Mapping

Please review the hardware user guide for the Versal™ AI Edge Carrier Card for an example implementation of the PMBus.

2.8 I2C MAC EEPROM

The VE2302 SOM uses a Microchip **AT24MAC402-MAHM** (8-pin UDFN package) I2C EEPROM 2Kbit 1MHz device. The EEPROM device is connected to the PMC I2C bus (PS bank 501 MIO[50:51]) and operated 1.8V. This device contains a unique EUI-48 ethernet MAC address for solutions that utilize the on-board ethernet and it can be used to store system level parameters/data.

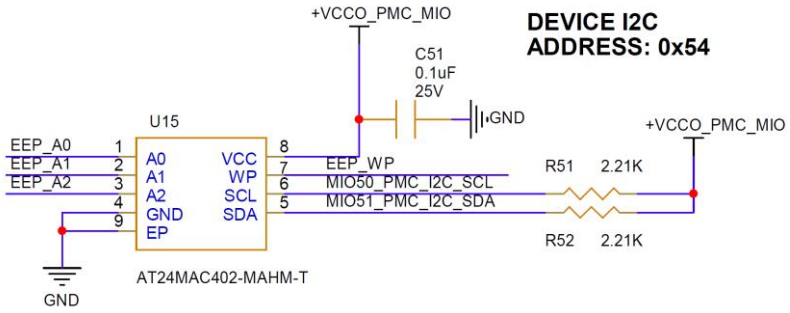

Figure 12 – I2C EEPROM Circuit

IO Name	TRM Signal Name	Net Name
PS_MIO50	SCL_OUT	MIO50_PMC_I2C_SCL
PS_MIO51	SDA_OUT	MIO51_PMC_I2C_SDA

Table 20 – I2C TRM Pin Mapping

The following table describes the connections to the I2C EEPROM.

EEPROM Name	EEPROM Pin	Function	Net Name
A0	1	ADDRESS INPUT	GND
A1	2	ADDRESS INPUT	GND
A2	3	ADDRESS INPUT	+VCCO_PMC_MIO
GND	4	GROUND	GND
SDA	5	SERIAL ADDR/DATA	MIO51_PMC_I2C_SDA
SCL	6	SERIAL CLOCK	MIO50_PMC_I2C_SCL
WP	7	WRITE PROTECT	GND
VCC	8	POWER	+VCCO_PMC_MIO

Table 21 – Microchip AT24MAC402 Pin Mapping

The following figure describes the addressing required to access the I2C EEPROM. Please see the appropriate device datasheet for further details regarding transactions to and from this device.

Access Area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEPROM	1	0	1	0	A2	A1	A0	R/$\overline{W}$
EUI or Serial Number Read	1	0	1	1	A2	A1	A0	1
Write-Protect Registers	0	1	1	0	A2	A1	A0	R/$\overline{W}$

Figure 13 – EEPROM I2C Addressing

2.9 User IO Pins

2.9.1 Processor MIO User Pins

The VE2302 SOM provides 13 end-user PMC MIO pins directly from Bank 501 and 12 end-user LPD MIO pins from Bank 502 to the JX1 Connector. The 25 MIO pins connect to the Adaptive SoC Processor Sub-System for the implementation of peripherals such as USB, SPI, SDIO, CAN, UART, and I2C. These I/O pins can also be used as general purpose I/O to connect push buttons, LEDs and/or switches to the VE2302 SOM from an end-user carrier card.

The VCCO for Bank 501 and Bank 502 is generated on the VE2302 SOM and set to +1.8V and is names **+VCCO_PMC_MIO**. This voltage rail is also provided on the JX1 connector pin A24 so that it may be utilized on circuits associated with the MIO pins on an end-user carrier card.

NOTE: The Bank 501 PMC MIO and Bank 502 LPD MIO connections to the JX1 connector are provided in a master table that documents all the JX Connections of the VE2302 SOM. Please refer to the **Expansion Headers** section of this document.

2.9.2 Programmable Logic IO User Pins

The VE2302 SOM provides 22 user HDIO pins from Bank 302, 28 user XPIO pins from bank 702 and 52 user XPIO pins from Bank 703 of the Versal™ Adaptive SoC. The 102 PL IO pins on the VE2302 SOM connect to the Programmable Logic Sub-System for user implementation of most any feasible interface.

Bank 302 provides 22 user HDIO (High Density) pins. These pins are routed to the JX1 connector and are available to implement peripherals on end-user custom carrier cards. The HDIO bank 302 pins can be operated between 1.8V and 3.3V. The bank voltage **+VCCO_302** is to be provided by the end-user carrier card via the JX1 connector. Please refer to the **Expansion Headers** section of this document for the location of the **+VCCO_302** pins on the JX1 connector. Please refer to **Power Supplies** section of this document for the power/sequencing requirements for bank 302 power rail.

The bank 302 HDIO pins are routed with matched lengths to the JX1 connectors. The matched pairs may be used as either single ended I/O or differential pairs depending on the end users design requirements. See the **VE2302 SOM Net Length** report for more details on the matched lengths to the JX1 connector.

Banks 702 and 703 provide 80 XPIO (High Performance) pins. These pins are routed to the JX2 connector and are available to implement peripherals on end-user custom carrier cards. The XPIO bank 702 and 703 pins can be operated between 1.0 to 1.5V. The bank voltages +**VCCO_702** and +**VCCO_703** are to be provided by the end-user custom carrier card via the JX2 connector. Please refer to the **Expansion Headers** section of this document for the location of the **+VCCO_702** and **+VCCO_703** pins on the JX2 connector. Please refer to **Power Supplies** section of this document for the power/sequencing requirements for the bank 702 and bank 703 power rails.

The bank 702 and bank 703 XPIO pins are routed with matched lengths to the JX2 connectors. The matched lengths differ here from bank 302 as the matching of lengths are done by AMD nibbles which are 6-pins. Each nibble within bank 702 and bank 703 is length matched. The matched pairs may be used as either single ended I/O or differential pairs depending on the end users design requirements. See the **VE2302 SOM Net Length** report for more details on the matched lengths to the JX2 connector.

It is recommended that any custom interface to be designed and run through the Vivado tool suite for a sanity check on place and route and timing closure in advance of end-user carrier card manufacturing.

NOTE: The bank 302 HDIO and bank 702 and 703 XPIO connections to the JX connectors are provided in a master table that documents all the JX Connections of the VE2302 SOM. Please refer to the **Expansion Headers** section of this document.

2.9.3 SFVA784 Device Package Delay Compensation for User I/O Interfaces

The VE2302 SOM device package delay is accommodated for in the layout of the User I/O interface signal trace lengths. The average of min and max values for package delay is utilized to compensate for the flight time caused by the delay associated with this package.

2.10 Clock Sources

The VE2302 SOM provides a 33.333MHz +/-10ppm single-ended 1.8V reference clock source to the PMC configuration Bank 503 **REF_CLK** input to act as a system reference clock. An **ECS-2520SMV-333.3-FN-TR** with 33-ohm series termination is used.

The VE2302 SOM can provide a Real-Time Clock (RTC). A 32.768 kHz crystal is connected to the PMC Configuration Bank 503 **RTC_PADI** and **RTC_PADO** pins for the RTC. The on-chip RTC uses the **+VCC_BATT** pin (provided by the end-user carrier card via the JX1 connector) for the backup battery. End user carrier cards will drive the **+VCC_BATT** pin with an appropriate battery if this functionality is required.

MIO Name	Package Pin Number	Net Name	JX1 Connector
RTC_PADI	AH7	RTC_PADI	-
RTC_PADO	AH8	RTC_PADO	-
VCC_BATT	W15	+VCC_BATT	JX1.D27

Table 22 – RTC Crystal Pin Assignments

The VE2302 SOM requires the end-user carrier card to provide a **SYSTEM CLOCK** that the LPDDR4 interfaces leverages. This **SYSTEM CLOCK** is provided to the LPDDR4 triplet via the JX1 connector. The **SYSTEM CLOCK** provided by the end-user carrier card should be **200MHz LVDS.** An example of the **SYSTEM CLOCK** is provided by the Versal™ AI Edge Carrier Card. Please refer to the **Versal™ AI Edge Carrier Card Hardware User Guide** for the example implementation of SYSTEM CLOCK.

Net Name	Package Pin Number	JX1 Connector
SYSCLK_P	Bank 702 – N23	JX1.D14
SYSCLK_N	Bank 702 – N24	JX1.D15

Table 23 – LPDDR4 System Clock Pin Assignments

The VE2302 SOM does provide termination for the SYSTEM CLOCK differential pair. The following figure shows the termination provided on the VE2302 SOM.

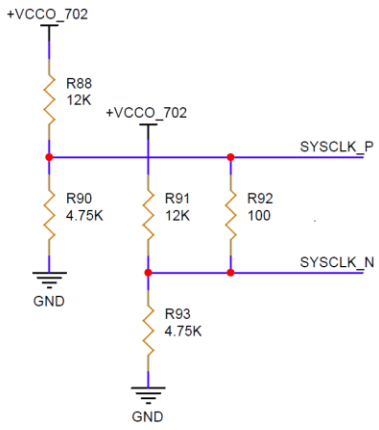

Figure 14 – SYSCLK Provided Termination

2.11 Control Signal Sources

2.11.1 Power-On Reset (POR) Control Signal

The Power-On Reset (**POR_B**) circuit for the AMD Versal™ AI Edge device is required to be implemented on the end-user carrier card. The **POR_B** is an active-low input signal to the AMD Versal™ AI Edge device that acts as a master reset. The signal name associated with **POR_B** port on the AMD Versal™ AI Edge device is **SOM_RESET_IN_B** and that signal is provided on the JX2 connector (**Pin JX2-B32**). The VE2302 SOM does provided a 10K-ohm pull-up to +VCCO_PMC_MIO (1.8V) on **SOM_RESET_IN_B**. See the **Versal™ AI Edge Carrier Card Hardware User Guide** for an example implementation of SOM_RESET_IN_B control.

The external reset, **SOM_RESET_IN_B**, can reset the end-user carrier card thru an open drain signal on the JX2 connector, **CC_RESET_OUT_B**. The VE2302 SOM is also capable of issuing a soft reset by asserting Port 5 of the I2C I/O Expander, **P5_CC_RST_B**, to the end-user carrier card using the VE2302 SOM two-wire serial interface. This will soft reset the end-user carrier card thru the same open drain signal on the JX2 connector (**Pin JX2-C14**), **CC_RESET_OUT_B**. See the **I2C 8-bit I/O Expander** section of this document for details regarding Port 5 of the I2C I/O Expander.

The following table is a list of the locations on the JX2 connecter of the power-on reset control signals.

Control Signal Name	JX2 Connector	Voltage	Active-State
SOM_RESET_IN_B	JX2-B32	+1.8V (SOM)	Low
CC_RESET_OUT_B	JX2-C14	Open-Drain to User	Low

Table 24 – Power-On Reset Control Pin Assignments

2.11.2 Power Supply Sequencing Control Signals

An end-user carrier card should design the on-board power solution to account for the bring up time of the individual power supplies and devise a method to ensure that power is valid prior to the release of **POR_B** control signal and the booting of the AMD Versal™ AI Edge device. The end-user carrier card is required to use the **SOM_PWR_ENB_IN, VCCO_702_ENB_OUT, VCCO_702_PG_IN,** and **SOM_PG_OUT** signals to control the bring-up and sequencing of the on-board power supplies. System overall power good should meet the time required for all power rails to be stable listed in the Versal™ AI Edge datasheet (**DS958**).

SOM_PWR_ENB_IN is the control signal used to enable the **POWER SEQUENCER** on the VE2302 SOM. This signal is required to be pulled up to +3.3V on the end-user carrier card. On the Versal™ AI Edge Carrier Card, this signal is enabled after the always-on regulators are stable which includes the VE2302 SOM +VIN rail of +5V.

VCCO_702_ENB_OUT is a control signal pulled up to +3.3V that is generated by the **POWER SEQUENCER** which informs the end user carrier card to enable the voltage regulator used to generate **+VCCO_702**. This is used to maintain the proper sequencing for the AMD Versal™ AI Edge device.

When the power for **+VCCO_702** is stable, the end user carrier card should assert **VCCO_702_PG_IN** back to the VE2302 SOM. This signal is required to be pulled up to +3.3V on the end-user carrier card.

When the power supplies on the VE2302 SOM are stable the **SOM_PG_OUT** will be asserted to +3.3V to the end-user carrier so that the remaining power supplies on that platform can be brought up in the proper sequence.

More details regarding the use of the power control signals listed here are provided in the **Power Supplies** section of this document. Please also refer to the **Versal™ AI Edge Carrier Card Hardware User Guide** and the **Versal™ AI Carrier Card Design Guide** for details regarding the implementation of the proper system power sequencing.

The following table is a list of the locations on the JX connecters of the power supply sequencing control signals.

Control Signal Name	JX2 Connector	Voltage	Active-State
SOM_PWR_ENB_IN	JX2-C32	+3.3V (Carrier)	High
VCCO_702_ENB_OUT	JX2-C8	+3.3V (SOM)	High
VCCO_702_PG_IN	JX2-D8	+3.3V (Carrier)	High
SOM_PG_OUT	JX1-B29	+3.3V (SOM)	High

Table 25 – Power Supply Sequencing Control Pin Assignments

2.11.3 PUDC_B Control Signal and Status Signals

PUDC_B by default has a pull-up resistor to the appropriate voltages applied. The **PUDC_B** does have a footprint available such that you can remove the pull-up and populated the secondary resistor and pull the **PUDC_B** signal to GND. **PUDC_B** is the pull-up during configuration pin that is used to select the behavior of the XPIO/HDIO during configuration. The default setting on the VE2302 SOM is HIGH, which means the XPIO and HDIO are put into tri-state mode. If **PUDC_B** is LOW then internal pull-ups would be enabled on the XPIO and HDIO during configuration.

DONE and **ERROR OUT** are configuration status signals from the AMD Versal™ AI Edge device bank 503. The **DONE** signal is a bidirectional pin that is an open-drain signal with a weak internal pull-up resistor. **DONE** is tri-stated and pulled HIGH when the BOOT sequence is complete. The **ERROR_OUT** signal is an output pin that is an open-drain signal with a weak internal pull-up resistor. **ERROR_OUT** is tri-stated and pulled HIGH when an error occurs in the AMD Versal™ AI Edge device. The end user carrier card can use these status signals to illuminate on-board LEDs to show BOOT sequence complete or that an error occurred. Please refer to the **Versal™ AI Edge Carrier Card Hardware User Guide** for details regarding the implementation of these status signals.

The following table is a list of the locations on the JX1 connecter of the bank 503 configuration status signals.

Control Signal Name	JX1 Connector	Voltage	Active-State
DONE	JX1-D28	Open-Drain (Carrier)	High
ERROR_OUT	JX1-D13	Open-Drain (Carrier)	High

Table 26 – Configuration Status Signal Pin Assignments

2.11.4 On-Board Peripheral Reset Control

The VE2302 SOM provides resets control signals to the various peripherals on the SOM via PMC MIO pins or through the I2C 8-bit I/O expander. All reset controls signals are active-LOW. The reset operation for the peripherals connected to the VE2302 SOM are as follows:

- **OPSI** – This device is reset via **POR_B** or the **PMC MIO[12]** signal.
- **USB 2.0 ULPI PHY** – This device is reset via **POR_B** or the **PMC MIO[13]** signal.
- **I2C 8-Bit I/O Expander** – This device is reset via **POR_B** or the **PMC MIO[28]** signal.
- **eMMC Device** – This device is reset via **POR_B** or **GPIO0** port of the I2C 8-bit I/O expander.
- **Gigabit Ethernet PHY** – This device is reset via **POR_B** or **GPIO1** port of the I2C 8-bit I/O expander.
- **2-Channel I2C Switch** – This device is reset via **POR_B** or **GPIO3** port of the I2C 8-bit I/O expander.
- **Carrier Card Reset** – The carrier card is reset via **POR_B** or **GPIO5** port of the I2C 8-bit I/O expander.

2.12 Expansion Headers

2.12.1 Micro Headers

The VE2302 SOM features three Micro Headers for connection to end-user carrier cards. The three Micro Headers consist of 160-pin connectors from Samtec, ADF6-40-03.5-L-4-0-A. These connectors are Samtec 0.635mm AcceleRate® HD High Density 4-Row Sockets with 160 Positions and have stack heights options from 5mm and 16mm, making it easy to connect to a variety of expansion or system boards depending on the end-user requirements. By default, the mating solution with the Versal™ AI Edge Carrier Card is set to 5mm. Each pin can carry 1.340A of current and support I/O speeds more than what the AMD Versal™ AI Edge device can deliver with performance up to 64Gbps PAM4.

The JX Micro Header connectors on the VE2302 SOM have a default height of 3.5mm. The height of the mating JX receptacles for end-user carrier cards must be selected such that the stack height combination is <= 12mm when the VE2302 SOM is attached to the end-user carrier card (this requirement must be met to meet the 32Gbps data rate for the GTYP transceivers connected to the JX3 connector). Also, the stack height combination has a minimum requirement that is dependent on circuit implementation on the bottom of the VE2302 SOM and any circuitry that could be implemented on the end-user carrier card under the VE2302 SOM. Care must be taken to avoid shorting components when implementing short stacking height via the end-user carrier card.

The JX1 connector is the main interface to MIO and HDIO signals for the end-user carrier card. The JX1 provides access to dedicated JTAG signals, various power rails, voltage sense signals, PMBUS interface, and control signals. Lastly, the JX1 connector also host signals for the Gigabit Ethernet and USB 2.0 connectors.

The JX2 connector is the main interface for the XPIO signals for the end-user carrier card. The JX2 signal also provides access to various power rails, voltage sense signals, and control signals.

The JX3 connector interfaces to the GTYP MGTs, GTYP Reference Clocks, and GTYP power supplies. The JX3 connector also contains various power rail as well as voltage sense signals for the end-user carrier card power supply feedback.

The following table summarizes connections to the VE2302 SOM JX Micro Header Connectors.

Micro Header JX1			
Interface	**Signal Name**	**Source**	**Pins**
PMC	Bank 502 PMC MIO	Bank 502	12
	Bank 501 PMC MIO	Bank 501	13
	JTAG_TMS, JTAG_TCK, JTAG_TDI, JTAG_TDO ERROR_OUT DONE_OUT MODE[0:3]	Bank 503	10
PL I/O	Bank 302 Differential Pair I/Os	Bank 302	22
	SYSCLK_P/N	Bank 702	2
Comms	I2C_P6_GPIO, I2C_P7_GPIO	I2C Expander	2
	USB2.0 PHY Interface	USB PHY	4
	Gigabit Ethernet PHY Interface	ETH PHY	10
SYSMON	SMON_V_P, SMON_V_N	Bank 500	8

Micro Header JX1			
Interface	**Signal Name**	**Source**	**Pins**
	SMON_VREF VCCAUX_SMON GND_SMON		
Control	PMBus	I2C Switch	3
	CC I2C BUS	I2C Switch	3
	SOM_PG_OUT	VE2302 SOM	1
Power	GND	Carrier Card	39
	+VCC_BATT		1
	+VCC_FUSE		1
	+VCC_RAM and VCC_RAM_SENSE		2
	+VCCO_302REF and VCCO_302_SENSE		3
	+VCCO_502	VE2302 SOM	1
	+VCCO_PMC_MIO	VE2302 SOM	1
	VCCINT_SENSE and GND_SENSE	VE2302 SOM	2
	+VCCINT	Carrier Card	20

Table 27 – Micro Header JX1 Summary

Micro Header JX2			
Interface	**Signal Name**	**Source**	**Pins**
PL	Bank 702 Differential Pair I/Os	Bank 702	28
	Bank 702 – DDRMC Do Not Connect	Bank 702	24
	Bank 703 Differential Pair I/Os	Bank 703	52
Control	SOM_RESET_IN_B, SOM_PWR_ENB_IN, VCCO_702_PG_IN	Carrier Card	3
	VCCO_702_ENB_OUT, CC_RESET_OUT_B	VE2302 SOM	2
Power	GND	Carrier Card	28
	+VCCO_702		2
	+VCCO_703		2
	+MGTYPAVCC		3
	+MGTYPVCCAUX		2
	+VCCAUX_PMC	VE2302 SOM	1
	VCCO_702_SENSE, VCCO_702_SENSE, MGTYPVCCAUX_SENSE, MGTYPAVCC_SENSE, MGTYPAVTT_SENSE		5
	+VCCINT	Carrier Card	8

Table 28 – Micro Header JX2 Summary

Micro Header JX3			
Interface	Signal Name	Source	Pins
GTYP	Bank 103 Differential Pair I/Os	Bank 103	20
	Bank 104 Differential Pair I/Os	Bank 104	20
Power	GND	Carrier Card	92
	+MGTYPAVTT		3
	VIN_SENSE	VE2302 SOM	1
	+VIN	Carrier Card	12
	+VCCINT		12

Table 29 – Micro Header JX3 Summary

2.12.2 JX Micro Headers Matched Lengths

The VE2302 SOM device package delay is accommodated for in the layout of the JX Micro Header signal trace lengths. The average of min and max values for package delay is utilized to compensate for the flight time caused by the delay associated with this package.

The bank 302 HDIO pins are routed with matched lengths to the JX1 connector. The matched pairs may be used as either single ended I/O or differential pairs depending on the end users design requirements.

The LPD MIO and routed with matched lengths to the JX1 connector. The PMC MIO are routed with matched lengths to the JX1 connector. The Ethernet signals are routed with matched lengths to the JX1 connector. The USB differential pair is routed with matched lengths to the JX1 connector. The JTAG interface is routed with matched lengths to the JX1 connector.

See the **VE2302 SOM Net Length** report for more details on the matched lengths to the JX1 connector.

The bank 702 and bank 703 XPIO pins are routed with matched lengths to the JX2 connector. The matched lengths differ here from bank 302 as the matching of lengths are done by AMD nibbles which are 6-pins. Each nibble within bank 702 and bank 703 is length matched. The matched pairs may be used as either single ended I/O or differential pairs depending on the end users design requirements.

See the **VE2302 SOM Net Length** report for more details on the matched lengths to the JX2 connector.

The GTYP Quad 103 RX pins are routed with matched lengths to the JX3 connector. The GTYP Quad 103 TX pins are routed with matched lengths to the JX3 connector. The GTYP Quad 103 REFCLK pins are routed with matched lengths to the JX3 connector.

The GTYP Quad 104 RX pins are routed with matched lengths to the JX3 connector. The GTYP Quad 104 TX pins are routed with matched lengths to the JX3 connector. The GTYP Quad 104 REFCLK pins are routed with matched lengths to the JX3 connector.

See the **VE2302 SOM Net Length** report for more details on the matched lengths to the JX3 connector.

2.12.3 JX Connector Master Table

The following tables list the VE2302 SOM JX Micro Header connections in master tables targeting each connector:

- Pins in **Orange** are DDRMC dedicated and are not available to be used
- Pins in **Pink** are Power, Ground, or Sense signals
- Pins in **Blue** are dedicated signals
- Pins in **Black** are multi-function/general-purpose pins
- Pins in **Black** with **_HDGC** designators inputs are clock capable pins in a HDIO bank
- Pins in **Black** with **_XCC** designators can accept a strobe to capture data
- Pins in **Black** with _**GC** and _**XCC** these pins can act as Global Clocks and/or XCCs inputs
- **PMC_MIO** stands for Platform Management Controller Multiplexed I/O
- **LPD_MIO** stands for Low Power Domain Multiplexed I/O
- **HDIO** stands for I/O from bank 302
- **XPIO** stands for I/O from bank 702 or bank 703
- **GTYP** stands for I/O from quad 103 or quad 104

XCVE2302 Pin #	Signal Name	JX1 Pin #		Signal Name	XCVE2302 Pin #
Many	+VCCINT	A1	B1	+VCCINT	Many
	+VCCINT	A2	B2	+VCCINT	
	+VCCINT	A3	B3	+VCCINT	
	+VCCINT	A4	B4	+VCCINT	
	+VCCINT	A5	B5	+VCCINT	
N/A	GND	A6	B6	GND	N/A
B13	HDIO_302_L10_P	A7	B7	HDIO_302_L9_P	B12
A14	HDIO_302_L10_N	A8	B8	HDIO_302_L9_N	A13
N/A	GND	A9	B9	GND	N/A
C14	HDIO_302_L1_P	A10	B10	HDIO_302_L2_P	E13
C13	HDIO_302_L1_N	A11	B11	HDIO_302_L2_N	D14
D13, F13	+VCCO_302	A12	B12	+VCCO_302	D13, F13
E12	HDIO_302_L3_P	A13	B13	HDIO_302_HDGC_L5_P	D11
D12	HDIO_302_L3_N	A14	B14	HDIO_302_HDGC_L5_N	C12
N/A	GND	A15	B15	GND	N/A
Y7	LPD_MIO23	A16	B16	LPD_MIO21	U6
T6	LPD_MIO22	A17	B17	LPD_MIO20	W6
N/A	GND	A18	B18	+VCC_FUSE	V15
AF10	PMC_MIO47	A19	B19	PMC_MIO49	AC10
AF9	PMC_MIO46	A20	B20	PMC_MIO48	AD10
N/A	GND	A21	B21	GND	N/A
AE9	PMC_MIO45	A22	B22	PMC_MIO43	AC9
AD9	PMC_MIO44	A23	B23	PMC_MIO42	AA9
U7, U8, V7, W8, V9, W9	+VCCO_PMC_MIO	A24	B24	GND	N/A

XCVE2302 Pin #	Signal Name	JX1 Pin #		Signal Name	XCVE2302 Pin #
N/A	CC_INT_B	A25	B25	CC_SCL	N/A
N/A	PMBUS_ALERT_B	A26	B26	GND	N/A
N/A	VCCO_302_SENSE	A27	B27	VCC_RAM_SENSE	N/A
N/A	GND	A28	B28	PMBUS_SDA	N/A
N/A	ETH_ACT	A29	B29	SOM_PG_OUT	N/A
N/A	ETH_LINK	A30	B30	USB_ID	N/A
N/A	GND	A31	B31	GND	N/A
N/A	ETH_MD4_P	A32	B32	ETH_MD3_P	N/A
N/A	ETH_MD4_N	A33	B33	ETH_MD3_N	N/A
N/A	GND	A34	B34	GND	N/A
AG8	MODE0	A35	B35	MODE1	AG7
N/A	GND	A36	B36	GND	N/A
AH10	JTAG_TCK	A37	B37	JTAG_TMS	AH9
N/A	GND	A38	B38	GND	N/A
R18	SMON_AGND	A39	B39	SMON_AGND	R18
U17	+SMON_VREF	A40	B40	SMON_V _P	T17
Many	+VCCINT	C1	D1	+VCCINT	Many
	+VCCINT	C2	D2	+VCCINT	
	+VCCINT	C3	D3	+VCCINT	
	+VCCINT	C4	D4	+VCCINT	
	+VCCINT	C5	D5	+VCCINT	
N/A	GND	C6	D6	GND	N/A
B11	HDIO_302_L8_P	C7	D7	HDIO_302_L7_P	B10
A11	HDIO_302_L8_N	C8	D8	HDIO_302_L7_N	A10
N/A	GND	C9	D9	GND	N/A
D10	HDIO_302_HDGC_L6_P	C10	D10	HDIO_302_L4_P	F11
C10	HDIO_302_HDGC_L6_N	C11	D11	HDIO_302_L4_N	E11
P20, T20	+VCC_RAM	C12	D12	+USB_VBUS	N/A
F14	HDIO_302_L0_P	C13	D13	ERROR_OUT	AH5
E14	HDIO_302_L0_N	C14	D14	SYSCLK_P	N23
N/A	GND	C15	D15	SYSCLK_N	N24
F10	VCCINT_SENSE	C16	D16	GND	N/A
F9	GND_SENSE	C17	D17	LPD_MIO17	V5
N/A	I2C_P6_GPIO	C18	D18	LPD_MIO16	U5
N/A	I2C_P7_GPIO	C19	D19	GND	N/A

XCVE2302 Pin #	Signal Name	JX1 Pin #		Signal Name	XCVE2302 Pin #
N/A	GND	C20	D20	LPD_MIO15	T5
Y6	LPD_MIO19	C21	D21	LPD_MIO14	T4
W5	LPD_MIO18	C22	D22	+VCCO_502	T8, T9
V4	LPD_MIO13	C23	D23	PMC_MIO39	AC8
W4	LPD_MIO12	C24	D24	PMC_MIO38	AE8
N/A	GND	C25	D25	GND	N/A
AA8	PMC_MIO41	C26	D26	PMC_MIO37	AE7
AB8	PMC_MIO40	C27	D27	+VCC_BATT	W15
N/A	GND	C28	D28	DONE_OUT	AF5
N/A	CC_SDA	C29	D29	USB_D_P	N/A
N/A	PMBUS_SCL	C30	D30	USB_D_N	N/A
N/A	GND	C31	D31	GND	N/A
N/A	ETH_MD2_P	C32	D32	ETH_MD1_P	N/A
N/A	ETH_MD2_N	C33	D33	ETH_MD1_N	N/A
N/A	GND	C34	D34	GND	N/A
AG6	MODE2	C35	D35	MODE3	AG5
N/A	GND	C36	D36	GND	N/A
AG10	JTAG_TDI	C37	D37	JTAG_TDO	AF8
N/A	GND	C38	D38	GND	N/A
R18	SMON_AGND	C39	D39	SMON_AGND	R18
U18	SMON_V_N	C40	D40	+VCCAUX_SMON	R17

Table 30 – JX1 Connector Pin-out

XCVE2302 Pin #	Signal Name	JX2 Pin #		Signal Name	XCVE2302 Pin #
Many	+VCCINT	A1	B1	+VCCINT	Many
	+VCCINT	A2	B2	+VCCINT	
A25	XPIO_703_L10_P	A3	B3	XPIO_703_XCC_L3_P	E27
A26	XPIO_703_L10_N	A4	B4	XPIO_703_XCC_L3_N	E28
N/A	GND	A5	B5	GND	N/A
B26	XPIO_703_L11_P	A6	B6	XPIO_703_GC_XCC_L9_P	C25
B27	XPIO_703_L11_N	A7	B7	XPIO_703_GC_XCC_L9_N	B25
AE21, AF20, AF21	+VCCO_702	A8	B8	+VCCO_702	AE21, AF20, AF21
C23	XPIO_703_L16_P	A9	B9	XPIO_702_L26_P	N25
B23	XPIO_703_L16_N	A10	B10	XPIO_702_L26_N	M25

XCVE2302 Pin #	Signal Name	JX2 Pin #		Signal Name	XCVE2302 Pin #
N/A	GND	A11	B11	GND	N/A
D24	XPIO_703_XCC_L15_P	A12	B12	XPIO_703_L17_P	A23
C24	XPIO_703_XCC_L15_N	A13	B13	XPIO_703_L17_N	A24
AA24, AA25, AB25	+VCCO_703	A14	B14	+VCCO_703	AA24, AA25, AB25
B20	XPIO_703_XCC_L21_P	A15	B15	XPIO_703_L22_P	A20
C21	XPIO_703_XCC_L21_N	A16	B16	XPIO_703_L22_N	A21
N/A	GND	A17	B17	GND	N/A
D20	XPIO_703_L20_P	A18	B18	XPIO_703_L23_P	C22
D21	XPIO_703_L20_N	A19	B19	XPIO_703_L23_N	B22
N/A	VCCO_702_SENSE	A20	B20	VCCO_703_SENSE	N/A
G21	XPIO_703_XCC_L18_P	A21	B21	XPIO_703_L19_P	E20
H22	XPIO_703_XCC_L18_N	A22	B22	XPIO_703_L19_N	F21
N/A	GND	A23	B23	GND	N/A
R27	XPIO_702_L1_P	A24	B24	XPIO_702_L2_P	P27
T28	XPIO_702_L1_N	A25	B25	XPIO_702_L2_N	R28
L7, N7	+MGTYPAVCC	A26	B26	+MGTYPAVCC	L7, N7
N28	XPIO_702_XCC_L3_P	A27	B27	XPIO_702_XCC_L0_P	U27
M28	XPIO_702_XCC_L3_N	A28	B28	XPIO_702_XCC_L0_N	U28
N/A	GND	A29	B29	GND	N/A
K27	XPIO_702_L5_P	A30	B30	XPIO_702_L4_P	M27
K28	XPIO_702_L5_N	A31	B31	XPIO_702_L4_N	L28
W12, W14	+VCCAUX_PMC	A32	B32	SOM_RESET_IN_B	N/A
K21	XPIO_702_XCC_L22_P	A33	B33	XPIO_702_L23_P	J21
L22	XPIO_702_XCC_L22_N	A34	B34	XPIO_702_L23_N	J22
N/A	GND	A35	B35	GND	N/A
T21	XPIO_702_L20_P	A36	B36	XPIO_702_XCC_L21_P	N21
R22	XPIO_702_L20_N	A37	B37	XPIO_702_XCC_L21_N	M21
N/A	GND	A38	B38	GND	N/A
R21	XPIO_702_L19_P	A39	B39	XPIO_702_XCC_L18_P	V21
P22	XPIO_702_L19_N	A40	B40	XPIO_702_XCC_L18_N	U22
Many	+VCCINT	C1	D1	+VCCINT	Many
	+VCCINT	C2	D2	+VCCINT	
D27	XPIO_703_L4_P	C3	D3	XPIO_703_L5_P	C27
C28	XPIO_703_L4_N	C4	D4	XPIO_703_L5_N	B28

XCVE2302 Pin #	Signal Name	JX2 Pin #		Signal Name	XCVE2302 Pin #
N/A	GND	C5	D5	GND	N/A
H27	XPIO_703_L1_P	C6	D6	XPIO_703_L2_P	G27
G28	XPIO_703_L1_N	C7	D7	XPIO_703_L2_N	F28
N/A	VCCO_702_ENB_OUT	C8	D8	VCCO_702_PG_IN	N/A
F23	XPIO_703_GC_XCC_L24_P	C9	D9	XPIO_703_XCC_L0_P	J27
F24	XPIO_703_GC_XCC_L24_N	C10	D10	XPIO_703_XCC_L0_N	H28
N/A	GND	C11	D11	GND	
D25	XPIO_703_L26_P	C12	D12	XPIO_703_L25_P	E24
D26	XPIO_703_L26_N	C13	D13	XPIO_703_L25_N	F25
N/A	CC_RESET_OUT_B	C14	D14	MGTYPVCCAUX_SENSE	N/A
G25	XPIO_703_L7_P	C15	D15	XPIO_703_L8_P	F26
G26	XPIO_703_L7_N	C16	D16	XPIO_703_L8_N	E26
N/A	GND	C17	D17	GND	N/A
E22	XPIO_703_L14_P	C18	D18	XPIO_703_GC_XCC_L6_P	H25
E23	XPIO_703_L14_N	C19	D19	XPIO_703_GC_XCC_L6_N	J26
N/A	MGTYPAVCC_SENSE	C20	D20	MGTYPAVTT_SENSE	N/A
H23	XPIO_703_GC_XCC_L12_P	C21	D21	XPIO_703_L13_P	F22
H24	XPIO_703_GC_XCC_L12_N	C22	D22	XPIO_703_L13_N	G23
N/A	GND	C23	D23	GND	N/A
M26	XPIO_702_L10_P	C24	D24	XPIO_702_L11_P	J25
L26	XPIO_702_L10_N	C25	D25	XPIO_702_L11_N	K26
L7, N7	+MGTYPAVCC	C26	D26	+MGTYPVCCAUX	G7, J7
L23	XPIO_702_L16_P	C27	D27	XPIO_702_GC_XCC_L9_P	P26
K24	XPIO_702_L16_N	C28	D28	XPIO_702_GC_XCC_L9_N	N27
N/A	GND	C29	D29	GND	N/A
K23	XPIO_702_L17_P	C30	D30	XPIO_702_XCC_L15_P	M22
J24	XPIO_702_L17_N	C31	D31	XPIO_702_XCC_L15_N	M23
N/A	SOM_PWR_ENB_IN	C32	D32	+MGTYPVCCAUX	G7, J7
P25	XPIO_702_L8_P	C33	D33	XPIO_702_L7_P	T25
R26	XPIO_702_L8_P	C34	D34	XPIO_702_L7_N	T26
N/A	GND	C35	D35	GND	N/A
U25	XPIO_702_GC_XCC_L6_P	C36	D36	XPIO_702_L13_P	T23
U26	XPIO_702_GC_XCC_L6_N	C37	D37	XPIO_702_L13_N	R24
N/A	GND	C38	D38	GND	N/A
U23	XPIO_702_GC_XCC_L12_P	C39	D39	XPIO_702_L14_P	R23

XCVE2302 Pin #	Signal Name	JX2 Pin #		Signal Name	XCVE2302 Pin #
T24	XPIO_702_GC_XCC_L12_N	C40	D40	XPIO_702_L14_N	P24

Table 31 – JX2 Connector Pin-out

XCVE2302 Pin #	Signal Name	JX3 Pin #		Signal Name	XCVE2302 Pin #
Many	+VCCINT	A1	B1	+VCCINT	Many
	+VCCINT	A2	B2	+VCCINT	
	+VCCINT	A3	B3	+VCCINT	
N/A	GND	A4	B4	GND	N/A
N/A	VIN_SENSE	A5	B5	+MGTYPAVTT	L9, M9, N9
N/A	GND	A6	B6	GND	N/A
H7	GTYP_104_REFCLK0_P	A7	B7	GND	N/A
H6	GTYP_104_REFCLK0_N	A8	B8	GND	N/A
N/A	GND	A9	B9	GND	N/A
N/A	GND	A10	B10	GTYP_104_REFCLK1_P	F7
N/A	GND	A11	B11	GTYP_104_REFCLK1_N	F6
N/A	GND	A12	B12	GND	N/A
N/A	GND	A13	B13	GND	N/A
D8	GTYP_104_TX1_P	A14	B14	GND	N/A
D7	GTYP_104_TX1_N	A15	B15	GND	N/A
N/A	GND	A16	B16	GND	N/A
N/A	GND	A17	B17	GTYP_104_TX3_P	B8
N/A	GND	A18	B18	GTYP_104_TX3_N	B7
N/A	GND	A19	B19	GND	N/A
C5	GTYP_104_TX2_P	A20	B20	GND	N/A
C4	GTYP_104_TX2_N	A21	B21	GND	N/A
N/A	GND	A22	B22	GND	N/A
N/A	GND	A23	B23	GTYP_104_TX0_P	E5
N/A	GND	A24	B24	GTYP_104_TX0_N	E4
N/A	GND	A25	B25	GND	N/A
G5	GTYP_103_TX3_P	A26	B26	GND	N/A
G4	GTYP_103_TX3_N	A27	B27	GND	N/A
N/A	GND	A28	B28	GND	N/A
N/A	GND	A29	B29	GTYP_103_TX2_P	J5
N/A	GND	A30	B30	GTYP_103_TX2_N	J4

XCVE2302 Pin #	Signal Name	JX3 Pin #		Signal Name	XCVE2302 Pin #
N/A	GND	A31	B31	GND	N/A
L5	GTYP_103_TX1_P	A32	B32	GND	N/A
L4	GTYP_103_TX1_N	A33	B33	GND	N/A
N/A	GND	A34	B34	GND	N/A
N/A	GND	A35	B35	GTYP_103_TX0_P	N5
N/A	GND	A36	B36	GTYP_103_TX0_N	N4
N/A	GND	A37	B37	GND	N/A
N/A	+VIN	A38	B38	+VIN	N/A
N/A	+VIN	A39	B39	+VIN	N/A
N/A	+VIN	A40	B40	+VIN	N/A
Many	+VCCINT	C1	D1	+VCCINT	Many
	+VCCINT	C2	D2	+VCCINT	
	+VCCINT	C3	D3	+VCCINT	
N/A	GND	C4	D4	GND	N/A
L9, M9, N9	+MGTYPAVTT	C5	D5	+MGTYPAVTT	L9, M9, N9
N/A	GND	C6	D6	GND	N/A
M7	GTYP_103_REFCLK0_P	C7	D7	GND	N/A
M6	GTYP_103_REFCLK0_N	C8	D8	GND	N/A
N/A	GND	C9	D9	GND	N/A
N/A	GND	C10	D10	GTYP_103_REFCLK1_P	K7
N/A	GND	C11	D11	GTYP_103_REFCLK1_N	K6
N/A	GND	C12	D12	GND	N/A
N/A	GND	C13	D13	GND	N/A
A5	GTYP_104_RX3_P	C14	D14	GND	N/A
A4	GTYP_104_RX3_N	C15	D15	GND	N/A
N/A	GND	C16	D16	GND	N/A
N/A	GND	C17	D17	GTYP_104_RX2_P	B2
N/A	GND	C18	D18	GTYP_104_RX2_N	B1
N/A	GND	C19	D19	GND	N/A
D2	GTYP_104_RX1_P	C20	D20	GND	N/A
D1	GTYP_104_RX1_N	C21	D21	GND	N/A
N/A	GND	C22	D22	GND	N/A
N/A	GND	C23	D23	GTYP_104_RX0_P	F2
N/A	GND	C24	D24	GTYP_104_RX0_N	F1
N/A	GND	C25	D25	GND	N/A

XCVE2302 Pin #	Signal Name	JX3 Pin #		Signal Name	XCVE2302 Pin #
H2	GTYP_103_RX3_P	C26	D26	GND	N/A
H1	GTYP_103_RX3_N	C27	D27	GND	N/A
N/A	GND	C28	D28	GND	N/A
N/A	GND	C29	D29	GTYP_103_RX2_P	K2
N/A	GND	C30	D30	GTYP_103_RX2_N	K1
N/A	GND	C31	D31	GND	N/A
M2	GTYP_103_RX1_P	C32	D32	GND	N/A
M1	GTYP_103_RX1_N	C33	D33	GND	N/A
N/A	GND	C34	D34	GND	N/A
N/A	GND	C35	D35	GTYP_103_RX0_P	P2
N/A	GND	C36	D36	GTYP_103_RX0_N	P1
N/A	GND	C37	D37	GND	N/A
N/A	+VIN	C38	D38	+VIN	N/A
N/A	+VIN	C39	D39	+VIN	N/A
N/A	+VIN	C40	D40	+VIN	N/A

Table 32 – JX3 Connector Pin-out

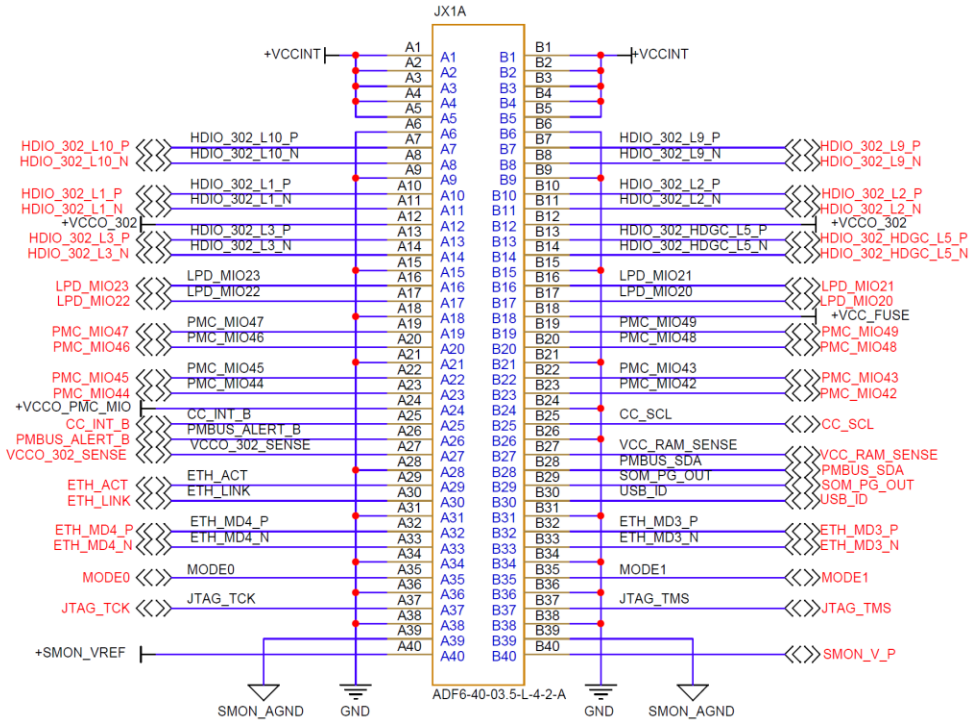

Figure 15 – JX1 Row A/B Connector Pinout

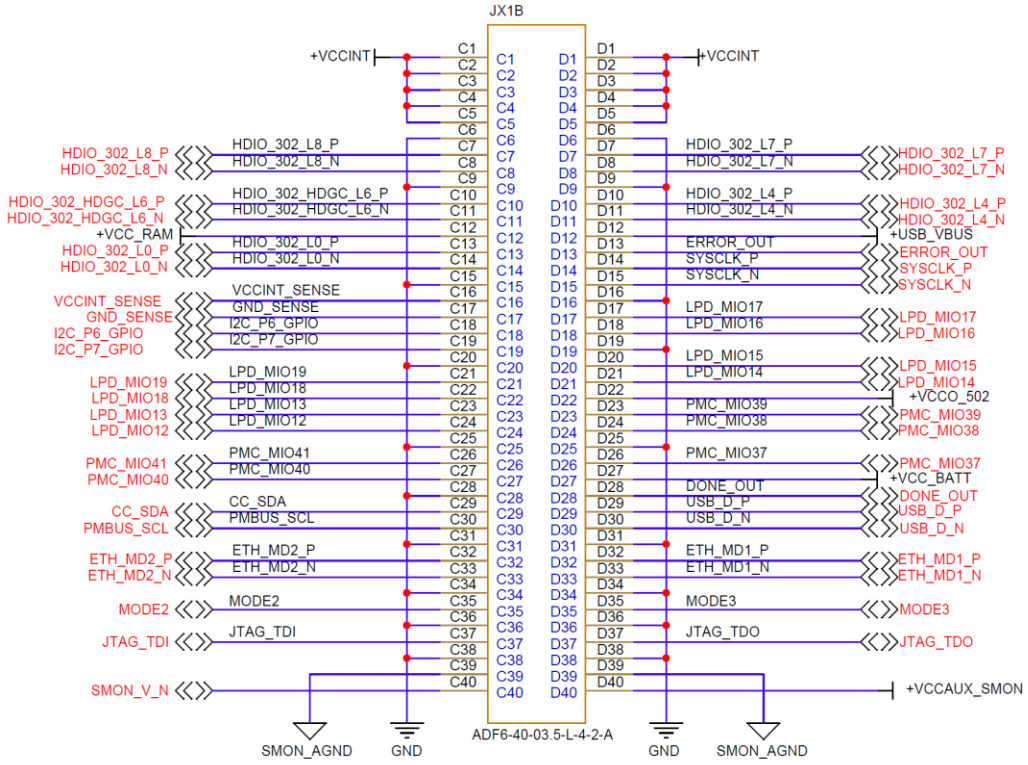

Figure 16 – JX1 Row C/D Connector Pinout

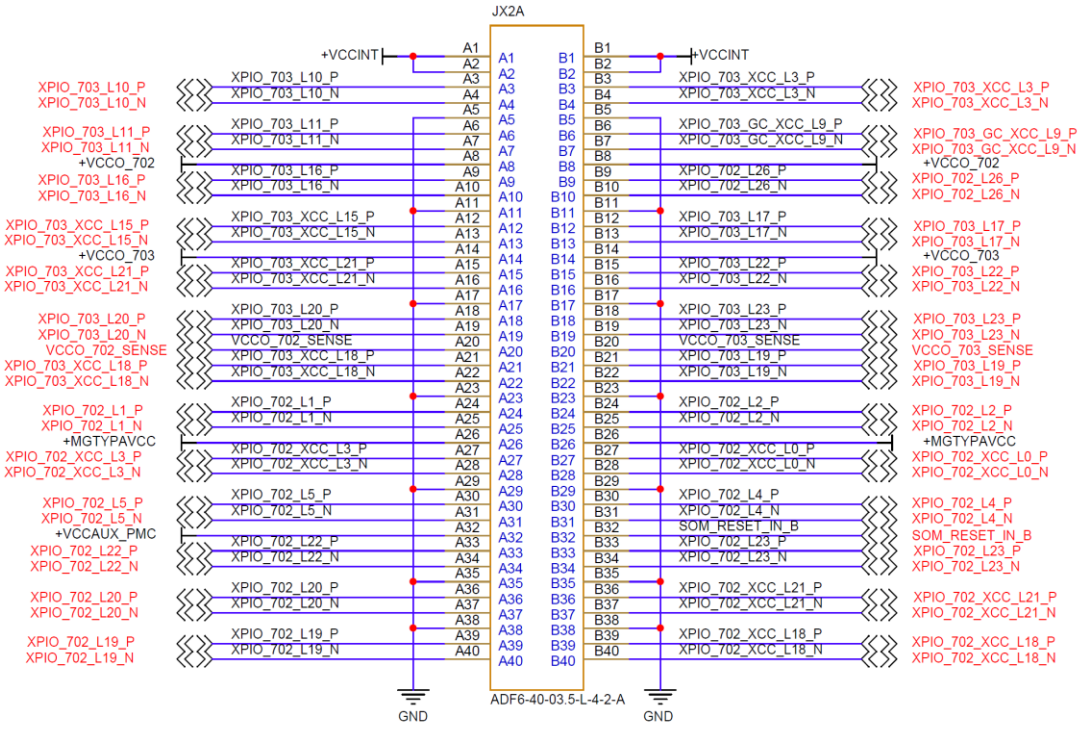

Figure 17 – JX2 Row A/B Connector Pinout

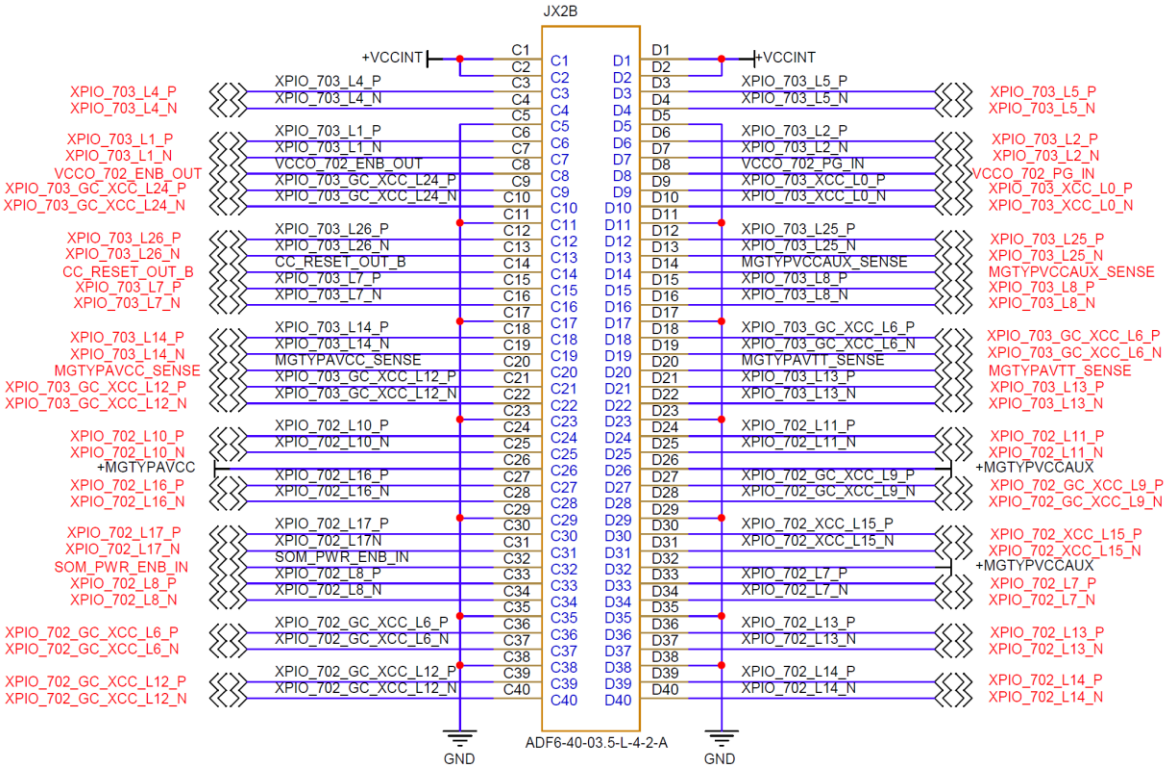

Figure 18 – JX2 Row C/D Connector Pinout

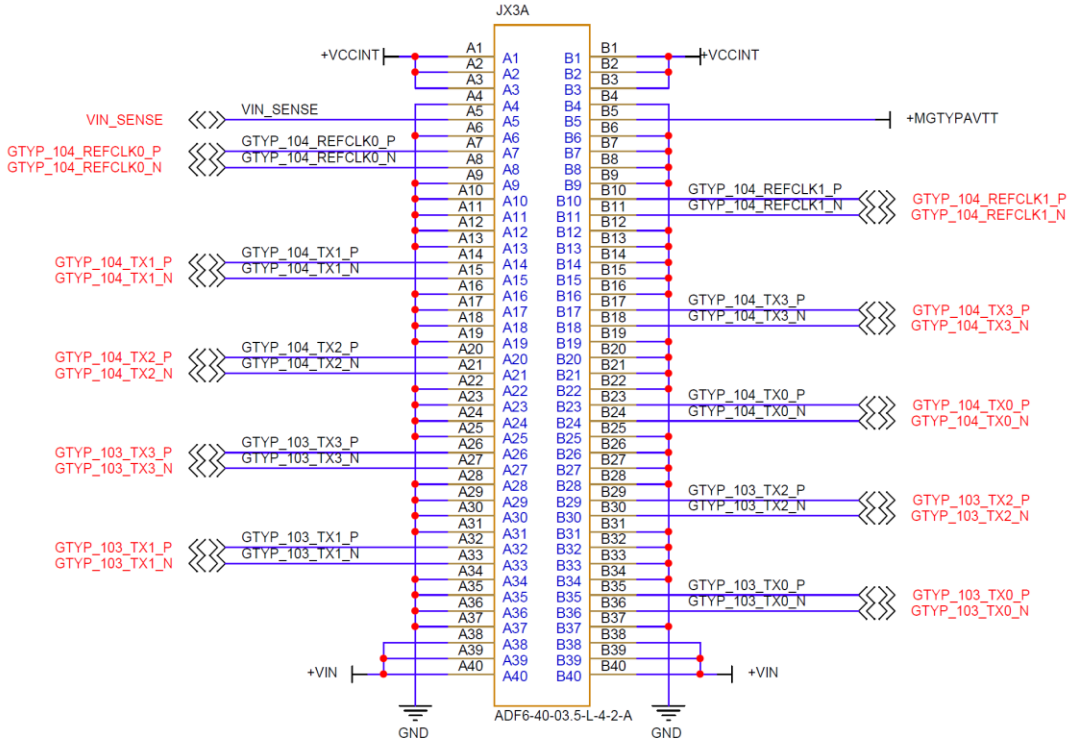

Figure 19 – JX3 Row A/B Connector Pinout

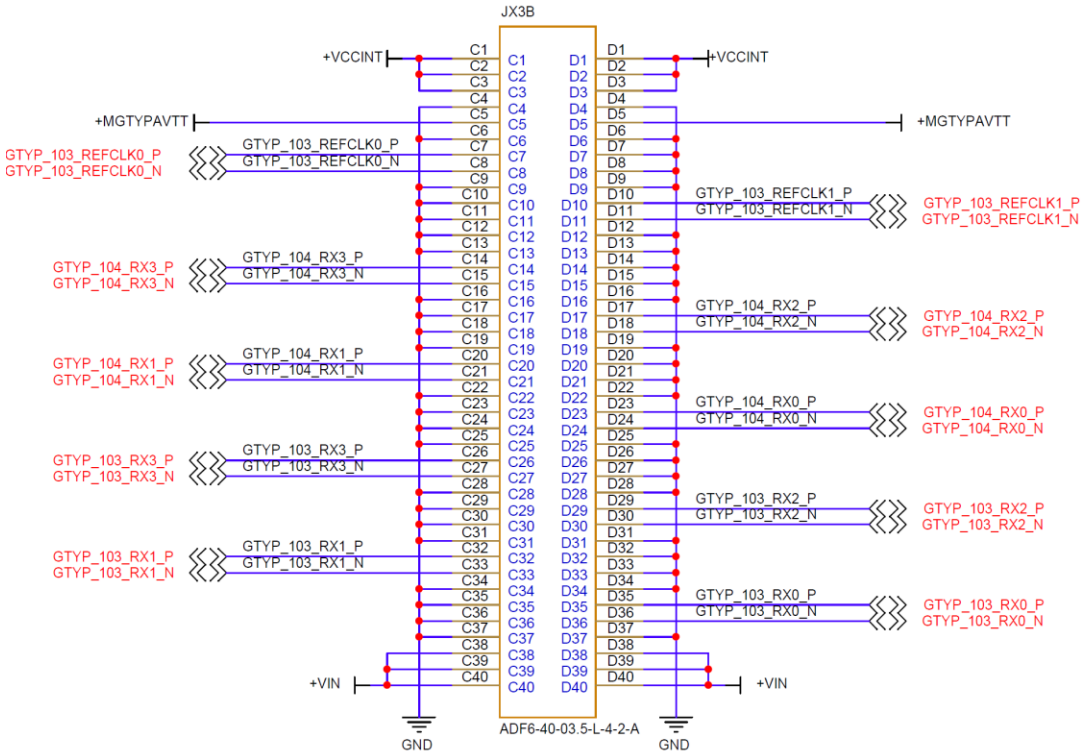

Figure 20 – JX3 Row C/D Connector Pinout

2.13 Supported Configuration Modes

The AMD Versal™ Adaptive SoC device uses a multi-stage boot process that supports both nonsecure and secure boot. The PLM is the master of the boot and configuration process. Upon reset, the device MODE pins are read to determine the primary boot device to be used. The VE2302 SOM in conjunction with the Versal™ AI Edge Carrier Card support several boot devices. OSPI, SD Card, and JTAG boot are easily accessible by changing the Boot Mode Switch on the Versal™ AI Carrier Card. Please refer to the **Versal™ AI Edge Carrier Card Hardware User Guide** for an example of a Boot Mode Switch implementation.

NOTE: The JTAG and/or SD card is to be implemented on the end-user carrier card. The SD card interface will need to utilize the user PMC MIO pins provided to the JX connector if implemented. Please refer to the **Versal™ AI Edge Carrier Card Hardware User Guide** for an example of JTAG and/or SD card implementation.

BOOT MODE	MODE PIN[3:0]	SW7[1-4]
JTAG	0x0	ON-ON-ON-ON
SD0/3.0 AUTODIR	0x3	ON-ON-OFF-OFF
OSPI	0x8	OFF-ON-ON-ON

Table 33 – Supported BOOT Modes

The VE2302 SOM routes the Boot Mode pins to the JX1 connector. End-user carrier cards should implement a small 4-position DIP switch for the Boot Mode pins. This switch will be connected to the MODE[3:0] pins of the PMC configuration bank 503 and allows users to select the primary boot device. The pin connections to the JX1 connector are described in the following table.

Signal Name	JX1 Pin Number		Signal Name
MODE0	A35	B35	MODE1
MODE2	C35	D35	MODE3

Table 34 – Boot Mode Interface Pin Assignments

2.14 JTAG Interface

The VE2302 SOM requires an external JTAG cable connector populated on the carrier card for JTAG operations. JTAG signals are routed from configuration bank 503 of the Versal Adaptive SoC device to the JX1 Micro Header. The following table shows the JTAG signal connections between the Versal Adaptive SoC device and the JX1 Micro Header.

The AMD Versal™ Adaptive SoC configuration bank 503 reference voltage, **+VCCO_PMC_MIO**, is connected to +1.8V. The JTAG interface is translated to +3.3V for ease of use. The **JTAG VREF,** if utilized, on the end-user carrier card should be connected to +3.3V to ensure compatibility between the interfaces. Please refer to the **Versal™ AI Edge Carrier Card Hardware User Guide** for an example implementation of a JTAG interface.

SoC Pin #	Net Name	JX1 Pin #
AH10	JTAG_TCK	A37
AH9	JTAG_TMS	B37
AG10	JTAG_TDI	C37
AF8	JTAG_TDO	D37

Table 35 –JTAG Interface Pin Assignments

2.15 Power Supplies

2.15.1 Power Requirements

The VE2302 SOM is powered through the JX Micro Header connection between itself and the end-user carrier card. It receives an input voltage, **+VIN**, of +5V from the end-user carrier card and generates the voltage rails required using this voltage source. The VE2302 SOM power architecture can optionally support many of the speed grades offered for the SFVA784 package while the power architecture default settings support the off-the-shelf populated AMD Versal™ AI Edge device.

There are voltage regulators and load switches that reside on the VE2302 SOM that provide properly sequenced versions of +0.70V, +0.80V, +1.10V, +1.50V, +1.80V, +2.50V, and +3.30V power rails. These voltages are used to power the peripheral devices as well as the VE2302 SOM. The regulators are powered from the end-user carrier card via the **+VIN** pins on the Micro Headers and are expecting to receive +5V at their inputs.

+VCC_RAM (+0.80V) and **+VCCINT** (+0.70V) core voltages are supplied from the end-user carrier card to the VE2302 SOM due to sequencing ease as well as to provide end-users with core voltage / current control. Particularly, the **+VCCINT** rail could have significant variance in the required current which is heavily dependent on the end-user's final application. By moving this voltage regulation to the end-user carrier card, the final solution of this regulator can be optimized for cost, space, and the targeted application whereas if it existed on the VE2302 SOM the final solution would be over-engineered to support the worst-case application.

There are three bank voltages that are supplied from the end-user carrier card to the VE2302 SOM. Bank 302 (**+VCCO_302**), bank 702 (**+VCCO_702**), and bank 703 (**+VCCO_703**) voltages are required to be generated on the end-user carrier card and connected to the VE2302 SOM via the JX Micro Headers. The voltage at which these banks operate is up to the end-user carrier card design as all the IO that connect to these banks is exclusive to the Micro Headers (except for bank 702 which shares 4-signals with the LPDDR4 interface). **NOTE:** The supported voltage for these rails depends on the IO type (HDIO versus XPIO). End-user carrier cards should take care not to operate these banks outside of the recommended voltage range listed in the AMD Versal™ AI Edge datasheet **DS958.**

There are three voltages that are supplied from the end-user carrier card to the VE2302 SOM that provide power to the GTYP quads 103 and 104. The voltages are **+MGTYPAVCC** (+0.92V), **+MGTYPAVTT** (+1.20V), and **+MGTYPVCCAUX** (+1.50V)

The VE2302 SOM provides voltage sense feedback (**VCCO_302_SENSE**, **VCCO_702_SENSE**, **VCCO_703_SENSE**, **VCC_RAM_SENSE**, **MGTYPAVCC_SENSE**, **MGTYPAVTT_SENSE**, and **MGTYPVCCAUX_SENSE**) for rails generated by the end-user carrier card via JX connectors. Please refer to **Expansion Headers** section of this document for the JX1, JX2, and JX3 detailed pinout information. The voltage sense feedback for each rail can be used by the regulator on the end-user carrier card to compensate for the voltage loss across the JX connectors. Please refer to the **DS958** (AMD Versal™ AI Edge Series datasheet) for percent variation on all the following voltage rails when designing the power system for the end-user carrier card.

The end-user carrier card is required to supply the following rails to the VE2302 SOM.

- +VCCINT (+0.70V) via JX connectors
- +VIN (+5.0V) main input voltage via JX3 connector
- Quad 103-104 Regulators via JX connectors
    - +MGTYPAVCC (+0.92V) via JX2 connector
    - +MGTYPAVTT (+1.2V) via JX3 connector
    - +MGTYPVCCAUX (+1.5V) via JX2 connector
- HDIO bank 302 VCCO
    - +VCCO_302 (+1.8V to +3.3V) via JX1 connector
- XPIO bank 702 VCCO
    - +VCCO_702 (+1.0V to +1.5V) via JX2 connector
- XPIO bank 703 VCCO
    - +VCCO_703 (+1.0V to +1.5V) via JX2 connector
- +VCC_RAM (+0.80V) via JX3 connector
- +VCC_BATT (+1.5V) via JX3 connector
- +VCC_FUSE (+1.8V) via JX3 connector

Please refer to the **Versal™ AI Edge Carrier Card Hardware User Guide** for example implementations of the end-user carrier card required power rails.

Voltage Rail Name	Power Domain	Voltage Value	Current	Voltage Sense Feedback
+VIN		+5.0V	12.000A	VIN_SENSE
+VCCO_PMC_MIO	PMC	+1.80V	2.000A	-
+VCC_PMC	PMC	+0.70V	1.000A	-
+VCCAUX_PMC	PMC	+1.50V	1.000A	-
+VCCAUX_SMON	PMC	+1.50V	SHARED	

Voltage Rail Name	Power Domain	Voltage Value	Current	Voltage Sense Feedback
+VCCO_502	LPD	+1.80V	0.375A	-
+VCC_PSLP	LPD	+0.70V *	0.300A	-
+VCC_PSFP	FPD	+0.70V *	1.900A	-
+VCCO_LPDDR4	SPD	+1.10V	3.00A	-
+VCCO_700	SPD	+1.10V	SHARED	-
+VCCO_701	SPD	+1.10V	SHARED	-
+VCCO_702	SPD	+1.0V to +1.5V	0.925A	VCCO_702_SENSE
+VCC_SOC	SPD	+0.80V *	3.333A	-
+VCC_IO	SPD	+0.80V *	SHARED	-
+VCCAUX	SPD	+1.50V	0.895A	-
+VCCO_703	PLPD	+1.0V to +1.5V	0.925A	VCCO_703_SENSE
+VCCO_302	PLPD	+1.8 to +3.3V	0.380A	VCCO_302_SENSE
+VCCINT	PLPD	+0.70V *	40.665A	VCCINT_SENSE
+VCC_RAM	PLPD	+0.80V *	0.210A	VCC_RAM_SENSE
+MGTYPAVCC	PLPD	+0.92V	1.500A	MGTYPAVCC_SENSE
+MGTYPVCCAUX	PLPD	+1.50V	0.015A	MGTYPVCCAUX_SENSE
+MGTYPAVTT	PLPD	+0.92V	1.870A	MGTYPAVTT_SENSE
+VCC_BATT	-	+1.50V	-	-
+VCC_FUSE	-	+1.80V	-	-

Table 36 – Example Power Requirements

NOTE: **+VCC_BATT** is provided by the end-user carrier card through the JX Connector. Voltage must be in the range of 1.425V-1.575V. If **+VCC_BATT** is unused, the end-user carrier card is responsible for setting the appropriate value to the **+VCC_BATT** pin.

NOTE: To prevent unintentional eFuse programming, **+VCC_FUSE** should power up after the PMC power domain is powered so that the PMC eFuse control circuits are powered up and are in a known state. The recommended **+VCC_FUSE** power-down sequence is the reverse of the power-on sequence. Ideally, **+VCC_FUSE** should only be powered up when performing eFuse programming. If not programming eFuse, **+VCC_FUSE** can be connected to GND.

2.15.2 Power Sequencing

The power-up and power-down sequencing of the VE2302 SOM and end-user carrier card solution should follow datasheet recommendations for the AMD Versal™ AI Edge Adaptive SoC device. The power architecture designed on the VE2302 SOM and the Versal™ AI Edge Carrier Card is a good example of a power architecture that follows the datasheet recommendations for power-up and power-down sequencing.

The PMC power domain must be powered first and remain on for all power modes except complete device power-down. During the PMC power domain power-on sequence, the **POR_B** input on the AMD Versal™ AI Edge device is asserted LOW and continues to be asserted for a minimum duration of **POR_B** (10uS)

after all the required supplies of the PMC power domain (+**VCCO_500**, +**VCCO_501**, +**VCCO_503**, +**VCC_PMC**, +**VCCAUX_PMC**, and +**VCCAUX_SMON**) have reached minimum operating voltage levels.

After PMC power domain power-on, **POR_B** can de-asserted HIGH to complete the device power-on-reset (POR). Please refer to the **Versal™ AI Edge Hardware User Guide** as it utilizes a header to monitor the +VCCAUX_PMC power rail for the case where **POR_B** is de-asserted at this point.

If other power domains are powered with the PMC domain and are expected to be functional at initial power-on without additional power management, then the **POR_B** input on the AMD Versal™ AI Edge device is held LOW until all applicable power domain supplies have reached minimum voltage levels. By design on the Versal™ AI Edge Carrier Card, a second **POR_B** de-assertion point is provided for targeting the end of the power-up sequence is provided. The header that monitors the **+VCCAUX_PMC** power rail can be changed to monitor the **+MGTYPAVTT_SENSE** signal to indicate the last power rail in the sequence is stable so that **POR_B** can be de-asserted HIGH to complete the device power-on-reset (POR).

The VE2302 SOM power sequencing requires several control signals to be utilized to sequence the VE2302 SOM and an end user carrier card in the most appropriate manner. The signals from the VE2302 SOM that will be used as enable signals to the end user carrier card are called **VCCO_702_ENB_OUT**, and **SOM_PG_OUT**. The proper end user carrier card voltage regulators should not be turned ON until the **VCCO_702_ENB_OUT** and **SOM_PG_OUT** signals are asserted. The control signals to the VE2302 SOM that are used are called **SOM_PWR_ENB_IN** and **VCCO_702_PG_IN**.

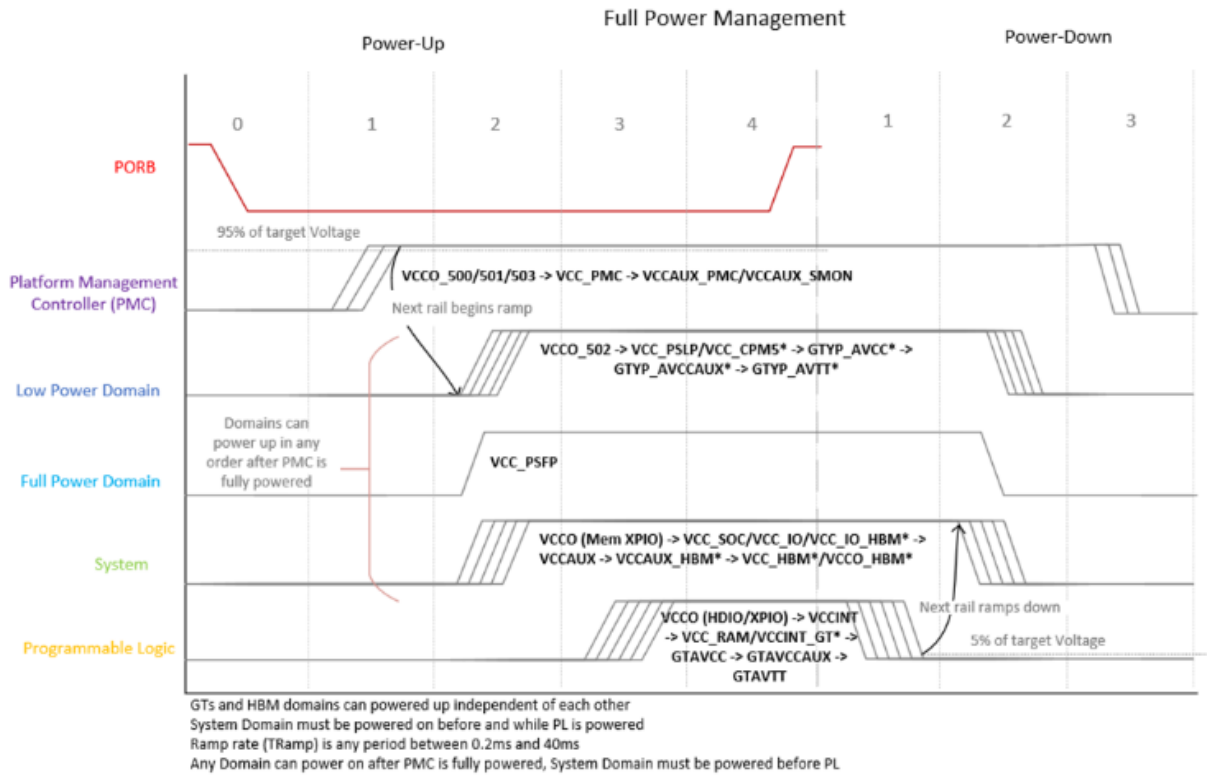

Figure 21 – Versal Power-On Sequence

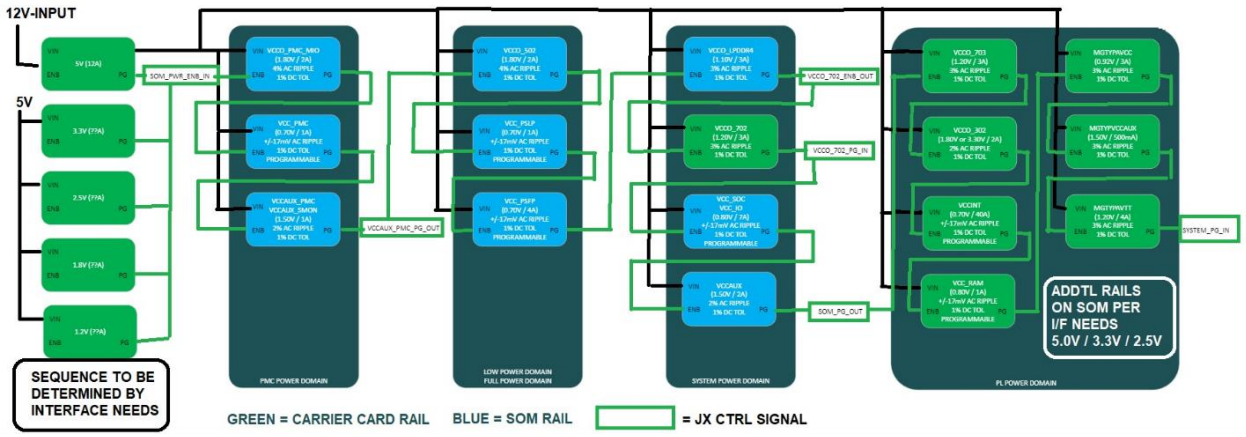

Figure 22 – Power Sequencing with End-User Carrier Card

To control the power sequencing for this power architecture, a custom power sequencer is implemented in a Renesas Greenpak device, base part number **SLG46620V**. The pre-programmed part number utilized is **SLG7A46723V** which is a custom designed power sequencer from Tria Technologies that can control the power-up and power-down sequence of up to 9 power supplies utilizing a single control signal. The power sequencer waits for the **SOM_PWR_ENB_IN** from the end-user carrier card to start the VE2302 SOM power-up sequence. If the **SOM_PWR_ENB_IN** signal from the end-user carrier card is de-asserted, the power sequencer will begin bringing down the power supplies in the reverse order.

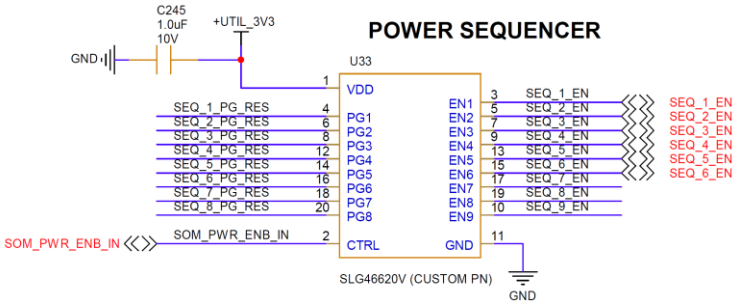

Figure 23 – Custom Power Sequencer Circuit

As you can see from Figure 22, as the power-up sequence progress, the VE2302 SOM will provide a **+VCCAUX_PMC** signal to the end-user carrier card this it can use to release the **POR_B** after the PMC power domain has been fully powered.

The VE2302 SOM power sequence progresses until it asserts the **VCCO_702_ENB_OUT** signal to the end-user carrier card. **VCCO_702_ENB_OUT** is the signal for the end-user carrier card to turn on the **+VCCO_702** rail. When the **+VCCO_702** rail is stable, it is expected that the end-user carrier card will then assert the **VCCO_702_PG_IN** signal to tell the VE2302 SOM to complete its power-up sequence.

Once the VE2302 SOM completes its power-up sequence, it will assert the **SOM_PG_OUT** signal to the end-user carrier card so that it can complete its power-up sequence. A good rule of thumb is to utilize an LED on the end-user carrier card to illuminate when the whole system power is valid. Please refer to the **Versal™ AI Edge Carrier Card Hardware User Guide** for an example of the whole system power good LED.

Signal Name	Source	JX1 Pin Number	Description
SOM_PWR_ENB_IN	Carrier Card	JX2-C32	Power enable signal to SOM after +VIN is stable.
+VCCAUX_PMC	SOM	JX2-A32	Rail for monitoring for early release of POR_B.
VCCO_702_ENB_OUT	SOM	JX2-C8	Bank 702 enable signal to Carrier Card.
VCCO_702_PG_IN	Carrier Card	JX2-D8	Bank 702 power good signal to SOM.
SOM_PG_OUT	SOM	JX1-B29	SOM power good indicator to carrier card to complete its remaining power sequence per **DS958**.

Table 37 – Power Sequencing Control Signals

2.15.3 PCB Bypass / Decoupling Strategy

The VE2302 SOM design follows the PCB decoupling strategy as outlined in **UG863** for the AMD Versal™ AI Edge Adaptive SoC in the SFVA784 package. The recommended decoupling quantities for core, auxiliary, and VCCO rails in the AMD Versal™ devices can be obtained via the (Power Design Manager) PDM tool.

2.15.4 Power Estimation Using PDM

Since the total power consumption of the system heavily depends on many factors regarding the configuration/utilization of the AMD Versal™ Adaptive SoC device, it is highly recommended that the end-user performs power estimation and analysis using the Power Design Manager (PDM). This tool is useful for plugging in various parameters and getting a power consumption estimate for the system.

When designing the VE2302 SOM architecture, the PDM tool was used to ensure that the VE2302 SOM system could supply enough power to the AMD Versal™ AI Edge device and its onboard peripherals using worst case parameters including logic utilization, operating frequency and temperature while still supporting various power modes and speed grade options.

Since the power supply for the VCCIO rails for banks 103, 104, 302, 702 and 703 are supplied from the end-user carrier card, it is important to make sure that the end-user carrier card power supplies are adequate to power these rails over the desired operating scenario.

NOTE: When designing an end-user carrier board, be sure to use PDM (Power Design Manager) to estimate the power needed by the AMD Versal Adaptive SoC device. The designer will need this figure in sizing the input power supplies to the VE2302 SOM.

NOTE: In addition to the PDM results for the Versal™ Adaptive SoC, the end user will need to add to their power estimate to compensate for the power that is needed for the on-board devices that exist on the VE2302 SOM such as the various memory, USB and Ethernet PHY devices, and serial devices.

NOTE: Beginning with the 2023.1 release, Power Design Manager (PDM) is the only supported tool for evaluating the power consumption of AMD Versal™ devices. Simply select the Import XPE File option when creating a project in PDM. All XPE project data, including resource usage and toggle rates, are migrated directly into the PDM project.

2.15.5 Speed Grades, Temperature Grades, and Operating Voltages

The AMD Versal™ AI Edge device can have voltage limits that can differ across the available speed grades,

temperature grades, and power grades. The VE2302 SOM can support the voltage requirements for the different grades with customization options for the VE2302 SOM. The customizations would require BOM changes to the off-the-shelf product including a potential change of the AMD Versal™ AI Edge device and power supply modifications.

Please contact **customize@avnet.com** to inquire about VE2302 SOMs that support the different available grades. Please refer to the Versal™ AI Edge Data Sheet (**DS958**): **Available Speed Grades and Operating Voltages** for potential customization options.

2.15.6 System Monitor (SYSMON) Interface

The AMD Versal™ AI Edge Architecture supports an on-chip system monitor. SYSMON monitors the physical environment via on-chip temperature and supply sensors with integrated analog-to-digital converters (ADC). An overview of the Versal System Monitor primitive, SYSMON, is provided by **AM006 – Versal Adaptive SoC System Monitor Architecture Manual**. The VE2302 SOM supports System Monitor functionality thru the JX connectors to a SYSMON header that would be implemented on the end-user carrier card. The VE2302 SOM contains selectable reference voltages via a 0-ohm resistor jumper.

The SYSMON interface is connected to bank 500 of the AMD Versal™ Adaptive SoC and consists of **VP**, **VN**, **VREFP, VREFN**, **VCCAUX_SMON** and **GND_SMON** pins. These pins are routed to the JX1 connector and can be used on end-user carrier cards to implement the low-speed analog interface. The SYSMON supply voltages, VCCAUX and VREF are provided on the VE2302 SOM. If not used, the SYSMON signals can be left unconnected on the end-user carrier card. The following table shows the VE2302 SOM SYSMON interface pins available on the JX1 connector.

Signal Name	JX1 Pin Number		Signal Name
SMON_AGND	A39 / C39	B39 / D39	SMON_AGND
SMON_VREF	A40	B40	SMON_V_P
SMON_V_N	C40	D40	VCCAUX_SMON

Table 38 – SYSMON Connections

Please refer to the **Versal™ AI Edge Carrier Card Hardware User Guide** for an example implementation of a SYSMON header for user by end-users.

2.15.7 Battery Backup – Device Secure Boot Encryption Key

The AMD Versal™ Adaptive SoC power rail **+VCC_BATT** is a 1.425V to 1.575V voltage supplied by a battery. This supply is used to maintain an encryption key in battery-backed RAM for device secure boot. The encryption key can alternatively be stored in eFuse which does not require a battery.

On the VE2302 SOM, **+VCC_BATT** is interfaced to the JX1 connector relying on the end-user carrier card to properly implement the battery functionality. To apply an external battery to AMD Versal™ Adaptive SoC from the end-user carrier card the proper voltage should be applied to the +**VCC _BATT** pin on the JX1 connector, JX1-PIN D27.

MIO Name	Package Pin Number	Net Name	JX1 Connector
VCC_BATT	W15	+VCC_BATT	D27

Table 39 – VCC_BATT Connection

Please refer to the **Versal™ AI Edge Carrier Card Hardware User Guide** for an example implementation of the **+VCC_BATT** interface. This circuit uses a Seiko TS621E rechargeable 1.5V lithium button-type battery soldered to the board. This battery is not populated on the Versal AI Edge Carrier Card due to shipping restrictions.

2.15.8 Thermal Management

Depending on the end-user application, the performance of the VE2302 SOM will require a thermal solution to help maintain performance across temperature.

The VE2302 SOM does not come with an example thermal solution. For the Versal™ AI Edge Development Kit, a thermal solution consisting of a 50mm heatsink and a fan assembly is utilized. This active arrangement is secured directly to the VE2302 SOM via hardware screws and nuts. An example heat-sink and fan assembly that has been tested is a skived 50mm copper BGA heat sink (**Boyd Laconia, LLC 342943**) and an active 12VDC square Fan **(Sanyo Denki America Inc 109P0512H701)** that are assembled and utilize an on-board fan header on the end-user carrier card that can provide active PWM control of the fan via from the AMD Versal™ AI Edge device.

It is expected that the end-user will be able to monitor the AMD Versal™ AI Edge device temperature via SYSMON and then actively speed up or slow down the fan speed to keep the desired temperature range. Please refer to the **VE2302 SOM Reference Design** webpage for an example design showing how to implement the control algorithm for the active-fan solution. Please refer to the **Versal™ AI Edge Hardware User Guide** for an example implementation of the fan control circuit / header.

Under most circumstances this example 50mm heat-sink and fan assembly should provide adequate relief across temperature, but it cannot be guaranteed to support all environmental conditions due to lack of knowledge regarding end-user's thermal environment and the possible enclosure of the VE2302 SOM. For aggressive applications it is recommended that an accurate worst-case power analysis be performed to avoid the pitfalls of over designing or under designing your product's power and thermal management system.

NOTE: The component selection for the SOM supports the given operating temperature. The operating temperature at the system level can be affected by carrier card design component selections, system enclosure, system air flow, etc. End-users should design a thermal management solution that is more conducive to the requirements of their system including alternative mounting techniques for the assembly which could enhance the thermal reliability of the system. It is recommended that necessary thermal system design tasks are completed prior to utilization of the SOM in the end-user application.

(TBD PHOTO)

Figure 24 – Example Heat Sink and Fan Assembly (TBD)

3 Device Bank Allocation

3.1 PMC and LPD MIO Bank Allocation

There are 78 I/O available in the PMC and LPD MIO Banks. The tables below list the number of required I/O per peripheral and the MIO locations where the interface exists.

Interface	I/O Required	Bank	MIO
OSPI FLASH	12	500	0-10,12
USB	13	500	13-25
ETHERNET	14	502	0-11, 24-25
eMMC	10	501	26-27, 29-36
I2C	2	501	50-51

Table 40 – Peripheral MIO Bank Interface Requirements

The General Purpose I/O assignments aren't specifically defined interfaces such as those that are defined in Table 35. The table below provides the MIO locations of the PMC and LPD MIO general purpose pins that support other functions.

Interface	I/O Required	Bank	MIO
MIO11_PMC_INT_B	1	500	11
MIO28_I2C_EXP_RST_B	1	501	28
General Purpose PMC_MIO	13	501	37-49
General Purpose LPD_MIO	12	502	12-23

Table 41 – GPIO MIO Bank Interface Requirements

The end-user is encouraged to utilize the **Versal™ Adaptive SoC TRM** in defining the MIO peripheral mappings that they would like to utilize on the end-user carrier card.

3.2 Device Bank Voltages

The I/O bank voltage assignments are shown in the table below.

Bank	Voltage (default)	Source
PS-Side		
MIO Bank 500	+VCCO_PMC_MIO (1.8V)	SOM
MIO Bank 501	+VCCO_PMC_MIO (1.8V)	SOM
MIO Bank 502	+VCCO_502 (1.8V)	SOM
MIO Bank 503	+VCCO_PMC_MIO (1.8V)	SOM
MIO Bank 103	+MGTYPAVCC, +MGTYPAVTT, +MGTYPVCCAUX	Carrier Card
MIO Bank 104		

PL-Side		
Bank 302	+VCCO_302 (ADJ)	Carrier Card
Bank 700	+VCCO_LPDDR4 (1.1V)	SOM
Bank 701	+VCCO_LPDDR4 (1.1V)	SOM
Bank 702	+VCCO_702 (ADJ)	Carrier Card
Bank 703	+VCCO_703 (ADJ)	Carrier Card

Table 42 – Bank Voltage Assignments

HDIO bank 302, XPIO bank702 and bank 703 are powered from the end-user carrier card. These bank supplies are designed to be independent on the VE2302 SOM. Maximum flexibility is allowed to the designer for these banks as the voltage level and standards are left to the end-user carrier card design. The designer of the end-user carrier card VCCO supplies is provided the choice of whether the IO banks use a shared voltage supply or independent voltage supplies.

When designing an end-user carrier card, please review the **Versal™ Adaptive SoC Datasheet DS958** for the appropriate supported bank voltages and tolerances.

4 Specifications and Ratings

This section contains the absolute maximum and the recommended operating ranges for SOM temperature, supply voltages, and I/O voltages. Values listed are those available at the time of publication. Users may want to consult the latest device manufacturer's specifications if their application approaches any of the limits.

4.1 Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes	Reference Document
Operating Temperature Range	0	85	°C	Commercial Temperature SOM	
Operating Temperature Range	-40	85	°C	Industrial Temperature SOM	

Table 43 – Absolute Maximum Temperature Rating

Parameter	Min	Max	Units	Notes	Reference Document
SOM					
+VIN	-0.3	6.5	V	AP7361C Limits Max	
*Sense	-	-	V	Voltage Sense outputs - Do not drive from carrier	
Versal AI Edge					
+VCC_BATT	0.5	1.65	V	Battery power supply	AMD Datasheet DS958
+VCC_FUSE	0.5	2.00	V	eFUSE programming power supply	
+VCC_RAM	0.5	0.97	V	PL RAM and clocking network power supply	
+VCCINT	0.5	0.97	V	PL primary power supply	

+VCCO_302	0.5	3.63	V	PL supply voltage for HDIO bank 302	
+VCCO_702	0.5	1.65	V	PL supply voltage for XPIO bank 702	
+VCCO_703	0.5	1.65	V	PL supply voltage for XPIO bank 703	
+MGTYPAVCC	0.5	0.97	V	GTYP supply voltage	
+MGTYPAVTT	0.5	1.65	V	GTYP termination voltage	
+MGTYPVCCAUX	0.5	1.65	V	GTYP auxiliary voltage	
Peripheral Devices					
+USB_VBUS	-0.5	6.0	V	USB supply voltage	Microchip Datasheet **USB3321**

Table 44 – Absolute Maximum Ratings for Supply Voltages

Parameter	Min	Max	Units	Notes	Reference Document
SOM Control / Handshaking					
SOM_RESET_IN_B	-0.5	3.63	V	Bank 503 POR_B	
CC_RESET_OUT_B	0	12	V	This is an open-drain output with pullup required on the carrier card.	
SOM_PWR_ENB_IN	-0.5	3.80	V	Power sequencer input – pullup required on carrier card	
+VCCAUX_PMC	-0.5	1.65	V	PMC Aux Power Supply	
VCCO_702_ENB_OUT	-0.5	3.80	V	Power sequencer output - Internal weak pullup	
VCCO_702_PG_IN	-0.5	6.5	V	Input to AND gate	
SOM_PG_OUT	-0.3	6.0	V	Pullup on SOM	
PMBUS_SDA	-0.5	7.0	V	I2C switch	
PMBUS_CLK	-0.5	7.0	V		
PMBUS_ALERT_B	-0.5	7.0	V		
CC_SDA	-0.5	7.0	V		
CC_SCL	-0.5	7.0	V		
CC_INT_B	-0.5	7.0	V		
Versal AI Edge Device					
SMON_*	-0.5	1.65	V	Bank 500	AMD Datasheet **DS958**
JTAG_*	-0.5	3.63	V	Bank 503	
MODE*	-0.5	3.63	V	Bank 503	
ERROR_OUT	-0.5	3.63	V	Bank 503	
DONE_OUT	-0.5	3.63	V	Bank 503	
SYSCLK_*	-0.5	1.65	V	Bank 702	

PMC_MIO[37:49]	-0.5	3.63	V	Bank 501	
LPD_MIO[12:23]	-0.5	3.63	V	Bank 502	
HDIO_302_*[0:10]	-0.5	3.63	V	Bank 302	
XPIO_702_*[0:23]	-0.5	1.65	V	Bank 702	
XPIO_702_L26_*	-0.5	1.65	V	Bank 702	
XPIO_703_*[0:26]	-0.5	1.65	V	Bank 703	
GTYP_103_TX*[0:3]	-0.5	1.25	V	Bank 103	
GTYP_103_RX*[0:3]	-0.5	1.25	V	Bank 103	
GTYP_103_REFCLK*	-0.5	1.35	V	AC coupled Bank 103	
GTYP_104_TX*[0:3]	-0.5	1.25	V	Bank 104	
GTYP_104_RX*[0:3]	-0.5	1.25	V	Bank 104	
GTYP_104_REFCLK*	-0.5	1.35	V	AC coupled Bank 104	
Peripheral Devices					
I2C_P[6:7]_GPIO	−0.5	4.0	V	I2C GPIO Expander	
ETH_MD*	-0.5	5.0	V		KSZ9131RNX Datasheet
ETH_ACT	-	12	V	MOSFET	
ETH_LINK	-	12	V	MOSFET	
USB_ID	-0.5	6.0	V		Microchip Datasheet USB3321
USB_D_*	-0.5	6.0	V		

Table 45 – Absolute Maximum Ratings for I/O Voltages

4.2 Recommended Operating Conditions

Parameter	Min	Max	Units	Notes	Reference Document
SOM					
VIN	4.5	6.0	V		
*Sense	-	-	V	Voltage Sense outputs - Do not drive from carrier	
Versal AI Edge					
+VCC_BATT	1.200	1.500	V	Battery power supply	AMD Datasheet DS958
+VCC_FUSE	1.745	1.854	V	eFUSE programming power supply	
+VCC_RAM *	0.775	0.825	V	PL RAM and clocking network power supply (L)	
+VCCINT *	0.676	0.724	V	PL primary power supply (L)	
+VCCO_302	1.710	3.400	V	PL supply voltage for HDIO bank 302	
+VCCO_702	0.950	1.575	V	PL supply voltage for XPIO bank 702	
+VCCO_703	0.950	1.575	V	PL supply voltage for XPIO bank 703	
+MGTYPAVCC	0.892	0.948	V	GTYP supply voltage	
+MGTYPAVTT	1.164	1.236	V	GTYP termination voltage	

+MGTYPVCCAUX	1.455	1.545	V	GTYP auxiliary voltage	
Peripheral Devices					
+USB_VBUS	0.0	5.5	V	USB supply voltage	Microchip Datasheet **USB3321**

Table 46 – Recommended Supply Voltages

Parameter	Info	Min	Max	Units	Notes	Reference Document
SOM Control / Handshaking						
SOM_RESET_IN_B	VIH	1.17	2.1	V	Bank 503 POR_B	
SOM_RESET_IN_B	VIL	-0.3	0.63	V	Bank 503 POR_B	
CC_RESET_OUT_B	Open drain	0	3.63	V	This is an open-drain output with no pullup on the SOM	
SOM_PWR_ENB_IN	VIH	1.95	3.63	V	Power sequencer input – pullup required on carrier card	
SOM_PWR_ENB_IN	VIL	0	1.28	V	Power sequencer input – pullup required on carrier card	
+VCCAUX_PMC	Output	1.455	1.545	V	PMC Aux Power Supply	
VCCO_702_ENB_OUT	VOH	2.713	3.63	V	Power sequencer output - Internal weak pullup	
VCCO_702_ENB_OUT	VOL	0	0.228	V	Power sequencer output - Internal weak pullup	
VCCO_702_PG_IN	VIH	1.17	3.63	V	Input to AND gate	
VCCO_702_PG_IN	VIL	-0.3	0.63	V	Input to AND gate	
SOM_PG_OUT	Output	0	3.63	V	Pullup on SOM	
PMBUS_SDA	VH	1.75	6.0	V	I2C Switch	
PMBUS_SDA	VL	-0.5	0.75	V		
PMBUS_CLK	VIH	1.75	6.0	V		
PMBUS_CLK	VIL	-0.5	0.75	V		
PMBUS_ALERT_B	VIH	1.75	6.0	V		
PMBUS_ALERT_B	VIL	-0.5	0.75	V		
CC_SDA	VH	1.75	6.0	V		
CC_SDA	VL	-0.5	0.75	V		
CC_SCL	VIH	1.75	6.0	V		
CC_SCL	VIL	-0.5	0.75	V		
CC_INT_B	VIH	1.75	6.0	V		
CC_INT_B	VIL	-0.5	0.75	V		
Versal AI Edge						
SMON*	I	1.455	1.545	V	Bank 500 set to 1.8V	

JTAG_TCK	I	1.71	1.89	V	Bank 503 I/O voltage set to 1.8V on SOM	AMD Datasheet **DS958**
JTAG_TDI	I	1.71	1.89	V		
JTAG_TDO	O	1.71	1.89	V		
JTAG_TMS	I	1.71	1.89	V		
MODE*	I	1.71	1.89	V		
ERROR_OUT	O	1.71	1.89	V		
DONE_OUT	O	1.71	1.89	V		
SYSCLK_*	O	0.95	1.575	V	Bank 702 – ADJ	
LPD_MIO[12:23]	IO	1.71	1.89	V	Bank 502 set to 1.8V	
PMC_MIO[37:49]	IO	1.71	1.89	V	Bank 501 set to 1.8V	
HDIO_302_L[0:10]*	IO	1.71	3.4	V	Bank 302 – ADJ	
XPIO_702_L[0:23]*	IO	0.95	1.575	V	Bank 702 - ADJ	
XPIO_702_L26*	IO	0.95	1.575	V	Bank 702 – ADJ	
XPIO_703_L[0:26]*	IO	0.95	1.575	V	Bank 703 – ADJ	
GTR_TX*/GTR_RX*	IO	0.500	1.250	V	Bank 103-104	
GTYP_REFCLK*	IO	0.500	1.350	V	AC coupled Bank 103-104	
Peripheral Devices						
I2C_P[6:7]_GPIO	O	0	1.8V	V	I2C GPIO Expander	
ETH_MD*	IO	-0.3	3.63	V		**KSZ9131RNX** Datasheet
ETH_ACT	I	-	12	V	MOSFET	
ETH_LINK	I	-	12	V	MOSFET	
USB_ID	I	0.0	3.3	V		Microchip Datasheet **USB3321**
USB_D_*	IO	0.0	3.3	V	DM/DP on USB3321	

Table 47 – Recommended Ratings for I/O Voltages

5 Mechanical Dimensions

The following figure shows the VE2302 SOM mechanical dimensions. VE2302 SOM measures 50.0mm x 50.0mm (approximately 1.97” x 1.97”). The plated mounting holes of the VE2302 SOM measure 3.0mm in diameter (approximately 0.12”).

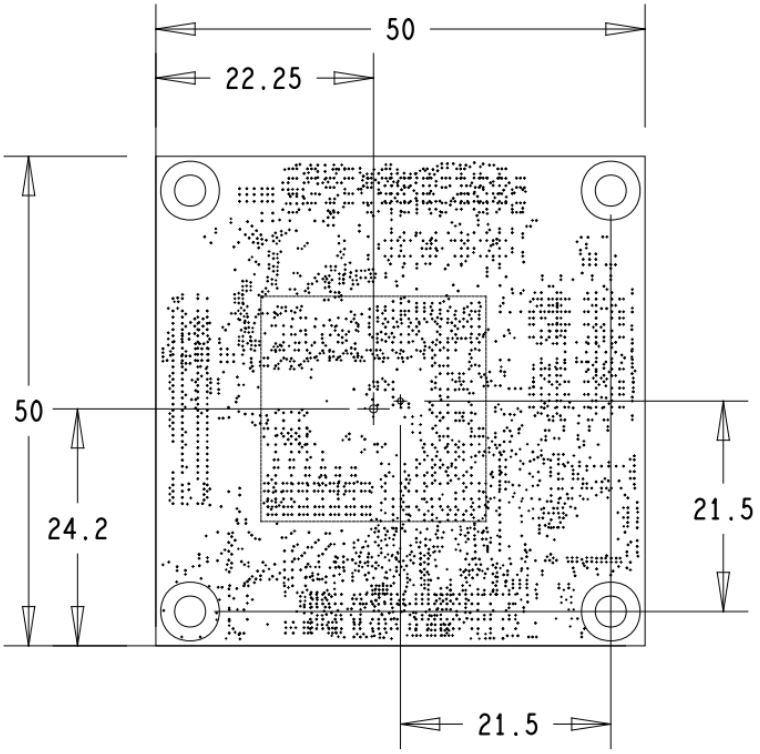

Figure 25 – Mechanical Dimensions – Top

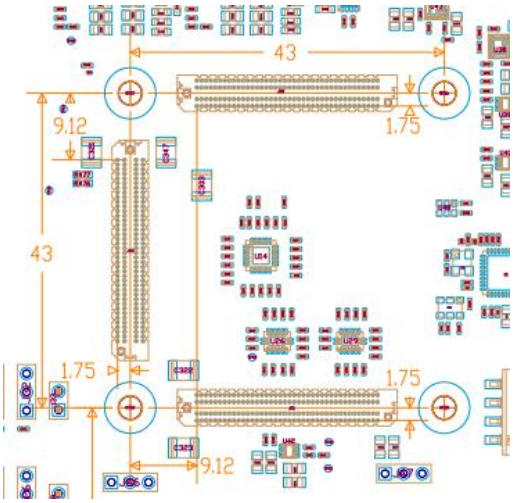

Figure 26 – Mechanical Dimensions – Bottom

The VE2302 SOM has a PCB thickness of X.XXmm +/- X.Xmm, top side maximum component height of X.XXmm and bottom side maximum component height of X.XXmm (non-JX connector) and a maximum component height of X.XXmm (JX connector).

(TBD DRAWING)

Figure 27 – Mechanical Dimensions – Height (TBD)

6 Versal™ AI Edge Development Kit

The VE2302 SOM is included in the Versal AI Edge Development Kit which is an ideal target for rapid development of applications targeting the VE2302 SOM. The Versal™ AI Edge Development Kit comes with BDF (Board Definition Files) support for the Vivado tool suite along with a Petalinux BSP to allow an end-user quick access to a reference system with embedded Linux.

NOTE: Image below is a photograph of a prototype version of the Versal™ AI Edge Development Kit. The production version of this kit may appear different from this image.

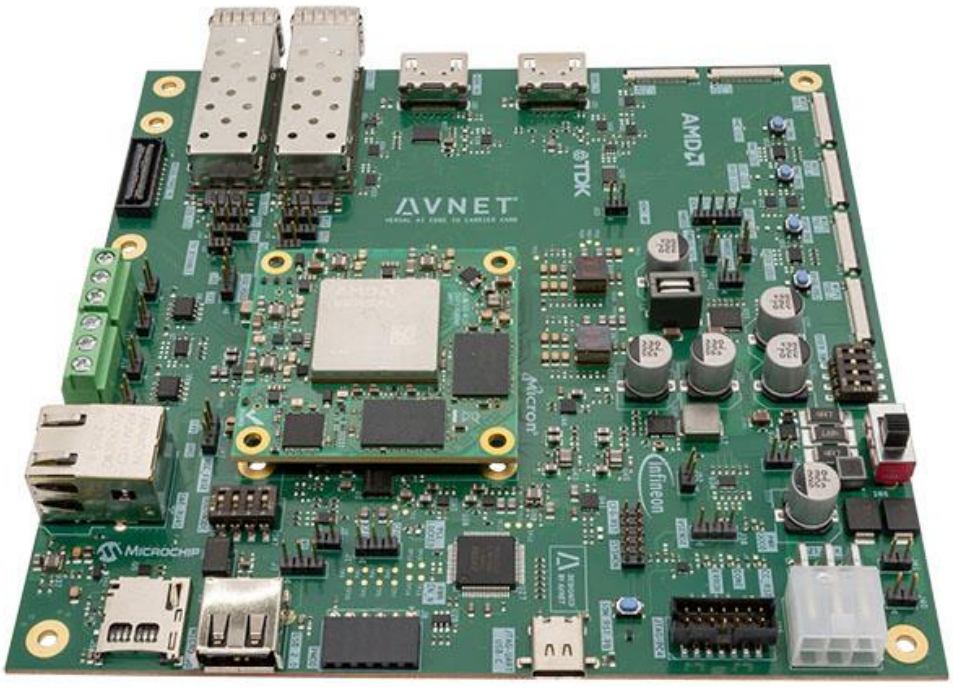

Figure 28 – Versal™ AI Edge Development Kit

7 Getting Help and Support

If additional support is required, Tria Technologies has many avenues to search depending on your needs.

For general question regarding VE2302 SOM, please visit our website at **http://avnet.me/ve2302-som**. Here you can find any available documentation, technical specifications, videos and tutorials, reference designs and other support.

For more information regarding the Versal™ AI Edge Development Kit, please visit our website at **http://avnet.me/ve2302-dk**.

Detailed questions regarding VE2302 SOM hardware design, software application development, using AMD tools, training and other topics can be posted on the VE2302 SOM Support Forum at **http://avnet.me/ve2302-som-forum**. The Tria technical support team monitors the forum during normal business hours in North America.

Those interested in customization options on VE2302 SOM can send inquiries to **customize@avnet.com**.

8 General Information

8.1 Disclaimer

Tria Technologies wants to highlight that the information presented in this user guide is subject to change, particularly due to the ongoing improvements in our product offerings. This document does not serve as a guarantee from Tria Technologies regarding the technical procedures outlined in the user guide or the product characteristics described therein. Tria Technologies holds no responsibility or liability for the use of the mentioned product(s), does not provide any licenses or rights related to patents, copyrights, or mask work rights for these products, and does not claim that these products are free from any infringements, unless explicitly stated. The applications showcased in this user guide are purely for illustrative purposes. Tria Technologies does not state that such applications are inherently suitable for the specified use without further testing or adjustments. It is essential to understand that this user guide offers a general overview of processes and instructions, which may not be universally applicable. If there are any uncertainties, please reach out to Tria Technologies.

https://tria-technologies.com

8.2 Intended Use

THIS DEVICE AND ASSOCIATED SOFTWARE ARE NOT DESIGNED, MANUFACTURED OR INTENDED FOR USE OR RESALE FOR THE OPERATION OF NUCLEAR FACILITIES, THE NAVIGATION, CONTROL OR COMMUNICATION SYSTEMS FOR AIRCRAFT OR OTHER TRANSPORTATION, AIR TRAFFIC CONTROL, LIFE SUPPORT OR LIFE SUSTAINING APPLICATIONS, WEAPONS SYSTEMS, OR ANY OTHER APPLICATION IN A HAZARDOUS ENVIRONMENT, OR REQUIRING FAIL-SAFE PERFORMANCE, OR IN WHICH THE FAILURE OF PRODUCTS COULD LEAD DIRECTLY TO DEATH, PERSONAL INJURY, OR SEVERE PHYSICAL OR ENVIRONMENTAL DAMAGE (COLLECTIVELY, “HIGH RISK APPLICATIONS”)

You understand and agree that your use of Tria Technologies devices as a component in High-Risk Applications is entirely at your risk. To minimize the risks associated with your products and applications, you should provide adequate design and operating safeguards. You are solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning your products. You are responsible to ensure that your systems (and any Tria Technologies hardware or software components incorporated in your systems) meet all applicable requirements. Unless otherwise stated in the product documentation, the Tria Technologies device is not provided with error-tolerance capabilities and cannot therefore be deemed as being engineered, manufactured or setup to be compliant for implementation or for resale as device in High-Risk Applications. All application and safety related information in this document (including application descriptions, suggested safety measures, suggested Tria Technologies products, and other materials) is provided for reference only.

Handling and operation of the product is permitted only for trained personnel within a workplace that is access controlled. Follow the “General Safety Instructions” supplied with the product.

This product is not suited for storage or operation in corrosive environments, under exposure to sulfur and chlorine and their compounds. For information on how to harden electronics and mechanics against these stress conditions, contact Tria Technologies’ Support.

8.3 RoHS Compliance

The product is designed by using RoHS compliant components and manufactured on lead free production process to IPC-A-600(*) Class 2 standards.

8.4 Electrostatic Discharge

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, to ensure product integrity at all times.

Do not handle this product out of its protective packaging while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe workstations. Where a safe workstation is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

8.5 Warranty

At the following weblink you will find information regarding warranty, RoHS compliance, and expected lifecycle information regarding these products.

Warranty Terms: **WARRANTY-AND-LIFECYCLE**