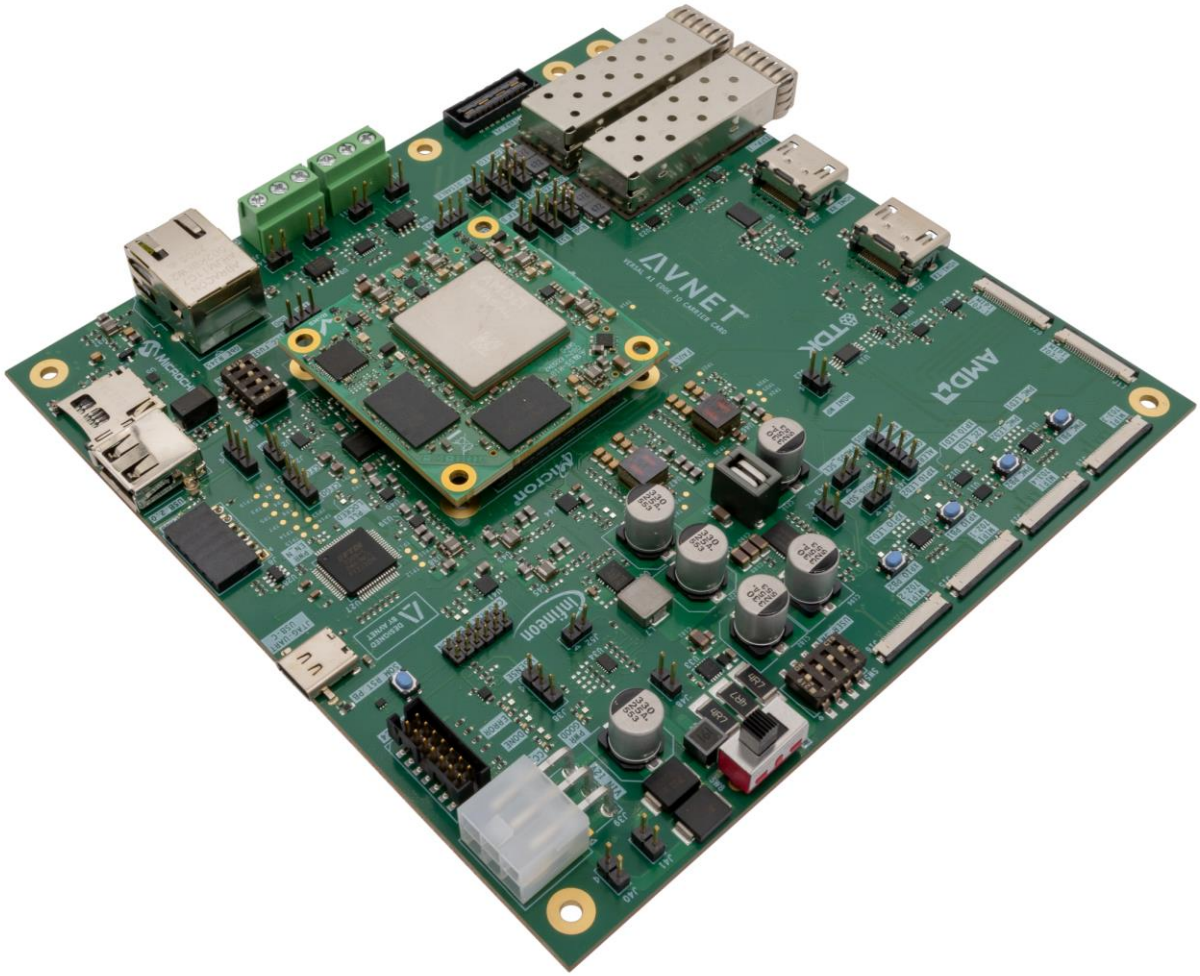

VE2302 SOM
Carrier Card Design Guide

Version 1.2

LIT# VE2302-CC-DG-V1P2

Contents

Figures

Tables

1 Document Control

Document Version: 1.2

Document Date: 5 August 2025

Document Author(s): Donny Saveski

2 Version History

Version	Date	Comment
1.0	6/13/2025	Initial Release
1.1	6/30/2025	Master JX Table Correction
1.2	8/5/2025	Master JX Table Correction

3 Introduction

This document provides guidelines for designing an end-user carrier card for the VE2302 SOM. It includes reference schematics for implementing the VE2302 SOM external peripherals as well as PCB design guidelines for the end-user carrier card.

The following table is a glossary of acronyms that could be used in description of the design guidelines for an end-user carrier card.

Term	Definition
PS	Adaptive SoC Processing System
PL	Adaptive SoC Programmable Logic
MIO	Multiplexed Input Output Pins
LPD	Low Power Domain
PMC	Platform Manager Controller
PLM	Platform Loader and Manager
POR	Power On Reset
APU	Application Processing Unit
RPU	Real-time Processing Unit
GPU	Graphics Processing Unit
SYSMON	System Monitor
ADC	Analog-to-Digital Converter
HDIO	High Density PL I/O Pins
XPIO	High Performance PL I/O Pins
PMBus	Power Management Bus
PDM	Power Design Manager
OOB	Out-of-Box

Table 1 – Glossary

3.1 Additional Information

Additional information and documentation on the AMD Versal™ Adaptive SoC can be found Here: **https://www.amd.com/en/products/adaptive-socs-and-fpgas/versal.html**

Additional information and documentation on the Tria Technologies VE2302 SOM product line can be found here: **http://avnet.me/ve2302-som**

Additional information and documentation on the Tria Technologies VE2302 Development Kit can be found here: **http://avnet.me/ve2302-dk**

4 VE2302 SOM

The Tria Technologies VE2302 SOM (System-On-Module) is a high-performance product targeted for broad use in many applications. The goal of the module is to offer a compact SOM (50mm x 50mm) solution with an AMD Versal™ AI Edge device in commercial (0C to 70C) and industrial (-40C to 85C) temperature grades for engineers to adopt in development, proof-of concept, and production designs. The features provided by the VE2302 SOM consist of:

- AMD XCVE2302-1LSESFVA784 (Pin compatible with the XCVE2202 device)
  - Pin compatible with the XCVE2102, XCVE2202, and XCVM1102
  - Primary configuration options: OSPI flash
  - Auxiliary configuration options via end user carrier card:
    - JTAG
    - microSD card
- Memory
  - LPDDR4 SDRAM (4GB, 2x32)
  - PMC OSPI Flash (Octal 256MB)
  - PMC eMMC Flash (x8 32GB)
  - I2C MAC EEPROM (2Kb)
- Interfaces
  - PMC USB 2.0 ULPI PHY (Connector required on end user carrier card)
  - Gigabit Ethernet RGMII PHY (Connector required on end user carrier card)
  - I2C 8-bit I/O Expander
  - 2-channel I2C Switch/Mux
  - 3 JX Micro-Header Connectors (3 x 160-pin)
    - 80 User XPIO Pins
    - 22 User HDIO Pins
    - 12 User LPD MIO Pins
    - 13 User PMC MIO Pins
    - 8 GTYP Transceivers
    - 4 GTYP Reference Clock Inputs
    - PMC JTAG Interface
    - PMC SYSMON interface
    - USB 2.0 Connector Interface
    - Gigabit Ethernet RJ45 Connector Interface
    - PMBus Interface
    - Carrier Card I2C Interface
    - SOM +VCC_BATT Battery Input
    - SOM Reset Input
    - Carrier Card Interrupt Input
    - Carrier Card Reset Output
    - SOM Power Good Output
    - SOM to Carrier Card Ground Pins
    - SOM Input Voltages and Output Sense Pins
  - Reference Clock
    - 33.333 MHz OSC
  - Real Time Clock (RTC)
- Power
  - On-Board Voltage Regulators
  - Custom Power Sequencer (Supports power-up and power-down sequencing)
  - Bank I/O and GTYP Transceiver Voltage Rails (Supplied via end user carrier card)

The following figure is a high-level block diagram of the VE2302 SOM and the peripherals attached to the Adaptive SoC Processing Sub-System and Programmable Logic Sub-System. The interfaces on the VE2302 SOM are divided into processing system (PS) interfaces and programmable logic (PL) interfaces. This document will describe the VE2302 SOM, its on-board resource, and external interface available to carrier cards.

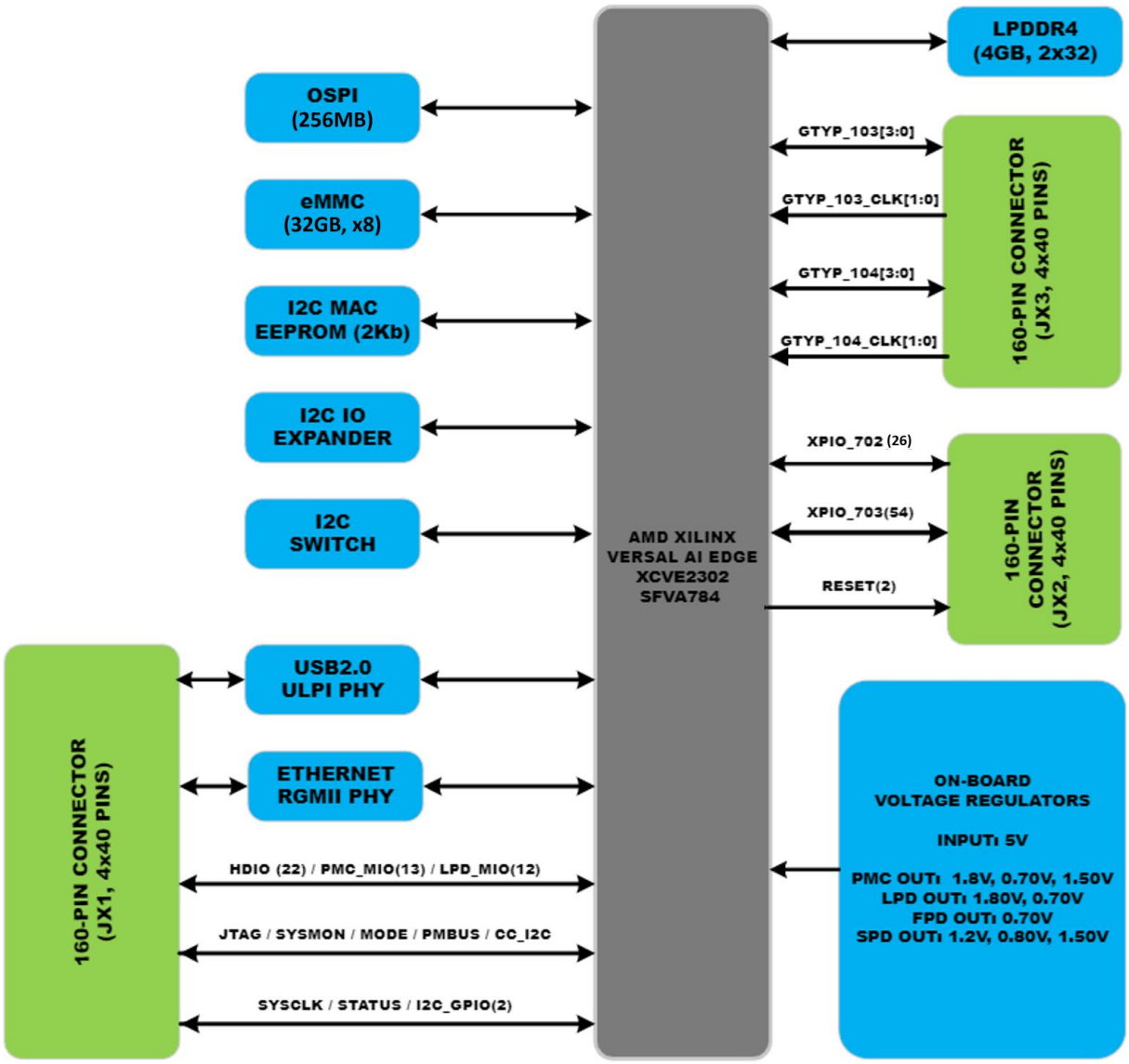

Figure 1 – VE2302 SOM Block Diagram

5 VE2302 SOM On-Board Resources

The following sections provide a brief description of each component/resource available on the VE2302 SOM.

5.1 AMD Versal™ AI Edge APSoC

The full default part number, **XCVE2302-1LSESFVA784,** populated on the VE2302 SOM. The VE2302 SOM utilizes the AMD **XCVE2302-SFVA784** device in -1 speed grade part (the VE2302 SOM is designed to support all speed grades for the **XCVE2302-SFVA784** device with customization). The **XCVE2302-SFVA784,** supports APU speed up to 1.65GHz, RPU speed up to 750MHz, and LPDDR4 speeds up to 4266Mbps. The **XCVE2302-SFVA784** device features the following resources:

- Dual-core Arm®-A72
- Dual-core Arm Cortex-R5F
- 34 AI Engine-ML Tiles
- 328,720 System Logic Cells
- 22 HD (High Density) IO pins (PL bank 302)
- 52 PMC (Platform Management Controller) MIO pins (PS bank 500 and 501)
- 26 LPD (Low Power Domain) MIO pins (PS bank 502)
- 208 XP (High Performance) IO pins (PL banks 700, 701, 702, and 703)
- 8 GTYP transceivers (PL quad 103 and 104)
- 4 GTYP reference clock inputs (PL quad 103 and 104)
- JTAG interface (PS bank 503)
- Real-Time Clock (PS bank 503)
- SYSMON interface (PS bank 500)

The following sections provide brief descriptions of how each XCVE2302 APSoC bank is used on the VE2302 SOM followed by detail descriptions in subsequent sections.

5.1.1 HDIO Bank 302

The HDIO bank 302 provides 22 HD (High Density) IO pins. These pins are routed to the **JX1** connector and are available for use by end-user carrier cards. The HDIO bank pins can be operated at 1.8V through 3.3V. The VCCO voltages for the HDIO bank are provided by the end-user carrier card via the **JX1** connector using **+VCCO_302** pins.

5.1.2 PMC MIO Bank 500

The PMC MIO bank 500 consists of 26 PMC MIO pins, **PMC_MIO[0:25]_500**. The PMC MIO pins for this bank are operated at 1.8V and used to implement the following interfaces on the VE2302 SOM:

- Octal SPI Flash
- USB2.0 ULPI PHY Interface
- System Monitor (SMON) pins

5.1.3 PMC MIO Bank 501

The PMC bank 501 consists of 26 PMC MIO pins, **PMC_MIO[26:51]_501**. The PMC MIO pins for this bank are operated at 1.8V. 12 of the PMC MIO pins are routed to the **JX1** connector and are available to end-user carrier cards. The other PMC MIO pins in this bank are used to implement the eMMC x8 Flash and PMC I2C interface.

- 12x PMC MIO Routed to JX1 Connector
- eMMC x8 Flash
- I2C MAC ID EEPROM (2Kb)
- I2C 8-Bit I/O Expander
- I2C Bus Switch

5.1.4 PMC MIO Bank 502

The PMC MIO bank 502 consists of 26 MIO pins, **LPD_MIO[0:25]_502**. The PMC MIO bank 502 pins are operated at 1.8V. 11 of the PMC MIO pins are routed to the **JX1** connector and are available to end-user carrier cards. The other PMC MIO pins in this bank are used to implement the Gigabit Ethernet RGMII PHY and MDIO interfaces.

5.1.5 PMC MIO Bank 503

The PMC MIO bank 503 is the configuration bank for the Versal™ AI Edge device. This bank contains the device power-on reset (POR_B) signal, reference clock, JTAG interface, boot mode pins, status signals ERROR_OUT and DONE_OUT, and the real-time clock oscillator inputs.

5.1.6 XPIO Bank 700-701

The XPIO banks 700 and 701 consist of the LPDDR4 interface pins. These pins are used on the VE2302 SOM to implement the LPDDR4 2x32 memory interface. The XPIO bank 700 and 701 IO are operated at 1.1V.

5.1.7 XPIO Bank 702-703

The XPIO banks 702 and 703 provides 80 XPIO pins. These pins are routed to the **JX2** connector and are available for use by end-user carrier cards. The XPIO bank pins can be operated at 1.0 through 1.5V. The VCCO voltages for the XPIO banks are provided by the end-user carrier card via the **JX2** connector using the **+VCCO_702** and **+VCCO_703** pins.

5.1.8 GTYP Quad Bank 103-104

The GTYP quads 103 and 104 consist of GTYP transceivers and their associated reference clock input pins (Device provides 8 GTYP transceivers along with 4 reference clock inputs). These pins are routed to the **JX3** connector and are available for use by end-user carrier cards.

NOTE: The GTYP transceiver power rails (**+MGTYPAVCC, +MGTYPAVTT**, and **+MGTYPVCCAUX**) are supplied by the end-user carrier card via the **JX2** and **JX3** connectors.

5.2 Reference Clock

The VE2302 SOM provides a 33.33 MHZ single-ended 1.8V reference clock input to the Versal™ AI Edge APSoC bank 503 **REF_CLK_503** pins.

5.3 Real-Time Clock

The Versal™ AI Edge device provides a built-in Real-Time Clock (RTC) function. A 32.768 KHz crystal is connected to the bank 503 **RTC_PADI** and **RTC_PADO** pins to support the RTC. The on-chip RTC uses the **+VCC_BATT** pin, that is to be provided by the end-user carrier card via **JX1** connector, for the backup battery.

5.4 I2C MAC EEPROM

The VE2302 SOM provide 2Kb of I2C EEPROM using a Microchip **AT24MAC402-MAHM** (8-pin UDFN package) device. The EEPROM device is connected to the PMC I2C bus (**PMC MIO[50:51]**) and operated with a VCC of 1.8V. This device contains a unique EUI-48 ethernet MAC address for solutions that utilize the on-board ethernet and it can be used to store system level parameters/data.

Please refer to the **VE2302 SOM Hardware User Guide** for implementation details regarding the I2C MAC EEPROM.

5.5 I2C 8-Bit IO Expander

The VE2302 SOM uses a onSemi **FXL6408UMX** (16-pin UMLP) I2C Low-Power 8-bit IO expander device for generating various resets and control signals on the VE2302 SOM. The I2C 8-bit IO expander device is connected to the PMC I2C bus (**PMC MIO[50:51]**) and operated with a VCC of 1.8V. The interrupt output (**INT#**) of the **FXL6408** device is connected to **PMC MIO[11]**. The following table shows how the I2C 8-bit IO expander ports are utilized.

NOTE: On power-up all I/O expander ports default to inputs. With the on-board pull-ups on all ports, all output reset signals shown in the following table will be in their inactive state.

IO Expander Port	Direction	Usage
GPIO0	Output	eMMC soft reset
GPIO1	Output	Gigabit Ethernet PHY soft reset
GPIO2	Input	Gigabit Ethernet PHY Interrupt
GPIO3	Output	2-Ch I2C Switch/Mux Reset
GPIO4	Input	2-Ch I2C Switch/Mux Interrupt
GPIO5	Output	Carrier Card Reset
GPIO6	Output	General Purpose IO – Port 6 (JX)
GPIO7	Output	General Purpose IO – Port 7 (JX)

Table 2 – I2C IO Expander Port Usage

Please refer to the **VE2302 SOM Hardware User Guide** for implementation details regarding the I2C 8-bit IO Expander.

5.6 2-Channel I2C Switch

The VE2302 SOM uses a 2-channel I2C switch to expand the PMC I2C bus (**PMC MIO[50:51]**). An NXP **PCA9543APW,118** (14-pin TSSOP) device is used for this interface. The use of this I2C switch provides isolation so that devices connected to the I2C bus on the VE2302 SOM and the I2C slave devices on an end-user carrier card, as well as PMBus voltage regulators are not physically placed on the same I2C bus preventing overlap.

The **PCA9543A** may also be used for voltage translation, allowing the use of different bus voltages on each SD/SC pair such that 1.8V, 2.5V, or 3.3V devices can communicate with the PMC bank 501 1.8V I2C MIO pins. This is achieved by using external pull-up resistors to pull the bus up to the desired voltage for the master and each slave channel. The **PCA9543A** has its VCC connected to 2.5V on the VE2302 SOM to support this translation.

NOTE: GPIO3 port of the I2C 8-bit IO expander can be used to soft reset the 2-channel I2C switch device. The following table shows how each **PCA9543A** channel is used on the VE2302 SOM.

NOTE: An end-user carrier card should place inline jumpers on SC1/SD1 to allow downstream voltage regulators on the PMBus to be removed from circuit. This would allow-end user carrier cards to implement third-part programming headers and avoid contention with the VE2302 SOM.

I2C Switch Channel	Usage	Note
Master Channel (SDA/SCL/INT)	This channel is connected to the PMC I2C port, MIO [51:50] and operated at 1.8V. The master INT_N output is connected to the GPIO4 port of the I2C 8-bit IO expander.	Pulled-up to 1.8V On the SOM
Slave Channel 0 (SD0/SC0/INT0)	This channel is connected to the JX1 connector (CC_SDA, CC_SCL, and CC_INT_N signals) to allow slave I2C devices on a carrier card to be virtually placed on the same PMC I2C bus (MIO [51:50]) as the I2C devices on the VE2302 SOM so that software can use a single PMC I2C core to communicate with I2C devices in the system.	Pulled-up to 1.8V, 2.5V, or 3.3V On the Carrier Card
Slave Channel 1 (SD1/SC1/INT1)	This channel is connected to the PMBus (PMBUS_SDA and PMBUS_SCL signals) of the VE2302 SOM. It is used to control/monitor PMBus voltage regulators on end-user carrier cards (the PMBus is connected to carrier cards via the JX1 connector). This feature allows the PMC I2C to control/monitor the PMBus voltage regulators used on end-user carrier cards for the purpose of power management and/or measurements.	Pulled-up to 1.8V, 2.5V, or 3.3V On the Carrier Card

Table 3 – I2C Switch Channel Usage

Please refer to the **VE2302 SOM Hardware User Guide** for implementation details regarding the 2-Channel I2C Switch.

5.7 LPDDR4 SDRAM

The VE2302 SOM provides 4GB of LPDDR4 memory in a 2x32 configuration using 2 Micron **MT53E512M32D1ZW-046 IT:B** (200-pin BGA package) x32 devices. The LPDDR4 devices are implemented in 512Mb x 32 configuration and supports up to 3200Mbps. The LPDDR4 devices are connected to the XPIO banks 700 and 701 and operated at 1.1V at the maximum supported bandwidth available in the PIN EFFICIENT implementation on the Versal™ AI Edge device.

Please refer to the **VE2302 SOM Hardware User Guide** for implementation details regarding the LPDDR4 SDRAM interface.

5.8 Octal SPI Flash

The VE2302 SOM provides 256MB of Octal SPI (OSPI) flash in a single (x8) configuration. One Micron **MT35XU512ABA1G12-0AAT** OSPI Flash device is used to implement the interface on the VE2302 SOM. The OSPI Flash device is connected to the PMC MIO bank 500 and operated at 1.8V. The OSPI Flash can be used as a primary boot device on the Versal VE2302 SOM. Please refer to the **AM011** (Versal Adaptive SoC Technical Reference Manual) for more information.

Signal Name	Description	Bank 500 SoC Pin	MIO
MIO0_OSPI_CLK	OSPI Serial Clock	AA1	MIO_0
MIO1_OSPI_IO0	OSPI Data [0]	AB1	MIO_1
MIO2_OSPI_IO1	OSPI Data [1]	AD1	MIO_2
MIO3_OSPI_IO2	OSPI Data [2]	AE1	MIO_3
MIO4_OSPI_IO3	OSPI Data [3]	AF1	MIO_4
MIO5_OSPI_IO4	OSPI Data [4]	AG1	MIO_5
MIO6_OSPI_DS	OSPI Data Strobe	AH2	MIO_6
MIO7_OSPI_IO5	OSPI Data [5]	AG2	MIO_7
MIO8_OSPI_IO6	OSPI Data [6]	AE2	MIO_8
MIO9_OSPI_IO7	OSPI Data [7]	AD2	MIO_9
MIO10_OSPI_CS_B	OSPI Chip Select Input	AC2	MIO_10
MIO12_OSPI_RST_B	OSPI Reset Input	AA3	MIO_12

Table 4 – Octal SPI Flash Pin Assignments

Please refer to the **VE2302 SOM Hardware User Guide** for implementation details regarding the OSPI Flash interface.

5.9 eMMC Flash

The VE2302 SOM provides 32GB of eMMC Flash to be used as a on-board storage. A single Micron **MTFC32GAZAQHD IT** (153-pin VFBGA package) device is used to implement the eMMC Flash x8 interface. The eMMC device is connected to the PS MIO bank 501 and operated at 1.8V. GPIO0 port of the VE2302 SOM I2C 8-bit IO expander can be used to soft reset the eMMC device.

Signal Name	MIO Pin Number	Notes
CLK	PMC_MIO26	eMMC Clock
DATA7	PMC_MIO27	eMMC DATA[7]
CMD	PMC_MIO29	eMMC Command
DATA0	PMC_MIO30	eMMC DATA[0]
DATA1	PMC_MIO31	eMMC DATA[1]
DATA2	PMC_MIO32	eMMC DATA[2]
DATA3	PMC_MIO33	eMMC DATA[3]
DATA4	PMC_MIO34	eMMC DATA[4]
DATA5	PMC_MIO35	eMMC DATA[5]
DATA6	PMC_MIO36	eMMC DATA[6]

Table 5 – eMMC Flash Interface Pin Assignments

Please refer to the **VE2302 SOM Hardware User Guide** for implementation details regarding of the eMMC flash interface and the use of port 0 of the I2C 8-bit IO Expander as a soft reset.

5.10 USB 2.0 PHY

The VE2302 SOM provides a single USB 2.0 PHY interface using the Microchip **USB3321C** USB 2.0 ULPI PHY in a 25-pin WLCSP package in industrial temperature range. The USB 2.0 ULPI PHY connector side (connected to the **JX1** connector) can be used on end-user carrier cards to implement a USB 2.0 interface with a single connector.

The USB peripheral is connected through **PMC MIO [13-25]** in MIO Bank 500 and operated at 1.8V. The USB Reset signal is active-low and signal is connected to **PMC MIO [13]** to soft reset the USB 2.0 ULPI PHY.

Signal Name	Description	SoC Bank	MIO	USB Pin
DATA[7:0]	USB Data lines	MIO Bank 500	14:17,19:22	D[7:0]
CLKOUT	USB Clock	MIO Bank 500	18	A5
DIR	ULPI DIR output signal	MIO Bank 500	23	A4
STP	ULPI STP input signal	MIO Bank 500	24	A3
NXP	ULPI NXT output signal	MIO Bank 500	25	B5
DP	DP pin of USB Connector	N/C	N/C	E1
DM	DM pin of USB Connector	N/C	N/C	D1
ID	ID pin of the USB connector	N/C	N/C	B1
RESET_B	Soft Active-Low Reset	MIO Bank 500	13	B2

Table 6 – ULPI Pin Assignment and Definitions

Please refer to the **VE2302 SOM Hardware User Guide** for implementation details regarding the USB ULPI PHY interface to the **JX1** connector.

5.11 Ethernet PHY

The VE2302 SOM provides a single Gigabit Ethernet PHY interface using the Microchip **KSZ9131RNXU** RGMII PHY device in 48-pin QFN package in industrial temperature range. The VE2302 SOM Gigabit Ethernet PHY connector side (connected to the **JX1** connector) along with an RJ45 GbE jack located on the end-user carrier card will be used to implement the Gigabit Ethernet port.

The Microchip **KSZ9131RNXU** RGMII Ethernet PHY host side IO is connected to the LPD MIO bank 502 and operated at 1.8V. GPIO1 Port of the I2C 8-bit IO expander can be used to soft reset the Gigabit Ethernet PHY while GPIO2 port of the I2C 8-bit IO expander can be used for the Gigabit Ethernet PHY Interrupt (INT) output.

Signal Name	SoC Pin
LPD_MIO25_GEM0_MDIO	Y9
LPD_MIO24_GEM0_MDC	Y8
LPD_MIO11_GEM0_RX_CTL	Y3
LPD_MIO10_GEM0_RXD3	V3
LPD_MIO9_GEM0_RXD2	U3
LPD_MIO8_GEM0_RXD1	T3
LPD_MIO7_GEM0_RXD0	U2
LPD_MIO6_GEM0_RX_CLK	V2
LPD_MIO5_GEM0_TX_CTL	W2
LPD_MIO4_GEM0_TXD3	Y2
LPD_MIO3_GEM0_TXD2	Y1
LPD_MIO2_GEM0_TXD1	W1
LPD_MIO1_GEM0_TXD0	U1
LPD_MIO0_GEM0_TX_CLK	T1
P1_GEM0_RST_B	N/C

Table 7 – Ethernet RGMII Pin Assignments

6 VE2302 SOM External Resources

The VE2302 SOM provides sufficient resources to end-user carrier cards to implement fully customized systems that meet their application requirements. The VE2302 SOM provides the following external interfaces to end-user carrier cards (signal directions are with respect to the VE2302 SOM) via three JX Micro Headers.:

- 80 User XPIO Pins
- 22 User HDIO Pins
- 12 User LPD MIO Pins
- 13 User PMC MIO Pins
- 8 GTYP Transceivers
- 4 GTYP Reference Clock Inputs
- System Reference Clock Inputs
- USB 2.0 Connector Interface
- Gigabit Ethernet RJ45 Jack Interface
- PMBus Interface
- Carrier Card I2C Interface
- SOM Boot Mode Interface
- SOM JTAG Interface
- SOM SYSMON interface
- SOM Reset Input
- SOM Status Signals
- Carrier Card Interrupt Input
- Carrier Card Reset Output
- SOM Input Voltages and Output Sense Pins
- Power Sequencing Control Signals

- SOM Power Good Output
- SOM Battery Input

The following tables summarize connections to the VE2302 SOM JX Micro Header Connectors to external interfaces.

Micro Header JX1			
Interface	**Signal Name**	**Source**	**Pins**
PMC	Bank 502 PMC MIO	Bank 502	12
	Bank 501 PMC MIO	Bank 501	13
	JTAG_TMS, JTAG_TCK, JTAG_TDI, JTAG_TDO ERROR_OUT DONE_OUT MODE[0:3]	Bank 503	10
PL I/O	Bank 302 Differential Pair I/Os	Bank 302	22
	SYSCLK_P/N	Bank 702	2
Comms	I2C_P6_GPIO, I2C_P7_GPIO	I2C Expander	2
	USB2.0 PHY Interface	USB PHY	4
	Gigabit Ethernet PHY Interface	ETH PHY	10
SYSMON	SMON_V_P, SMON_V_N SMON_VREF VCCAUX_SMON GND_SMON	Bank 500	8
Control	PMBus	I2C Switch	3
	CC I2C BUS	I2C Switch	3
	SOM_PG_OUT	VE2302 SOM	1
Power	GND	Carrier Card	39
	+VCC_BATT		1
	+VCC_FUSE		1
	+VCC_RAM and VCC_RAM_SENSE		2
	+VCCO_302 and VCCO_302_SENSE		3
	+VCCO_502	VE2302 SOM	1
	+VCCO_PMC_MIO	VE2302 SOM	1
	VCCINT_SENSE and GND_SENSE	VE2302 SOM	2
	+VCCINT	Carrier Card	20

Table 8 – Micro Header JX1 Summary

Micro Header JX2			
Interface	**Signal Name**	**Source**	**Pins**
PL	Bank 702 Differential Pair I/Os	Bank 702	28
	Bank 702 – DDRMC Do Not Connect	Bank 702	24
	Bank 703 Differential Pair I/Os	Bank 703	52
Control	SOM_RESET_IN_B, SOM_PWR_ENB_IN, VCCO_702_PG_IN	Carrier Card	3
	VCCO_702_ENB_OUT, CC_RESET_OUT_B	VE2302 SOM	2
Power	GND	Carrier Card	28
	+VCCO_702		2
	+VCCO_703		2
	+MGTYPAVCC		3
	+MGTYPVCCAUX		2
	+VCCAUX_PMC	VE2302 SOM	1
	VCCO_702_SENSE, VCCO_702_SENSE, MGTYPVCCAUX_SENSE, MGTYPAVCC_SENSE, MGTYPAVTT_SENSE		5
	+VCCINT	Carrier Card	8

Table 9 – Micro Header JX2 Summary

Micro Header JX3			
Interface	**Signal Name**	**Source**	**Pins**
GTYP	Bank 103 Differential Pair I/Os	Bank 103	20
	Bank 104 Differential Pair I/Os	Bank 104	20
Power	GND	Carrier Card	92
	+MGTYPAVTT		3
	VIN_SENSE	VE2302 SOM	1
	+VIN	Carrier Card	12
	+VCCINT		12

Table 10 – Micro Header JX3 Summary

The following table shows the VE2302 SOM external interfaces with a brief description of each interface.

Signal Name	# of Pins	Description
LPD_MIO[12:23]	12	**LPD MIO Interface** – 12 LPD MIO pins from bank 502.
PMC_MIO[37:49]	13	**PMC MIO Interface** – 13 PMC MIO pins from bank 501.
USB_D_P, USB_D_N, USB_ID, USB_VBUS,	4	**USB 2.0 PHY Interface** – These pins are used by end-user carrier cards to implement a USB 2.0 interface. Please refer to the USB3321 datasheet for AC and DC spec of these signals.
ETH_MD[1:4]_P, ETH_MD[1:4]_N, ETH_ACT, ETH_LINK,	10	**Gigabit Ethernet PHY Interface** – These pins are used by end-user carrier cards to implement a Gigabit Ethernet interface. Please refer to the KSZ9131 datasheet for AC and DC spec of these signals.
GTYP_10[3:4]_TX[0:3]_P, GTYP_10[3:4]_TX[0:3]_N, GTYP_10[3:4]_RX[0:3]_P, GTYP_10[3:4]_RX[0:3]_N, GTYP_10[3:4]_REFCLK[0:1]_P, GTYP_10[3:4]_REFCLK[0:1]_N	40	**GTYP Transceivers Interface** – The transceiver data and clock signals are used by the end-user carrier cards to implement various multi-gigabit interfaces. Please refer to the Xilinx DS958 (Versal AI Edge SoC DataSheet) datasheet for AC and DC spec of these signals.
CC_SDA, CC_SCL, CC_INT_B	3	**Carrier Card I2C Interface** – This I2C interface will be used to interface to end-user carrier cards I2C slave devices.
XPIO_702_* XPIO_703_*	80	**XPIO User Interfaces** – These pins are connected to the PL banks 702 and 703. These signals can be used by end-user carrier cards as single-ended or differential pairs. Please refer to the Xilinx AM010 and DS958 for more information on the XPIOs.
HDIO_302_*	22	**HDIO** – These pins are connected to the HDIO bank 302. These signals can be used by end-user carrier cards as single-ended or differential pairs. Please refer to the Xilinx AM010 and DS958 for more information on the HDIOs.
JTAG_TMS, JTAG_TCK, JTAG_TDI, JTAG_TDO	4	**JTAG Interface** – These pins are used to interface to the APSoC JTAG port and driven by a JTAG cable on end-user carrier cards.
SMON_V_P, SMON_V_N, SMON_VREF, VCCAUX_SMON, SMON_AGND (x4)	8	**SYSMON Interface** – End-user carrier cards can use these pins to drive low speed analog signals into the System Monitor interface. Please refer to the Xilinx AM006 and DS958 for more information on the System Monitor interface.
PMBUS_DATA, PMBUS_CLK, PMBUS_ALERT_B	3	**PMBus Interface** – This PMBus interface is used to program and/or monitor the PMBus voltage regulators on end-user carrier cards (optional).
I2C_P6_GPIO, I2C_P7_GPIO	2	**I2C Expander GPIO** – These pins are connected to the I2C 8-Bit IO Expander. These signals can be used end-user carrier cards as single-ended input or output signals.
MODE[0:3]	4	**Boot Mode Signals** – These signals are used to select the primary boot device.
SYSCLK_P, SYSCLK_N	2	**System Reference Clock** – 200MHz LVDS oscillator sourced by the end-user carrier card and used by LPDDR4 interface.

ERROR_OUT	1	**Bank 503 Error Signal** – 1.8V sourced by the SOM indicating a boot error occurred.
DONE_OUT	1	**Bank 504 Done Signal** – 1.8V sourced by the SOM indicating configuration complete.
SOM_RESET_IN_B, CC_RESET_OUT_B	2	**Reset Signals** – These reset signals are used to reset the SOM or the devices on end-user carrier cards.
+VCCO_302	2	**Bank 302 VCCO** – 1.8 to 3.3V sourced by the end-user carrier cards dependent on interface implementation.
+VCCO_702	2	**Bank 702 VCCO** – 1.0 to 1.5V sourced by the end-user carrier card dependent on interface implementation.
+VCCO_703	2	**Bank 703 VCCO** – 1.0 to 1.5V sourced by the end-user carrier card dependent on interface implementation.
+MGTYPAVCC	3	**GTYP Core Voltage** – 0.92V sourced by the end-user carrier card if GTYPs are implemented.
+MGTYPAVTT	3	**GTYP Termination Voltage** – 1.2V sourced by the end-user carrier card if GTYPs are implemented.
+MGTYPVCCAUX	2	**GTYP Auxiliary Core Voltage** – 1.5V sourced by the end-user carrier card if GTYPs are implemented.
+VCCINT	40	**SOM VCCINT Power** – 0.70V (or 0.80V, 0.88V) sourced by the end-user carrier card. Proper regulator sizing is dependent on end-user design implementation. Please reference AMD Power Design Manager (PDM) for proper estimating of needs for this regulator.
+VCC_RAM	1	**SOM RAM VCC** – 0.80V (or 0.88V) sourced by the end-user carrier card due to proper sequencing requirements and desire to limit unnecessary handshaking between SOM and carrier card.
+VCC_BATT	1	**VBATT Input** – 1.5V sourced by the end-user carrier card to support battery backup functionality.
+VCC_FUSE	1	**eFUSE Input** – 1.8V (or 0V) sourced by the end-user carrier cards to support eFuse functionality.
+VCCO_PMC_MIO	1	**SOM PMC MIO VCCO** – 1.8V sourced by the VE2302 SOM to provide proper reference voltage to carrier card interfaces.
+VCCAUX_PMC	1	**SOM PMC VCCAux** – 1.5V sourced by the VE2302 SOM and is used in determination of release point of SOM_RESET_IN_B (POR_B) control signal.
+VCCO_502	1	**Bank 502 VCCO** – 1.8V sourced by the VE2302 SOM to provide proper reference voltage to carrier card interfaces.
MGTYPAVCC_SENSE, MGTYPAVTT_SENSE, MGTYPVCCAUX_SENSE, VCCO_302_SENSE, VCCO_702_SENSE, VCCO_703_SENSE, VCC_RAM_SENSE, VCCINT_SENSE, VIN_SENSE, GND_SENSE	10	**Voltage Sense Feedback** – These output pins are used by end-user carrier cards to compensate for the voltage loss across the JX connectors by providing feedback at the termination point of the load.

SOM_PG_OUT	1	SOM Power Good Output – This signal is used to enable the end-user carrier card voltage regulators.
GND	159	**Ground Pins**
+VIN	12	**Main Input Voltage** – 5V DC.

Table 11 – VE2302 SOM External Interface Signals

6.1 SYSMON Header

The SYSMON interface is connected to bank 500 of the Versal™ APSoC and consists of **VP**, **VN**, **VREF**, **VCCAUX** and **AGND** pins. These pins are routed to the **JX1** connector and can be used on end-user carrier cards to implement low speed analog interfaces. The SYSMON supply voltages, **VCCAUX** and **VREF** are provided on the VE2302 SOM. If not used, the SYSMON signals can be left unconnected on the end-user carrier card.

The following table shows the VE2302 SOM SYSMON interface pins available on the JX1 connector.

Signal Name	JX1 Pin Number		Signal Name
SMON_AGND	A39 / C39	B39 / D39	SMON_AGND
SMON_VREF	A40	B40	SMON_V_P
SMON_V_N	C40	D40	VCCAUX_SMON

Table 12 – SYSMON Interface Pin Assignments

Please refer to the **Versal™ AI Edge Carrier Card Hardware User Guide** for example implementation details regarding the SYSMON interface to the **JX1** connector.

6.2 System Clock

The VE2302 SOM requires a differential clock be provided to it from the end-user carrier card to support LPDDR4 implementation. The end-user carrier card shall provide a 200MHz LVDS differential pair to the bank 702 **SYSCLK_P/N** differential pins to the **JX1** connector.

JX1 Pin Number	Signal Name	APSoC Pin Number
D14	SYSCLK_P	Bank 702 – N23
D15	SYSCLK_N	Bank 702 – N24

Table 13 –System Clock Interface Pin Assignments

As an example, the Versal™ AI Edge Carrier Card implements a 200MHz LVDS oscillator:

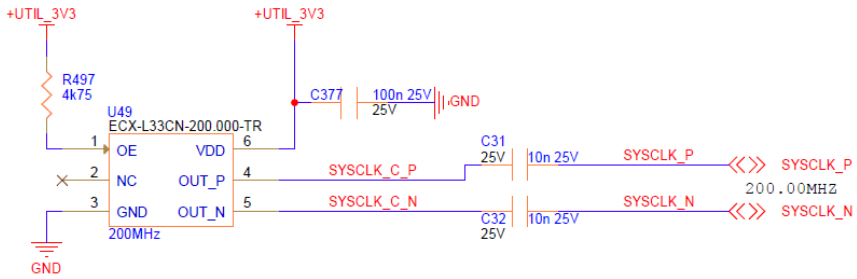

Figure 2 – Example System Clock Schematic

NOTE: The following figure shows the VE2302 SOMs implementation of the termination scheme for the system clock differential pair, **SYSCLK_P/N**.

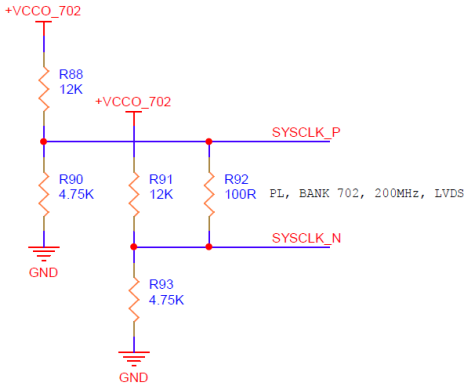

Figure 3 –System Clock SOM Termination Schematic

6.3 Boot Mode Interface

The VE2302 SOM routes the boot mode pins to the **JX1** connector. End-user carrier cards should implement a method to control the boot mode pins. An example is provided in the figure below of a small 4-position DIP switch is used to provide control of the boot mode pins. The switch is connected to the **MODE[0:3]** pins of the **JX1** connector and allows users to select the primary boot device.

The **MODE[0:3]** signals are referenced to **+VCCO_PMC_MIO** voltage rail which is provided on the **JX1** connector.

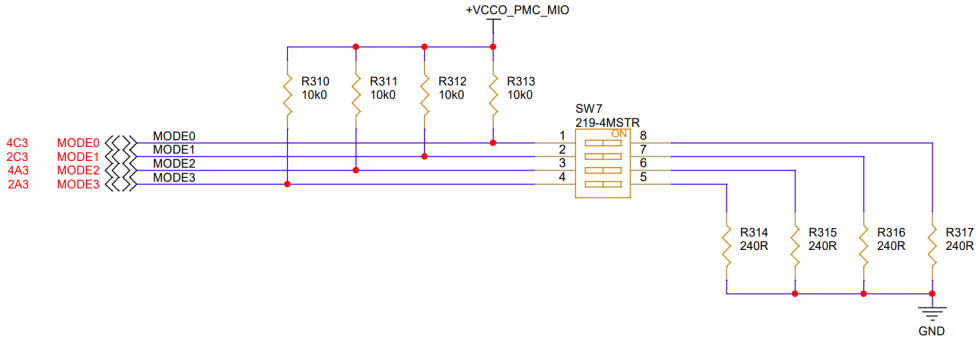

Figure 4 – Example Boot Mode Switch Schematic

BOOT MODE	MODE PIN[3:0]	SW7[1-4]
JTAG	0x0	ON-ON-ON-ON
SD0/3.0 AUTODIR	0x3	ON-ON-OFF-OFF
OSPI	0X8	OFF-ON-ON-ON

Table 14 – Supported Boot Modes

Signal Name	JX1 Pin Number		Signal Name
MODE0	A35	B35	MODE1
MODE2	C35	D35	MODE3

Table 15 – Boot Mode Interface Pin Assignments

6.4 JTAG Interface

The VE2302 SOM routes the JTAG interface to the **JX1** connector. End-user carrier card must provide the JTAG to the VE2302 SOM to ensure debug and programming capability. The JTAG interface pull-ups and series termination resistors will exist on the end-use carrier card. The JTAG TCK line has an RC (two-footprints) routed on the VE2302 SOM near the Versal™ AI Edge device.

End-user carrier cards can implement the JTAG interface using JTAG header interfaces such as the Xilinx PC4 header, a USB-JTAG module such as the Digilent SMT2 module or designing the JTAG interface using chip-down methods such as with an FTDI device.

The JTAG interface on end-user carrier cards must drive the JTAG interface on the **JX1** connector with 1.8V IO signaling. The following table shows the VE2302 SOM JTAG interface pins available on the JX1 connector.

The JTAG interface signals are referenced to **+VCCO_PMC_MIO** voltage rail which is provided on the **JX1** connector.

Signal Name	JX1 Pin Number		Signal Name
JTAG_TCK	A37	B37	JTAG_TMS
JTAG_TDI	C37	D37	JTAG_TDO

Table 16 – JTAG Interface Pin Assignments

Please refer to the **Versal™ AI Edge Carrier Card Hardware User Guide** for an example implementation of a USB JTAG-UART with a PC4 header tied to the VE2302 SOM JTAG interface.

6.5 Status Signals

The VE2302 SOM routes two status signals to the **JX1** connector. End-user carrier card should implement a method to monitor and/or respond to status signals. The **two status** signals are referenced to **+VCCO_PMC_MIO** voltage rail which is provided on the **JX1** connector.

As an example, the Versal™ AI Edge Carrier Card implements a Blue Diffused 2SMD LED (**D36**) indicating the configuration complete. The **DONE_OUT** signal is a 1.8V signal and care must be taken to ensure that the LED illuminates properly.

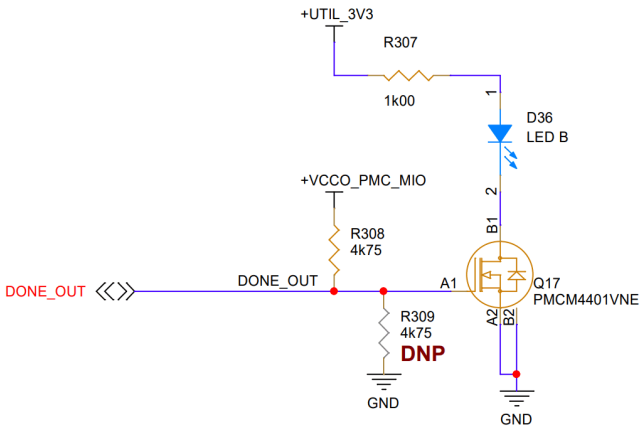

Figure 5 – DONE_OUT LED Schematic

I/O Net Name	JX Connector
DONE_OUT	JX1-D28

Table 17 – DONE_OUT LED Pin Assignment

Similarly, as an example, the Versal™ AI Edge Carrier Card implements an **ERROR_OUT** Red Diffused 2SMD LED (**D37**). The **ERROR_OUT** signal is a 1.8V signal and care must be taken to ensure that the LED illuminates properly.

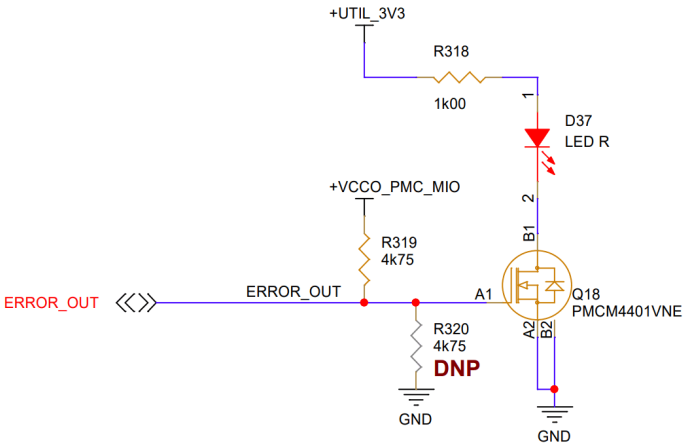

Figure 6 – ERROR_OUT LED Schematic

I/O Net Name	JX Connector
ERROR_OUT	JX1-D13

Table 18 – ERROR_OUT LED Pin Assignment

6.6 Power-On Reset

The Power-On Reset (**POR_B**) circuit for the AMD Versal™ AI Edge device is required to be implemented

on the end-user carrier card. The **POR_B** is an active-low input signal to the AMD Versal™ AI Edge device that acts as a master reset. The signal name associated with **POR_B** port on the AMD Versal™ AI Edge device is **SOM_RESET_IN_B** and that signal is provided on the **JX2** connector (**Pin JX2-B32**). The VE2302 SOM does provided a 10K-ohm pull-up to **+VCCO_PMC_MIO** (1.8V) on **SOM_RESET_IN_B**. The **SOM_RESET_IN_B** signal is referenced to **+VCCO_PMC_MIO** voltage rail which is provided on the **JX1** connector.

Please refer to the **Versal™ AI Edge Carrier Card Hardware User Guide** for an example implementation of **SOM_RESET_IN_B** control.

The external reset, **SOM_RESET_IN_B**, can reset the end-user carrier card thru an open-drain signal on the J**X2** connector, **CC_RESET_OUT_B**. The VE2302 SOM is also capable of issuing a soft reset to the end-user carrier card by asserting Port 5 of the I2C I/O Expander, **P5_CC_RST_B**, using the VE2302 SOM two-wire serial interface. This will soft reset the end-user carrier card thru the same open-drain signal on the **JX2** connector (**Pin JX2-C14**), **CC_RESET_OUT_B**.

NOTE: Gate U16 re[resents a logic NAND function.

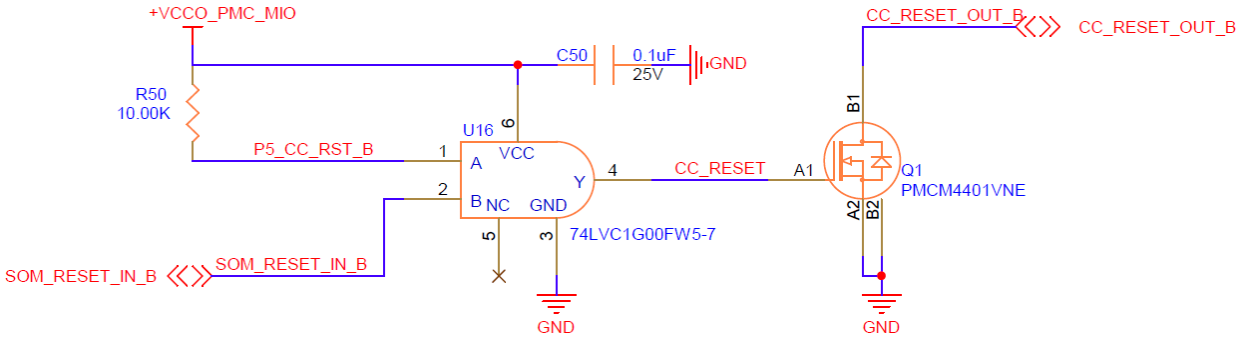

Figure 7 – Carrier Card Output Reset Circuit

Please refer to the **VE2302 SOM Hardware User Guide** for implementation details regarding Port 5 of the I2C 8-bit IO Expander a soft reset for end-user carrier cards.

Please refer to the **Versal™ AI Edge Carrier Card Hardware User Guide** for an example implementation of **CC_RESET_OUT_B** control.

Control Signal Name	JX2 Connector	Voltage	Active-State
SOM_RESET_IN_B	JX2-B32	+1.8V (SOM)	Low
CC_RESET_OUT_B	JX2-C14	Open-Drain to User	Low

Table 19 – Power-On Reset Pin Assignments

6.7 Carrier Card I2C Interface

The VE2302 SOM provides an isolated I2C bus (**CC_SDA**, **CC_SCL**, and **CC_INT_B**) to the end-user carrier cards via an on-board I2C switch. The carrier card I2C interface is provided to the end-user carrier card via the **JX1** connector so that software can communicate with slave I2C devices that reside on the end-user carrier card with little concern to I2C address overlap with slave I2C devices that exist on the VE2302 SOM.

The carrier card I2C interface is connected to channel 0 of the I2C 2-channel switch device on the VE2302 SOM. End-user carrier cards can drive the **INT0** of the channel 0 via **CC_INT_B** if desired. The **CC_INT_B** (an active low signal) is not specific to the I2C interface and can be used as a general-purpose interrupt from end-user carrier cards to the VE2302 SOM. If not used, the **CC_INT_B** signal must be pulled up to 1.8V, 2.5V, or 3.3V on the carrier card.

There are no I2C pullups implemented on carrier card I2C interface on the VE2302 SOM. This allows the end-user carrier card designer to tailor the I2C implementation toward the I2C bus needs on that board.

Signal Name	JX1 Pin Number		Signal Name
CC_INT_B	A25	B25	CC_SCL
CC_SDA	C29		

Table 20 – Carrier Card I2C Interface Pin Assignments

Please refer to the **VE2302 SOM Hardware User Guide** for implementation details regarding the 2-Channel I2C Switch.

6.8 PMBus Interface

The VE2302 SOM provides an isolated I2C bus (**PMBUS_SDA**, **PMBUS_SCL**, and **PMBUS_ALERT_B**) to the end-user carrier cards via an on-board I2C switch. The carrier card PMBus interface is provided to the end-user carrier card via the **JX1** connector so that software can communicate with slave PMBuS / I2C devices that reside on the end-user carrier card with little concern to I2C address overlap with slave I2C devices that exist on the VE2302 SOM.

The carrier card PMBus interface is connected to channel 1 of the I2C 2-channel switch device on the VE2302 SOM. End-user carrier cards can drive the **INT1** of the channel 0 via **PMBUS_ALERT_B** if desired. The **PMBUS_ALERT_B** (an active low signal) is not specific to the I2C interface and can be used as a general-purpose interrupt from end-user carrier cards to the VE2302 SOM. If not used, the **PMBUS_ALERT_B** signal must be pulled up to 1.8V, 2.5V, or 3.3V on the carrier card.

For PMBus based voltage regulators, after initial programming of the regulators, the VE2302 SOM can utilize the PMBus (via channel 1 of the I2C switch) to control/monitor the PMBus voltage regulators for the purpose of power management and/or monitoring.

There are no PMBus pullups implemented on carrier card PMBus interface on the VE2302 SOM. This allows the end-user carrier card designer to tailor the PMBus implementation toward the PMBus needs on that board.

Signal Name	JX1 Pin Number		Signal Name
PMBUS_ALERT_B	A26	B28	PMBUS_SDA
PMBUS_SCL	C30		

Table 21 – PMBus Interface Pin Assignments

Please refer to the **VE2302 SOM Hardware User Guide** for implementation details regarding the 2-Channel I2C Switch.

Please refer to the **Versal™ AI Edge Carrier Card Hardware User Guide** for example implementation details regarding the PMBus, PMBus programming header, and a PMBus based voltage regulator.

6.9 I2C GPIO Expander Ports

The I2C 8-bit IO expander on the VE2302 SOM provides 2 GP (General Purpose) IO pins for use on end-user carrier cards. These I2C driven general purpose pins are routed to the **JX1** connector and can be used to implement any interface that does not demand high performance. These GPIO ports are open-drain and require pull-ups be implemented on the end-user carrier card.

Please refer to the **FXL6408UMX** device datasheet for the supported voltages on the GPIO ports of the I2C 8-bit IO expander.

The following table shows the end-user carrier card I2C 8-bit expander pins available on the **JX1** connector.

Signal Name	JX1 Pin Number
I2C_P6_GPIO	C18
I2C_P7_GPIO	C19

Table 22 – IO Expander GPIO PIN Assignments

Please refer to the **VE2302 SOM Hardware User Guide** for implementation details regarding the I2C 8-bit Expander.

Please refer to the **VE2302 SOM Hardware User Guide** for an example implementation regarding the two available I2C GPIO Expander ports.

6.10 USB2.0 Connector

The physical USB connector is not populated on the VE2302 SOM. The SOM is designed to have the physical USB connector reside on the end-user carrier card. The three USB connector signals (**USB_D_P**, **USB_D_N** and **USB_ID**) and +**USB_VBUS** are connected to the **JX1** Micro Header. The table below shows the connections of these signals at JX1.

Signal Name	JX1 Pin
USB_D_P	D29
USB_D_N	D30
USB_ID	B30
+USB_VBUS	D12

Table 23 – USB2.0 PHY JX1 Pin Assignments

Please refer to the **Versal™ AI Edge Carrier Card Hardware User Guide** for example implementation details regarding the USB2.0 Type-A Connector.

6.11 RJ45 GbE Jack

The physical RJ45 GbE jack and magnetics are not populated on the VE2302 SOM. The VE2302 SOM is designed to have the physical RJ45 GbE jack and magnetics reside on the end-user carrier card. The RJ45 GbE jack connector signals are connected to the **JX1** Micro Header.

Signal Name	JX1 Pin
ETH_MD1_P	D32
ETH_MD1_N	D33
ETH_MD2_P	C32
ETH_MD2_N	C33
ETH_MD3_P	B32
ETH_MD3_N	B33
ETH_MD4_P	A32
ETH_MD4_N	A33
ETH_ACT	A29
ETH_LINK	A30

Table 24 – Ethernet PHY JX1 Pin Assignments

Please refer to the **Versal™ AI Edge Carrier Card Hardware User Guide** for example implementation details regarding the RJ45 GbE jack.

6.12 PMC MIO Interfaces

The PMC MIO interface consists of 13 PMC MIO pins (**PMC_MIO[37:49]**) connected to the PMC MIO bank 501. These MIO pins are routed to the **JX1** connector and are available for processor interface implementation on end-user carrier cards. These PMC MIO banks are operated at 1.8V and are referenced to **+VCCO_PMC_MIO** voltage.

On the Versal™ AI Edge Carrier Card, PMC MIO pins are used to implement the following interfaces:

- microSD
- Push Buttons x2
- LEDs x2

Please refer to the **Versal™ AI Edge Carrier Card Hardware User Guide** for example implementation details regarding the physical interfaces mapped to the LPD MIO pins.

Signal Name	JX1 Pin Number		Signal Name
PMC_MIO49	B19	B23	PMC_MIO42
PMC_MIO48	B20	C26	PMC_MIO41
PMC_MIO47	A19	C27	PMC_MIO40
PMC_MIO46	A20	D23	PMC_MIO39
PMC_MIO45	A22	D24	PMC_MIO38
PMC_MIO44	A23	D26	PMC_MIO37
PMC_MIO43	B22	-	-

Table 25 – PMC MIO Pin Assignments

Please review the Versal™ Adaptive SoC Technical Reference Manual (**AM011**) for interfaces that can be mapped to the 13 available PMC MIO pins.

6.13 LPD MIO Interfaces

The LPD MIO interface consists of 12 LPD MIO pins (**LPD_MIO[12:32]**) connected to the LPD MIO bank 502. These MIO pins are routed to the **JX1** connector and are available for processor interface implementation on end-user carrier cards. These LPD MIO banks are operated at 1.8V and are referenced to **+VCCO_PMC_MIO** voltage.

On the Versal™ AI Edge Carrier Card, LPD MIO pins are used to implement the following interfaces:

- CAN Interfaces x2
- I2C Interface
- UART

Please refer to the **Versal™ AI Edge Carrier Card Hardware User Guide** for example implementation details regarding the physical interfaces mapped to the LPD MIO pins.

Signal Name	JX1 Pin Number		Signal Name
LPD_MIO23	A16	D17	LPD_MIO17
LPD_MIO22	A17	D18	LPD_MIO16
LPD_MIO21	B16	D20	LPD_MIO15
LPD_MIO20	B17	D21	LPD_MIO14
LPD_MIO19	C21	C23	LPD_MIO13
LPD_MIO18	C22	C24	LPD_MIO12

Table 26 – LPD MIO Pin Assignments

Please review the Versal™ Adaptive SoC Technical Reference Manual (**AM011**) for interfaces that can be mapped to the 12 available LPD MIO pins.

6.14 HDIO Interfaces

The HDIO interface consists of 22 HD (High Density) IO pins (**HDIO_302_L[0:10]_P/N]**) connected to VE2302 SOM via the HDIO bank 302. These HDIO pins are routed to the **JX1** connector and are available for programmable interface implementation on end-user carrier cards. The HDIO banks is operated at between 1.8V and 3.3V and are referenced to **+VCCO_302** voltage from the end-user carrier card via the **JX1** connector.

On the Versal™ AI Edge Carrier Card, the HDIO pins are used to implement the following interfaces:

- High-Speed IO (HSIO) Expansion Port

Please refer to the **Versal™ AI Edge Carrier Card Hardware User Guide** for example implementation details regarding the HSIO Expansion Port mapping to the HDIO pins as well as how **+VCCO_302** provide +1.8V or +3.3V onto that voltage rail for bank 302.

Signal Name	JX1 Pin Number		Signal Name
HDIO_302_L10_P	A7	D10	HDIO_302_L4_P
HDIO_302_L10_N	A8	D11	HDIO_302_L4_N
HDIO_302_L9_P	B7	A13	HDIO_302_L3_P
HDIO_302_L9_N	B8	A14	HDIO_302_L3_N
HDIO_302_L8_P	C7	B10	HDIO_302_L2_P
HDIO_302_L8_N	C8	B11	HDIO_302_L2_N
HDIO_302_L7_P	D7	A10	HDIO_302_L1_P
HDIO_302_L7_N	D8	A11	HDIO_302_L1_N
HDIO_302_HDGC_L6_P	C10	C13	HDIO_302_L0_P
HDIO_302_HDGC_L6_N	C11	C14	HDIO_302_L0_N
HDIO_302_HDGC_L5_P	B13	-	-
HDIO_302_HDGC_L5_N	B14	-	-

Table 27 – HDIO Pin Assignments

6.15 XPIO Interfaces

The XPIO interface consists of 54 XP (Extended Performance) IO pins from bank 703 (**XPIO_703_L[0:26]_P/N]**) and 26 XP (Extended Performance) IO pins from bank 702 (**XPIO_702_L[*]_P/N**) connected to VE2302 SOM. These XPIO pins are routed to the **JX2** connector and are available for programmable interface implementation on end-user carrier cards. The XPIO banks are operated at between 1.1V and 1.5V and are referenced to **+VCCO_702** and **+VCCO_703** bank voltages from the end-user carrier card via the **JX2** connector.

On the Versal™ AI Edge Carrier Card, the XPIO pins are used to implement the following interfaces:

- MIPI Interfaces x4
- HDMI Control Signals
- SFP28 Control Signals

Please refer to the **Versal™ AI Edge Carrier Card Hardware User Guide** for example implementation details regarding bank 702 and bank 703 mapping of the XPIO pins to physical interfaces.

NOTE: XPIO Bank 702 contains four signals mapped to the PIN EFFICIENT LPDDR4 interface. These four signals are associated to a bank voltage of +1.1V which creates a potential for a mismatch with the bank voltage desired to be utilized on bank 702 by an end-user carrier card, such as a bank voltage like 1.2V or 1.5V. A workaround for this exists and is documented in **AMD Answer Record 35358** which helps to resolve voltage standard conflicts for pin efficient topologies.

NOTE: Link to Answer Record 35358: **Versal™ Adaptive SOC DDRMC - Change LPDDR4 RESET_N and SYS_CLK IO Standards for Pin Efficient Topologies**

Signal Name	JX2 Pin Number		Signal Name
XPIO_703_L26_P	C12	C21	XPIO_703_GC_XCC_L12_P
XPIO_703_L26_N	C13	C22	XPIO_703_GC_XCC_L12_N
XPIO_703_L25_P	D12	A6	XPIO_703_L11_P
XPIO_703_L25_N	D13	A7	XPIO_703_L11_N
XPIO_703_GC_XCC_L24_P	C9	A3	XPIO_703_L10_P
XPIO_703_GC_XCC_L24_N	C10	A4	XPIO_703_L10_N
XPIO_703_L23_P	B18	B6	XPIO_703_GC_XCC_L9_P
XPIO_703_L23_N	B19	B7	XPIO_703_GC_XCC_L9_N
XPIO_703_L22_P	B16	D15	XPIO_703_L8_P
XPIO_703_L22_N	B16	D16	XPIO_703_L8_N
XPIO_703_XCC_L21_P	A15	C15	XPIO_703_L7_P
XPIO_703_XCC_L21_N	A16	C16	XPIO_703_L7_N
XPIO_703_L20_P	A18	D18	XPIO_703_GC_XCC_L6_P
XPIO_702_L20_N	A19	D19	XPIO_703_GC_XCC_L6_N
XPIO_703_L19_P	B21	D3	XPIO_703_L5_P
XPIO_703_L19_N	B22	D4	XPIO_703_L5_N
XPIO_703_XCC_L18_P	A21	C3	XPIO_703_L4_P
XPIO_703_XCC_L18_N	A22	C4	XPIO_703_L4_N
XPIO_703_L17_P	B12	B3	XPIO_703_XCC_L3_P
XPIO_703_L17_N	B13	B4	XPIO_703_XCC_L3_N
XPIO_703_L16_P	A9	D6	XPIO_703_L2_P
XPIO_703_L16_N	A10	D7	XPIO_703_L2_N
XPIO_703_XCC_L15_P	A12	C6	XPIO_703_L1_P
XPIO_703_XCC_L15_N	A13	C7	XPIO_703_L1_N
XPIO_703_L14_P	C18	D9	XPIO_703_XCC_L0_P
XPIO_703_L14_N	C19	D10	XPIO_703_XCC_L0_N
XPIO_703_L13_P	D21	-	-
XPIO_703_L13_N	D22	-	-

Table 28 – XPIO 703 Pin Assignments

Signal Name	JX2 Pin Number		Signal Name
XPIO_702_L26_P	B9	C30	XPIO_702_L17_P
XPIO_702_L26_N	B10	C31	XPIO_702_L17_N
XPIO_702_L23_P	B33	C27	XPIO_702_L16_P
XPIO_702_L23_N	B34	C28	XPIO_702_L16_N
XPIO_702_L22_P	A33	D30	XPIO_702_XCC_L15_P
XPIO_702_L22_N	A34	D31	XPIO_702_XCC_L15_N
XPIO_702_XCC_L21_P	B36	D39	XPIO_702_L14_P
XPIO_702_XCC_L21_N	B37	D40	XPIO_702_L14_N
XPIO_702_L20_P	A36	D36	XPIO_702_L13_P
XPIO_702_L20_N	A37	D37	XPIO_702_L13_N
XPIO_702_L19_P	A39	C39	XPIO_702_XCC_L12_P
XPIO_702_L19_N	A40	C40	XPIO_702_XCC_L12_N
XPIO_702_XCC_L18_P	B39	-	-
XPIO_702_XCC_L18_N	B40	-	-

Table 29 – XPIO 702 Pin Assignments

6.16 GTYP Interfaces

The VE2302 SOM provides 8 GTYP transceivers along with 4 differential reference clock inputs to the end-user carrier card via the **JX3** connector. Routing all 4 reference clock inputs to the end-user carrier card will provide users with maximum flexibility in how these clocks will be driven. The GTYP transceivers in the Versal™ architecture are power-efficient transceivers, supporting line rates from 1.25 Gb/s to 32.75 Gb/s. The 8 GTYP transceivers can be used on an end-user carrier card to implement a variety of interfaces.

NOTE: End-user carrier card designers will need to determine the maximum line rates they desire to support with their interface needs and design carrier card appropriately including PCB materials selection, PCB HDI design techniques, multi-gigabit routing techniques, and simulations to ensure design success!

Please refer to the **AM002** (Versal Adaptive SoC GTY and GTYP Transceivers Architecture Manual) for more information on how each GTYP transceiver can be used in a design.

For designs that use the GTYP transceivers, the GTYP transceiver power rails (0.92V, 1.2V, and 1.5V) must be supplied by the end-user carrier card via the **JX2** and **JX3** connectors.

Signal Name	JX3 Pin Number		Signal Name
GTYP_104_REFCLK0_P	A7	B10	GTYP_104_REFCLK1_P
GTYP_104_REFCLK0_N	A8	B11	GTYP_104_REFCLK1_N
GTYP_104_TX1_P	A14	B17	GTYP_104_TX3_P
GTYP_104_TX1_N	A15	B18	GTYP_104_TX3_N
GTYP_104_TX2_P	A20	B23	GTYP_104_TX0_P
GTYP_104_TX2_N	A21	B24	GTYP_104_TX0_N
GTYP_103_TX3_P	A26	B29	GTYP_103_TX2_P
GTYP_103_TX3_N	A27	B30	GTYP_103_TX2_N
GTYP_103_TX1_P	A32	B35	GTYP_103_TX0_P
GTYP_103_TX1_N	A33	B36	GTYP_103_TX0_N
GTYP_103_REFCLK0_P	C7	D10	GTYP_103_REFCLK1_P
GTYP_103_REFCLK0_N	C8	D11	GTYP_103_REFCLK1_N
GTYP_104_RX3_P	C14	D17	GTYP_104_RX2_P
GTYP_104_RX3_N	C15	D18	GTYP_104_RX2_N
GTYP_104_RX1_P	C20	D23	GTYP_104_RX0_P
GTYP_104_RX1_N	C21	D24	GTYP_104_RX0_N
GTYP_103_RX3_P	C26	D29	GTYP_103_RX2_P
GTYP_103_RX3_N	C27	D30	GTYP_103_RX2_N
GTYP_103_RX1_P	C32	D35	GTYP_103_RX0_P
GTYP_103_RX1_N	C33	D36	GTYP_103_RX0_N

Table 30 – GTYP Interface Pin Assignments

Please refer to the **Versal™ AI Edge Carrier Card Hardware User Guide** for example implementation details regarding GTYP transceivers and GTYP transceiver reference clocks.

7 Power Requirements

The VE2302 SOM requires the following voltage rails to be supplied by the end-user carrier card. In return, the VE2302 SOM will provide voltage sense feedback for each rail to the carrier card. The voltage sense feedback for each rail can be used by the regulator on the carrier card to compensate for the voltage loss across the JX connectors and provide the proper voltage at the load on the VE2302 SOM.

Please refer to the Versal™ AI Edge Series Data Sheet (**DS958**) for the requirements for the respective voltage rails when designing the power system for the end-user carrier card.

The end-user carrier card is required to supply the following rails to the VE2302 SOM where applicable:

- **+VIN** VE2302 SOM Main Input Voltage via **JX3** Connector
- **+VCCINT** Programmable Logic Core Voltage via **JX1**, **JX2**, and **JX3** connectors
- **+VCC_RAM** Programmable Logic RAM / Clocking Network Voltage via **JX1** connector
- **+VCC_BATT** Battery Backup Power Supply via **JX1** connector
- **+VCC_FUSE** eFUSE Programming Power Supply via **JX1** connector

- **+VCCO_302** Programmable Logic HDIO Bank 302 VCCO via **JX1** connector
- **+VCCO_702** Programmable Logic XPIO Bank 702 VCCO via **JX2** connector
- **+VCCO_703** Programmable Logic XPIO Bank 703 via **JX2** connector
- **+MGTYPAVCC** GTYP Transceiver Primary Analog Supply via **JX2** connector
- **+MGTYPAVTT** GTYP Transceiver Termination Power Supply via **JX3** connector
- **+MGTYPVCCAUX** GTYP Transceiver Auxiliary Analog PLL Supply via **JX2** connector

NOTE: These are the power supplies required for the VE2302 SOM. It may not be all the required supplies for an end-user solution. It is up to the end-user designing the carrier card to implement a power architecture that accounts for required voltages and currents to support their system while still meeting the power needs of the VE2302 SOM.

Voltage Rail Name	Voltage Value	Current Requirement	Voltage Sense Feedback
+VIN	5V	12A	VIN_SENSE
+VCCINT	0.70V	Up to 40A	VCCINT_SENSE
+VCC_RAM	0.80V	1A	VCC_RAM_SENSE
+VCC_BATT	1.5V		NA
+VCC_FUSE	1.8V		NA
+VCCO_302	1.8V – 3.3V	2A	VCCO_302_SENSE
+VCCO_702	1.0V – 1.5V	2A	VCCO_702_SENSE
+VCCO_703	1.0V – 1.5V	2A	VCCO_703_SENSE
+MGTYPAVCC	1.2V	3A	MGTRAVCC_SENSE
+MGTYPAVTT	0.92V	4A	MGTRAVTT_SENSE
+MGTYPVCCAUX	1.5V	0.5A	MGTYPVCCAUX_SENSE

Table 31 – VE2302 SOM Power Requirements

NOTE: The current requirements listed above are generic and represents the VE2302 SOM and Versal™ AI Edge Carrier Card solution. It is expected that an end-user will run **Power Design Manager (PDM)** on the application targeting the Versal™ AI Edge device and determine an accurate power estimation for the system.

NOTE: Please refer to the JX Master Tables for proper pin locations on the JX connectors for all the required power rails and voltage sense signals.

NOTE: **+VCCINT** voltage rail was made a requirement for the end-user carrier card such that an end-user could accurately determine their current requirements and determine a suitable core voltage solution that met the system's needs. The alternative would be to have included this on the VE2302 SOM which would then require a worse case solution being placed to support significant current which would lead to additional cost, size, and potential thermal issues due to regulator inefficiencies.

NOTE: +VCC_RAM voltage rail was made a requirement for the end-user carrier card to simplify the power sequencing handshaking required.

NOTE: **+VCC_BATT** voltage must be in the range of 1.425V-1.575V. If **+VCC_BATT** is unused, the end-user carrier card should connect this pin to ground.

NOTE: **+VCC_FUSE** voltage must be in the range of 1.745v – 1.854V when using eFUSE programming. If **+VCC_FUSE** is unused, the end-user carrier card should connect this pin to ground.

NOTE: Please refer to the **Versal™ AI Edge Carrier Card Hardware User Guide** for an example power architecture implementation.

7.1 Power-On Reset Timing

The end-user carrier card controls the release of the **SOM_RESET_IN_B** input to the VE2302 SOM. This signal controls the **POR_B** signal to the Versal™ AI Edge device. The end-user carrier card is required to control the release of the **POR_B** signal dependent on system requirements.

At a minimum, the end-user carrier card should monitor the **+VCCAUX_PMC** voltage rail provided by the VE2302 SOM via the **JX2** connector as the stability of this rail is the earliest release point of the **POR_B** signal.

Regarding the **POR_B** signal, the PMC power domain must be powered first and remain on for all power modes except complete device power-down. During the PMC power domain power-on sequence, the **POR_B** input on the AMD Versal™ AI Edge device is asserted LOW and continues to be asserted for a minimum duration of **POR_B** (10uS) after all the required supplies of the PMC power domain have reached minimum operating voltage levels.

After PMC power domain power-on (indicated by **+VCCAUX_PMC** stability), **POR_B** can de-asserted HIGH to complete the device power-on-reset (**POR**). If other power domains are powered with the PMC domain and are expected to be functional at initial power-on without additional power management, then the **POR_B** input on the AMD Versal™ AI Edge device is held LOW until all applicable power domain supplies have reached minimum voltage levels.

At a maximum, the end-user carrier card should monitor the **+MGTYPAVTT** voltage rail provided by the VE2302 SOM via the **JX3** connector as the stability of this rail is the latest release point of the **POR_B** signal.

NOTE: Please refer to the **Versal™ AI Edge Carrier Card Hardware User Guide** for an example implementation of the **SOM_RESET_IN_B** as this signal control the **POR_B** at the Versal™ AI Edge device.

7.2 Power Sequencing

The power-up and power-down sequencing of the VE2302 SOM and end-user carrier card should follow datasheet recommendations for the AMD Versal™ AI Edge Adaptive SoC device, **DS958**. The power architecture designed on the Versal™ AI Edge Carrier Card is a good example of a power architecture that follows the datasheet recommendations for power-up and power-down sequencing.

The VE2302 SOM power sequencing requires several control signals to be utilized to sequence the VE2302 SOM and an end-user carrier card in the most appropriate manner. The signals from the VE2302 SOM that will be used as enable signals to the end-user carrier card are called **VCCO_702_ENB_OUT** and **SOM_PG_OUT**. The proper end-user carrier card voltage regulators should not be turned ON until the **VCCO_702_ENB_OUT** and **SOM_PG_OUT** signals are asserted. The control signals to the VE2302 SOM that are used are called **SOM_PWR_ENB_IN** and **VCCO_702_PG_IN**.

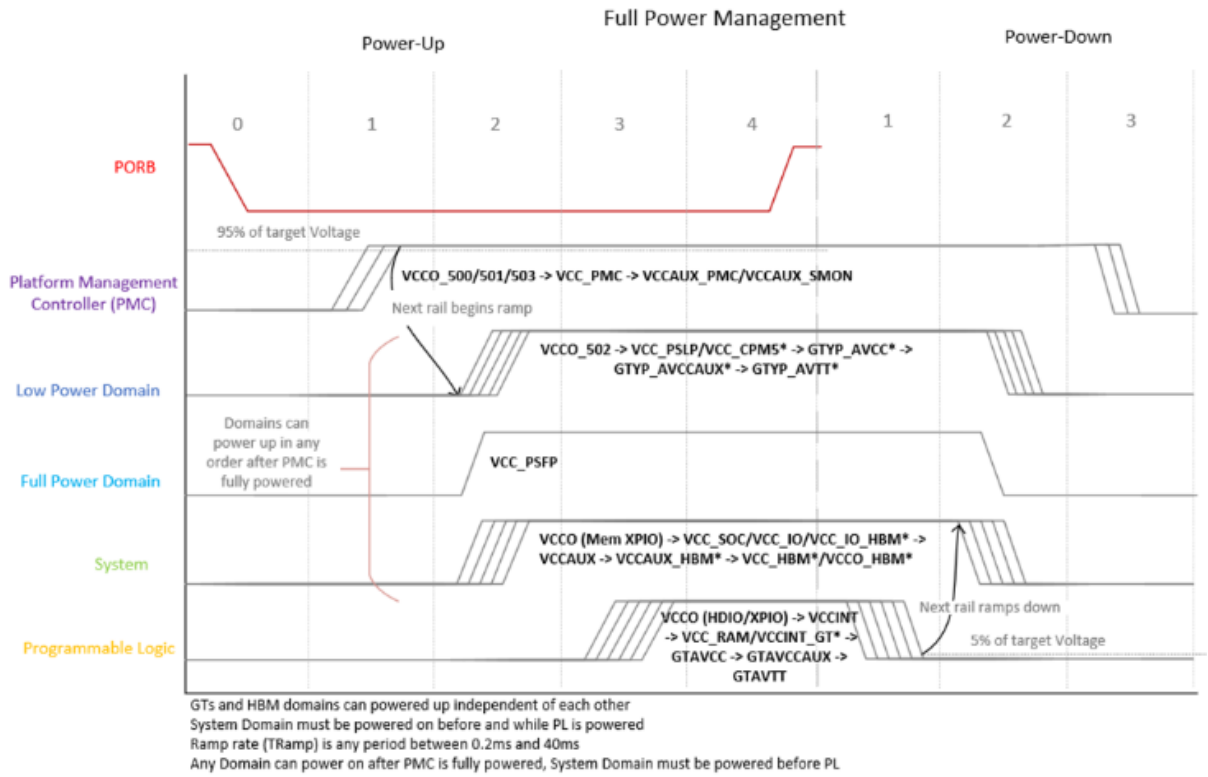

Figure 8 – Versal Power-On Sequence

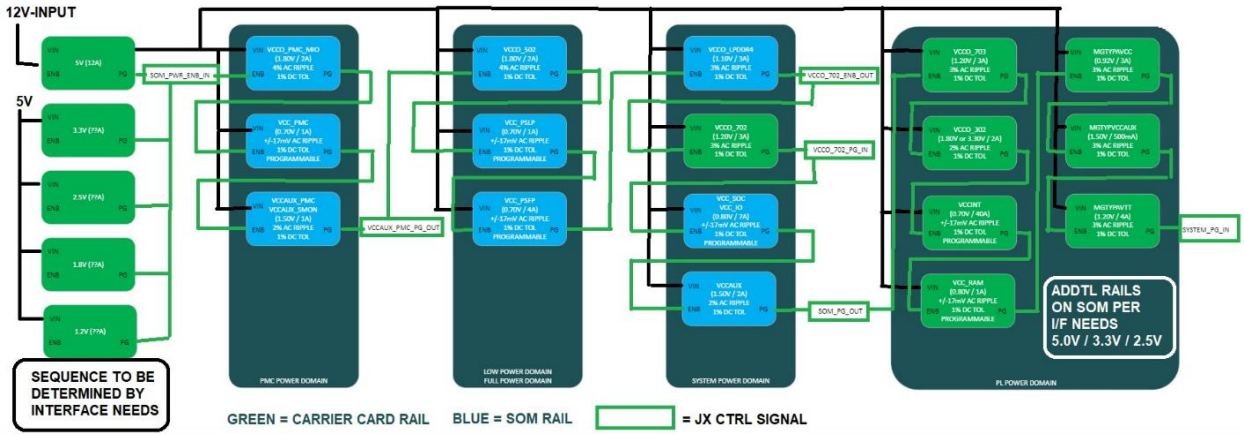

Figure 9 – Example Power Sequencing with End-User Carrier Card

To control the power sequencing for the example power architecture, a custom power sequencer was implemented in a Renesas Greenpak device, base part number **SLG46620V**. The pre-programmed part number utilized is **SLG7A46723V** which is a custom designed power sequencer from Tria Technologies that can control the power-up and power-down sequence of up to 9 power supplies utilizing a single control signal. The power sequencer waits for the **SOM_PG_OUT** from the VE2302 SOM prior to starting the end-user carrier card power-up sequence. If the **SOM_PG_OUT** signal from the VE2302 SOM is de-asserted, the power sequencer will begin bringing down the power supplies in the reverse order.

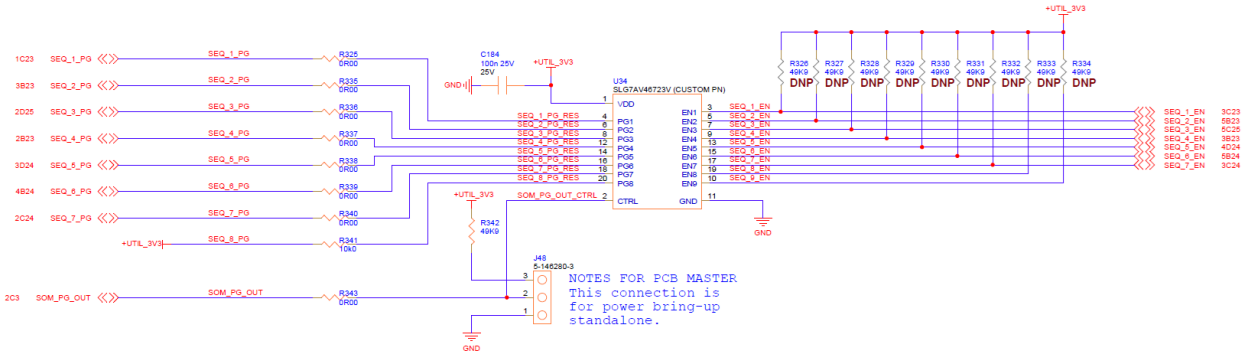

Figure 10 – Custom Power Sequencer Circuit

As you can see from the power sequencing figure above, as the power-up sequence progress, the VE2302 SOM provides **+VCCAUX_PMC** to the end-user carrier card so it can be used to release the **POR_B** after the PMC power domain has been fully powered.

The VE2302 SOM power sequence progresses until it asserts the **VCCO_702_ENB_OUT** signal to the end-user carrier card. **VCCO_702_ENB_OUT** is the signal from the VE2302 SOM to turn on the **+VCCO_702** rail. When the **+VCCO_702** rail is stable, it is expected that the end-user carrier card will then assert the **VCCO_702_PG_IN** signal to tell the VE2302 SOM to complete its power-up sequence.

NOTE: Please refer to the **Versal™ AI Edge Carrier Card Hardware User Guide** for an example implementation of proper power sequencing.

Once the VE2302 SOM completes its power-up sequence, it will assert the **SOM_PG_OUT** signal to the end-user carrier card so that it can complete its power-up sequence. A good rule of thumb is to utilize an LED on an end-user carrier card to illuminate when the whole system power is valid.

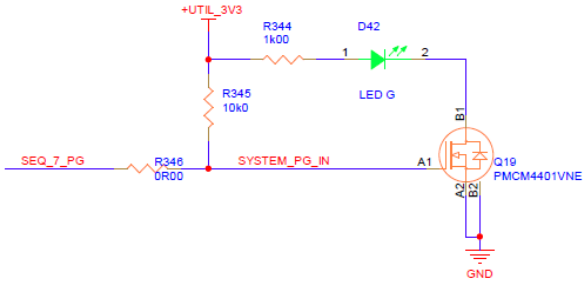

Figure 11 – System Power Good LED

Signal Name	Source	JX1 Pin Number	Description
SOM_PWR_ENB_IN	Carrier	JX2-C32	Power enable signal to SOM after +VIN is stable.
+VCCAUX_PMC	SOM	JX2-A32	Rail for monitoring for early release of POR_B.
+MGTYPAVTT_SENSE	SOM	JX2-D20	Rail for monitoring for last release of POR_B.
VCCO_702_ENB_OUT	SOM	JX2-C8	Bank 702 enable signal to Carrier Card.
VCCO_702_PG_IN	Carrier	JX2-D8	Bank 702 power good signal to SOM.
SOM_PG_OUT	SOM	JX1-B29	SOM power good indicator to carrier card.

Table 32 – Power Sequencing Control Signals

7.3 Recommended Carrier Card Power Sequence

1) +VIN VE2302 SOM Main Input Voltage via **JX3** Connector
2) +VCCO_702 Programmable Logic XPIO Bank 702 VCCO via **JX2** connector
3) +VCCO_703 Programmable Logic XPIO Bank 703 via **JX2** connector
4) +VCCO_302 Programmable Logic HDIO Bank 302 VCCO via **JX1** connector
5) +VCCINT Programmable Logic Core Voltage via **JX1**, **JX2**, and **JX3** connectors
6) +VCC_RAM Programmable Logic RAM / Clocking Network Voltage via **JX1** connector
7) +MGTYPAVCC GTYP Transceiver Primary Analog Supply via **JX2** connector
8) +MGTYPVCCAUX GTYP Transceiver Auxiliary Analog PLL Supply via **JX2** connector
9) +MGTYPAVTT GTYP Transceiver Termination Power Supply via **JX3** connector

8 JX Micro Headers

End-user carrier cards are required to implement 3 Samtec 4-Row connectors used to access the VE2302 SOM IO pins (**ADM6 series**). The end-user carrier card to SOM connectors is designated as "JX" connectors. All the connectors, JX1, JX2 and JX3, are 160 pins. These connectors carry the following signals and power/ground pins (signal directions are with respect to the VE2302 SOM):

- **JX1 Connector** (160-pin Terminal, Samtec part number: **ADF6-40-03.5-L-4-0-A**)
  - **JTAG** Pins (**JTAG_TMS**, **JTAG_TCK**, **JTAG_TDI**, and **JTAG_TDO**)
  - **SYSMON** Pins (**SMON_V_P**, **SMON_V_N**, **SMON_VREF**, **+VCCAUX_SMON**, **SMON_AGND**)
  - **MODE** Pins (**MODE0**, **MODE1**, **MODE2**, **MODE3**)
  - 13 PMC MIO Bank 501 Pins (**MIO[49:37]**)
  - 12 LPD MIO Bank 502 Pins (**MIO[23:12]**)
  - 22 Single Ended / 11 Differential HDIO Bank 302 Pins (**HDIO_302_L10_P/N: HDIO_302_L0_P/N**)
  - USB 2.0 Connector Interface (**USB_D_P**, **USB_D_N**, **USB_ID**, and **+USB_VBUS**)
  - Gigabit Ethernet Connector Interface (**ETH_MD[1:4]_P**, **ETH_MD[1:4]_N**, **ETH_ACT**, **ETH_LINK**)
  - Differential System Clock Input (**SYSCLK_CH0_CH1_P/N**)
  - I2C Driven General Purpose Pins (**I2C_P6_GPIO** and **I2C_P7_GPIO**)
  - **SOM_PG_OUT** Output
  - **DONE_OUT** Output
  - **ERROR_OUT** Output
  - Carrier Card I2C interface (**CC_SDA**, **CC_SCL**, and **CC_INT_B**)
  - PMBus Signals (**PMBUS_SDA**, **PMBUS_SCL**, and **PMBUS_ALERT_N**)
  - Power and ground pins (**+VCCINT**, **+VCCO_302**, **+VCC_RAM**, **+VCC_BATT** and **GND**)

- Voltage Sense Feedback Output Pins (**VCCO_302_SENSE**, **VCC_RAM_SENSE**, **VCCINT_SENSE**, **GND_SENSE**)

- **JX2 Connector** (160-pin Terminal, Samtec part number: **ADF6-40-03.5-L-4-0-A**)
  - 54 Single Ended / 27 Differential XPIO Bank 703 Signals (**XPIO_703_L26_P/N: XPIO_703_L0_P/N**)
  - 26 Single Ended / 13 Differential XPIO Bank 702 Signals (**XPIO_702_L*_P/N**)
  - **VCCO_702_ENB_OUT** Output
  - **VCCO_702_PG_IN** Input
  - **SOM_RESET_IN_B** Input
  - **CC_RESET_OUT_B** Output
  - Power and Ground Pins (**+VCCINT**, **+VCCO_702**, **+VCCO_703**, **+MGTYPAVCC**, **+MGTYPAVTT**, **+MGTYPVCCAUX**, and **GND**)
  - Voltage Sense Feedback Output Pins (**VCCO_702_SENSE**, **VCCO_703_SENSE**, **MGTYPAVCC_SENSE**, **MGTYPAVTT_SENSE**, **MGTYPVCCAUX_SENSE**, **VCCAUX_PMC_SENSE**)

- **JX3 Connector** (160-pin Terminal, Samtec part number: **ADF6-40-03.5-L-4-0-A**)
  - **GTYP_103[3:0]**, **GTYP_103_REFCLK[1:0]**
  - **GTYP_104[3:0]**, **GTYP_104_REFCLK[1:0]**
  - Power and Ground Pins (**+VIN**, **+VCCINT**, and **GND**)

8.1 Mating JX Receptacle Connectors

The JX1, JX2, and JX3 plugs on the VE2302 SOM have a default height of 3.5mm. The height of the mating JX receptacles for the end-user carrier cards must be selected such that the Stack Height is <= 12mm when the VE2302 SOM is plugged onto the end-user carrier card (this requirement must be met in order to meet the 32Gbps data rate for the GTYP transceivers connected to the JX3 connector). The Stack Height is calculated as follows:

On the Versal™ AI Edge Carrier Card, the JX1, JX2, and JX3 receptacles have a 1.5mm height (for a total height of 5mm):

- JX1 Connector (160-pin Receptacle, Samtec part number: **ADM6-40-01.5-L-4-0-A**)
- JX2 Connector (160-pin Receptacle, Samtec part number: **ADM6-40-01.5-L-4-0-A**)
- JX3 Connector (160-pin Receptacle, Samtec part number: **ADM6-40-01.5-L-4-0-A**)

The end-user carrier card mating JX receptacles for the VE2302 SOM plugs can have different heights. The following table shows valid receptacles that can be used on end-user carrier cards and the total height achieved with the SOM connectors.

MATED HEIGHTS *

ADF6 LEAD STYLE	ADM6 LEAD STYLE			
	–01.5	–03.5	–06.5	–08.5
–03.5	(5 mm) .197"	(7 mm) .276"	(10 mm) .394"	(12 mm) .472"
–07.5	(9 mm) .354"	(11 mm) .433"	(14 mm) .551"	(16 mm) .630"

* Processing conditions will affect mated height.

Figure 12 – Connectors mated heights

8.2 JX Micro Headers Matched Lengths

The VE2302 SOM device package delay is accommodated for in the layout of the JX Micro Header signal trace lengths. The average of min and max values for package delay is utilized to compensate for the flight time caused by the delay associated with this package.

The bank 302 HDIO pins are routed with matched lengths to the JX1 connector. The matched pairs may be used as either single ended I/O or differential pairs depending on the end users design requirements.

The LPD MIO and routed with matched lengths to the JX1 connector. The PMC MIO are routed with matched lengths to the JX1 connector. The Ethernet signals are routed with matched lengths to the JX1 connector. The USB differential pair is routed with matched lengths to the JX1 connector. The JTAG interface is routed with matched lengths to the JX1 connector.

See the **VE2302 SOM Net Length** report for more details on the matched lengths to the JX1 connector.

The bank 702 and bank 703 XPIO pins are routed with matched lengths to the JX2 connector. The matched lengths differ here from bank 302 as the matching of lengths are done by AMD nibbles which are 6-pins. Each nibble within bank 702 and bank 703 is length matched. The matched pairs may be used as either single ended I/O or differential pairs depending on the end users design requirements.

See the **VE2302 SOM Net Length** report for more details on the matched lengths to the JX2 connector.

The GTYP Quad 103 RX pins are routed with matched lengths to the JX3 connector. The GTYP Quad 103 TX pins are routed with matched lengths to the JX3 connector. The GTYP Quad 103 REFCLK pins are routed with matched lengths to the JX3 connector.

The GTYP Quad 104 RX pins are routed with matched lengths to the JX3 connector. The GTYP Quad 104 TX pins are routed with matched lengths to the JX3 connector. The GTYP Quad 104 REFCLK pins are routed with matched lengths to the JX3 connector.

See the **VE2302 SOM Net Length** report for more details on the matched lengths to the JX3 connector.

8.3 JX Connector Master Table

The following table summarizes connections to the VE2302 SOM JX Micro Header Connectors.

SOM Connector	Signal Name	VE2302 Bank	Voltage Domain
JX1	HDIO_302_[0:10]_P/N, VCCO_302 (x2)	302	VCCO_302
	LPD_MIO[12:23], VCCO_502	502	VCCO_502
	PMC_MIO[37:49], VCCO_PMC_MIO	501	VCCO_PMC_MIO
	SYSCLK_P/N	702	VCCO_702
	JTAG_TMS, JTAG_TCK, JTAG_TDI, JTAG_TDO ERROR_OUT DONE_OUT MODE[0:3]	503	VCCO_PMC_MIO
	I2C_P6_GPIO, I2C_P7_GPIO	NA	VCCO_PMC_MIO

SOM Connector	Signal Name	VE2302 Bank	Voltage Domain
	PMBUS_SDA, PMBUS_SCL, PMBUS_ALERT_B	NA	Pulled-up to 1.8V, 2.5V, or 3.3V on the Carrier Card
	CC_INT_B, CC_SCL, CC_SDA	NA	Pulled-up to 1.8V, 2.5V, or 3.3V on the Carrier Card
	USB_D_P, USB_D_N, USB_ID, USB_VBUS,	500	1.8V
	ETH_MD[1:4]_P, ETH_MD[1:4]_N, ETH_ACT, ETH_LINK,	NA	1.8V
	SMON_V_P, SMON_V_N, SMON_VREF, VCCAUX_SMON, SMON_AGND (x4)	500	VCCO_PMC_MIO
	SOM_PG_OUT	NA	3.3V
	VCC_BATT		1.5V
	VCC_FUSE		0V–1.8V
	VCC_RAM		0.80V, or 0.88V
	VCCO_302_SENSE		VCCO_302
	VCCO_RAM_SENSE		VCC_RAM
	VCCINT_SENSE		VCCINT
	GND_SENSE		GND
	VCCINT		0.70V, 0.80V, or 0.88V
JX2	XPIO_702_L[0:23]_P/N, XPIO_702_L26_P/N, VCCO_702 (x2)	702	VCCO_702
	XPIO_703_L[0:26]_P/N, VCCO_703 (x2)	703	VCCO_703
	SOM_RESET_IN_B CC_RESET_OUT_B SOM_PWR_ENB_IN	NA	1.8V Pulled-up to 1.8V, 2.5V, or 3.3V on the Carrier Card 3.3V
	VCCO_702_ENB_OUT		3.3V
	VCCO_702_PG_IN		3.3V
	MGTYPAVCC		1.2V
	MGTYPVCCAUX		1.5V
	VCCAUX_PMC		1.5V
	VCCO_702_SENSE		VCCO_702
	VCCO_703_SENSE		VCCO_703
	MGTYPAVCC_SENSE		MGTYPAVCC
	MGTYPVCCAUX_SENSE		MGTYPVCCAUX
	MGTYPAVTT_SENSE		MGTYPAVTT
	VCCINT		0.70V, 0.80V, or 0.88V

SOM Connector	Signal Name	VE2302 Bank	Voltage Domain
JX3	GTYP_103_TX[0:3]_P/N, GTYP_103_RX[0:3]_P/N, GTYP_103_REFCLK0_P/N, GTYP_103_REFCLK1_P/N, MGTYPAVTT	103	MGTYPAVCC, MGTYPVCCAUX, MGTYPAVTT
	GTYP_104_TX[0:3]_P/N, GTYP_104_RX[0:3]_P/N, GTYP_104_REFCLK0_P/N, GTYP_104_REFCLK1_P/N, MGTYPAVTT	104	MGTYPAVCC, MGTYPVCCAUX, MGTYPAVTT
	VIN_SENSE	NA	VIN
	VIN		5V
	VCCINT		0.70V, 0.80V, or 0.88V

Table 33 – JX Micro Header Connectors Pinout Summary

The following tables list the VE2302 SOM JX Micro Header connections in master tables targeting each connector:

- Pins in **Orange** are DDRMC dedicated and are not available to be used
- Pins in **Pink** are Power, Ground, or Sense signals
- Pins in **Blue** are dedicated signals
- Pins in **Black** are multi-function/general-purpose pins
- Pins in **Black** with **_HDGC** designators inputs are clock capable pins in a HDIO bank
- Pins in **Black** with **_XCC** designators can accept a strobe to capture data
- Pins in **Black** with **_GC** and **_XCC** these pins can act as Global Clocks and/or XCCs inputs
- **PMC_MIO** stands for Platform Management Controller Multiplexed I/O
- **LPD_MIO** stands for Low Power Domain Multiplexed I/O
- **HDIO** stands for I/O from bank 302
- **XPIO** stands for I/O from bank 702 or bank 703
- **GTYP** stands for I/O from quad 103 or quad 104

XCVE2302 Pin #	Signal Name	JX1 Pin #		Signal Name	XCVE2302 Pin #
Many	+VCCINT	A1	B1	+VCCINT	Many
	+VCCINT	A2	B2	+VCCINT	
	+VCCINT	A3	B3	+VCCINT	
	+VCCINT	A4	B4	+VCCINT	
	+VCCINT	A5	B5	+VCCINT	
N/A	GND	A6	B6	GND	N/A
B13	HDIO_302_L10_P	A7	B7	HDIO_302_L9_P	B12
A14	HDIO_302_L10_N	A8	B8	HDIO_302_L9_N	A13
N/A	GND	A9	B9	GND	N/A
C14	HDIO_302_L1_P	A10	B10	HDIO_302_L2_P	E13

XCVE2302 Pin #	Signal Name	JX1 Pin #		Signal Name	XCVE2302 Pin #
C13	HDIO_302_L1_N	A11	B11	HDIO_302_L2_N	D14
D13, F13	+VCCO_302	A12	B12	+VCCO_302	D13, F13
E12	HDIO_302_L3_P	A13	B13	HDIO_302_HDGC_L5_P	D11
D12	HDIO_302_L3_N	A14	B14	HDIO_302_HDGC_L5_N	C12
N/A	GND	A15	B15	GND	N/A
Y7	LPD_MIO23	A16	B16	LPD_MIO21	U6
T6	LPD_MIO22	A17	B17	LPD_MIO20	W6
N/A	GND	A18	B18	+VCC_FUSE	V15
AF10	PMC_MIO47	A19	B19	PMC_MIO49	AC10
AF9	PMC_MIO46	A20	B20	PMC_MIO48	AD10
N/A	GND	A21	B21	GND	N/A
AE9	PMC_MIO45	A22	B22	PMC_MIO43	AC9
AD9	PMC_MIO44	A23	B23	PMC_MIO42	AA9
U7, U8, V7, W8, V9, W9	+VCCO_PMC_MIO	A24	B24	GND	N/A
N/A	CC_INT_B	A25	B25	CC_SCL	N/A
N/A	PMBUS_ALERT_B	A26	B26	GND	N/A
N/A	VCCO_302_SENSE	A27	B27	VCC_RAM_SENSE	N/A
N/A	GND	A28	B28	PMBUS_SDA	N/A
N/A	ETH_ACT	A29	B29	SOM_PG_OUT	N/A
N/A	ETH_LINK	A30	B30	USB_ID	N/A
N/A	GND	A31	B31	GND	N/A
N/A	ETH_MD4_P	A32	B32	ETH_MD3_P	N/A
N/A	ETH_MD4_N	A33	B33	ETH_MD3_N	N/A
N/A	GND	A34	B34	GND	N/A
AG8	MODE0	A35	B35	MODE1	AG7
N/A	GND	A36	B36	GND	N/A
AH10	JTAG_TCK	A37	B37	JTAG_TMS	AH9
N/A	GND	A38	B38	GND	N/A
R18	SMON_AGND	A39	B39	SMON_AGND	R18
U17	+SMON_VREF	A40	B40	SMON_V _P	T17
Many	+VCCINT	C1	D1	+VCCINT	Many
	+VCCINT	C2	D2	+VCCINT	
	+VCCINT	C3	D3	+VCCINT	
	+VCCINT	C4	D4	+VCCINT	

XCVE2302 Pin #	Signal Name	JX1 Pin #		Signal Name	XCVE2302 Pin #
	+VCCINT	C5	D5	+VCCINT	
N/A	GND	C6	D6	GND	N/A
B11	HDIO_302_L8_P	C7	D7	HDIO_302_L7_P	B10
A11	HDIO_302_L8_N	C8	D8	HDIO_302_L7_N	A10
N/A	GND	C9	D9	GND	N/A
D10	HDIO_302_HDGC_L6_P	C10	D10	HDIO_302_L4_P	F11
C10	HDIO_302_HDGC_L6_N	C11	D11	HDIO_302_L4_N	E11
P20, T20	+VCC_RAM	C12	D12	+USB_VBUS	N/A
F14	HDIO_302_L0_P	C13	D13	ERROR_OUT	AH5
E14	HDIO_302_L0_N	C14	D14	SYSCLK_P	N23
N/A	GND	C15	D15	SYSCLK_N	N24
F10	VCCINT_SENSE	C16	D16	GND	N/A
F9	GND_SENSE	C17	D17	LPD_MIO17	V5
N/A	I2C_P6_GPIO	C18	D18	LPD_MIO16	U5
N/A	I2C_P7_GPIO	C19	D19	GND	N/A
N/A	GND	C20	D20	LPD_MIO15	T5
Y6	LPD_MIO19	C21	D21	LPD_MIO14	T4
W5	LPD_MIO18	C22	D22	+VCCO_502	T8, T9
V4	LPD_MIO13	C23	D23	PMC_MIO39	AC8
W4	LPD_MIO12	C24	D24	PMC_MIO38	AE8
N/A	GND	C25	D25	GND	N/A
AA8	PMC_MIO41	C26	D26	PMC_MIO37	AE7
AB8	PMC_MIO40	C27	D27	+VCC_BATT	W15
N/A	GND	C28	D28	DONE_OUT	AF5
N/A	CC_SDA	C29	D29	USB_D_P	N/A
N/A	PMBUS_SCL	C30	D30	USB_D_N	N/A
N/A	GND	C31	D31	GND	N/A
N/A	ETH_MD2_P	C32	D32	ETH_MD1_P	N/A
N/A	ETH_MD2_N	C33	D33	ETH_MD1_N	N/A
N/A	GND	C34	D34	GND	N/A
AG6	MODE2	C35	D35	MODE3	AG5
N/A	GND	C36	D36	GND	N/A
AG10	JTAG_TDI	C37	D37	JTAG_TDO	AF8
N/A	GND	C38	D38	GND	N/A
R18	SMON_AGND	C39	D39	SMON_AGND	R18

XCVE2302 Pin #	Signal Name	JX1 Pin #		Signal Name	XCVE2302 Pin #
U18	SMON_V_N	C40	D40	+VCCAUX_SMON	R17

Table 34 – JX1 Connector Pin-out

XCVE2302 Pin #	Signal Name	JX2 Pin #		Signal Name	XCVE2302 Pin #
Many	+VCCINT	A1	B1	+VCCINT	Many
	+VCCINT	A2	B2	+VCCINT	
A25	XPIO_703_L10_P	A3	B3	XPIO_703_XCC_L3_P	E27
A26	XPIO_703_L10_N	A4	B4	XPIO_703_XCC_L3_N	E28
N/A	GND	A5	B5	GND	N/A
B26	XPIO_703_L11_P	A6	B6	XPIO_703_GC_XCC_L9_P	C25
B27	XPIO_703_L11_N	A7	B7	XPIO_703_GC_XCC_L9_N	B25
AE21, AF20, AF21	+VCCO_702	A8	B8	+VCCO_702	AE21, AF20, AF21
C23	XPIO_703_L16_P	A9	B9	XPIO_702_L26_P	N25
B23	XPIO_703_L16_N	A10	B10	XPIO_702_L26_N	M25
N/A	GND	A11	B11	GND	N/A
D24	XPIO_703_XCC_L15_P	A12	B12	XPIO_703_L17_P	A23
C24	XPIO_703_XCC_L15_N	A13	B13	XPIO_703_L17_N	A24
AA24, AA25, AB25	+VCCO_703	A14	B14	+VCCO_703	AA24, AA25, AB25
B20	XPIO_703_XCC_L21_P	A15	B15	XPIO_703_L22_P	A20
C21	XPIO_703_XCC_L21_N	A16	B16	XPIO_703_L22_N	A21
N/A	GND	A17	B17	GND	N/A
D20	XPIO_703_L20_P	A18	B18	XPIO_703_L23_P	C22
D21	XPIO_703_L20_N	A19	B19	XPIO_703_L23_N	B22
N/A	VCCO_702_SENSE	A20	B20	VCCO_703_SENSE	N/A
G21	XPIO_703_XCC_L18_P	A21	B21	XPIO_703_L19_P	E20
H22	XPIO_703_XCC_L18_N	A22	B22	XPIO_703_L19_N	F21
N/A	GND	A23	B23	GND	N/A
R27	XPIO_702_L1_P	A24	B24	XPIO_702_L2_P	P27
T28	XPIO_702_L1_N	A25	B25	XPIO_702_L2_N	R28
L7, N7	+MGTYPAVCC	A26	B26	+MGTYPAVCC	L7, N7
N28	XPIO_702_XCC_L3_P	A27	B27	XPIO_702_XCC_L0_P	U27
M28	XPIO_702_XCC_L3_N	A28	B28	XPIO_702_XCC_L0_N	U28

XCVE2302 Pin #	Signal Name	JX2 Pin #		Signal Name	XCVE2302 Pin #
N/A	GND	A29	B29	GND	N/A
K27	XPIO_702_L5_P	A30	B30	XPIO_702_L4_P	M27
K28	XPIO_702_L5_N	A31	B31	XPIO_702_L4_N	L28
W12, W14	+VCCAUX_PMC	A32	B32	SOM_RESET_IN_B	N/A
K21	XPIO_702_XCC_L22_P	A33	B33	XPIO_702_L23_P	J21
L22	XPIO_702_XCC_L22_N	A34	B34	XPIO_702_L23_N	J22
N/A	GND	A35	B35	GND	N/A
T21	XPIO_702_L20_P	A36	B36	XPIO_702_XCC_L21_P	N21
R22	XPIO_702_L20_N	A37	B37	XPIO_702_XCC_L21_N	M21
N/A	GND	A38	B38	GND	N/A
R21	XPIO_702_L19_P	A39	B39	XPIO_702_XCC_L18_P	V21
P22	XPIO_702_L19_N	A40	B40	XPIO_702_XCC_L18_N	U22
Many	+VCCINT	C1	D1	+VCCINT	Many
	+VCCINT	C2	D2	+VCCINT	
D27	XPIO_703_L4_P	C3	D3	XPIO_703_L5_P	C27
C28	XPIO_703_L4_N	C4	D4	XPIO_703_L5_N	B28
N/A	GND	C5	D5	GND	N/A
H27	XPIO_703_L1_P	C6	D6	XPIO_703_L2_P	G27
G28	XPIO_703_L1_N	C7	D7	XPIO_703_L2_N	F28
N/A	VCCO_702_ENB_OUT	C8	D8	VCCO_702_PG_IN	N/A
F23	XPIO_703_GC_XCC_L24_P	C9	D9	XPIO_703_XCC_L0_P	J27
F24	XPIO_703_GC_XCC_L24_N	C10	D10	XPIO_703_XCC_L0_N	H28
N/A	GND	C11	D11	GND	
D25	XPIO_703_L26_P	C12	D12	XPIO_703_L25_P	E24
D26	XPIO_703_L26_N	C13	D13	XPIO_703_L25_N	F25
N/A	CC_RESET_OUT_B	C14	D14	MGTYPVCCAUX_SENSE	N/A
G25	XPIO_703_L7_P	C15	D15	XPIO_703_L8_P	F26
G26	XPIO_703_L7_N	C16	D16	XPIO_703_L8_N	E26
N/A	GND	C17	D17	GND	N/A
E22	XPIO_703_L14_P	C18	D18	XPIO_703_GC_XCC_L6_P	H25
E23	XPIO_703_L14_N	C19	D19	XPIO_703_GC_XCC_L6_N	J26
N/A	MGTYPAVCC_SENSE	C20	D20	MGTYPAVTT_SENSE	N/A
H23	XPIO_703_GC_XCC_L12_P	C21	D21	XPIO_703_L13_P	F22
H24	XPIO_703_GC_XCC_L12_N	C22	D22	XPIO_703_L13_N	G23
N/A	GND	C23	D23	GND	N/A

XCVE2302 Pin #	Signal Name	JX2 Pin #		Signal Name	XCVE2302 Pin #
M26	XPIO_702_L10_P	C24	D24	XPIO_702_L11_P	J25
L26	XPIO_702_L10_N	C25	D25	XPIO_702_L11_N	K26
L7, N7	+MGTYPAVCC	C26	D26	+MGTYPVCCAUX	G7, J7
L23	XPIO_702_L16_P	C27	D27	XPIO_702_GC_XCC_L9_P	P26
K24	XPIO_702_L16_N	C28	D28	XPIO_702_GC_XCC_L9_N	N27
N/A	GND	C29	D29	GND	N/A
K23	XPIO_702_L17_P	C30	D30	XPIO_702_XCC_L15_P	M22
J24	XPIO_702_L17_N	C31	D31	XPIO_702_XCC_L15_N	M23
N/A	SOM_PWR_ENB_IN	C32	D32	+MGTYPVCCAUX	G7, J7
P25	XPIO_702_L8_P	C33	D33	XPIO_702_L7_P	T25
R26	XPIO_702_L8_P	C34	D34	XPIO_702_L7_N	T26
N/A	GND	C35	D35	GND	N/A
U25	XPIO_702_GC_XCC_L6_P	C36	D36	XPIO_702_L13_P	T23
U26	XPIO_702_GC_XCC_L6_N	C37	D37	XPIO_702_L13_N	R24
N/A	GND	C38	D38	GND	N/A
U23	XPIO_702_GC_XCC_L12_P	C39	D39	XPIO_702_L14_P	R23
T24	XPIO_702_GC_XCC_L12_N	C40	D40	XPIO_702_L14_N	P24

Table 35 – JX2 Connector Pin-out

XCVE2302 Pin #	Signal Name	JX3 Pin #		Signal Name	XCVE2302 Pin #
Many	+VCCINT	A1	B1	+VCCINT	Many
	+VCCINT	A2	B2	+VCCINT	
	+VCCINT	A3	B3	+VCCINT	
N/A	GND	A4	B4	GND	N/A
N/A	VIN_SENSE	A5	B5	+MGTYPAVTT	L9, M9, N9
N/A	GND	A6	B6	GND	N/A
H7	GTYP_104_REFCLK0_P	A7	B7	GND	N/A
H6	GTYP_104_REFCLK0_N	A8	B8	GND	N/A
N/A	GND	A9	B9	GND	N/A
N/A	GND	A10	B10	GTYP_104_REFCLK1_P	F7
N/A	GND	A11	B11	GTYP_104_REFCLK1_N	F6
N/A	GND	A12	B12	GND	N/A
N/A	GND	A13	B13	GND	N/A
D8	GTYP_104_TX1_P	A14	B14	GND	N/A

XCVE2302 Pin #	Signal Name	JX3 Pin #		Signal Name	XCVE2302 Pin #
D7	GTYP_104_TX1_N	A15	B15	GND	N/A
N/A	GND	A16	B16	GND	N/A
N/A	GND	A17	B17	GTYP_104_TX3_P	B8
N/A	GND	A18	B18	GTYP_104_TX3_N	B7
N/A	GND	A19	B19	GND	N/A
C5	GTYP_104_TX2_P	A20	B20	GND	N/A
C4	GTYP_104_TX2_N	A21	B21	GND	N/A
N/A	GND	A22	B22	GND	N/A
N/A	GND	A23	B23	GTYP_104_TX0_P	E5
N/A	GND	A24	B24	GTYP_104_TX0_N	E4
N/A	GND	A25	B25	GND	N/A
G5	GTYP_103_TX3_P	A26	B26	GND	N/A
G4	GTYP_103_TX3_N	A27	B27	GND	N/A
N/A	GND	A28	B28	GND	N/A
N/A	GND	A29	B29	GTYP_103_TX2_P	J5
N/A	GND	A30	B30	GTYP_103_TX2_N	J4
N/A	GND	A31	B31	GND	N/A
L5	GTYP_103_TX1_P	A32	B32	GND	N/A
L4	GTYP_103_TX1_N	A33	B33	GND	N/A
N/A	GND	A34	B34	GND	N/A
N/A	GND	A35	B35	GTYP_103_TX0_P	N5
N/A	GND	A36	B36	GTYP_103_TX0_N	N4
N/A	GND	A37	B37	GND	N/A
N/A	+VIN	A38	B38	+VIN	N/A
N/A	+VIN	A39	B39	+VIN	N/A
N/A	+VIN	A40	B40	+VIN	N/A
Many	+VCCINT	C1	D1	+VCCINT	Many
	+VCCINT	C2	D2	+VCCINT	
	+VCCINT	C3	D3	+VCCINT	
N/A	GND	C4	D4	GND	N/A
L9, M9, N9	+MGTYPAVTT	C5	D5	+MGTYPAVTT	L9, M9, N9
N/A	GND	C6	D6	GND	N/A
M7	GTYP_103_REFCLK0_P	C7	D7	GND	N/A
M6	GTYP_103_REFCLK0_N	C8	D8	GND	N/A
N/A	GND	C9	D9	GND	N/A

XCVE2302 Pin #	Signal Name	JX3 Pin #		Signal Name	XCVE2302 Pin #
N/A	GND	C10	D10	GTYP_103_REFCLK1_P	K7
N/A	GND	C11	D11	GTYP_103_REFCLK1_N	K6
N/A	GND	C12	D12	GND	N/A
N/A	GND	C13	D13	GND	N/A
A5	GTYP_104_RX3_P	C14	D14	GND	N/A
A4	GTYP_104_RX3_N	C15	D15	GND	N/A
N/A	GND	C16	D16	GND	N/A
N/A	GND	C17	D17	GTYP_104_RX2_P	B2
N/A	GND	C18	D18	GTYP_104_RX2_N	B1
N/A	GND	C19	D19	GND	N/A
D2	GTYP_104_RX1_P	C20	D20	GND	N/A
D1	GTYP_104_RX1_N	C21	D21	GND	N/A
N/A	GND	C22	D22	GND	N/A
N/A	GND	C23	D23	GTYP_104_RX0_P	F2
N/A	GND	C24	D24	GTYP_104_RX0_N	F1
N/A	GND	C25	D25	GND	N/A
H2	GTYP_103_RX3_P	C26	D26	GND	N/A
H1	GTYP_103_RX3_N	C27	D27	GND	N/A
N/A	GND	C28	D28	GND	N/A
N/A	GND	C29	D29	GTYP_103_RX2_P	K2
N/A	GND	C30	D30	GTYP_103_RX2_N	K1
N/A	GND	C31	D31	GND	N/A
M2	GTYP_103_RX1_P	C32	D32	GND	N/A
M1	GTYP_103_RX1_N	C33	D33	GND	N/A
N/A	GND	C34	D34	GND	N/A
N/A	GND	C35	D35	GTYP_103_RX0_P	P2
N/A	GND	C36	D36	GTYP_103_RX0_N	P1
N/A	GND	C37	D37	GND	N/A
N/A	+VIN	C38	D38	+VIN	N/A
N/A	+VIN	C39	D39	+VIN	N/A
N/A	+VIN	C40	D40	+VIN	N/A

Table 36 – JX3 Connector Pin-out

9 SOM Mechanical Dimensions

The following figure shows the VE2302 SOM mechanical dimensions. VE2302 SOM measures 50.0mm x 50.0mm (approximately 1.97” x 1.97”).

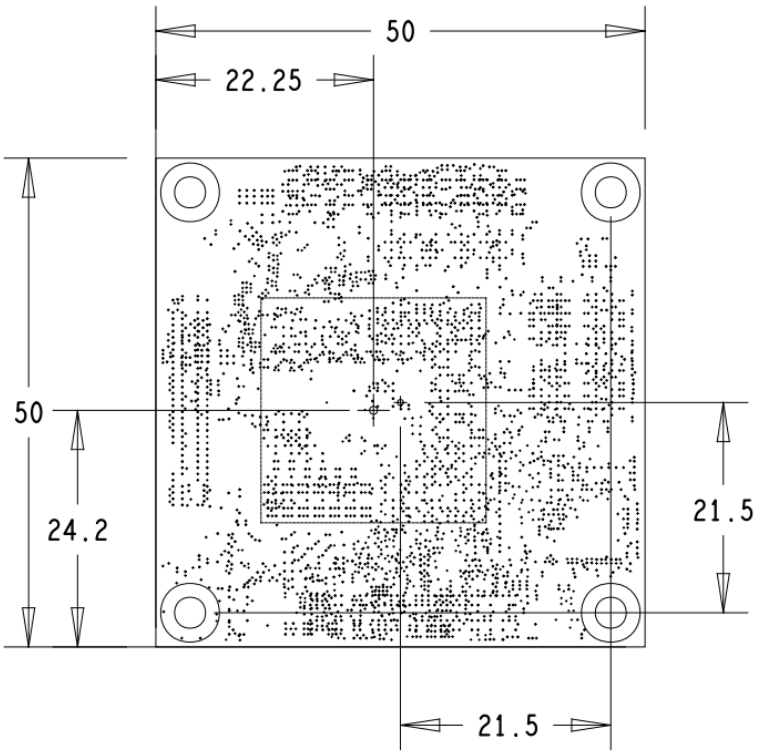

Figure 13 – Top Mechanical Dimensions

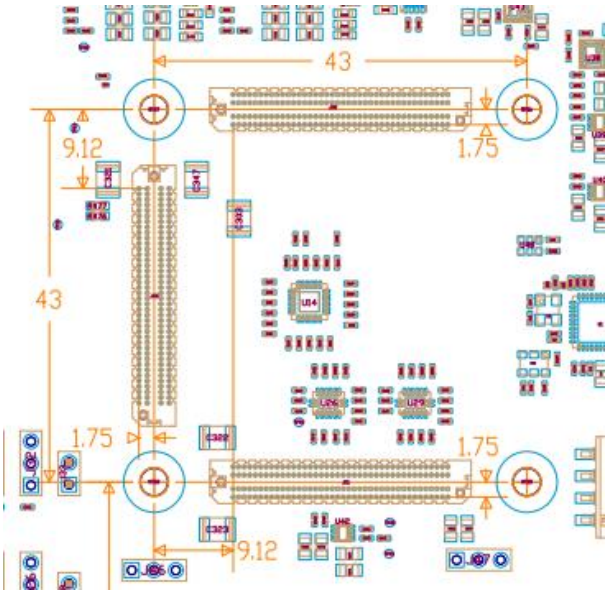

Figure 14 – Bottom Mechanical Dimensions

(INSERT Side Mechanical Dimensions Image)

Figure 15 – Side Mechanical Dimensions (TBD)

10 Carrier Card PCB Design Guidelines

The following sections provide general PCB design guidelines for designing with the VE2302 SOM.

10.1 Connector Land and Alignment

It is extremely important that carrier card designers ensure that the JX Micro Headers have the proper land patterns and that the connectors are aligned correctly. Connector alignment is ensured if the alignment pin holes in the PCB connector pattern are in the correct positions and if the holes are drilled to the proper size and tolerance by the PCB fabricator.

Please refer to the VE2302 SOM mechanical drawing available on the VE2302 SOM documentation page at **http://avnet.me/ve2302-som** for more information.

10.2 USB and Ethernet Connector Signal Routing

Due to critical timing that exists between the physical PHYs for the Gigabit Ethernet and USB2.0 interfaces to the associated controllers in the AMD Versal™ AI Edge APSoC device, the decision was made to implement the Gigabit Ethernet and USB 2.0 PHYs on the VE2302 SOM. The outputs of the PHYs are connected to the JX connectors. It is the responsibility of the end-user carrier card designer to implement the proper connections to an RJ45 GbE jack for Gigabit Ethernet and a USB connector for its USB2.0 interface.

NOTE: Please refer to the **Versal™ AI Edge Carrier Card Hardware User Guide** for an example implementation RJ45 GbE jack and the USB2.0 Type-A connector.

NOTE: Please refer to the **VE2302 SOM Net Length Report** for information on specific net lengths of the individual signals routing to the JX1, JX2, or JX3 connectors.

10.2.1 Ethernet Connector Pin routing

- ETH_MD1-4 differential pairs are to be routed 100Ω differential impedance, with a 10% tolerance.
- The differential pair trace tuning should be within 2mils of each other.

10.2.2 USB Connector Pin routing

- All USB Control signals are to be routed 50Ω characteristic impedance.
- The USB differential pair is to be routed with 90Ω differential impedance, with a 10% tolerance.
- Length tune the differential signals to 2 mils from longest to shortest.
- SHIELD_USB-A and SHIELD_USB-B can be an isolated plane cutout separate from GND and then connected to GND via the TWO COMPONENTS (CAP / RES).

10.3 GTYP Transceiver Signal Routing

It is highly recommended that the guidelines described in the Xilinx document “Versal Adaptive SoC GTY and GTYP Transceivers Architecture Manual” (**AM002**), be reviewed prior to designing and routing GTYP circuits. Here are some general guidelines that are followed on GTYP routing:

- All Multi-Gigabit Transceiver signals shall be routed Strip-line. It is expected that these signals will utilize via-in-pad to transition immediately to signal layers for routing on performance rated high speed material layers.
- It is encouraged to route the GTYP signals without signals stubs. This requires HDI (high density interconnect) techniques to accomplish this. This provides for best performance.
- If HDI techniques are not possible, the Multi-Gigabit Transceiver signals should have BACK DRILLING of all stubs to the nearest layer to the signal layer being used. It is expected that all VIAs used for the Multi-Gigabit Transceiver signals will be BACK DRILLED.
- All Multi-Gigabit Transceiver TX, RX and related clock differential signals shall be routed differential at appropriate differential impedance per datasheet requirements.
- All Multi-Gigabit Transceiver differential signals can be treated as a group and shall be length tuned as close as possible to facilitate 32Gbps data rates.
- All Multi-Gigabit Transceiver signals within a single pair (P and N) shall be length tuned to as close as possible of each other (P-to-N) to facilitate 32Gbps data rates.
- No more than two transitions (vias) are allowed for these signals.
- It is expected that the routing of the MGTs will be performed with smooth traces, i.e. – no sharp direction changes.
- Multi-Gigabit Transceiver reference clocks do not need to be length tuned to the data signal pairs but should be length tuned to each other as close as possible to facilitate 32Gbps data rates.
- The GTYP routing on the end-user carrier card should utilize Signal Integrity (SI) analysis prior to fabrication to ensure the ability to achieve the design GTYP performance in the system.

NOTE: Please refer to the **VE2302 SOM Net Length Report** for information on specific net lengths of the individual signals routing to the JX1, JX2, or JX3 connectors.

10.4 PMC and LPD MIO Routing

The routing of the PMC MIO and LPD MIO signals on the end-user carrier cards depends on how these signals are defined and used.

When routing the PMC and LPD MIO signals, they should be length matched within each interface type.

The following states general guidelines for routing the PMC and LPD MIO signals on end-user carrier cards.

- All signals are to be routed 50Ω characteristic impedance.
- Route all PMC MIO and LPD MIO signals as single-ended 50Ω traces.
- Implement length matching as required by the interface used on individual MIO signal groups defined by the application MIO configuration.
- All MIO signals must be 1.8V compatible.

NOTE: Please refer to the **VE2302 SOM Net Length Report** for information on specific net lengths of the individual signals routing to the JX1, JX2, or JX3 connectors.

10.5 SYSMON Signal Routing

The SYSMON interface is connected to the bank 500 of the Versal™ Adaptive SoC and consists of **VP**, **VN**, **VREF**, **VCCAUX** and **AGND** pins. These pins are routed to the **JX1** connector and can be used on end-user carrier cards to implement low speed analog interface. The SYSMON supply voltages are provided on the VE2302 SOM.

Here are some general guidelines for designing the SYSMON interface on end-user carrier cards.

- Use 4X spacing on the traces.

- Single ended impedance is 50Ω and differential is 100Ω.
- All paired signals should be routed to within 50mils of each other.
- All interface signals should be routed to within 100mils of each other

10.6 HDIO and XPIO Signal Routing

The following states general guidelines for routing the PL single-ended and differential signal routing on the custom Carrier Card.

- All single ended signals are to be routed 50Ω characteristic impedance.
- The differential pairs are to be routed with 100Ω differential impedance.

NOTE: Please refer to the **VE2302 SOM Net Length Report** for information on specific net lengths of the individual signals routing to the JX1, JX2, or JX3 connectors.

10.7 JX1, JX2, and JX3 Routing Delays

The following tables can be used when routing the PL single-ended and/or differential signals on the end-user carrier cards. This table shows the average routing delays (ns) for all signals connected from the Versal™ AI Edge APSoC device to the JX1/JX2/JX3 connectors on the VE2302 SOM. The JX1/JX2/JX3 signals are divided into groups and traces are delay matched within each group. Since not all signals are routed to the JX1/JX2/JX3 connectors using equal routing delay, routing delay matching must be done on the end-user carrier cards when an interface uses multiple signal groups.

Net Name	IO Bank	Routing Delay (ns)
HDIO_302_L10_P	302	0.36414
HDIO_302_L10_N	302	0.36494
HDIO_302_L9_P	302	0.36266
HDIO_302_L9_N	302	0.36309
HDIO_302_L8_P	302	0.36197
HDIO_302_L8_N	302	0.36168
HDIO_302_L7_P	302	0.36233
HDIO_302_L7_N	302	0.36263
HDIO_302_HDGC_L6_P	302	0.36474
HDIO_302_HDGC_L6_N	302	0.36378
HDIO_302_HDGC_L5_P	302	0.36542
HDIO_302_HDGC_L5_N	302	0.36544
HDIO_302_L4_P	302	0.36509
HDIO_302_L4_N	302	0.365
HDIO_302_L3_P	302	0.36795
HDIO_302_L3_N	302	0.36733
HDIO_302_L2_P	302	0.36915
HDIO_302_L2_N	302	0.36903
HDIO_302_L1_P	302	0.36566

Net Name	IO Bank	Routing Delay (ns)
HDIO_302_L1_N	302	0.36575
HDIO_302_L0_P	302	0.36277
HDIO_302_L0_N	302	0.36303
LPD_MIO23	502	0.2762
LPD_MIO22	502	0.27767
LPD_MIO21	502	0.27612
LPD_MIO20	502	0.27538
LPD_MIO19	502	0.27616
LPD_MIO18	502	0.27625
LPD_MIO17	502	0.2747
LPD_MIO16	502	0.27601
LPD_MIO15	502	0.27632
LPD_MIO14	502	0.27595
LPD_MIO13	502	0.27611
LPD_MIO12	502	0.27656
PMC_MIO49	501	0.35072
PMC_MIO48	501	0.35105
PMC_MIO47	501	0.35085
PMC_MIO46	501	0.35119
PMC_MIO45	501	0.35263
PMC_MIO44	501	0.35151
PMC_MIO43	501	0.35208
PMC_MIO42	501	0.35091
PMC_MIO41	501	0.3502
PMC_MIO40	501	0.35287
PMC_MIO39	501	0.35153
PMC_MIO38	501	0.35264
PMC_MIO37	501	0.3511

Table 37 – JX1 Connector Routing Delay

Net Name	IO Bank	Routing Delay (ns)
XPIO_702_L26_P	702	NA
XPIO_702_L26_N	702	NA
XPIO_702_L23_P	702	0.36031
XPIO_702_L23_N	702	0.36043
XPIO_702_L22_P	702	0.36041

Net Name	IO Bank	Routing Delay (ns)
XPIO_702_L22_N	702	0.36051
XPIO_702_XCC_L21_P	702	0.36034
XPIO_702_XCC_L21_N	702	0.36049
XPIO_702_L20_P	702	0.34802
XPIO_702_L20_N	702	0.34799
XPIO_702_L19_P	702	0.34798
XPIO_702_L19_N	702	0.34783
XPIO_702_XCC_L18_P	702	0.34794
XPIO_702_XCC_L18_N	702	0.34803
XPIO_702_L17_P	702	0.35324
XPIO_702_L17_N	702	0.3532
XPIO_702_L16_P	702	0.35322
XPIO_702_L16_N	702	0.35314
XPIO_702_XCC_L15_P	702	0.35323
XPIO_702_XCC_L15_N	702	0.35318
XPIO_702_L14_P	702	0.41595
XPIO_702_L14_N	702	0.41591
XPIO_702_L13_P	702	0.4159
XPIO_702_L13_N	702	0.41583
XPIO_702_GC_XCC_L12_P	702	0.41598
XPIO_702_GC_XCC_L12_N	702	0.41591
XPIO_702_L11_P	702	0.34718
XPIO_702_L11_N	702	0.34718
XPIO_702_L10_P	702	0.3472
XPIO_702_L10_N	702	0.34723
XPIO_702_GC_XCC_L9_P	702	0.34713
XPIO_702_GC_XCC_L9_N	702	0.34719
XPIO_702_L8_P	702	0.34513
XPIO_702_L8_N	702	0.34529
XPIO_702_L7_P	702	0.34535
XPIO_702_L7_N	702	0.34523
XPIO_702_GC_XCC_L6_P	702	0.34525
XPIO_702_GC_XCC_L6_N	702	0.3451
XPIO_702_L5_P	702	0.37219
XPIO_702_L5_N	702	0.37215
XPIO_702_L4_P	702	0.37224

Net Name	IO Bank	Routing Delay (ns)
XPIO_702_L4_N	702	0.3722
XPIO_702_XCC_L3_P	702	0.3722
XPIO_702_XCC_L3_N	702	0.37227
XPIO_702_L2_P	702	0.31216
XPIO_702_L2_N	702	0.31212
XPIO_702_L1_P	702	0.3123
XPIO_702_L1_N	702	0.3122
XPIO_702_XCC_L0_P	702	0.31227
XPIO_702_XCC_L0_N	702	0.31223
XPIO_703_L26_P	703	0.31731
XPIO_703_L26_N	703	0.31712
XPIO_703_L25_P	703	0.31722
XPIO_703_L25_N	703	0.31726
XPIO_703_GC_XCC_L24_P	703	0.31718
XPIO_703_GC_XCC_L24_N	703	0.31726
XPIO_703_L23_P	703	0.33675
XPIO_703_L23_N	703	0.33681
XPIO_703_L22_P	703	0.33689
XPIO_703_L22_N	703	0.33675
XPIO_703_XCC_L21_P	703	0.33684
XPIO_703_XCC_L21_N	703	0.33698
XPIO_703_L20_P	703	0.34151
XPIO_703_L20_N	703	0.34125
XPIO_703_L19_P	703	0.34139
XPIO_703_L19_N	703	0.34138
XPIO_703_XCC_L18_P	703	0.34146
XPIO_703_XCC_L18_N	703	0.34147
XPIO_703_L17_P	703	0.33302
XPIO_703_L17_N	703	0.33289
XPIO_703_L16_P	703	0.33306
XPIO_703_L16_N	703	0.33312
XPIO_703_XCC_L15_P	703	0.33298
XPIO_703_XCC_L15_N	703	0.33316
XPIO_703_L14_P	703	0.33819
XPIO_703_L14_N	703	0.33826
XPIO_703_L13_P	703	0.3381

Net Name	IO Bank	Routing Delay (ns)
XPIO_703_L13_N	703	0.33823
XPIO_703_GC_XCC_L12_P	703	0.33807
XPIO_703_GC_XCC_L12_N	703	0.33818
XPIO_703_L11_P	703	0.35377
XPIO_703_L11_N	703	0.35382
XPIO_703_L10_P	703	0.35362
XPIO_703_L10_N	703	0.35372
XPIO_703_GC_XCC_L9_P	703	0.35374
XPIO_703_GC_XCC_L9_N	703	0.35382
XPIO_703_L8_P	703	0.3193
XPIO_703_L8_N	703	0.31946
XPIO_703_L7_P	703	0.31945
XPIO_703_L7_N	703	0.31947
XPIO_703_GC_XCC_L6_P	703	0.31946
XPIO_703_GC_XCC_L6_N	703	0.31935
XPIO_703_L5_P	703	0.34927
XPIO_703_L5_N	703	0.34935
XPIO_703_L4_P	703	0.34929
XPIO_703_L4_N	703	0.34948
XPIO_703_XCC_L3_P	703	0.34932
XPIO_703_XCC_L3_N	703	0.3492
XPIO_703_L2_P	703	0.32863
XPIO_703_L2_N	703	0.32869
XPIO_703_L1_P	703	0.32862
XPIO_703_L1_N	703	0.32883
XPIO_703_XCC_L0_P	703	0.32858
XPIO_703_XCC_L0_N	703	0.32867

Table 38 – JX2 Connector Routing Delay

Net Name	IO Bank	Routing Delay (ns)
GTYP_103_RX3_P	103	0.23271
GTYP_103_RX3_N	103	0.23273
GTYP_103_RX2_P	103	0.23266
GTYP_103_RX2_N	103	0.2327
GTYP_103_RX1_P	103	0.23266
GTYP_103_RX1_N	103	0.23264

Net Name	IO Bank	Routing Delay (ns)
GTYP_103_RX0_P	103	0.23267
GTYP_103_RX0_N	103	0.23274
GTYP_103_TX3_P	103	0.23055
GTYP_103_TX3_N	103	0.23055
GTYP_103_TX2_P	103	0.2304
GTYP_103_TX2_N	103	0.23051
GTYP_103_TX1_P	103	0.23054
GTYP_103_TX1_N	103	0.2306
GTYP_103_TX0_P	103	0.23066
GTYP_103_TX0_N	103	0.23053
GTYP_103_REFCLK1_P	103	0.24585
GTYP_103_REFCLK1_N	103	0.24602
GTYP_103_REFCLK0_P	103	0.24601
GTYP_103_REFCLK0_N	103	0.24594
GTYP_104_RX3_P	104	0.25697
GTYP_104_RX3_N	104	0.25694
GTYP_104_RX2_P	104	0.25689
GTYP_104_RX2_N	104	0.25689
GTYP_104_RX1_P	104	0.25682
GTYP_104_RX1_N	104	0.25688
GTYP_104_RX0_P	104	0.25702
GTYP_104_RX0_N	104	0.25697
GTYP_104_TX3_P	104	0.27445
GTYP_104_TX3_N	104	0.27441
GTYP_104_TX2_P	104	0.27438
GTYP_104_TX2_N	104	0.27453
GTYP_104_TX1_P	104	0.27436
GTYP_104_TX1_N	104	0.27439
GTYP_104_TX0_P	104	0.27446
GTYP_104_TX0_N	104	0.27451
GTYP_104_REFCLK1_P	104	0.25367
GTYP_104_REFCLK1_N	104	0.2535
GTYP_104_REFCLK0_P	104	0.25356
GTYP_104_REFCLK0_N	104	0.25347

Table 39 – JX3 Connector Routing Delay

10.8 JTAG Interface Signal Routing

The four dedicated JTAG signals are routed to the JX1 connector. An end-user carrier card must utilize these JTAG signals to program and debug the VE230 SOM as a JTAG programming header is not implemented on VE2302 SOM. When connecting additional JTAG devices in-line with the VE2302, be sure that TCK and TMS are properly buffered.

NOTE: Please refer to the **Versal™ AI Edge Carrier Card Hardware User Guide** for an example implementation of a JTAG interface.

NOTE: Please refer to the **VE2302 SOM Net Length Report** for information on specific net lengths of the individual signals routing to the JX1, JX2, or JX3 connectors.

10.9 Decoupling Caps

Decoupling capacitors, filters or other components must be placed as close as possible to the power ICs or JX connector.

- All switching components (inductors, capacitors, transistors, MOSFETs) will be placed according to the datasheet recommendations. If a data sheet is not available, the inductors must be placed on the top side of the board within 250 mils of the drive IC. The output capacitors after the inductor must be a low impedance, high current path and not to be placed further than 250 mils from the respective inductor.

- Feedback components and sense signal points much must be routed within 100 mils of the end power point (at the output filter capacitor junction for instance).

Additional decoupling should be provided on the end-user carrier card for the following rails as these were omitted to save space on the VE2302 SOM:

+VIN	Enough to support overall system design (Recommend 1x 330uF and 8x 47uF)
+VCCINT	2x 330uF-1210 and 3x 100uF-0805
+MGTYPAVCC	1x 330uF-1210 and 1x 100uF-0805
+MGTYPAVTT	1x 330uF-1210 and 1x 100uF-0805

10.10 Mechanical Considerations

VE2302 SOM measures 50.0mm x 50.0mm (approximately 1.97” x 1.97”). End-user carrier cards would have to be large enough to support the dimensions shown.

The end-user carrier card design should take care when adding components underneath the VE2302 SOM as components from the SOM could short with components from the end-user carrier card. Also, it is difficult to provide thermal relief to components under the SOM so designers should attempt to limit circuitry placed directly beneath the SOM.

The end-user carrier card design should consider additional height for thermal solutions that will be required in development of a system using the VE2302 SOM.

10.11 Thermal Considerations

Thermal relief is an important design factor in each VE2302-based system design. A detailed thermal analysis should be performed for each specific application of VE2302 SOM, and an end-user designed carrier card.

The four mounting holes on the four corners of VE2302 SOM are electrically connected to a heavier ground plane. With the mounting holes of the VE2302 SOM, system designers may choose to attach the VE2302 SOM to their carrier card using metal standoffs providing another path for heat dissipation.

It is expected that a system designer will perform worst case analysis of the thermal environment of the final solution and devise a proper thermal solution for the challenges presented in the system operating environment. Depending on the end-user application, the performance of the VE2302 SOM will require a thermal solution to ensure expected performance across all temperature ranges due to lack of knowledge regarding end-user's thermal environment and the possible enclosure of the VE2302 SOM.

For aggressive applications it is recommended that an accurate worst-case power analysis be performed to avoid the pitfalls of over designing or under designing your product's power and thermal management system. End users should design a heatsink and fan assembly that is more conducive to the requirements of their system including alternative mounting techniques for the assembly which could enhance the thermal reliability of the system.

11 Getting Help and Support

If additional support is required, Tria Technologies has many avenues to search depending on your needs.

For general question regarding the Versal™ AI Edge Carrier Card, please visit our website at **http://avnet.me/ve2302-dk**. Here you can find any available documentation, technical specifications, videos and tutorials, reference designs and other support.

For more information regarding the VE2302 SOM, please visit our website at **http://avnet.me/ve2302-som**.

Detailed questions regarding VE2302 SOM hardware design, software application development, using AMD tools, training and other topics can be posted on the VE2302 SOM Support Forum at **http://avnet.me/ve2302-som-forum**. The Tria technical support team monitors the forum during normal business hours in North America.

Those interested in customization options on Versal™ AI Edge Carrier Card can send inquiries to **customize@avnet.com**.

12 General Information

Tria Technologies wants to highlight that the information presented in this user guide is subject to change, particularly due to the ongoing improvements in our product offerings. This document does not serve as a guarantee from Tria Technologies regarding the technical procedures outlined in the user guide or the product characteristics described therein. Tria Technologies holds no responsibility or liability for the use of the mentioned product(s), does not provide any licenses or rights related to patents, copyrights, or mask work rights for these products, and does not claim that these products are free from any infringements, unless explicitly stated. The applications showcased in this user guide are purely for illustrative purposes. Tria Technologies does not state that such applications are inherently suitable for the specified use without further testing or adjustments. It is essential to understand that this user guide offers a general overview of processes and instructions, which may not be universally applicable. If there are any uncertainties, please reach out to Tria Technologies.

12.1 Intended Use

THIS DEVICE AND ASSOCIATED SOFTWARE ARE NOT DESIGNED, MANUFACTURED OR INTENDED FOR USE OR RESALE FOR THE OPERATION OF NUCLEAR FACILITIES, THE NAVIGATION, CONTROL OR COMMUNICATION SYSTEMS FOR AIRCRAFT OR OTHER TRANSPORTATION, AIR TRAFFIC CONTROL, LIFE SUPPORT OR LIFE SUSTAINING APPLICATIONS, WEAPONS SYSTEMS, OR ANY OTHER APPLICATION IN A HAZARDOUS ENVIRONMENT, OR REQUIRING FAIL-SAFE PERFORMANCE, OR IN WHICH THE FAILURE OF PRODUCTS COULD LEAD DIRECTLY TO DEATH, PERSONAL INJURY, OR SEVERE PHYSICAL OR ENVIRONMENTAL DAMAGE (COLLECTIVELY, “HIGH RISK APPLICATIONS”)

You understand and agree that your use of Tria Technologies devices as a component in High-Risk Applications is entirely at your risk. To minimize the risks associated with your products and applications, you should provide adequate design and operating safeguards. You are solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning your products. You are responsible to ensure that your systems (and any Tria Technologies hardware or software components incorporated in your systems) meet all applicable requirements. Unless otherwise stated in the product documentation, the Tria Technologies device is not provided with error-tolerance capabilities and cannot therefore be deemed as being engineered, manufactured or setup to be compliant for implementation or for resale as device in High-Risk Applications. All application and safety related information in this document (including application descriptions, suggested safety measures, suggested Tria Technologies products, and other materials) is provided for reference only.

Handling and operation of the product is permitted only for trained personnel within a workplace that is access controlled. Follow the “General Safety Instructions” supplied with the product.

This product is not suited for storage or operation in corrosive environments, under exposure to sulfur and chlorine and their compounds. For information on how to harden electronics and mechanics against these stress conditions, contact Tria Technologies’ Support.

12.2 RoHS Compliance

The product is designed by using RoHS compliant components and manufactured on lead free production process to IPC-A-600(*) Class 2 standards.

12.3 Electrostatic Discharge

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, to ensure product integrity at all times.

Do not handle this product out of its protective packaging while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe workstations. Where a safe workstation is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

12.4 Warranty

At the following weblink you will find information regarding warranty, RoHS compliance, and expected lifecycle information regarding these products.

Warranty Terms: **WARRANTY-AND-LIFECYCLE**