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PicoZed™ Based Embedded Computing Systems Carrier Design Guide

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Version	Date	Comment
1.0	3/28/2014	Initial Release
1.1	4/21/2014	Update Images
1.2	4/25/2014	Update PicoZed 7015/7030 Pin Outs
1.3	5/8/2014	PicoZed PS GbE and PS USB Implementations
1.4	9/4/2014	Production Release
1.5	10/2/2014	Minor Update to USB Implementation
2.0	12/10/2014	Table Corrections, Added Appendix A
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2.3	12/3/2015	Minor Wording Correction
2.4	02/29/2018	Corrected Connector Land and Alignment Section
2.5	8/17/2020	Corrected Table 8 and updated Section 3.1.4, and Section 4.3 for eFuse Integrity control of PG_MODULE.

Table of Contents

1 INTRODUCTION

This document provides information for designing a custom system carrier card for PicoZed. It includes reference schematics for the external circuitry required to implement the various PicoZed peripheral functions. It also explains how to extend the supported busses and how to add additional peripherals and expansion slots.

1.1 Glossary

Term	Definition
MIO	Multiplexed Input Output – the dedicated I/O available on the PS
PL	Programmable Logic
POR	Power On Reset
PS	Processing System

1.2 Additional Documentation

Additional information and documentation on Xilinx's Zynq®-7000 All Programmable SoCs can be found at www.xilinx.com/zynq. Additional information and documentation on PicoZed can be found at www.picozed.org.

2 PICOZED OPTIONS

PicoZed comes in 7010, 7015, 7020, and 7030 versions. Additionally, each version is offered populated with Commercial temperature grade (0° C to 70° C) or Industrial temperature Grade (-40° C to 85° C).

2.1 PL Resources

The resource comparison between the various Zynq devices can be seen in Xilinx document XMP087.

2.2 PL I/O

PicoZed connects 50 I/Os from both Bank 34 and Bank 35. Additionally, the PicoZed 7020 version adds another 25 I/O from Bank 13 while the PicoZed 7015 and 7030 add a total of 35 I/O from Bank13. The Micro Headers provide for independent Vcco pins for Bank 13, which provides for additional voltage flexibility. Please note the PL IO Bank power rails (Vccio_34, Vccio_35, and Vccio_13 [7015/7020/7030 versions]) must be powered from a Carrier Card via JX1, JX2, and JX3 if used.

2.3 Transceiver I/O

The 7010 and 7020 devices do not support transceivers and thus PicoZed with the 7010 or 7020 does not populate the JX3 Micro Header with the transceiver signals or transceiver power. In this case, you can omit the requirement of providing connections to the transceiver signals or providing transceiver power rails from the Carrier Card design.

The PicoZed 7015/7030 offers GTP transceivers in the 7015 and GTX transceivers in the 7030. The Carrier Card design should carefully examine desired performance requirements of the transceivers and provide adequate signalling and transceiver power on the associated pins of the JX3 connector. In the case where the transceivers are not needed, the Carrier Card should take care to follow the UNUSED TRANSCEIVER guidelines defined in the respective Transceiver User Guide.

NOTE: The transceivers differ between the 7015 and the 7030 in power requirements and care should be taken depending on which platform is desired in your system. Review the Transceiver User's Guides for details surrounding the difference between designs using the 7015 versus the 7030.

2.4 Thermal

The wide range of devices supported by PicoZed has significantly varying internal PL resources. Take care to design a thermal management system to account for your final design needs. PicoZed has provided a 3.3V/5V Active Fan header and the 7010/7020 modules provide thru-holes for push-pin heat sinks.

3 PICOZED INTERFACES

A Carrier Card may utilize several Zynq interfaces on the PicoZed. A table showing the Signals, Pin Count, and Zynq source is shown below.

Micro Header #1 (JX1)			
Signal Name		Source	Pin Count
PL	Bank 34 I/Os (except for PUDC_B)	Zynq Bank 34 or Zynq Bank 35	49 ##
	Bank 13 I/Os	Zynq Bank 13	8 **
JTAG	TMS_0	Zynq Bank 0	5
	TDI_0	Zynq Bank 0	
	TCK_0	Zynq Bank 0	
	TDO_0	Zynq Bank 0	
	Carrier_SRST#	Carrier	
Analog	VP_0	Zynq Bank 0	4
	VN_0	Zynq Bank 0	
	DXP_0	Zynq Bank 0	
	DXN_0	Zynq Bank 0	
C	PUDC_B / IO	Zynq Bank 34	2
	DONE	Zynq Bank 0	
Power	PWR_Enable	Carrier	1
	Vin	Carrier	4
	GND	Carrier	23
	VCCO_34	Carrier	3
	VBATT	Carrier	1
		TOTAL	100

Table 1 – JX1 Micro Header Pinout

** PicoZed 7015/7020/7030
PicoZed 7010/7020 Bank 34 and PicoZed 7015/7030 Bank 35

Micro Header #2 (JX2)			
Signal Name		Source	Pin Count
PL	Bank 35 I/Os	Zynq Bank 35 or Zynq Bank 34	50 ##
	Bank 13 I/Os	Zynq Bank 13	7 **
PS	PS MIO [0,9-15]	Zynq Bank 500	8
C	Init_B_0	Zynq Bank 0	1
Power	VCCIO_EN	Module/Carrier	1
	PG_MODULE	Module/Carrier	1
	Vin	Carrier	5
	GND	Carrier	23
	VCCO_13	Carrier	1
	VCCO_35	Carrier	3
		TOTAL	100

Table 2 – JX2 Micro Header Pinout

** PicoZed 7015/7020/7030
PicoZed 7010/7020 Bank 35 and PicoZed 7015/7030 Bank 34

Micro Header #3 (JX3)			
Signal Name		Source	Pin Count
PL	Bank 13 I/Os	Zynq Bank 13	20 **
XCVR	MGTTX I/Os	Zynq Bank 112	20 ##
	MGTRX I/Os	Zynq Bank 112	
	MGTREFCLK I/Os	Zynq Bank 112	
PS	MIO[40-51]	Zynq Bank 501	26
	ETHERNET	Zynq Bank 501	
	USB 2.0	Zynq Bank 500	
Power	USB_VBUS_OTG	Carrier	1
	VCCO_13	Carrier	2
	MGTAVCC	Carrier	4
	MGTAVTT	Carrier	2
	GND	Carrier	25
		TOTAL	100

Table 3 – JX3 Micro Header Pinout

** PicoZed 7020 has 10 I/O and PicoZed 7015/7030 adds 20 I/O
PicoZed 7015/7030 only

3.1 PS

3.1.1 MIO BANK 500

Eight PS MIOs (0, 9-15) are shared between the eMMC on-board PicoZed and the JX2 Micro Header. Care must be taken when it is desired to use the eMMC and the PS MIO signals that go to the carrier card.

A multiplexer has been implemented on PicoZed to allow these interfaces to be shared depending on the customers end design. The multiplexer select line is capable of being controlled via MIO0 from a SW perspective or the select line can be fixed via a hardware pull-up or pull-down resistor on PicoZed. By default, the multiplexer select line is pulled down selecting the eMMC interface on PicoZed. In the scenario where MIO0 is used to control the select line via software, MIO0 is unavailable on the JX2 PS interface and the end user should not utilize the MIO0 pin from the carrier card. This leaves the JX2 PS interface at 7 processor pins.

If it is desired that the user only utilizes the JX2 PS interface, the proper solution would be to set the PS_MIO0_SEL resistor to select the JX2 PS interface. The PS_MIO0_SEL resistor can be set to select the JX2 PS interface, and the PS_MIO0 resistor can be set to PS_MIO0_MUX in order to make MIO0 available on the JX2 PS interface. The end user can than utilize the MIO0 pin from the carrier card. This would give the JX2 PS interface all 8 processor pins.

Please review the PicoZed Hardware User Guide for further details surrounding the eMMC / JX2 PS MIO Interface Multiplexer.

PicoZed 7015/7030 Pin #	PicoZed 7010/7020 Pin #	MIO	Net Name	JX2 Pin #	JX2 Pin #	Net Name	MIO	PicoZed 7010/7020 Pin #	PicoZed 7015/7030 Pin #
500 – G16	500 - E9	10	MIO10	1	2	MIO13	13	500 - E9	500 – A17
500 – B17	500 - C5	14	MIO14	3	4	MIO15	15	500 - C5	500 – E17
500 – C18	500 - D9	12	MIO12	5	6	MIO11	11	500 - D9	500 – B19
500 – G17	500 - E6	0	MIO0	7	8	MIO9	9	500 - E6	500 – C19

Table 4 – JX2 PS MIO Connections

3.1.2 MIO BANK 501

Twelve PS MIOs (40-51) are mapped to the JX3 Micro Header.

PicoZed 7015/7030 Pin #	PicoZed 7010/7020 Pin #	MIO	Net Name	JX3 Pin #	JX3 Pin #	Net Name	MIO	PicoZed 7010/7020 Pin #	PicoZed 7015/7030 Pin #
501 – E9	501 - D14	40	PS_MIO40	43	41	PS_MIO46	46	501 - D16	501 – D11
501 – C15	501 - C17	41	PS_MIO41	34	40	PS_MIO47	47	501 - B14	501 - B13
501 – D15	501 - E12	42	PS_MIO42	37	42	PS_MIO48	48	501 - B12	501 – D12
501 – B12	501 - A9	43	PS_MIO43	36	44	PS_MIO49	49	501 - C12	501 – C9
501 – E10	501 - F13	44	PS_MIO44	39	66	PS_MIO50	50	501 - B13	501 – D10
501 – B14	501 - B15	45	PS_MIO45	38	64	PS_MIO51	51	501 - B9	501 – C13

Table 5 – JX3 PS MIO Connections

Depending on the desired design solution, multiple Zynq PS peripherals can map to the eight BANK 500 PS MIO pins and the twelve BANK 501 PS MIO pins. A new hardware platform should be designed to enable the desired peripheral. Please review the Zynq SOC TRM, UG585, for the mapping requirements of the various available Zynq PS peripherals when designing a PicoZed carrier card.

3.1.3 PS GbE Ethernet and PS USB – Special Considerations

Due to critical timing that exists between the physical PHYs for the Gigabit Ethernet and USB2.0 interfaces to the associated PS controllers in the Xilinx Zynq devices, Avnet has decided to implement the Gigabit Ethernet and USB 2.0 PHYs on the PicoZed SOMs. The outputs of the PHYs are connected to the JX3 Micro Header. It is the responsibility of the Customer Carrier Card designer to implement the proper connections to an RJ45 connector for Gigabit Ethernet and a USB connector for its USB2.0 interface. The following table depicts the necessary JX3 connections and the two subsequent figures shows examples of the Gigabit Ethernet and USB2.0 implementations that could exist on a PicoZed Carrier Card. It is recommended that these designs be used as an example and that the final solution will be tailored to the solution as required by the specific custom Carrier Card requirements.

Net Name	JX3 Pin #	JX3 Pin #	Net Name
ETH_PHY_LED0	47	48	ETH_PHY_LED1
ETH_MD1_P	51	52	ETH_MD2_P
ETH_MD1_N	53	54	ETH_MD2_N
ETH_MD3_P	57	58	ETH_MD4_P
ETH_MD3_N	59	60	ETH_MD4_N
USB_OTG_ID	63	68	USB_VBUS_OTG
USB_OTG_P	67	70	USB_OTG_CPEN
USB_OTG_N	69		

Table 6 – JX3 Gigabit Ethernet and USB2.0 Connections

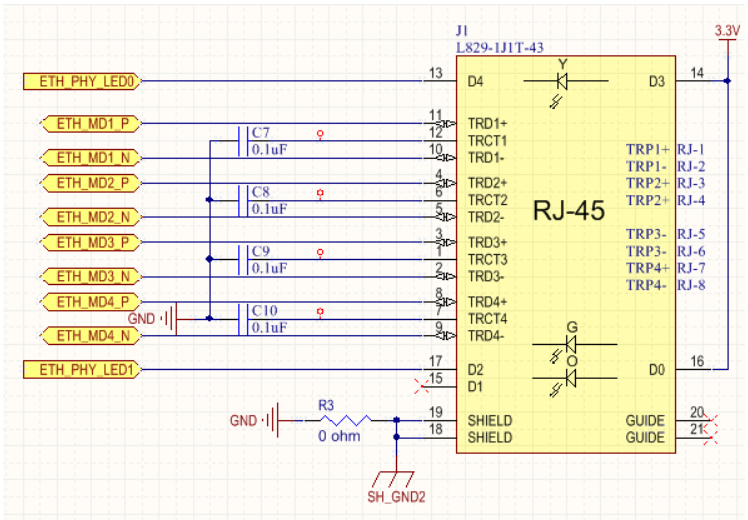

Figure 1 – PicoZed Carrier Card Example Gigabit Ethernet Implementation

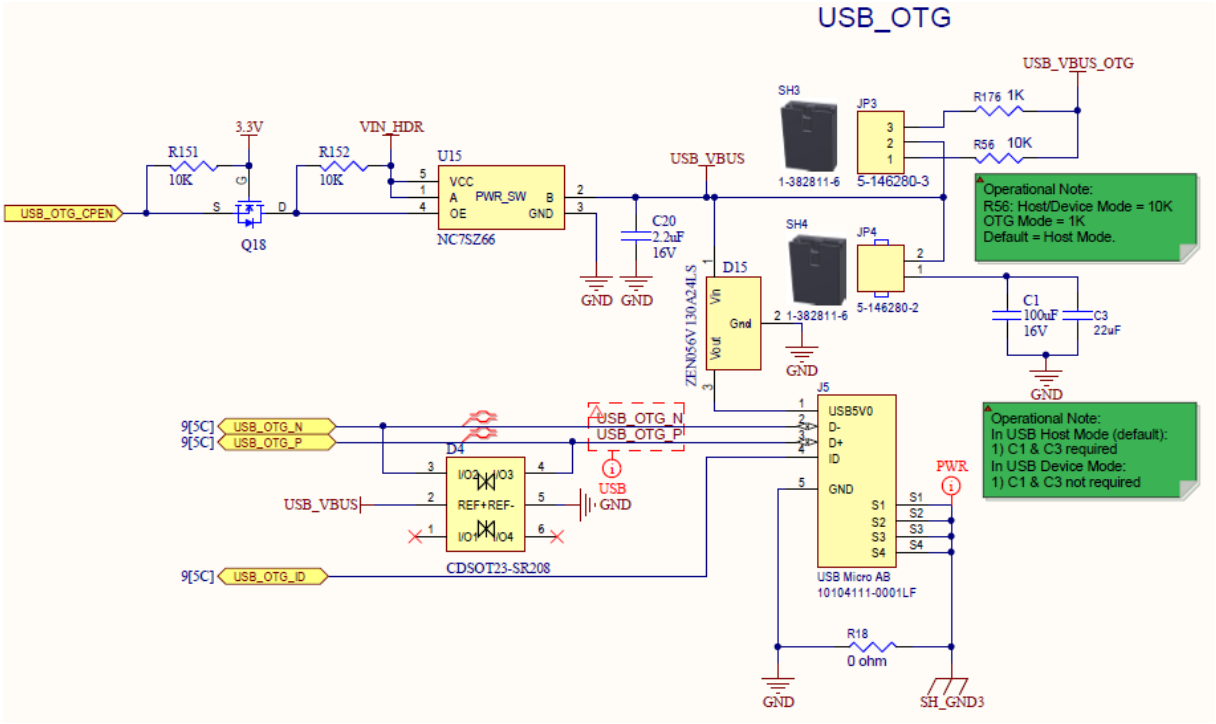

Figure 2 – PicoZed Carrier Card Example USB2.0 Implementation

3.1.4 Control

PicoZed routes two system control signals to the Micro Headers, CARRIER_SRST# and PG_MODULE.

Function	Signal Name	Micro Header Connection	Subsection	PicoZed 7010/7020 Pin #	PicoZed 7015/7030 Pin #
External System Reset	CARRIER_SRST#	JX1.6	PS (MIO Bank 501)	B10	C14
External Power-on-Reset	PG_MODULE	JX2.11	PS (MIO Bank 500)	C7	B18

Table 7 – System Control Signals

External system reset, labelled CARRIER_SRST#, resets the processor as well as erases all debug configurations. The external system reset allows the user to reset all the functional logic within the device without disturbing the debug environment. For example, the previous break points set by the user remain valid after system reset. Due to security concerns, system reset erases all memory content within the PS, including the OCM. The PL is also reset in system reset. System reset does not re-sample the boot mode strapping pins.

CARRIER_SRST# is an active-low signal. Asserting this signal asserts Zynq signal PS_SRST_B.

If this pin is not used in the system, it can be left floating since it is pulled up on the PicoZed.

Note: This signal cannot be asserted while the boot ROM is executing following a POR reset. If PS_SRST# is asserted while the boot ROM is running through a POR reset sequence it will trigger a lock-down event preventing the boot ROM from completing. To recover from lockdown the device either needs to be power cycled or PS_POR_B needs to be asserted.

The Zynq PS supports an external power-on reset signal labelled PG_MODULE. The power-on reset is the master reset of the entire chip. This signal resets every register in the device capable of being reset. The PG_MODULE signal is connected to the power good output of the final stage of the power regulation circuitry. These power supplies have open drain outputs that pull this signal low until the output voltage is valid. A carrier card should also wire-OR to this net and not release it until the carrier card power is also good. Other circuits on PicoZed are reset by this signal as well. The PG_MODULE signal can also be actively pulled low to initiate a power-on reset.

To stall Zynq boot-up, this signal should be held low. Other typical FPGA architecture signals (SRST, PROGRAM_B, INIT_B) are not capable of performing this function.

Important Carrier Card Design Requirement Update: PG_MODULE

The PG_MODULE signal connects to the Zynq-7000 signal PS_POR_B. This open-drain signal should be utilized in a custom carrier card design in order to meet the Power-On and Power-Off requirements documented in the Zynq-7000 datasheet and further documented in the Xilinx Zynq-7000 eFuse integrity Answer Record #65240. Failure to adhere to the guidelines presented in the data sheet and answer record could lead to damage to the PicoZed modules.

Xilinx Answer Record #65240: https://www.xilinx.com/support/answers/65240.html

On Power-On, PS_POR_B (PG_MODULE) needs to be asserted and held LOW for a minimum of 100uS after PS supply voltages reaches minimum levels. Also, care must be taken to ensure that the PS_POR_B (PG_MODULE) signal is not de-asserted HIGH during the Secure Lock Down Window described in the Xilinx Zynq-7000 datasheets and Xilinx Answer Record #63149.

Xilinx Answer Record #63149: https://www.xilinx.com/support/answers/63149.html

On Power-Off, PS_POR_B (PG_MODULE) needs to be asserted and held LOW prior to the PS power rails falling below acceptable thresholds identified in Xilinx Answer Record #65240 and maintain assertion through critical voltage levels as the PS power rails decay.

3.2 PL IO SIGNALS

PicoZed connects 50 I/Os from both Bank 34 and Bank 35. Additionally, the PicoZed 7020 version adds another 25 I/O from Bank 13 while the PicoZed 7015 and 7030 add a total of 35 I/O from Bank13. Each of these banks has independent power pins for Vcco on the Micro Headers. When flexibility in voltage standard is needed, each bank can be powered from a separate regulator. When cost is a concern, then all PL I/O banks can be tied to the same Vcco regulator.

A detailed discussion of the PL I/Os are available in the *PicoZed Hardware User Guide.*

3.3 Analog

The Zynq XADC pins are connected through the Micro Headers. For details of how this might be connected refer to Chapter 30 of the Zynq TRM, UG585, and UG480.

Carrier Net Name	PicoZed 7010/7020 JX Connections	PicoZed 7010/7020 Pin#	PicoZed 7015/7030 JX Connections	PicoZed 7015/7030 Pin#	Description
XADC_VP_0_P	JX1, pin 97	Bank 0, K9	JX1, pin 97	Bank 0, L12	XADC dedicated differential analog input
XADC_VP_0_N	JX1, pin 99	Bank 0, L10	JX1, pin 99	Bank 0, M11	
XADC_DXP_0_P	JX1, pin 98	Bank 0, M9	JX1, pin 98	Bank 0, N12	Temperature-sensing diode pins
XADC_DXN_0_N	JX1, pin 100	Bank 0, M10	JX1, pin 100	Bank 0, N11	
XADC_AD0_P	JX2, pin 17	Bank 35, C20	JX1, pin 67	Bank 35, F7	
XADC_AD0_N	JX2, pin 19	Bank 35, B20	JX1, pin 69	Bank 35, E7	
XADC_AD1_P	JX2, pin 23	Bank 35, E17	JX1, pin 35	Bank 35, E8	
XADC_AD1_N	JX2, pin 25	Bank 35, D18	JX1, pin 37	Bank 35, D8	
XADC_AD2_P	JX2, pin 36	Bank 35, M19	JX1, pin 82	Bank 35, C8	
XADC_AD2_N	JX2, pin 38	Bank 35, M20	JX1, pin 84	Bank 35, B8	
XADC_AD3_P	JX2, pin 35	Bank 35, L19	JX1, pin 74	Bank 35, A7	
XADC_AD3_N	JX2, pin 37	Bank 35, L20	JX1, pin 76	Bank 35, A6	
XADC_AD4_P	JX2, pin 54	Bank 35, J18	JX1, pin 48	Bank 35, D3	
XADC_AD4_N	JX2, pin 56	Bank 35, H18	JX1, pin 50	Bank 35, C3	
XADC_AD5_P	JX2, pin 68	Bank 35, J20	JX1, pin 61	Bank 35, E2	
XADC_AD5_N	JX2, pin 70	Bank 35, H20	JX1, pin 63	Bank 35, D2	
XADC_AD6_P	JX2, pin 73	Bank 35, K14	JX1, pin 23	Bank 35, G4	
XADC_AD6_N	JX2, pin 75	Bank 35, J14	JX1, pin 25	Bank 35, F4	
XADC_AD7_P	JX2, pin 82	Bank 35, L14	JX1, pin 17	Bank 35, G3	
XADC_AD7_N	JX2, pin 84	Bank 35, L15	JX1, pin 19	Bank 35, G2	Differential auxiliary analog inputs
XADC_AD8_P	JX2, pin 18	Bank 35, B19	JX1, pin 62	Bank 35, D7	
XADC_AD8_N	JX2, pin 20	Bank 35, A20	JX1, pin 64	Bank 35, D6	
XADC_AD9_P	JX2, pin 29	Bank 35, E18	JX1, pin 12	Bank 35, F5	
XADC_AD9_N	JX2, pin 31	Bank 35, E19	JX1, pin 14	Bank 35, E5	
XADC_AD10_P	JX2, pin 41	Bank 35, M17	JX1, pin 81	Bank 35, B7	
XADC_AD10_N	JX2, pin 43	Bank 35, M18	JX1, pin 83	Bank 35, B6	
XADC_AD11_P	JX2, pin 42	Bank 35, K19	JX1, pin 68	Bank 35, A5	
XADC_AD11_N	JX2, pin 44	Bank 35, J19	JX1, pin 70	Bank 35, A4	
XADC_AD12_P	JX2, pin 62	Bank 35, F19	JX1, pin 54	Bank 35, A2	
XADC_AD12_N	JX2, pin 64	Bank 35, F20	JX1, pin 56	Bank 35, A1	
XADC_AD13_P	JX2, pin 67	Bank 35, G19	JX1, pin 30	Bank 35, B2	
XADC_AD13_N	JX2, pin 69	Bank 35, G20	JX1, pin 32	Bank 35, B1	
XADC_AD14_P	JX2, pin 81	Bank 35, N15	JX1, pin 24	Bank 35, E4	
XADC_AD14_N	JX2, pin 83	Bank 35, N16	JX1, pin 26	Bank 35, E3	
XADC_AD15_P	JX2, pin 88	Bank 35, K16	JX1, pin 36	Bank 35, H1	
XADC_AD15_N	JX2, pin 90	Bank 35, J16	JX1, pin 38	Bank 35, G1	

Table 8 - XADC Pinout

The XADC internal reference voltage is selected (VREFP and VREFN shorted AGND).

VCCADC is the on-board 1.8V filtered through a ferrite bead, with 0.1uF and 0.47uF bypass caps.

If you plan to make use of the XADC on your Carrier, it is suggested that you place anti-aliasing filters close to JX1 and JX2. Be aware that the analog signal level is maximum 1Vpp. Please refer to Xilinx User Guide UG480.

When the XADC is not used, DXP/N, VP/N pins should be connected to GND. All the auxiliary analog inputs become digital I/O.

3.4 JTAG

The four dedicated JTAG signals are routed to the Micro Headers. A Carrier Card must utilize these JTAG signals in order to program and debug with the PicoZed as a JTAG programming header is not implemented on board.

When connecting additional JTAG devices in-line with the PicoZed, be sure that TCK and TMS are properly buffered. For example, if you wanted to Device XYZ into the JTAG chain, you would design your Carrier Card with a PC4-socket, with TMS and TCK buffers after the socket. The buffered TMS and TCK would route to both Device XYZ and the Micro Headers. Then the TDI/TDO connections would daisy-chain.

PC4 TDI → JX1.4

JX1.3 → Device XYZ TDI

Device XYZ TDO → PC4 TDO

PicoZed 7015/7030 Pin #	PicoZed 7010/7020 Pin #	Net Name	JX1 Pin #	JX1 Pin #	Net Name	PicoZed 7010/7020 Pin #	PicoZed 7015/7030 Pin #
Bank 0, H11	Bank 0, F9	JTAG_TCK	1	2	JTAG_TMS	Bank 0, J6	Bank 0, H10
Bank 0, G9	Bank 0, F6	JTAG_TDO	3	4	JTAG_TDI	Bank 0, G6	Bank 0, H9

Table 9 – JX1 Connections

3.5 Configuration

3.5.1 PUDC_B

This signal is the Pull-Up during Configuration signal. The net name on PicoZed 7010/7020 is JX1_LVDS_2_P. The net name on PicoZed 7015/7030 is JX2_LVDS_2_P. This signal has a resistor jumper option to pull-up to VCCO or pull-down to GND. The default is to pull it up via a 1K-ohm resistor, which disables the pull-ups during configuration.

This signal is routed to the Carrier. The default pull-up can be over-ridden with a stronger pull-down if pull-ups during configuration are desired.

Function	Signal Name	Micro Header Connection	Subsection	Zynq pin
PicoZed 7010/7020 PUDC_B	JX1_LVDS_2_P	JX1.17	PL (Bank 34)	U13
PicoZed 7015/7030 PUDC_B	JX2_LVDS_2_P	JX2.23	PL (Bank 34)	K7

Table 10 – PUDC_B

NOTE: Due to PUDC_B functionality, the JX1_LVDS_2_P/N pair on PicoZed 7010/7020 and the JX2_LVDS_2_P/N pair on PicoZed 7015/7030 are not suitable for use as a differential pair.

3.5.2 DONE

The DONE signal is pulled-up on PicoZed via a 240-ohm resistor. The DONE signal is routed to the Carrier and can be used as a control input to signal when the PL is DONE configuring. It is recommended that the Carrier implement an LED to signal DONE is active.

Function	Signal Name	Micro Header Connection	Subsection	PicoZed 7010/7020 Pin#	PicoZed 7015/7030 Pin#
PL Config DONE	FPGA_DONE	JX1.8	Bank 0	R11	T10

Table 11 – DONE

3.5.3 INIT_B

INIT_B is pulled-up via 4.7K-ohm on the PicoZed. If not needed as a controls signal on the Carrier, this can be left disconnected.

Function	Signal Name	Micro Header Connection	Subsection	PicoZed 7010/7020 Pin#	PicoZed 7015/7030 Pin#
PL Initialization	INIT#	JX2.9	Bank 0	R10	T8

Table 12 – INIT_B

3.5.4 PROGRAM_B

PROGRAM_B is pulled-up via 4.7K-ohm on the PicoZed. For Zynq applications, it is not typical that a system would use this signal. The PicoZed does not provide connection to PROGRAM_B to the Carrier.

Function	Signal Name	Micro Header Connection	Subsection	PicoZed 7010/7020 Pin#	PicoZed 7015/7030 Pin#
PL Program	PROGRAM#	none	Bank 0	L6	V10

Table 13 – PROGRAM_B

3.6 Ethernet MAC ID

From the factory, PicoZed does not store a MAC ID for the Ethernet. A designer could choose to implement this in the PicoZed Flash using their own MAC ID assignments.

A MAC ID could also be implemented using a dedicated MAC ID EEPROM.

4 POWER AND RESET

4.1 General Power Requirements

The Carrier card provides system power to the PicoZed as well as providing power directly to the PL I/O banks on the Zynq device. The voltages that must be provided to PicoZed are listed below:

- VIN (PicoZed requires 5V)
- VCCO_34 (Vcco for bank 34 on the Zynq device)
- VCCO_35 (Vcco for bank 35 on the Zynq device)
- VCCO_13 (Vcco for bank 13 on the Zynq device)
- USB_VBUS_OTG (USB 2.0 OTG 5V VBUS)
- MGTAVCC (Transceiver AVCC)
- MGTAVTT (Transceiver AVTT)

The total power budget is the power required for the carrier card (including the power supply inefficiencies) summed with the PicoZed power. This budget must include the anticipated current draw from the carrier card in “worst case” conditions, which is typically maximum I/O current sourcing, maximum data transfer rates across the high-speed interfaces and a high temperature environment.

4.2 Power Estimation of PL using XPE

Refer to the *PicoZed Hardware Users Guide* for a detailed breakdown of the power requirements on the PicoZed. Xilinx Power Estimator (XPE) should be used to generate worst case power estimations for selecting power devices for the I/O banks. The Xilinx Power Estimator (XPE) spreadsheet is available on Xilinx’ website that can help you get started with your own power estimation. You may download this file and add or modify your desired PL utilization to provide a worst-case estimation for your own VCCO supplies.

4.3 Proper Sequencing

All three Vccio banks that receive power from the Carrier can be independent or tied together depending on the specific design needs. To maintain proper start up sequencing, these Vccio supplies should be enabled by the VCCIO_EN signal tied to JX2 pin 10. Note that this enable signal is the PGOOD from the 1.8V supply on PicoZed. It is vital to ensure that the enable threshold for the regulators chosen is compatible with a 1.8V signal. If 1.8V is not high enough to reliably enable the device, an external circuit must be used to boost this voltage.

To enable power to the PicoZed, PWR_ENABLE must be pulled high. PWR_ENABLE is tied to JX1 pin 5 and is pulled up to VIN on the PicoZed. To shut down power to the PicoZed, PWR_ENABLE and VCCIO_EN should be pulled low. VCCIO_EN should be pulled low first to maintain proper shutdown sequencing.

Important Carrier Card Design Requirement Update: PG_MODULE

An important aspect of carrier card design is the final control of the master system reset. This signal on the Zynq-7000 is PS_POR_B which is tied to PG_MODULE signal on carrier card designs. The PG_MODULE signal is used to tell the SOM that all system power supplies are good and that the SOM can begin its boot process.

The open-drain PG_MODULE signal should be utilized in a custom carrier card design in order to meet the Power-On and Power-Off requirements documented in the Zynq-7000 datasheet and further documented in the Xilinx Zynq-7000 eFuse integrity Answer Record #65240. Failure to adhere to the guidelines presented in the data sheet and answer record could lead to damage to the PicoZed modules.

Xilinx Answer Record #65240: https://www.xilinx.com/support/answers/65240.html

On Power-On, PS_POR_B (PG_MODULE) needs to be asserted and held LOW for a minimum of 100uS after PS supply voltages reaches minimum levels. Also, care must be taken to ensure that the PS_POR_B (PG_MODULE) signal is not de-asserted HIGH during the Secure Lock Down Window described in the Xilinx Zynq-7000 datasheets and Xilinx Answer Record #63149.

Xilinx Answer Record #63149: https://www.xilinx.com/support/answers/63149.html

On Power-Off, PS_POR_B (PG_MODULE) needs to be asserted and held LOW prior to the PS power rails falling below acceptable thresholds identified in Xilinx Answer Record #65240 and maintain assertion through critical voltage levels as the PS power rails decay.

4.4 Power Handling of PL I/O Banks and MGT Supplies

For designing the power supplies for the PL I/O banks and the MGTs, Xilinx Power Estimator (XPE) should be used to generate worst case power estimations. The Xilinx Power Estimator (XPE) spreadsheet is available on Xilinx' website that can help you get started with your own power estimation. The power estimation results can then be used to budget for the power that will be needed by the PicoZed PL I/O banks and MGTs. This current should be added to the Carrier power estimate when designing your power system. The MGT Supplies are only necessary when planning a Carrier Card to support the PicoZed 7015/7030.

4.5 Proper Handling of VCCBAT

If battery backup is required, VCCBATT_0 must be tied to a 1.8V battery source through JX1 pin 7. Note that PicoZed by default ties VCCBATT_0 directly to 1.8V Vccaux. If using VCCBATT_0 as a battery backup, the 0-ohm resistor on VCCBATT_0 should be removed.

4.6 Proper Handling of XADC Power

The XADC interface operates from a 1.8V supply voltage with a 1.25V reference. Be sure to design your interface with these values in mind. Do not exceed 1.8V on the XADC inputs. Additional

information on designing with this interface please refer to Xilinx Application Note XAPP554 – XADC Layout Guidelines.

4.7 Need for Additional Bypass Capacitors

Bulk and decoupling/bypass capacitance is provided on PicoZed. Additional capacitance should be added to the user designed Carrier as recommended by the device manufacturers for each interface.

5 CARRIER BOARD PCB GUIDELINES

The majority of the PicoZed PL signals are routed to the JX connectors to facilitate user design flexibility and application development. Differential pairs and single ended signals are available for custom carrier card designs. All high-speed routing must follow the specific device manufacturers' recommendations for routing, impedance, trace length and layout guidelines. This is applicable to any high speed or low noise signals such as DDR RAM, Ethernet PHY, PMODs, XADC or USB extensions. The design engineer must be diligent in these areas to ensure intended data rates and performance.

The specific design requirements for a user application will ultimately drive the trace-length, trace spacing, signalling topology (differential or single ended) and impedance requirements. This variability cannot be accounted for and data throughput, signal integrity and overall performance will vary based on the design approach.

In all circumstances the design of a user Carrier board, the following documents should be consulted and adhered to: PicoZed User Guide, the PicoZed Carrier Card User Guide, and Xilinx's UG430. These documents provide critical insight into how the Avnet products were designed.

For general guidelines on how to achieve the performance of the Avnet Carrier Card designs, Avnet Engineering Services suggests the following design requirements be adhered to.

5.1 Suggested Requirements for Optimum Carrier Card Performance

5.1.1 Global Target Impedances (Unless otherwise noted)

- 100Ω differential impedance
- 50Ω single ended impedance
- USB: 45Ω single ended, 90Ω differential
- DDR: 40Ω single ended, 80Ω differential

5.1.2 Pair Matching and Length Tuning

- Use 4x spacing between pairs
- All signals should be routed using strip line or microstrip techniques.
- Length tune all signal pairs to within 10 mils within each pair (P to N)
- Length tune all signal pairs to within 250 mils pair-to-pair (depending on transfer rates)
- For high speed interfaces such as DDR memory Zynq internal package flight delays should be considered. Package flight delays for specific parts and packages can be obtained from the Vivado design tool. For package flight tolerances specific to DDR interfaces refer to Xilinx document UG586 Chapter 1.
- Both PicoZed 7010/7020 and PicoZed 7015/7030 length tune all the traces between the Zynq and the JX1/JX2 connectors to be equal. Each connector is treated as a separate interface. Please refer to Appendix A for the actual routed net lengths on the PicoZed SOMs.

5.1.3 Routing Considerations for Additional DDR Modules (PL via JX Connectors)

- LPDDR2, DDR2, and DDR3 should be selected based on MIG tool for a Zynq processor.

- Use the MIG tool pin-out information to route from the JX1 and JX2 connectors on the carrier board.
- Place memory IC (or ICs), pending topology and memory density, as close as possible to the JX1 and JX2 Micro headers for maximum data transfer rates and to minimize long trace lengths.
- Follow specific memory manufacturer's routing guidelines, trace impedance requirements and termination topology. The PicoZed uses a 40Ω ohm single ended and 80Ω differential trace impedance for the specific DDR3 with a 3X spacing between pairs, matching the memory manufacturer's recommendations.
- Routing, impedance and termination requirements will vary depending on the memory manufacture, the quantity of DDR ICs, the topology and the desired data throughput performance.
- As a rule, for high speed memory, Avnet adheres and recommends memory trace lengths to be less than 5000 mil in total length.
- All memory signals should be length tuned according to total propagation delay or "flight time" as recommended by Xilinx and the chosen memory manufacturer.
- Avnet recommends routing all memory signals on inner layers only, within 10mils of each other pair to pair, less than 50mils for a byte-lane associated to each DQS, and all memory signals to be within 100 mils of each other.

5.2 Routing 1Gb/s Ethernet and USB Through the PL

- Using Vivado IP integrator or ISE Core Generator, develop a MAC interface for the Zynq PL.
- All Giga-bit signals should be routed strip line using micro-vias between the appropriate layers.
- Use 4x spacing between pairs.
- Single pair (P and N) should be length tuned to within 25 mils of each other (P to N) at 100Ω differential impedance, with no more than two transitions (vias) for these signals.
- All Data, clock and control signals should be routed at 50Ω impedance and not exceed the PHY manufacturers' recommended length requirements.
- All interface signals should be routed to within 250mils of each other.
- If RGMII interface is used, the related VCCO must supply 1.8V or 2.5V to support fast slew.
- The Ethernet PHY must be compatible with VCCO levels used.

5.3 Routing MGTs on the Carrier Card

It is highly suggested that the guidelines described in the Xilinx document(s) "7-Series FPGAs GTP Transceivers" (UG482) Chapter 5 and "7-Series FPGAs GTX/GTH Transceivers User's Guide" (UG476), Chapter 5 be reviewed prior to designing and routing GTP/GTX circuits.

Here are some general guidelines that are followed on the SOMs' GTP/GTX routing:

- All gigabit transceiver signals shall be routed Strip line.
- All gigabit transceiver TX, RX and related clock differential signals shall be routed differential at 100 ohms differential impedance.
- Use 4x spacing between pairs.
- All gigabit transceiver signals shall be length tuned to within 100 mils shortest pair to longest pair.
- All gigabit transceiver signals within a single pair (P and N) shall be length tuned to within 25 mils of each other (P to N).
- No more than two transitions (vias) are allowed for these signals.

5.4 Routing AMS/XADC Signals

The XADC header provides analog connectivity for analog reference designs, including AMS daughter cards such as Xilinx's AMS Evaluation Card. Both analog and digital IO can be easily supported for a plug-in card.

The pin out has been chosen to provide tightly coupled differential analog pairs on the ribbon cable and to also provide AGND isolation between channels.

To minimize signal aliasing, the following filters should be used for the XADC inputs:

– VP/VN
– VAUX0P/VAUX0N
– VAUX8P/VAUX8N

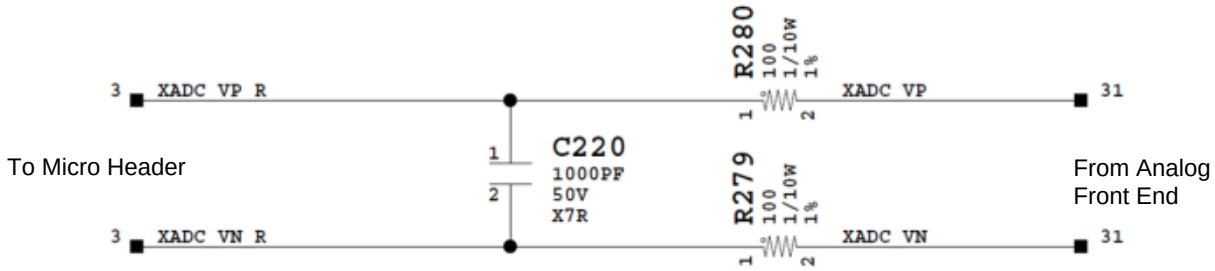

Figure 3 – Anti-Aliasing Filters for XADC Inputs

– The 100Ω filtering resistors and 1000pF capacitor should be placed within 500 mils of the associated FPGA pins.
– Use 4X spacing on the traces.
– Single ended impedance is 50Ω and differential is 100Ω.
– All paired signals should be routed to within 50mils of each other.
– All interface signals should be routed to within 100mils of each other.
– Anti-aliasing filters should be placed as close to the Micro Header as possible.

5.4.1 XADC alternate GPIO function

If the XADC function is not desired, the port can be used for additional GPIO expansion as necessary. However, care must be taken to ensure the appropriate logic voltage levels are observed when using these signals. VCCIO_35 sets the acceptable voltage levels for the XADC_GIOx signals. For AD*_P/N signals must be limited to 1.8V logic levels.

To facilitate a high-performance interface, the suggested layout guidelines should be followed.

6 PICOZED CONNECTORS

Each PicoZed SOM features three 100-pin Micro Headers (JX1, JX2, and JX3) that allow for connection to customer Carrier cards. The Micro Headers route I/O signals and power between PicoZed and a custom carrier card.

6.1 Connector Description and Selection

The Micro Headers used on PicoZed are FCI 0.8mm BergStak® 100-position Dual Row, BTB Vertical Receptacles (61082-101400LF). These receptacles mate with any of the FCI 0.8mm BergStak® 100-position Dual Row BTB Vertical Plugs (61083-10x400LF) to provide variable stack heights of 5mm, 6mm, 7mm or 8mm. See table below for additional detail.

Custom PicoZed modules can be ordered with specific receptacles while custom carrier cards can be populated with specific plugs allowing system designers to choose optimal stacking heights (5mm – 16mm in 1mm increments) for their application. See table below for additional detail.

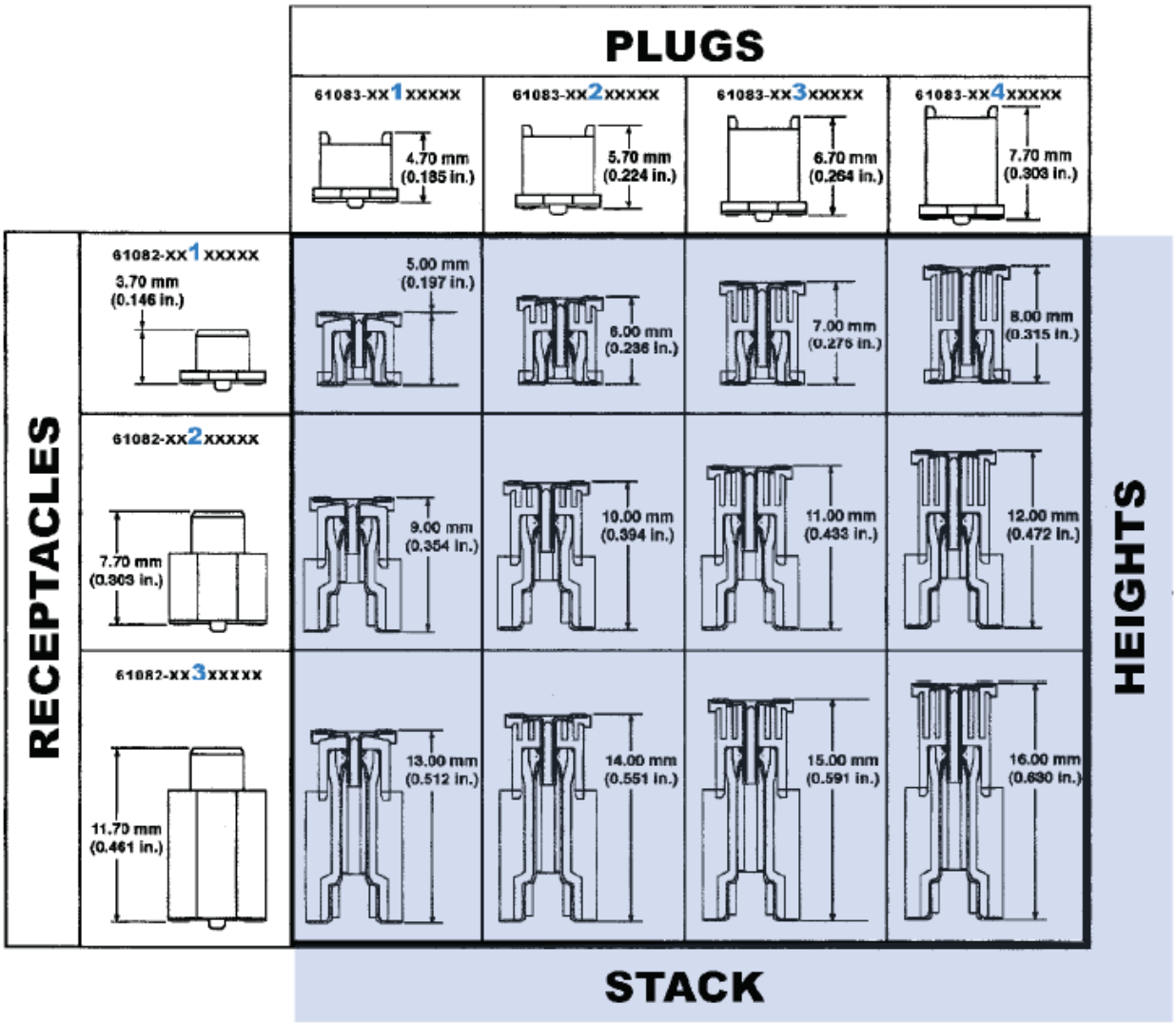

Figure 4 - FCI BergStak Mating Options

Additionally, each Micro Header pin can carry 500mA of current and can support data rates up to 8Gbps. More information on FCI's BergStak connectors can be found at www.fciconnect.com/bergstak.

Avnet will keep the following FCI part numbers in Table 12 in stock to assist prototype build of custom carrier cards. See www.em.avnet.com/avnetsomconnectors for more details.

61082-10140xLF*	61083-10140xLF*
61082-10240xLF*	61083-10240xLF*
61082-10340xLF*	61083-10340xLF*
	61083-10440xLF*

Table 14 - FCI BERGSTAK Connectors

* "x" can be 0, 2 or 9 depending on packaging.

Avnet will keep the following FCI part numbers in Table 12 in stock to assist prototype build of custom carrier cards. See www.em.avnet.com/avnetsomconnectors for more details.

6.1.1 Connector Shock and Vibration Specifications

Shock:

EIA-364-27, Test Condition A

Accelerated velocity ----- 490 m/s2 (50G).

Waveform ---------- half-sine shock pulse.

Duration ---------- 11 mSec.

Velocity change ---------- 11.3 feet per second

Number of cycles --------- 18

Vibration:

EIA-364-28 Test Condition V, Letter D

Frequency ---------- 50 to 2000 Hz

Power spectral Density -------- 0.1 g2/Hz

Overall rms g ---------- 11.95

Duration ---------- 1 1/2 hours in each of three mutually perpendicular axes (4 1/2 hours total).

6.2 Micro Header Pinouts

PicoZed 7015/7030 Pin #	PicoZed 7010/7020 Pin #	Net Name	JX1 Pin #	JX1 Pin #	Net Name	PicoZed 7010/7020 Pin #	PicoZed 7015/7030 Pin #
0 – H11	0 - F9	JTAG_TCK	1	2	JTAG_TMS	0 - J6	0 – H10
0 – G9	0 - F6	JTAG_TDO	3	4	JTAG_TDI	0 - G6	0 – H9
N/A	N/A	PWR_ENABLE	5	6	CARRIER_SRST#	501 - B10	501 – C14
0 – G14	0 - F11	FPGA_VBATT	7	8	FPGA_DONE	0 - R11	0 – T10
35 – H6	34 - R19	JX1_SE_0	9	10	JX1_SE_1	34 - T19	35 – H5
35 – H4	34 - T11	JX1_LVDS_0_P	11	12	JX1_LVDS_1_P	34 - T12	35 – F5
35 – H3	34 - T10	JX1_LVDS_0_N	13	14	JX1_LVDS_1_N	34 - U12	35 – E5
N/A	N/A	**GND**	15	16	**GND**	N/A	N/A
35 – G3	34 - U13	JX1_LVDS_2_P	17	18	JX1_LVDS_3_P	34 - V12	35 – F2
35 – G2	34 - V13	JX1_LVDS_2_N	19	20	JX1_LVDS_3_N	34 - W13	35 – F1
N/A	N/A	**GND**	21	22	**GND**	N/A	N/A
35 – G4	34 - T14	JX1_LVDS_4_P	23	24	JX1_LVDS_5_P	34 - P14	35 – E4
35 – F4	34 - T15	JX1_LVDS_4_N	25	26	JX1_LVDS_5_N	34 - R14	35 – E3
N/A	N/A	**GND**	27	28	**GND**	N/A	N/A
35 – G6	34 - Y16	JX1_LVDS_6_P	29	30	JX1_LVDS_7_P	34 - W14	35 – B2
35 – F6	34 - Y17	JX1_LVDS_6_N	31	32	JX1_LVDS_7_N	34 - Y14	35 – B1
N/A	N/A	**GND**	33	34	**GND**	N/A	N/A
35 – E8	34 - T16	JX1_LVDS_8_P	35	36	JX1_LVDS_9_P	34 - V15	35 – H1
35 – D8	34 - U17	JX1_LVDS_8_N	37	38	JX1_LVDS_9_N	34 - W15	35 – G1
N/A	N/A	**GND**	39	40	**GND**	N/A	N/A
35 – C6	34 - U14	JX1_LVDS_10_P	41	42	JX1_LVDS_11_P	34 - U18	35 – D5
35 – C5	34 - U15	JX1_LVDS_10_N	43	44	JX1_LVDS_11_N	34 - U19	35 – C4
N/A	N/A	**GND**	45	46	**GND**	N/A	N/A
35 – B4	34 - N18	JX1_LVDS_12_P	47	48	JX1_LVDS_13_P	34 - N20	35 – D3
35 – B3	34 - P19	JX1_LVDS_12_N	49	50	JX1_LVDS_13_N	34 - P20	35 – C3
N/A	N/A	**GND**	51	52	**GND**	N/A	N/A
35 – D1	34 - T20	JX1_LVDS_14_P	53	54	JX1_LVDS_15_P	34 - V20	35 – A2
35 – C1	34 - U20	JX1_LVDS_14_N	55	56	JX1_LVDS_15_N	34 - W20	35 – A1
N/A	N/A	**VIN_HDR**	57	58	**VIN_HDR**	N/A	N/A
N/A	N/A	**VIN_HDR**	59	60	**VIN_HDR**	N/A	N/A
35 – E2	34 - Y18	JX1_LVDS_16_P	61	62	JX1_LVDS_17_P	34 - V16	35 – D7
35 – D2	34 - Y19	JX1_LVDS_16_N	63	64	JX1_LVDS_17_N	34 - W16	35 – D6
N/A	N/A	**GND**	65	66	**GND**	N/A	N/A
35 – F7	34 - R16	JX1_LVDS_18_P	67	68	JX1_LVDS_19_P	34 - T17	35 – A5
35 – E7	34 - R17	JX1_LVDS_18_N	69	70	JX1_LVDS_19_N	34 - R18	35 – A4
N/A	N/A	**GND**	71	72	**GND**	N/A	N/A
35 – G8	34 - V17	JX1_LVDS_20_P	73	74	JX1_LVDS_21_P	34 - W18	35 – A7
35 – G7	34 - V18	JX1_LVDS_20_N	75	76	JX1_LVDS_21_N	34 - W19	35 – A6

PicoZed 7015/7030 Pin #	PicoZed 7010/7020 Pin #	Net Name	JX1 Pin #	JX1 Pin #	Net Name	PicoZed 7010/7020 Pin #	PicoZed 7015/7030 Pin #
N/A	N/A	**GND**	77	78	**VCCO_34**	N/A	N/A
N/A	N/A	**VCCO_34**	79	80	**VCCO_34**	N/A	N/A
35 – B7	34 - N17	JX1_LVDS_22_P	81	82	JX1_LVDS_23_P	34 - P15	35 – C8
35 – B6	34 - P18	JX1_LVDS_22_N	83	84	JX1_LVDS_23_N	34 - P16	35 – B8
N/A	N/A	**GND**	85	86	**GND**	N/A	N/A
13 – AA14	13 - U7	BANK13_LVDS_0_P	87	88	BANK13_LVDS_1_P	13 - T9	13 – Y14
13 – AA15	13 - V7	BANK13_LVDS_0_N	89	90	BANK13_LVDS_1_N	13 - U10	13 – Y15
13 – U19	13 - V8	BANK13_LVDS_2_P	91	92	BANK13_LVDS_3_P	13 - T5	13 – V18
13 – V19	13 - W8	BANK13_LVDS_2_N	93	94	BANK13_LVDS_3_N	13 - U5	13 – W18
N/A	N/A	**GND**	95	96	**GND**	N/A	N/A
0 – L12	0 - K9	VP_0_P	97	98	DXP_0_P	0 - M9	0 – N12
0 – M11	0 - L10	VN_0_N	99	100	DXN_0_N	0 - M10	0 – N11

Table 15 – JX1 Connections

PicoZed 7015/7030 Pin #	PicoZed 7010/7020 Pin #	PicoZed Net	JX2 Pin #	JX2 Pin #	PicoZed Net	PicoZed 7010/7020 Pin #	PicoZed 7015/7030 Pin #
500 - G16	500 - E8	MIO10	1	2	MIO13	500 - E9	500 – A17
500 - B17	500 - C6	MIO14	3	4	MIO15	500 - D9	500 – E17
500 - C18	500 - E6	MIO12	5	6	MIO11	500 - B5	500 – B19
500 - G17	500 - C5	MIO0	7	8	MIO9	500 - C8	500 – C19
0 – T8	0 - R10	INIT#	9	10	VCCIO_EN	N/A	N/A
500 – B18	500 - C7	PG_MODULE	11	12	**VIN_HDR**	N/A	N/A
34 – H8	35 - G14	JX2_SE_0	13	14	JX2_SE_1	35 - J15	34 – R8
N/A	N/A	**GND**	15	16	**GND**	N/A	N/A
34 – M4	35 - C20	JX2_LVDS_0_P	17	18	JX2_LVDS_1_P	35 - B19	34 – J2
34 – M3	35 - B20	JX2_LVDS_0_N	19	20	JX2_LVDS_1_N	35 - A20	34 – J1
N/A	N/A	**GND**	21	22	**GND**	N/A	N/A
34 – K7	35 - E17	JX2_LVDS_2_P	23	24	JX2_LVDS_3_P	35 - D19	34 – J3
34 – L7	35 - D18	JX2_LVDS_2_N	25	26	JX2_LVDS_3_N	35 - D20	34 – K2
N/A	N/A	**GND**	27	28	**GND**	N/A	N/A
34 – P7	35 - E18	JX2_LVDS_4_P	29	30	JX2_LVDS_5_P	35 - F16	34 – L2
34 – R7	35 - E19	JX2_LVDS_4_N	31	32	JX2_LVDS_5_N	35 - F17	34 – L1
N/A	N/A	**GND**	33	34	**GND**	N/A	N/A
34 – N4	35 - L19	JX2_LVDS_6_P	35	36	JX2_LVDS_7_P	35 - M19	34 – P3
34 – N3	35 - L20	JX2_LVDS_6_N	37	38	JX2_LVDS_7_N	35 - M20	34 – P2
N/A	N/A	**GND**	39	40	**GND**	N/A	N/A
34 – M2	35 - M17	JX2_LVDS_8_P	41	42	JX2_LVDS_9_P	35 - K19	34 – N1
34 – M1	35 - M18	JX2_LVDS_8_N	43	44	JX2_LVDS_9_N	35 - J19	34 – P1
N/A	N/A	**GND**	45	46	**GND**	N/A	N/A

PicoZed 7015/7030 Pin #	PicoZed 7010/7020 Pin #	PicoZed Net	JX2 Pin #	JX2 Pin #	PicoZed Net	PicoZed 7010/7020 Pin #	PicoZed 7015/7030 Pin #
34 – K4	35 - L16	JX2_LVDS_10_P	47	48	JX2_LVDS_11_P	35 - K17	34 – L5
34 – K3	35 - L17	JX2_LVDS_10_N	49	50	JX2_LVDS_11_N	35 - K18	34 – L4
N/A	N/A	**GND**	51	52	**GND**	N/A	N/A
34 – T2	35 - H16	JX2_LVDS_12_P	53	54	JX2_LVDS_13_P	35 - J18	34 – U2
34 – T1	35 - H17	JX2_LVDS_12_N	55	56	JX2_LVDS_13_N	35 - H18	34 – U1
N/A	N/A	**VIN_HDR**	57	58	**VIN_HDR**	N/A	N/A
N/A	N/A	**VIN_HDR**	59	60	**VIN_HDR**	N/A	N/A
34 – R3	35 - G17	JX2_LVDS_14_P	61	62	JX2_LVDS_15_P	35 - F19	34 – L6
34 – R2	35 - G18	JX2_LVDS_14_N	63	64	JX2_LVDS_15_N	35 - F20	34 – M6
N/A	N/A	**GND**	65	66	**GND**	N/A	N/A
34 – J5	35 - G19	JX2_LVDS_16_P	67	68	JX2_LVDS_17_P	35 - J20	34 – R5
34 – K5	35 - G20	JX2_LVDS_16_N	69	70	JX2_LVDS_17_N	35 - H20	34 – R4
N/A	N/A	**GND**	71	72	**GND**	N/A	N/A
34 – J7	35 - K14	JX2_LVDS_18_P	73	74	JX2_LVDS_19_P	35 - H15	34 – P6
34 – J6	35 - J14	JX2_LVDS_18_N	75	76	JX2_LVDS_19_N	35 - G15	34 – P5
N/A	N/A	**GND**	77	78	**VCCO_35**	N/A	N/A
N/A	N/A	**VCCO_35**	79	80	**VCCO_35**	N/A	N/A
34 – J8	35 - N15	JX2_LVDS_20_P	81	82	JX2_LVDS_21_P	35 - L14	34 – N6
34 – K8	35 - N16	JX2_LVDS_20_N	83	84	JX2_LVDS_21_N	35 - L15	34 – N5
N/A	N/A	**GND**	85	86	**GND**	N/A	N/A
34 – M8	35 - M14	JX2_LVDS_22_P	87	88	JX2_LVDS_23_P	35 - K16	34 – N8
34 – M7	35 - M15	JX2_LVDS_22_N	89	90	JX2_LVDS_23_N	35 - J16	34 – P8
N/A	N/A	**GND**	91	92	**GND**	N/A	N/A
13 – AB21	13 - Y12	BANK13_LVDS_4_P	93	94	BANK13_LVDS_5_P	13 - V11	13 – AB18
13 – AB22	13 - Y13	BANK13_LVDS_4_N	95	96	BANK13_LVDS_5_N	13 - V10	13 – AB19
13 – AA19	13 - V6	BANK13_LVDS_6_P	97	98	**VCCO_13**	N/A	N/A
13 – AA20	13 - W6	BANK13_LVDS_6_N	99	100	BANK13_SE_0	13 - V5	13 – T16

Table 16 – JX2 Connections

PicoZed 7015/7030 Pin #	PicoZed 7010/7020 Pin #	PicoZed Net	JX3 Pin #	JX3 Pin #	PicoZed Net	PicoZed 7010/7020 Pin #	PicoZed 7015/7030 Pin #
112 – U9	N/A	MGTREFCLK0_P	1	2	MGTREFCLK1_P	N/A	112 – U5
112 – V9	N/A	MGTREFCLK0_N	3	4	MGTREFCLK1_N	N/A	112 – V5
N/A	N/A	**MGTAVCC**	5	6	**GND**	N/A	N/A
N/A	N/A	**MGTAVCC**	7	8	MGTRX0_P	N/A	112 – AA7
N/A	N/A	**MGTAVCC**	9	10	MGTRX0_N	N/A	112 – AB7
N/A	N/A	**MGTAVCC**	11	12	**GND**	N/A	N/A
112 – AA3	N/A	MGTTX0_P	13	14	MGTRX1_P	N/A	112 – W8
112 – AB3	N/A	MGTTX0_N	15	16	MGTRX1_N	N/A	112 – Y8

PicoZed 7015/7030 Pin #	PicoZed 7010/7020 Pin #	PicoZed Net	JX3 Pin #	JX3 Pin #	PicoZed Net	PicoZed 7010/7020 Pin #	PicoZed 7015/7030 Pin #
N/A	N/A	**GND**	17	18	**GND**	N/A	N/A
112 – W4	N/A	MGTTX1_P	19	20	MGTRX2_P	N/A	112 – AA9
112 – Y4	N/A	MGTTX1_N	21	22	MGTRX2_N	N/A	112 – AB9
N/A	N/A	**GND**	23	24	**GND**	N/A	N/A
112 –	N/A	MGTTX2_P	25	26	MGTRX3_P	N/A	112 – W6
112 –	N/A	MGTTX2_N	27	28	MGTRX3_N	N/A	112 – Y6
N/A	N/A	**GND**	29	30	**MGTAVTT**	N/A	N/A
112 – W2	N/A	MGTTX3_P	31	32	**MGTAVTT**	N/A	N/A
112 – Y2	N/A	MGTTX3_N	33	34	PS_MIO41	501 – C17	501 – C15
N/A	N/A	**GND**	35	36	PS_MIO43	501 – A9	501 – B12
501 –	501 – D14	PS_MIO42	37	38	PS_MIO45	501 – B15	501 – B14
501 – E10	501 – F13	PS_MIO44	39	40	PS_MIO47	501 - B14	501 - B13
501 –	501 – D16	PS_MIO46	41	42	PS_MIO48	501 – B12	501 – D12
501 – E9	501 – D14	PS_MIO40	43	44	PS_MIO49	501 – C12	501 – C9
N/A	N/A	**VCCO_13**	45	46	**VCCO_13**	N/A	N/A
N/A	N/A	ETH_PHY_LED0	47	48	ETH_PHY_LED1	N/A	N/A
N/A	N/A	**GND**	49	50	**GND**	N/A	N/A
N/A	N/A	ETH_MD1_P	51	52	ETH_MD2_P	N/A	N/A
N/A	N/A	ETH_MD1_N	53	54	ETH_MD2_N	N/A	N/A
N/A	N/A	**GND**	55	56	**GND**	N/A	N/A
N/A	N/A	ETH_MD3_P	57	58	ETH_MD4_P	N/A	N/A
N/A	N/A	ETH_MD3_N	59	60	ETH_MD4_N	N/A	N/A
N/A	N/A	**GND**	61	62	**GND**	N/A	N/A
N/A	N/A	USB_OTG_ID	63	64	PS_MIO51	501 – B9	501 – C13
N/A	N/A	**GND**	65	66	PS_MIO50	501 – B13	501 – D10
N/A	N/A	USB_OTG_P	67	68	**USB_VBUS_OTG**	N/A	N/A
N/A	N/A	USB_OTG_N	69	70	USB_OTG_CPEN	N/A	N/A
N/A	N/A	**GND**	71	72	**GND**	N/A	N/A
13-Y18	13-Y7	BANK13_LVDS_7_P	73	74	BANK13_LVDS_8_P	13-Y9	13-AA16
13-Y19	13-Y6	BANK13_LVDS_7_N	75	76	BANK13_LVDS_8_N	13-Y8	13-AA17
N/A	N/A	**GND**	77	78	**GND**	N/A	N/A
13-AA11	13-W10	BANK13_LVDS_9_P	79	80	BANK13_LVDS_10_P	13-U9	13-Y12
13-AB11	13-W9	BANK13_LVDS_9_N	81	82	BANK13_LVDS_10_N	13-U8	13-Y13
N/A	N/A	**GND**	83	84	**GND**	N/A	N/A
13-V11	13-W11	BANK13_LVDS_11_P	85	86	BANK13_LVDS_12_P	N/A	13-V13
13-W11	13-Y11	BANK13_LVDS_11_N	87	88	BANK13_LVDS_12_N	N/A	13-V14
N/A	N/A	**GND**	89	90	**GND**	N/A	N/A
13-W12	N/A	BANK13_LVDS_13_P	91	92	BANK13_LVDS_14_P	N/A	13-R17
13-W13	N/A	BANK13_LVDS_13_N	93	94	BANK13_LVDS_14_N	N/A	13-T17
N/A	N/A	**GND**	95	96	**GND**	N/A	N/A
13-V15	N/A	BANK13_LVDS_15_P	97	98	BANK13_LVDS_16_P	N/A	13-V16
13-W15	N/A	BANK13_LVDS_15_N	99	100	BANK13_LVDS_16_N	N/A	13-W16

Table 17 – JX3 Connections

6.3 Connector Land and Alignment

It is extremely important that Carrier card designers ensure that the Micro Headers have the proper land patterns and that the connectors are aligned correctly. The land pattern is featured in the *Mechanical Considerations* section of this document. Connector alignment is ensured if the alignment pin holes in the PCB connector pattern are in the correct positions and if the holes are drilled to the proper size and tolerance by the PCB fabricator.

If a customer would like a template for laying out their custom board, Avnet-qualified customers can request the source through their local Avnet FAE.

7 MECHANICAL CONSIDERATIONS

PicoZed measures 2.25” x 4.00” (57.15 mm x 101.6 mm). Custom carrier cards would have to be large enough to support the dimension shown below. Figure 3 is referenced as the footprint on a customer carrier card top view.

PicoZed comes with four grounded and plated mounting holes in each of the four corners of the board. The diameter of each mounting hole is 0.125” (3.175mm). Assuming the standard 5mm board-to-board spacing between PicoZed and the carrier card, spacers (i.e. Harwin R30-3000502 with M3x5mm metal screw and M3 x 1mm metal nut) can be added to mechanically strengthen the attachment of PicoZed to the Carrier card. Metal standoffs provide an additional heat dissipation path for any possible heat build-up on the ground layer.

PicoZed 7010/7020 comes with two un-plated mounting holes near the Zynq device. The diameter of each mounting hole is 0.093” (2.362mm). These can be used to secure thermal relief elements like fans or a heat spreader. M2 diameter screws, spacers and nuts can be used on the mounting holes. See the following figures for more detail. PicoZed 7015/7030 does not have mounting holes near the Zynq device and would require a thermal adhesive to mount thermal relief elements.

7.1 Form Factor

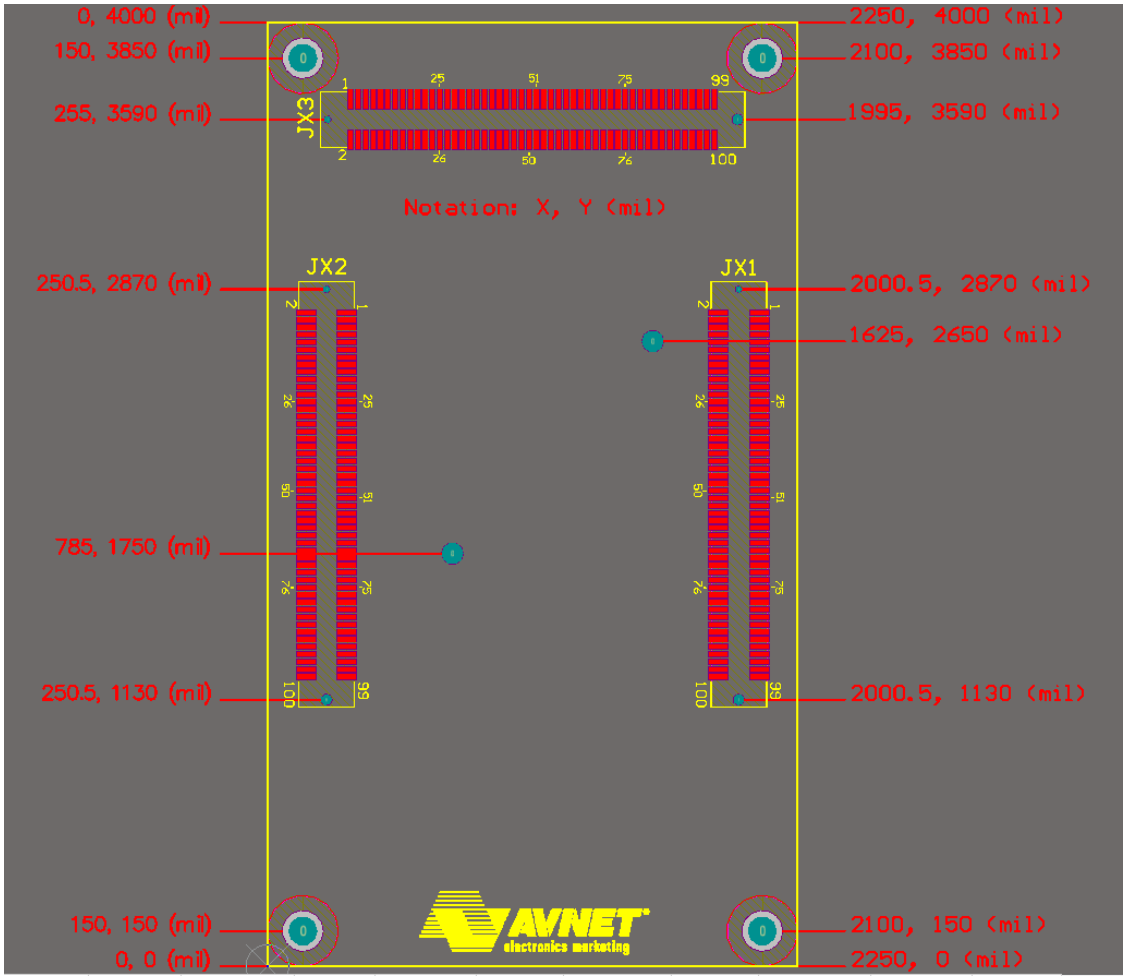

Figure 5 - Mechanical Layout of PicoZed Carrier Card
Micro Header Connectors and Mounting Holes

7.2 Thermal Considerations

Thermal relief is an important design factor in each PicoZed-based system design. A detailed thermal analysis should be performed for each specific application of PicoZed and a customer designed carrier card. In support of this, PicoZed has many design features to help dissipate heat from a system level.

The first feature is the fan header. This header provides two ground connections and one connection to the V_{IN} voltage (3.3V or 5V Selectable). This allows a fan to be added to any PicoZed-based system. For maximum heat dissipation, any system airflow should pass parallel to the surface of the Zynq.

Related to the fan header are two mounting holes located next to the Zynq 7010/7020 device. This allows for a fan, heat sink or fan and heatsink combination to be added to the PicoZed 7010/7020. System engineers may decide to mount a heat spreader here in extreme situations. The Zynq

7015/7030 does not contain these mounting holes and any thermal solution would be required to adhere to the Zynq device.

Lastly, the four mounting holes on the four corners of PicoZed are electrically connected to a heavier ground plane. With the additional mounting holes added to PicoZed, system designers may choose to attach PicoZed to their customer carrier card using metal standoff providing another path for heat dissipation.

In some instances, adding a passive heat sink with appropriate thermal bonding material to the Zynq may be sufficient to dissipate any extra heat. The Zynq package used on PicoZed 7010/7020 measures 17mm by 17mm or 19mmx19mm for the PicoZed 7015/7030. For maximum heat transfer, passive heat sinks attached to the Zynq device should cover the entire area. Suggested devices below serve as a starting point for basic heat dissipation needs.

Manufacturer	Part Number	L x W X H (mm)	Thermal Resistance (°C/W)
AavidThermalloy	10-53190245-C2-HSG	19 x 19 x 24.5	6.5
AavidThermalloy	10-53190145-C1-R0G	19 x 19 x 14.5	12
AavidThermalloy	10-53190095-C1-R0G	19 x 19 x 9.5	22
CTS	APF19-19-06CB	19 x 19 x 6.3	7.1*
CTS	APF19-19-10CB	19 x 19 x 9.5	5.3*
CTS	APF19-19-13CB	19 x 19 x 12.7	4.0*

Table 18 – PicoZed Heatsink Options

*@200LFM

8 GETTING HELP AND SUPPORT

If additional support is required, Avnet has many avenues to search depending on your needs.

For general question regarding PicoZed and PicoZed Carrier Card or accessories, please visit our website at http://www.picozed.org. Here you can find documentation, technical specifications, videos and tutorials, reference designs and other support.

Detailed questions regarding PicoZed hardware design, software application development, using Xilinx tools, training and other topics can be posted on the PicoZed Support Forums at http://www.picozed.org/forums/zed-english-forum. Avnet's technical support team monitors the forum during normal business hours.

Those interested in customer-specific options on PicoZed can send inquiries to customize@avnet.com.

Avnet's Embedded Software Store addresses the need for software in the embedded architecture development space. The goal of this store is to provide a market place for engineers to easily purchase software components for given hardware architectures. Support for the Xilinx Zynq AP SoC includes Board Support Packages, Middleware, Operating Systems and various tools

The Embedded Software and Services Group (ESSG) of Avnet Embedded offer a suite of software services that optimize the entire embedded software stack. Flexible end-to-end solutions enhance operating systems, middleware, application layers and cloud solutions based on the embedded system needs. More information can be found at http://www.em.avnet.com/en-us/services/Pages/Software-Solutions.aspx.

9 APPENDIX A – SOM JX1/JX2 Routed Net Lengths

JX1			
Signal Name	Routed Length (mm)	Signal Name	Routed Length (mm)
JX1_LVDS_0_N	53.34586	JX1_LVDS_12_N	53.35833
JX1_LVDS_0_P	53.36018	JX1_LVDS_12_P	53.34178
JX1_LVDS_1_N	53.35983	JX1_LVDS_13_N	53.36333
JX1_LVDS_1_P	53.35398	JX1_LVDS_13_P	53.35989
JX1_LVDS_2_N	53.35609	JX1_LVDS_14_N	53.34808
JX1_LVDS_2_P	70.2251	JX1_LVDS_14_P	53.3403
JX1_LVDS_3_N	53.36077	JX1_LVDS_15_N	53.35542
JX1_LVDS_3_P	53.36214	JX1_LVDS_15_P	53.35019
JX1_LVDS_4_N	53.35765	JX1_LVDS_16_N	53.36307
JX1_LVDS_4_P	53.35587	JX1_LVDS_16_P	53.34049
JX1_LVDS_5_N	53.35846	JX1_LVDS_17_N	53.34221
JX1_LVDS_5_P	53.36009	JX1_LVDS_17_P	53.35386
JX1_LVDS_6_N	53.36413	JX1_LVDS_18_N	53.35733
JX1_LVDS_6_P	53.36256	JX1_LVDS_18_P	53.36006
JX1_LVDS_7_N	53.3534	JX1_LVDS_19_N	53.35973
JX1_LVDS_7_P	53.36214	JX1_LVDS_19_P	53.36263
JX1_LVDS_8_N	53.34164	JX1_LVDS_20_N	53.34091
JX1_LVDS_8_P	53.34088	JX1_LVDS_20_P	53.34478
JX1_LVDS_9_N	53.3433	JX1_LVDS_21_N	53.36104
JX1_LVDS_9_P	53.34174	JX1_LVDS_21_P	53.36226
JX1_LVDS_10_N	53.35965	JX1_LVDS_22_N	53.34404
JX1_LVDS_10_P	53.34218	JX1_LVDS_22_P	53.34395
JX1_LVDS_11_N	53.35778	JX1_LVDS_23_N	53.35964
JX1_LVDS_11_P	53.33845	JX1_LVDS_23_P	53.34965

JX2			
Signal Name	Routed Length (mm)	Signal Name	Routed Length (mm)
JX2_LVDS_0_N	47.26055	JX2_LVDS_12_N	47.24897
JX2_LVDS_0_P	47.25534	JX2_LVDS_12_P	47.25238
JX2_LVDS_1_N	47.25124	JX2_LVDS_13_N	47.25514
JX2_LVDS_1_P	47.25089	JX2_LVDS_13_P	47.25181
JX2_LVDS_2_N	47.25042	JX2_LVDS_14_N	47.24709
JX2_LVDS_2_P	47.25141	JX2_LVDS_14_P	47.24586
JX2_LVDS_3_N	47.25283	JX2_LVDS_15_N	47.24932
JX2_LVDS_3_P	47.25402	JX2_LVDS_15_P	47.26317
JX2_LVDS_4_N	47.24588	JX2_LVDS_16_N	47.25663
JX2_LVDS_4_P	47.24599	JX2_LVDS_16_P	47.24868
JX2_LVDS_5_N	47.2457	JX2_LVDS_17_N	47.26515
JX2_LVDS_5_P	47.26181	JX2_LVDS_17_P	47.26486
JX2_LVDS_6_N	47.25232	JX2_LVDS_18_N	47.25741

JX2			
Signal Name	Routed Length (mm)	Signal Name	Routed Length (mm)
JX2_LVDS_6_P	47.24677	JX2_LVDS_18_P	47.25201
JX2_LVDS_7_N	47.2533	JX2_LVDS_19_N	47.25326
JX2_LVDS_7_P	47.25958	JX2_LVDS_19_P	47.24875
JX2_LVDS_8_N	47.26117	JX2_LVDS_20_N	47.26709
JX2_LVDS_8_P	47.25046	JX2_LVDS_20_P	47.26462
JX2_LVDS_9_N	47.25023	JX2_LVDS_21_N	47.25029
JX2_LVDS_9_P	47.26234	JX2_LVDS_21_P	47.25291
JX2_LVDS_10_N	47.24518	JX2_LVDS_22_N	47.24486
JX2_LVDS_10_P	47.24713	JX2_LVDS_22_P	47.25044
JX2_LVDS_11_N	47.26117	JX2_LVDS_23_N	47.24732
JX2_LVDS_11_P	47.24948	JX2_LVDS_23_P	47.24773

Table 19 – PicoZed 7010/7020 JX1/JX2 Net Lengths

JX1			
Signal Name	Routed Length (mm)	Signal Name	Routed Length (mm)
JX1_LVDS_0_N	44.50527	JX1_LVDS_12_N	44.50403
JX1_LVDS_0_P	44.50506	JX1_LVDS_12_P	44.5038
JX1_LVDS_1_N	44.50476	JX1_LVDS_13_N	44.50433
JX1_LVDS_1_P	44.5043	JX1_LVDS_13_P	44.50356
JX1_LVDS_2_N	44.50538	JX1_LVDS_14_N	44.50302
JX1_LVDS_2_P	44.5043	JX1_LVDS_14_P	44.50476
JX1_LVDS_3_N	44.50519	JX1_LVDS_15_N	44.50491
JX1_LVDS_3_P	44.50452	JX1_LVDS_15_P	44.50492
JX1_LVDS_4_N	44.50484	JX1_LVDS_16_N	44.50378
JX1_LVDS_4_P	44.50542	JX1_LVDS_16_P	44.50424
JX1_LVDS_5_N	44.50387	JX1_LVDS_17_N	44.50436
JX1_LVDS_5_P	44.50435	JX1_LVDS_17_P	44.50286
JX1_LVDS_6_N	44.50351	JX1_LVDS_18_N	44.50441
JX1_LVDS_6_P	44.50555	JX1_LVDS_18_P	44.50395
JX1_LVDS_7_N	44.50371	JX1_LVDS_19_N	44.50472
JX1_LVDS_7_P	44.50378	JX1_LVDS_19_P	44.50431
JX1_LVDS_8_N	44.5047	JX1_LVDS_20_N	44.50348
JX1_LVDS_8_P	44.50549	JX1_LVDS_20_P	44.50347
JX1_LVDS_9_N	44.50485	JX1_LVDS_21_N	44.50558
JX1_LVDS_9_P	44.50547	JX1_LVDS_21_P	44.50407
JX1_LVDS_10_N	44.52918	JX1_LVDS_22_N	44.50468
JX1_LVDS_10_P	44.50329	JX1_LVDS_22_P	44.50432
JX1_LVDS_10_P	44.50329	JX1_LVDS_22_P	44.50432
JX1_LVDS_11_N	44.50445	JX1_LVDS_23_N	44.50563
JX1_LVDS_11_P	44.5027	JX1_LVDS_23_P	44.50387

JX2			
Signal Name	Routed Length (mm)	Signal Name	Routed Length (mm)
JX2_LVDS_0_N	45.20049	JX2_LVDS_12_N	45.20002
JX2_LVDS_0_P	45.19971	JX2_LVDS_12_P	45.20012
JX2_LVDS_1_N	45.20017	JX2_LVDS_13_N	45.19981
JX2_LVDS_1_P	45.19991	JX2_LVDS_13_P	45.19992
JX2_LVDS_2_N	45.19973	JX2_LVDS_14_N	45.19997
JX2_LVDS_2_P	47.43536	JX2_LVDS_14_P	45.20025
JX2_LVDS_3_N	45.20016	JX2_LVDS_15_N	45.19991
JX2_LVDS_3_P	45.20007	JX2_LVDS_15_P	45.20023
JX2_LVDS_4_N	45.20047	JX2_LVDS_16_N	45.2003
JX2_LVDS_4_P	45.19976	JX2_LVDS_16_P	45.20032
JX2_LVDS_5_N	45.20038	JX2_LVDS_17_N	45.19977
JX2_LVDS_5_P	45.2	JX2_LVDS_17_P	45.19976
JX2_LVDS_6_N	45.20017	JX2_LVDS_18_N	45.19982
JX2_LVDS_6_P	45.19982	JX2_LVDS_18_P	45.19978
JX2_LVDS_7_N	45.2	JX2_LVDS_19_N	45.1999
JX2_LVDS_7_P	45.20017	JX2_LVDS_19_P	45.19987
JX2_LVDS_8_N	45.19987	JX2_LVDS_20_N	45.19967
JX2_LVDS_8_P	45.20028	JX2_LVDS_20_P	45.20023
JX2_LVDS_9_N	45.20034	JX2_LVDS_21_N	45.1998
JX2_LVDS_9_P	45.19988	JX2_LVDS_21_P	45.19984
JX2_LVDS_10_N	45.20044	JX2_LVDS_22_N	45.20015
JX2_LVDS_10_P	45.1996	JX2_LVDS_22_P	45.20034
JX2_LVDS_11_N	45.19986	JX2_LVDS_23_N	45.19989
JX2_LVDS_11_P	45.20024	JX2_LVDS_23_P	45.19987

Table 20 – PicoZed 7015/7030 JX1/JX2 Net Lengths