Automotive PMIC Series for Processors, FPGAs Applications

Configurable PMIC Including 4ch Switching DCDC Regulators and 3ch LDOs

BD96801Q30-C

General Description

BD96801Q30-C is an automotive grade configurable PMIC (Power Management Integrated Circuit) with supporting Functional Safety features for application processors, SoCs and FPGAs.
It has a scalable approach of output currents and rails by using internal MOSFET delivering up to 8 A output or using external Driver MOS with 40 A output.

Features

- AEC-Q100 Qualified*(Note 1)*
- ISO 26262 Process Compliant to Support ASIL-D
- Ultra-high Buck Switching Frequency up to 4 MHz
- Built-in MOSFETs or External Driver MOS (BD96340MFF-C) Selectable for BUCK1 and BUCK2
- Built-in MOSFETs for BUCK3 and BUCK4
- Dual Phase Operation for BUCK1 and BUCK2
- Dual Phase Operation for BUCK3 and BUCK4
- Remote Sensing for Accurate Voltage at the Point of Load
- Multipurpose LDO for LDO5, LDO6
- Load Switch or LDO Selectable for LDO7 Output
- Programmable Power Sequencer by OTP (One-time Programmable Memory), EEPROM, or I^2C
- High Precision Built-in Supervision
  OVD (Over Voltage Detection), UVD (Under Voltage Detection), TW (Thermal Warning)
- Built-in Protection
  OVP (Over Voltage Protection), UVP (Under Voltage Protection), TSD (Thermal Shutdown)
- Built-in UVLO (Under Voltage Lockout) for VIN, PVIN1 to PVIN7, and VREG15IN
- Built-in Digital Self-test for OTP, Power Sequence, and Detection
- Built-in Analog Self-test for Detection
- Built-in Self-test for Critical Signal Pins (PRSTB, INTB_ADDPRSTB1, EN)
- Built-in Mutual Monitoring of VREF and OSC
- Q&A Watchdog Timer
- I^2C Support Fast Mode (Max 400 kHz) and Fast Mode Plus (Max 1 MHz) with CRC

(Note 1) Grade1

Applications

- Advanced Driver Assistance Systems (ADAS)
- Instrument Cluster Panel
- In-vehicle Infotainment Systems (IVI Systems)

Key Specifications

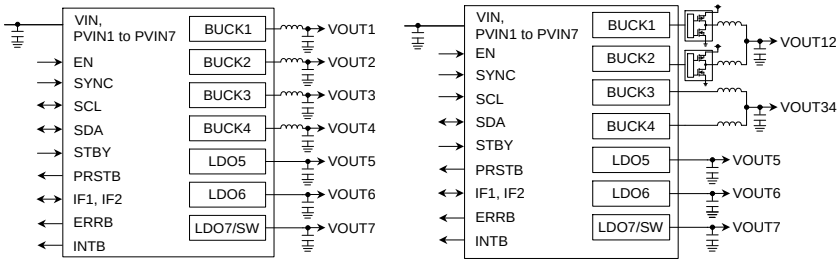
- Input Voltage Range: 2.7 V to 5.5 V
- BUCK1, BUCK2 Output Voltage Range
  Single Phase Internal FET Mode: 0.5 V to 3.3 V
  Dual Phase Internal FET Mode: 0.5 V to 1.2 V
  DRMOS Mode: 0.5 V to 1.0 V
- BUCK1, BUCK2
  Output Current Built-in FET: 2 A (Max)
- BUCK3, BUCK4 Output Voltage Range
  Single Phase Mode: 0.5 V to 3.3 V
  Dual Phase Mode: 0.5 V to 1.2 V
- BUCK3, BUCK4 Output Current: 4 A (Max)
- Switching Frequency: 2.25 MHz, 4 MHz
- LDO5 Output Voltage Range: 0.3 V to 3.3 V
- LDO5 Output Current: 300 mA (Max)
- LDO6 Output Voltage Range: 0.3 V to 3.3 V
- LDO6 Output Current: 300 mA (Max)
- LDO7 Output Voltage Range: 0.3 V to 3.3 V
- LDO7 Output Current: 300 mA (Max)
- Standby Current: 0 µA (Typ)
- Operating Ambient Temperature Range: -40 °C to +125 °C

Packages	**W (Typ) x D (Typ) x H (Max)**
UQFN48FV6060	6.0 mm x 6.0 mm x 1.0 mm

Special Characteristics

- Output Voltage :
  (BUCK1, BUCK2, BUCK3, BUCK4, LDO5, LDO6, LDO7)

Typical Application Circuit



Contents

Pin Configuration

(TOP VIEW)

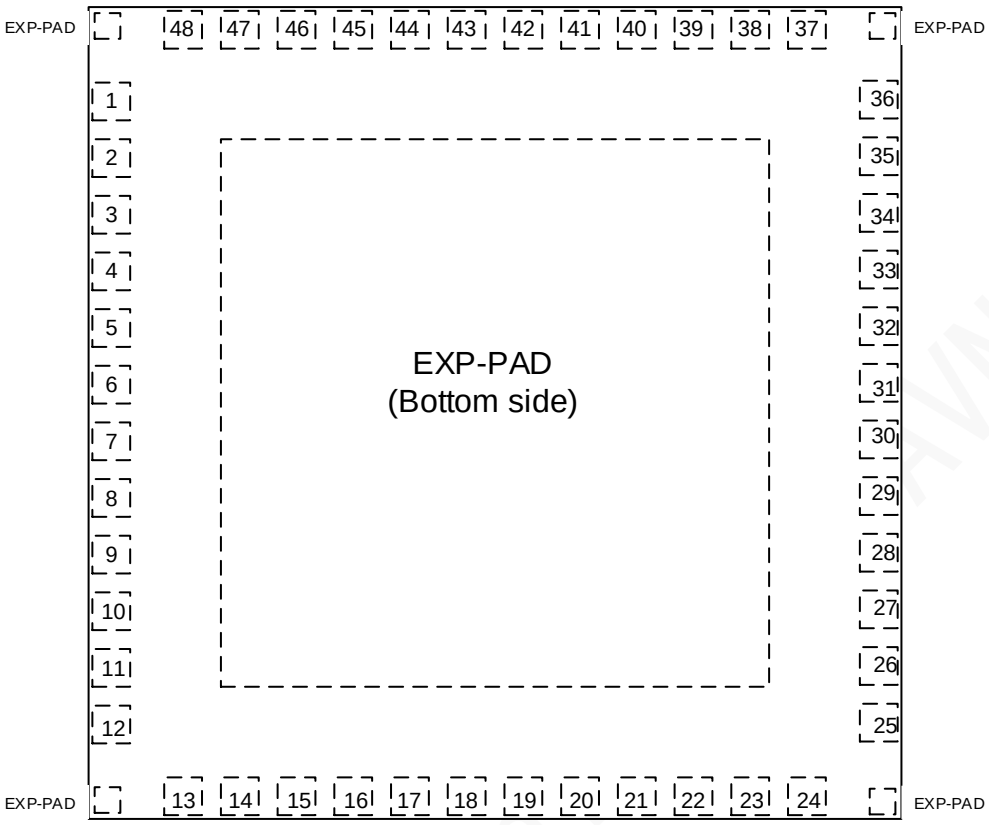


Figure 1. Pin Configuration

Pin Descriptions

Table 1. Pin Descriptions

Pin No.	Pin Name	Function	When not in use
1	IF1_ADDEN1	IF1 or ADD_EN1 selectable by (3Eh) ADD_EN1 register. IF1 function is selected when ADD_EN1 is 00h. Dedicated clock pin for communication between BD96801Qxx-C and BD96802Qxx-C. ADD_EN1 function is selected when ADD_EN1 is not 00h. Additional enable function pin for ADD_EN1 channels set by register. This pin has typical 10 µs de-bounce time when ADD_EN1 mode.	GND.
2	IF2	Dedicated data pin for communication between BD96801Qxx-C and BD96802Qxx-C.	GND.
3	VREG15	Output pin for VREG15 (LDO).	-
4	VREG15IN	1.5 V power supply pin. Connect to the VREG15 output.	-
5	SDA	Serial interface data input and output pin for I^2C access.	GND or Pull high to VIN.
6	SCL	Serial interface clock input and output pin for I^2C access.	GND or Pull high to VIN.
7	EN	Enable input pin. This pin has typical 10 µs de-bounce time. Regarding the relationship between STBY and EN, refer to explanation of the STBY pin.	VIN.
8	INTB_ADDPRSTB1	INTB or ADD_PRSTB1 selectable by the (3Dh) ADD_PRSTB1 register. INTB function is selected when ADD_PRSTB1 is 00h. Open-drain interrupt signal pin. This pin is active low. ADD_PRSTB1 is selected when ADD_PRSTB1 is not 00h. Open-drain power good reset signal pin of ALWAYS_ON, ADD_EN1, or ADD_EN2 channels which is selected by the ADD_PRSTB1 register. This pin is active low.	OPEN.
9	SYNC_ADDEN2	SYNC or ADD_EN2 selectable by (3Fh) ADD_EN2 register. SYNC function is selected when ADD_EN2 is 00h. Synchronize the DCDC switching frequency with the external clock. ADD_EN2 function is selected when ADD_EN2 is not 00h. Additional enable function pin for ADD_EN2 channels set by register. This pin has typical 10 µs de-bounce time when ADD_EN2 mode.	OPEN.
10	VIN	System power supply pin.	VIN.
11	DREN1	Enable output pin for Driver MOS connected to BUCK1.	OPEN.
12	PWM1	PWM output pin for Driver MOS connected to BUCK1.	OPEN.
13	FBP1	Positive remote sense input pin for BUCK1.	OPEN or GND.
14	FBN1	Negative remote sense input pin for BUCK1.	GND.
15	PVIN1	Power supply pin for BUCK1 power MOSFET. Connect to the same voltage as VIN.	VIN.
16	SW1_ISENSE1	SW1 or ISENSE1 is selected by (0Ah) BUCK1_IntFET. SW1 is selected when BUCK1_IntFET is 1. Switch pin for BUCK1 internal FET mode. ISENSE1 is selected when BUCK1_IntFET is 0. Output current sense input pin for BUCK1 Driver MOS mode.	OPEN.
17	PGND12	Power GND for BUCK1 and BUCK2.	GND.
18	SW2_ISENSE2	SW2 or ISENSE1 is selected by (0Ah) BUCK2_IntFET. SW2 is selected when BUCK2_IntFET is 1. Switch pin for BUCK2 internal FET mode. ISENSE2 is selected when BUCK2_IntFET is 0. Output current sense input pin for BUCK2 Driver MOS mode.	OPEN.
19	PVIN2	Power supply pin for BUCK2 power MOSFET. Connect to the same voltage as VIN.	VIN.
20	FBN2	Negative remote sense input pin for BUCK2.	GND.
21	FBP2	Positive remote sense input pin for BUCK2.	OPEN or GND.
22	TSENSE1	Driver MOS Die temperature monitoring pin for Driver MOS connected to BUCK1.	OPEN.
23	TSENSE2	Driver MOS Die temperature monitoring pin for Driver MOS connected to BUCK2.	OPEN.
24	GATE7	Control Gate of External PMOS SW for LDO7.	OPEN.
25	PWM2	PWM output pin for Driver MOS connected to BUCK2.	OPEN.
26	DREN2	Enable output pin for Driver MOS connected to BUCK2.	OPEN.

Pin No.	Pin Name	Function	When not in use
27	PVIN7	Power supply pin for LDO7 power MOSFET.	OPEN.
28	VOUT7	Output pin for LDO7.	OPEN.
29	PVIN6	Power supply pin for LDO6 power MOSFET.	OPEN.
30	VOUT6	Output pin for LDO6.	OPEN.
31	GND	GND.	GND.
32	VOUT5	Output pin for LDO5.	OPEN.
33	PVIN5	Power supply pin for LDO5 power MOSFET.	OPEN.
34	STBY	Stand-by request input pin. This pin has typical 10 µs de-bounce time. When the STBY pin is active (high), then PMIC enters STANDBY state as soon as PMIC is disabled (EN = L). When PMIC is re-enabled (EN = H) while being in STANDBY state, PMIC will not re-run PMIC system checks and initialization (BIST, OTP READ, EEP READ etc.). If STANDBY state is inhibited by keeping the STBY pin low, PMIC will first execute PMIC system checks and initialization as soon as it is enabled (STBY = L, EN = H). Note, that some PMIC registers can be modified via I^2C commands only when PMIC is in STANDBY state. For more details, please refer to Figure 5. Main State Machine.	VIN.
35	PRSTB	Open-drain reset signal output pin for SoC / FPGA. This pin is active low.	OPEN.
36	ERRB_ADDPRSTB2	ERRB or ADD_PRSTB2 selectable by the (3Dh) ADD_PRSTB2 register. ERRB function is selected when ADD_PRSTB2 is 00h. Open-drain error signal pin. This pin is active low. ADD_PRSTB2 is selected when ADD_PRSTB2 is not 00h. Open-drain power good reset signal pin of ALWAYS_ON, ADD_EN1, or ADD_EN2 channels which is selected by the ADD_PRSTB2 register. This pin is active low.	OPEN.
37	FBP3	Positive remote sense input pin for BUCK3.	OPEN or GND.
38	FBN3	Negative remote sense input pin for BUCK3.	GND.
39	PVIN3	Power supply pin for BUCK3 power MOSFET. Connect to the same voltage as VIN.	VIN.
40	SW3	Switch pin for BUCK3.	OPEN.
41	SW3	Switch pin for BUCK3.	OPEN.
42	PGND34	Power GND for BUCK3 and BUCK4.	GND.
43	PGND34	Power GND for BUCK3 and BUCK4.	GND.
44	SW4	Switch pin for BUCK4.	OPEN.
45	SW4	Switch pin for BUCK4.	OPEN.
46	PVIN4	Power supply pin for BUCK4 power MOSFET. Connect to the same voltage as VIN.	VIN.
47	FBN4	Negative remote sense input pin for BUCK4.	GND.
48	FBP4	Positive remote sense input pin for BUCK4.	OPEN or GND.
-	EXP-PAD (CENTER)	GND.	GND.
-	EXP-PAD (CORNER)	GND. Connect to floating PCB pattern or GND PCB pattern.	OPEN or GND.

Block Diagram

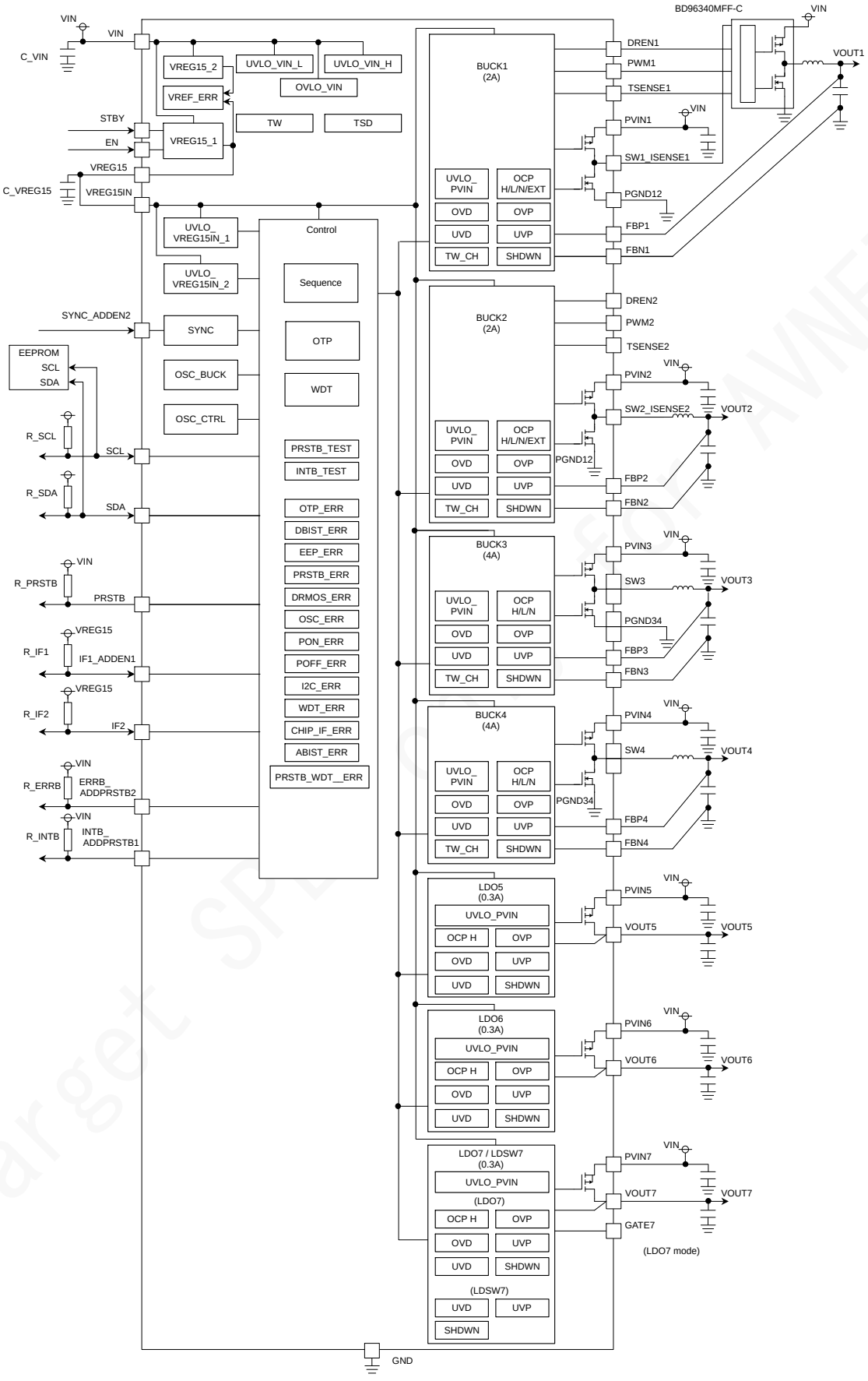


Figure 2. Block Diagram and an Example of External Component

Block Diagram – continued

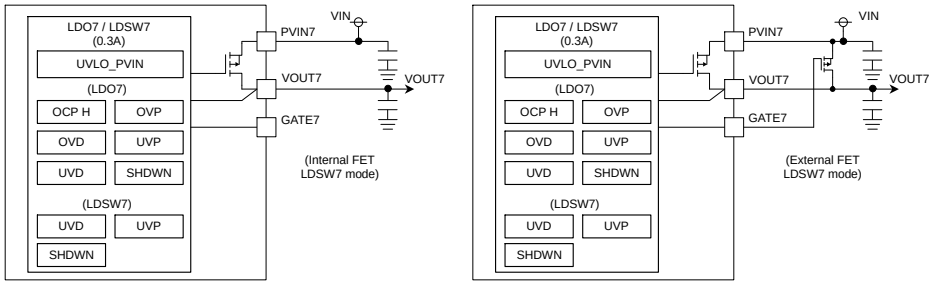


Figure 3. LDSW7 Mode Connection

Description of Blocks

General Block

Table 2. General Blocks Description

Name	Description
VREG15_1	Internal Regulator. This is also used as internal reference.
VREG15_2	Internal Regulator for monitoring VREG15_1.
OSC_BUCK	Internal Oscillator for BUCK1 to BUCK4.
OSC_CTRL	Internal Oscillator for Control Block.
SYNC	When external clock is input to the SYNC_ADDEN2 pin, BUCKs switching frequency is synchronized.
BUCK1 to BUCK4	Step-down Regulator Control.
LDO5, LDO6	LDO Control.
LDO7	LDO Control / Load Switch Control.
Sequence	Protection, Sequence, Register setting, and Interface Control Block. Refer to each section for protection control.
OTP	One-time Programmable Memory.
WDT	Q&A or IF watchdog timer used to monitor an external processor, SoC or FPGA.
SHDWN	Output voltage comparator for Power OFF detection.
PRSTB_TEST	Using for system BIST. When (register 3Bh) PRSTB_MANUAL = 0, the PRSTB pin is forced L.
INTB_TEST	Using for system BIST. When (register 3Bh) INTB_MANUAL = 0, the INTB_ADDPRSTB1 pin is forced L.

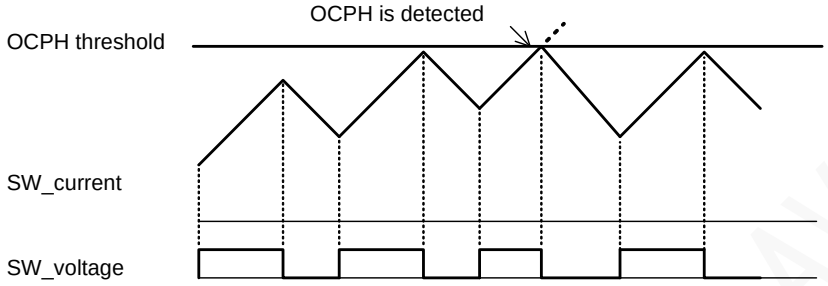
Description of Blocks – continued

Protect and Warning Block

Table 3. Protection and Warning Block Description

Name	Description
UVLO_VIN_L	Lower threshold Under Voltage Lockout for VIN. When UVLO_VIN_L is detected, internal block will shutdown and all register data are cleared.
UVLO_VIN_H	Higher threshold Under Voltage Lockout for VIN. When UVLO_VIN_H is detected for 10 µs, VOUT1 to VOUT7 will shutdown.
UVLO_VREG15IN_1	Under Voltage Lockout for VREG15IN. 1 and 2 are multiplexing.
UVLO_VREG15IN_2	
OVLO_VIN	Over Voltage Lockout for VIN.
OTP_ERR	Digital Built-in self-test for OTP block. ECC for OTP data.
DBIST_ERR	Digital Built-in self-test for Control Block.
EEP_ERR	CRC error detection for EEPROM data.
ABIST_ERR	Analog Built-in self-test for UVD, OVD, and TW.
PRSTB_ERR	In ACTIVE state, when the PRSTB pin is forced L from outside for 10 µs, error is detected. For example, in case of PMICs combination mode, when only other PMIC detects an error and outputs the PRSTB pin low, this error is detected.
DRMOS_ERR	After the DREN1 or DREN2 outputs high by PMIC, when the DREN1 or DREN2 pin is forced L from outside, error is detected immediately. For example, when DRMOS detects internal OCP, DRMOS outputs DREN low, and PMIC detects the DRMOS error.
VREF_ERR	Monitoring the difference of the voltage between VREG15_1 and VREG15_2. When the difference is typical 3 % or more, error is detected.
TSD	Latch-type Thermal Shutdown protection.
OSC_ERR	Monitoring the OSC_BUCK and OSC_CTRL while EN = H.
PON_ERR	Monitoring the completion of all VOUT power-on in POWER_ON state within the time set by PON_OVERTIME in resister 3Ah.
POFF_ERR	Monitoring the completion of all VOUT power-off in POWER_OFF1 and POWER_OFF2 state within the time set by POFF_OVERTIME in resister 3Ah.
UVLO_PVIN	Under Voltage Lockout for PVIN1 to PVIN7. When the PVIN voltage is under threshold for 7 µs, the UVLO_PVINx_STAT (x: 1 to 7) register becomes 1. The error channel and the same group channels will shutdown.
OVP	Over Voltage Protection for BUCK1 to BUCK4 and LDO5 to LDO7. When the voltage reaches OVP threshold, the XXX_OVP_STAT register becomes 1 and the ERRB is L asserted immediately. (XXX: BUCK1 to BUCK4 and LDO5 to LDO7) If the over voltage continues for 10 µs, the error channel and the same group channels will shutdown.
UVP	Under Voltage Protection for BUCK1 to BUCK4 and LDO5 to LDO7. When the voltage reaches UVP threshold, the XXX_UVP_STAT register becomes 1 and the ERRB is L asserted immediately. (XXX: BUCK1 to BUCK4 and LDO5 to LDO7) If the under voltage continues for 1 ms, the error channel and the same group channels will shutdown.

Protection and Warning Block - continued

Name	Description
OCP H	High-side Over Current Protection for BUCK1 to BUCK4 (internal FET mode) and LDO5 to LDO7. The threshold is selectable by register. In case of BUCK1 to BUCK4 internal FET mode. When bit SHD_INTB in register 20h is set to 0, the PMIC continues switching even when OCPH is detected. However, the on-time is decreased such that the switch peak current does not exceed the OCPH threshold. Consequently, also the output voltage will gradually decrease.  After OCPH detection, PMIC starts to count the number of consecutive normal switching cycles that don't trigger OCPH. If OCPH is detected again, the counter is cleared. When the counter is smaller than 8 after 10 µs since the 1st OCPH detection, the BUCKx_OCPH_STAT (x: 1 to 4) register becomes 1. In addition, when bit SHD_INTB in register 20h is set to 1 and 8 times consecutive normal switching cycles have not occur after 512 µs since the 1st OCPH detection, the error channel and the same group channels will shutdown. The BUCK OCPH threshold is not average current, but inductor peak current. The average current is calculated by below. $$I_{average} = OCPH\ threshold - \frac{(VIN - VOUT) \times VOUT}{2 \times L \times fsw \times VIN}\ [A]$$ In case of LDO5 to LDO7. When a LDO OCPH is detected, the output current is limited. If OCPH detection is continuing for 10 µs, the LDOx_OCPH_STAT (x: 5 to 7) register becomes 1. In addition, if the detection continue for 512 µs, the error channel and the same group channels will shutdown when the register 20h SHD_INTB = 1. In case of BUCK1 and BUCK2 dual phase Driver MOS mode. The BUCKx_OCPH_STAT (x: 1 to 2) register means detection of current difference between DRMOS1 and DRMOS2. When the SW1_ISENSE1 pin voltage is typical 775 mV larger than the SW2_ISENSE2 pin voltage, current difference is detected. If the detection continue for 10 µs, the BUCK1_OCPH_STAT register becomes 1. When the SW2_ISENSE2 pin voltage is typical 775 mV larger than the SW1_ISENSE1 pin voltage, current difference is detected. If the detection continue for 10 µs, the BUCK2_OCPH_STAT register becomes 1. In addition, if the detection continue for 512 µs, the error channel and the same group channels will shutdown when the register 20h SHD_INTB = 1.
OCP L	Low-side Over Current Protection for BUCK1 to BUCK4 (internal FET mode). Typical 6.2 A for BUCK1 to BUCK2. Typical 10.2 A for BUCK3 to BUCK4. When OCPL is detected, the SW ON will be skipped. If 8 times normal switching don't continue for 10 µs, the BUCKx_OCPL_STAT (x: 1 to 4) register becomes 1. In addition, if 8 times normal switching don't continue by 512 µs, the error channel and the same group channels will shutdown when the register 20h SHD_INTB = 1. In case of BUCK1 and BUCK2 dual phase Driver MOS mode. The BUCKx_OCPL_STAT (x: 1 to 2) register means detection of current difference between DRMOS1 and DRMOS2. When the SW1_ISENSE1 pin voltage is typical 500 mV smaller than the SW2_ISENSE2 pin voltage, current difference is detected. If the detection continue for 10 µs, the BUCK1_OCPL_STAT register becomes 1. When the SW2_ISENSE2 pin voltage is typical 500 mV smaller than the SW1_ISENSE1 pin voltage, current difference is detected. If the detection continue for 10 µs, the BUCK2_OCPL_STAT register becomes 1. In addition, if the detection continue for 512 µs, the error channel and the same group channels will shutdown when the register 20h SHD_INTB = 1.

Protection and Warning Block - continued

Name	Description
OCP N	Negative Low-side Over Current Protection for BUCK1 to BUCK4 (internal FET mode). Typical -3.1 A for BUCK1 to BUCK2. Typical -6.2 A for BUCK3 to BUCK4. When OCPN is detected, the SW is set to High to reduce negative current. If 8 times normal switching don't continue for 10 µs, the BUCK1_OCPN_OCPEXT_STAT, BUCK2_OCPN_OCPEXT_STAT, BUCK3_OCPN_STAT, or BUCK4_OCPN_STAT register becomes 1. In addition, if 8 times normal switching don't continue by 512 µs, the error channel and the same group channels will shutdown when the register 20h SHD_INTB = 1.
OCP EXT	Over Current Protection for BUCK1 to BUCK2 when Driver MOS using. When the SW1_ISENSE1 or SW2_ISENSE2 pin voltage is over the OCP threshold voltage selected by the BUCK1_EXT_OCP or BUCK2_EXT_OCP register for 10 µs, the BUCK1_OCPN_OCPEXT_STAT or BUCK2_OCPN_OCPEXT_STAT register becomes 1. When the register 20h SHD_INTB = 1 and detection continues for 512 µs, the error channel and the same group channels will shutdown. DRMOS outputs ISENSE voltage which is ISENSE gain times the average current. The OCP current threshold is calculated by threshold voltage and ISENSE gain. $$OCP\ current\ threshold = \ threshold\ voltage \div ISENSE\ gain$$ For ISENSE gain, refer to DRMOS specification. For example, ISENSE gain of BD96340MFF-C is 2.13 µ times R_ISET which is the resistor connected to the ISET pin of BD96340MFF-C.
OVD	Over Voltage Detection for VOUT1 to VOUT7. OVD has mask time selected by the OVD_MASK_TIME register. When over voltage is detected longer than OVD_MASK_TIME, the XXX_OVD_STAT register becomes 1. (XXX: BUCK1 to BUCK4 and LDO5 to LDO7) When the register 20h SHD_INTB = 1 and OVD is detected for 512 µs, the error channel and the same group channels will shutdown.
UVD	Under Voltage Detection for VOUT1 to VOUT7. UVD has mask time selected by the UVD_MASK_TIME register. When over voltage is detected longer than UVD_MASK_TIME, the XXX_UVD_STAT register becomes 1. (XXX: BUCK1 to BUCK4 and LDO5 to LDO7) In case of BUCK1 to BUCK4 or LDO5 to LDO7: When the register 20h SHD_INTB = 1 and UVD is detected for 512 µs, the error channel and the same group channels will shutdown. In case of LDSW7: When the register 20h SHD_INTB = 1 and UVD is detected for 256 µs, the error channel and the same group channels will shutdown.
TW_CH	Thermal Warning for Driver MOS or each internal Power MOSFET of BUCK. TW_CH has mask time selected by the TW_MASK_TIME register. When thermal warning is detected longer than TW_MASK_TIME, the XXX_TW_CH_STAT register becomes 1. (XXX: BUCK1 to BUCK4) When the register 20h SHD_INTB = 1 and TW_CH is detected for 512 µs, the error channel and the same group channels will shutdown.
TW	Thermal Warning in the center of die chip. TW has mask time selected by the TW_MASK_TIME register. When thermal warning is detected longer than TW_MASK_TIME, the TW_STAT register becomes 1. When the register 20h SHD_INTB = 1 and TW is detected for 512 µs, all channels will shutdown.
I2C_ERR	I^2C error checking. Mode is selectable by the CRC_ON register. When I^2C communication CRC error occurs, the I2C_INT_STAT register becomes 1.
WDT_ERR	Watch Dog Timer error. Refer to WDT section. When WDT error occurs, the WDT_INT_STAT register becomes 1.
CHIP_IF_ERR	IF1 and IF2 communication error checking. When continuous 15 times communication error occurs, the CHIP_IF_ERR_STAT register becomes 1 and all channels will shutdown. If (39h) CHIP_IF_SHD_OFF = 1, the CHIP_IF_ERR_STAT register doesn't become 1, the ERRB_ADDPRSTB2 (ERRB mode) pin doesn't become low, and any channel don't shutdown by this error.
CHIP_IF_INT	IF1 and IF2 communication CRC error checking. When IF1 and IF2 communication CRC error occurs, the CHIP_IF_INT_STAT register becomes 1.
PRSTB_WDT_ERR	When PRSTB_WDT_TO = 1, if a control device cannot control WDT enable with in timeout time from PRSTB H de-assertion, the PRSTB_WDT_ERR_STAT register becomes 1 and system be shutdown. The kind of PRSTB signal is selected by the PRSTB_WDT register. The time of timeout is selected by the PRSTB_WDT_TO_SEL register.

Description of Blocks – continued

Protection Control

The following describes the behavior of PMIC when an error or warning occurs.

Table 4. Protection and Warning Behavior

Function	Each Power channel and PRSTB behavior				Register Reset	Pin behavior	
	All CHs and PRSTB	Error CH	Other CHs and PRSTB			ERRB	INTB
			Same Group	Other Group			
UVLO_VREG15IN_1	OFF	-	-	-	Reset	H	H
UVLO_VREG15IN_2	OFF	-	-	-	Reset	H	H
UVLO_VIN_L	OFF	-	-	-	Reset	H	H
UVLO_VIN_H	OFF	-	-	-	-	L	-
OVLO_VIN	OFF	-	-	-	-	L	-
OTP_ERR	OFF	-	-	-	-	L	-
DBIST_ERR	OFF	-	-	-	-	L	-
EEP_ERR	OFF	-	-	-	-	L	-
ABIST_ERR	OFF	-	-	-	-	L	-
PRSTB_ERR	OFF	-	-	-	-	L	-
DRMOS_ERR	OFF	-	-	-	-	L	-
VREF_ERR	OFF	-	-	-	-	L	-
TSD	OFF	-	-	-	-	L	-
OSC_ERR	OFF	-	-	-	-	L	-
PON_ERR	OFF	-	-	-	-	L	-
POFF_ERR	OFF	-	-	-	-	L	-
CHIP_IF_ERR	OFF	-	-	-	-	L	-
PRSTB_WDT_ERR	OFF	-	-	-	-	L	-
UVLO_PVIN	-	OFF(*2)		CONTINUE	-	L	-
OVP	-	OFF(*2)			-	L	-
UVP	-	OFF(*2)			-	L	-
OCP H	-	CONTINUE /OFF(*1)(*2)			-	-	L
OCP L	-				-	-	L
OCP N	-				-	-	L
OCP EXT	-				-	-	L
OVD	-				-	-	L
UVD	-				-	-	L
TW_CH	-				-	-	L
TW	CONTINUE /OFF(*1)	-	-	-	-	-	L
WDT_ERR	-	-	-	-	-	-	L
I2C_ERR	-	-	-	-	-	-	L
CHIP_IF_INT	-	-	-	-	-	-	L

(*1) When each interrupt event is detected, it is selectable in either CONTINUE (20h, SHD_INTB = 0) or OFF (20h, SHD_INTB = 1).
(*2) When the error CH becomes OFF, also the same group channels (1Dh to 20h registers setting) become OFF.
If Always ON, normal EN, ADD_EN1, and ADD_EN2 channels are same group, the group OFF is difference from this table.
Refer to Table 5.

ERRB and INTB are active low.
ERRB is OR of L (active low) of the registers “Detect to ERRB”. INTB is OR of L (active low) of the registers “Detect to INTB”.
Each factor of INTB or ERRB can be masked by resister setting.

Protection Control - continued

When the group setting is same and EN signal is different, the group OFF is represented by this table.
When the always ON or normal EN channel error is detected, all channels become OFF.
When the ADD_EN1 or ADD_EN2 channel error is detected, only ADD_EN1 or ADD_EN2 channels becomes OFF.

Table 5. Protection behavior when the group setting is same and EN signal is different

channel	Before Error	Always ON channel Error	EN channel Error	ADD_EN1 channel Error	ADD_EN2 channel Error
Always ON channels	ON	OFF	OFF	CONTINUE	CONTINUE
EN channels	ON/OFF	OFF	OFF	CONTINUE	CONTINUE
ADD_EN1 channels	ON/OFF	OFF	OFF	OFF	CONTINUE
ADD_EN2 channels	ON/OFF	OFF	OFF	CONTINUE	OFF

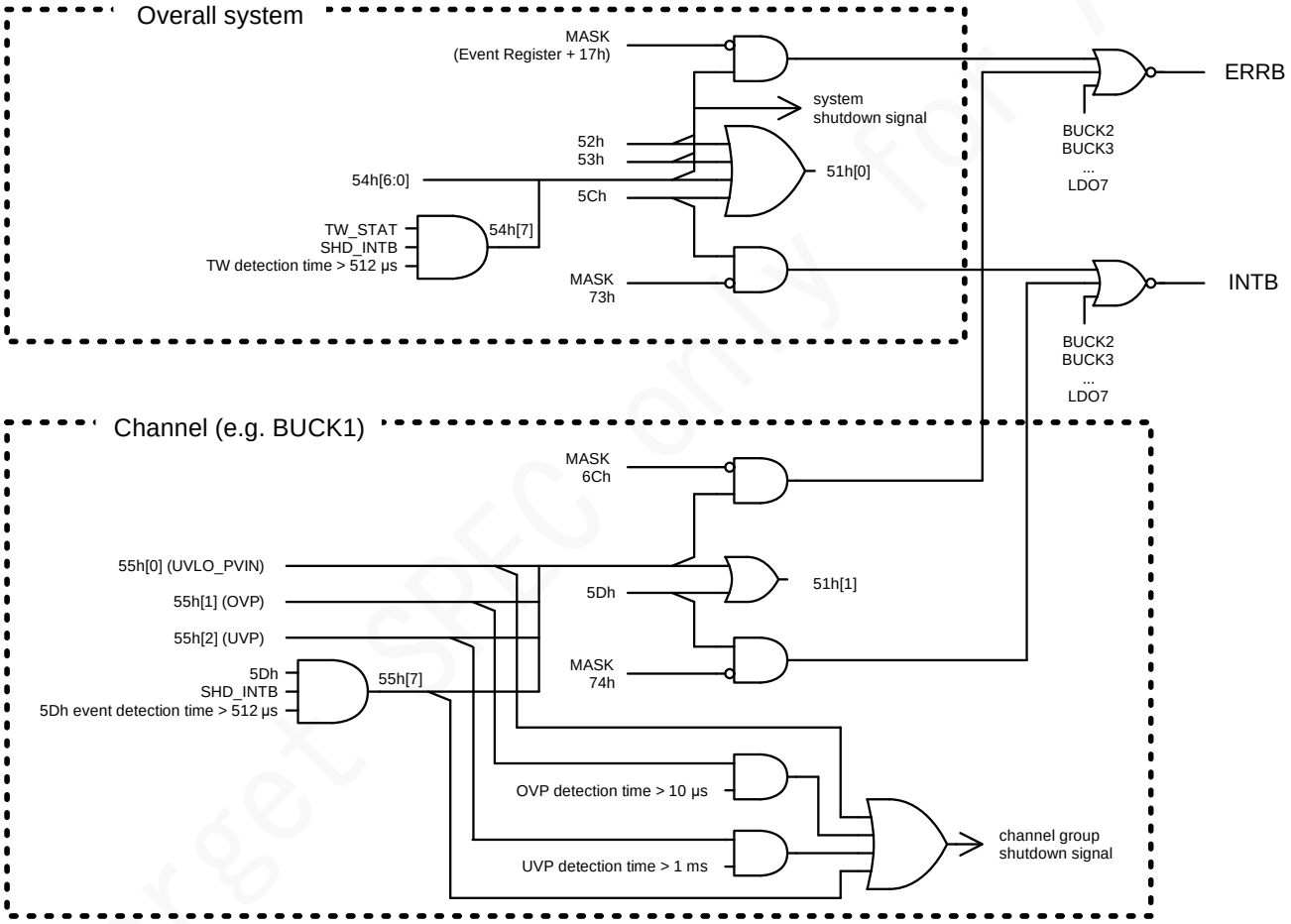


Figure 4. ERRB and INTB

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage1	V_{IN}, V_{PVIN1}, V_{PVIN2}, V_{PVIN3}, V_{PVIN4} (same voltage)	-0.3 to +6.0	V
Supply Voltage2	V_{PVIN5}, V_{PVIN6}, V_{PVIN7}	-0.3 to +6.0	V
Input or Output Voltage	V_{REG15}, $V_{REG15IN}$	-0.3 to +2.0	V
	V_{SDA}, V_{SCL}	-0.3 to +6.0	V
	V_{EN}, V_{SYNC_ADDEN2}, V_{STBY}, V_{PRSTB}, $V_{INTB\_ADDPRSTB1}$, $V_{ERRB\_ADDPRSTB2}$, $V_{TSENSE1}$,$V_{TSENSE2}$, V_{IF1_ADDEN1}, V_{IF2}	-0.3 to VIN+0.3	V
	V_{PWM1}, $V_{SW1\_ISENSE1}$, V_{DREN1}, V_{FBP1}, V_{FBN1}	-0.3 to PVIN1+0.3	V
	V_{PWM2}, $V_{SW2\_ISENSE2}$, V_{DREN2}, V_{FBP2}, V_{FBN2}	-0.3 to PVIN2+0.3	V
	V_{SW3}, V_{FBP3}, V_{FBN3}	-0.3 to PVIN3+0.3	V
	V_{SW4}, V_{FBP4}, V_{FBN4}	-0.3 to PVIN4+0.3	V
	V_{OUT5}	-0.3 to PVIN5+0.3	V
	V_{OUT6}	-0.3 to PVIN6+0.3	V
	V_{OUT7}, V_{GATE7}	-0.3 to PVIN7+0.3	V
Maximum Junction Temperature	Tjmax	+150	°C
Storage Temperature Range	Tstg	-55 to +150 *(Note 1)*	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) Operation is not guaranteed.

Thermal Resistance *(Note 2)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 4)*	2s2p*(Note 5)*	
UQFN48FV6060				
Junction to Ambient	θ_{JA}	85.0	35.1	°C/W
Junction to Top Characterization Parameter*(Note 3)*	Ψ_{JT}	13	11	°C/W

(Note 2) Based on JESD51-2A(Still-Air).
(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 4) Using a PCB board based on JESD51-3.
(Note 5) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 6)*	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 6) This thermal via connect with the copper pattern of layers 1,2, and 4. The placement and dimensions obey a land pattern.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage1	V_{IN}, V_{PVIN1}, V_{PVIN2}, V_{PVIN3}, V_{PVIN4}	2.7	3.3	5.5	V
Power Supply Voltage2	V_{PVIN5}, V_{PVIN6}	1.76	3.30	5.50	V
Power Supply Voltage3	V_{PVIN7} (LDO)	1.76	3.30	5.50	V
Power Supply Voltage4	V_{PVIN7} (Load SW)	2.7	3.3	5.5	V
Operating Temperature	Topr	-40	+25	+125	°C
Operating Junction Temperature	Tj	-40	+25	+150	°C

Voltage and MODE Setting by OTP

Channel	Voltage [V] or (LDO7) LDSW mode	Enable / Disable	Single / Dual	(BUCK1, BUCK2) IntFET / Driver MOS or (LDSW7) IntFET / ExtFET	EN / ALWAYS_ON / ADD_EN1/ ADD_EN2
BUCK1	1.8	Enable	Single	IntFET	EN
BUCK2	1.35	Enable		IntFET	EN
BUCK3	1.0	Enable	Single	-	EN
BUCK4	3.3	Enable		-	EN
LDO5	1.2	Enable	-	-	EN
LDO6	2.5	Enable	-	-	EN
LDO7	3.3	Enable	-	-	EN
PRSTB	-	-	-	-	EN

Electrical Characteristics
(Unless otherwise specified Tj = -40 °C to +150 °C, V_{IN} / V_{PVIN1} to V_{PVIN7} = 5 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
[General]						
VIN Total Current 1	I_{VIN1}	-	0	200	µA	EN = L, STBY = L, VIN and PVIN1 to PVIN7
VIN Total Current 2	I_{VIN2}	-	3.5	12	mA	EN = L, STBY = H, VIN and PVIN1 to PVIN7
VIN Total Current 3	I_{VIN3}	-	8.2	25	mA	EN = H, STBY = H, No switching, No load, VIN and PVIN1 to PVIN7
UVLO_VREG15IN Detect Voltage	$V_{UVLO\_VREG15IN}$	1.15	1.20	1.25	V	VREG15IN: Sweep down
UVLO_VREG15IN Hysteresis Voltage	$V_{UVLO\_VREG15IN\_Hys}$	-	0.2	-	V	VREG15IN: Sweep up
UVLO_VIN_L Detect Voltage	V_{UVLO_L}	2.21	2.30	2.39	V	VIN: Sweep down
UVLO_VIN_L Hysteresis Voltage	$V_{UVLO\_L\_Hys}$	-	0.09	-	V	VIN: Sweep up
UVLO_VIN_H Detect Voltage	V_{UVLO_H}	2.50	2.55	2.60	V	VIN: Sweep down
UVLO_VIN_H Hysteresis Voltage	$V_{UVLO\_H\_Hys}$	-	0.07	-	V	VIN: Sweep up
OVLO_VIN Threshold Voltage	V_{OVLO}	5.70	5.85	6.00	V	VIN: Sweep up
OVLO_VIN Hysteresis Voltage	V_{OVLO_Hys}	-	0.08	-	V	VIN: Sweep down
VREG15 Output Voltage	V_{REG15}	1.521	1.536	1.551	V	
Switching Frequency	fsw	2.025	2.250	2.475	MHz	(0Ch) SW_FREQ = 00b
SYNC Frequency Range	f_{SYNC}	4.05	4.50	4.95	MHz	(0Ch) SW_FREQ = 00b
SYNC Input Duty Range	D_{SYNC}	45	50	55	%	
TSD Detect Temperature	T_{TSD}	-	175	-	°C	Temperatures above 150 °C are only allowed for short periods
TSD Hysteresis Temperature	T_{TSD_Hys}	-	15	-	°C	
TW Detect Temperature	T_{TW}	131	140	149	°C	

Electrical Characteristics – continued
(Unless otherwise specified Tj = -40 °C to +150 °C, V_{IN} / V_{PVIN1} to V_{PVIN7} = 5 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
[CTRL] (STBY, SYNC, EN, ADD_EN1(*1), ADD_EN2)						
CTRL Input Voltage Low	V_{IL_CTRL}	-0.3	-	+0.5	V	
CTRL Input Voltage High	V_{IH_CTRL}	1.2	-	VIN+0.3	V	
CTRL Pull Down Resistance	R_{IN_CTRL}	40	100	160	kΩ	
[I²C] (SDA, SCL)						
I²C Input Voltage Low	V_{IL_I2C}	-0.3	-	+0.5	V	
I²C Input Voltage High	V_{IH_I2C}	1.2	-	VIN+0.3	V	
I²C Input Current	I_{IN_I2C}	-1	0	+1	µA	V_{SDA} = V_{SCL} = 3.3 V
I²C Output Voltage Low	V_{OL_SDA}	-0.3	-	+0.4	V	Iload = -20 mA
[Open Drain Pin] (PRSTB, ERRB, INTB, ADD_PRSTB1, ADD_PRSTB2)						
Open Drain Output Voltage Low	V_{OL_OD}	-	-	+0.7	V	Iload = -3 mA
Pull Up Voltage Range	V_{PU}	1.2	-	VIN	V	
[IF Pin] (IF1(*2), IF2)						
IF Input Voltage Low	V_{IL_IF}	-0.3	-	+0.5	V	
IF Input Voltage High	V_{IH_IF}	1.2	-	VIN+0.3	V	
IF Input Current	I_{IN_IF}	-1	0	+1	µA	V_{IF} = 3.3 V
IF Output Voltage Low	V_{OL_IF}	-0.1	-	+0.1	V	Iload = -3 mA

(*1) When ADDEN1 function is selected from the IF1_ADDEN1 pin.
(*2) When IF1 function is selected from the IF1_ADDEN1 pin.

Electrical Characteristics – continued
(Unless otherwise specified Tj = -40 °C to +150 °C, V_{IN} / V_{PVIN1} to V_{PVIN7} = 5 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
[BUCK1 to BUCK4 (Internal FET mode)]						
DC Output Voltage BUCK1	V_{BUCK1}	1.778	1.800	1.822	V	(21h) BUCK1_INI_VOUT = CEh
DC Output Voltage BUCK2	V_{BUCK2}	1.333	1.350	1.367	V	(22h) BUCK2_INI_VOUT = AAh
DC Output Voltage BUCK3	V_{BUCK3}	0.988	1.000	1.012	V	(23h) BUCK3_INI_VOUT = 64h
DC Output Voltage BUCK4	V_{BUCK4}	3.260	3.300	3.340	V	(24h) BUCK4_INI_VOUT = ECh
Soft-Start Time Rate BUCKx	-	4.5	5.0	5.5	V/ms	(28h to 2Bh) BUCKx_SR = 01b (x: 1 to 4)
High-side FET On-Resistance BUCK1, BUCK2	R_{ONH_BUCK1} R_{ONH_BUCK2}	-	80	160	mΩ	
High-side FET On-Resistance BUCK3, BUCK4	R_{ONH_BUCK3} R_{ONH_BUCK4}	-	40	80	mΩ	
Low-side FET On-Resistance BUCK1, BUCK2	R_{ONL_BUCK1} R_{ONL_BUCK2}	-	70	140	mΩ	
Low-side FET On-Resistance BUCK3, BUCK4	R_{ONL_BUCK3} R_{ONL_BUCK4}	-	35	70	mΩ	
Output Discharge Resistance BUCK1	R_{DIS_BUCK1}	8	30	70	Ω	(2Fh) BUCK1_RDIS = 01b I_{FBP1} = -10 mA Between FBP1 and GND
Output Discharge Resistance BUCK2	R_{DIS_BUCK2}	8	30	70	Ω	(2Fh) BUCK2_RDIS = 01b I_{FBP2} = -10 mA Between FBP2 and GND
Output Discharge Resistance BUCK3	R_{DIS_BUCK3}	5	22	50	Ω	(2Fh) BUCK3_RDIS = 10b I_{FBP3} = -10 mA Between FBP3 and GND
Output Discharge Resistance BUCK4	R_{DIS_BUCK4}	8	30	70	Ω	(2Fh) BUCK4_RDIS = 01b I_{FBP4} = -10 mA Between FBP4 and GND
UVLO_PVINx Threshold Voltage	V_{UVLO_PVINx}	2.21	2.30	2.39	V	PVINx: Sweep down (x: 1 to 4)
UVLO_PVINx Hysteresis Voltage	$V_{UVLO\_PVINx\_Hys}$	-	0.06	-	V	PVINx: Sweep up (x: 1 to 4)
OVP Detecting Rate BUCKx	-	+17	+20	+23	%	(30h) BUCKx_OVP = 11b (x: 1 to 4)
UVP Detecting Voltage BUCK1	V_{UVP_BUCK1}	1.314	1.440	1.566	V	(21h) BUCK1_INI_VOUT = CEh
UVP Detecting Voltage BUCK2	V_{UVP_BUCK2}	0.985	1.080	1.175	V	(22h) BUCK2_INI_VOUT = AAh
UVP Detecting Voltage BUCK3	V_{UVP_BUCK3}	0.730	0.800	0.870	V	(23h) BUCK3_INI_VOUT = 64h
UVP Detecting Voltage BUCK4	V_{UVP_BUCK4}	2.409	2.640	2.871	V	(24h) BUCK4_INI_VOUT = ECh
Over Current Protection BUCK1	I_{OCPH_BUCK1}	2.94	4.20	5.46	A	(32h) BUCK1_INTR_OCPH = 11b
Over Current Protection BUCK2	I_{OCPH_BUCK2}	2.31	3.30	4.29	A	(32h) BUCK2_INTR_OCPH = 10b
Over Current Protection BUCK3	I_{OCPH_BUCK3}	4.90	7.00	9.10	A	(33h) BUCK3_OCPH = 11b
Over Current Protection BUCK4	I_{OCPH_BUCK4}	3.96	5.66	7.36	A	(33h) BUCK4_OCPH = 10b
OVD Detecting Offset Voltage(*1) BUCKx	V_{OVD_BUCKx}	+10	+20	+30	mV	(35h) BUCKx_OVD_UVD = 11b (x: 1 to 4)
UVD Detecting Offset Voltage(*1) BUCKx	V_{UVD_BUCKx}	-30	-20	-10	mV	(35h) BUCKx_OVD_UVD = 11b (x: 1 to 4)
SHDWN Detecting Voltage	V_{SHDWN_BUCKx}	-	0.1	-	V	(x: 1 to 4)
TW_CH Detect Temperature	$T_{TW\_CH\_DET\_BUCKx}$	131	140	149	°C	(x: 1 to 4)

(*1) Delta against the VOUT voltage including DC accuracy from register setting voltage.

Electrical Characteristics – continued
(Unless otherwise specified Tj = -40 °C to +150 °C, V_{IN} / V_{PVIN1} to V_{PVIN7} = 5 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
[LDO5 to LDO7]						
DC Output Voltage LDO5	V_{LDO5}	1.182	1.200	1.218	V	(25h) LDO5_INI_VOUT = 24h
DC Output Voltage LDO6	V_{LDO6}	2.462	2.500	2.538	V	(26h) LDO6_INI_VOUT = 58h
DC Output Voltage LDO7	V_{LDO7}	3.250	3.300	3.350	V	(27h) LDO7_INI_VOUT = 78h
Soft-Start Time Rate LDO5	-	1.8	2.0	2.2	V/ms	(2Ch) LDO5_SR = 0
Soft-Start Time Rate LDO6	-	3.6	4.0	4.4	V/ms	(2Dh) LDO6_SR = 0
Soft-Start Time Rate LDO7	-	3.6	4.0	4.4	V/ms	(2Eh) LDO7_SR = 0
Dropout Voltage LDOx	V_{DROP_LDOx}	-	-	0.1	V	I_{VOUTx} = 50 mA Between PVINx and VOUTx (x: 5 to 7)
Output Discharge Resistance LDOx	R_{DIS_LDOx}	15	55	125	Ω	Between VOUTx and GND I_{VOUTx} = -10 mA (2Ch to 2Eh) LDOx_RDIS = 0 (x: 5 to 7)
UVLO_PVIN5 Threshold Voltage	V_{UVLO_PVIN5}	1.51	1.60	1.69	V	PVIN5: Sweep down (2Ch) LDO5_UVLO_LVL = 1
UVLO_PVIN5 Hysteresis Voltage	$V_{UVLO\_PVIN5\_Hys}$	-	0.04	-	V	PVIN5: Sweep up (2Ch) LDO5_UVLO_LVL = 1
UVLO_PVIN6 Threshold Voltage	V_{UVLO_PVIN6}	2.21	2.30	2.39	V	PVIN6: Sweep down (2Dh) LDO6_UVLO_LVL = 0
UVLO_PVIN6 Hysteresis Voltage	$V_{UVLO\_PVIN6\_Hys}$	-	0.06	-	V	PVIN6: Sweep up (2Dh) LDO6_UVLO_LVL = 0
UVLO_PVIN7 Threshold Voltage	V_{UVLO_PVIN7}	2.21	2.30	2.39	V	PVIN7: Sweep down (2Eh) LDO7_UVLO_LVL = 0
UVLO_PVIN7 Hysteresis Voltage	$V_{UVLO\_PVIN7\_Hys}$	-	0.06	-	V	PVIN7: Sweep up (2Eh) LDO7_UVLO_LVL = 0
OVP Detecting Rate LDOx	-	+17	+20	+23	%	(31h) LDOx_OVP = 11b (x: 5 to 7)
UVP Detecting Voltage LDO5	V_{UVP_LDO5}	0.876	0.960	1.044	V	(25h) LDO5_INI_VOUT = 24h
UVP Detecting Voltage LDO6	V_{UVP_LDO6}	1.825	2.000	2.175	V	(26h) LDO6_INI_VOUT = 58h
UVP Detecting Voltage LDO7	V_{UVP_LDO7}	2.409	2.640	2.871	V	(27h) LDO7_INI_VOUT = 78h
Over Current Protection LDOx	I_{OCPH_LDOx}	300	500	-	mA	(x: 5 to 7)
OVD Detecting Offset Voltage(*1) LDO5	V_{OVD_LDO5}	+25.7	+40.0	+54.3	mV	(36h) LDO5_OVD_UVD = 11b
OVD Detecting Offset Voltage(*1) LDO6	V_{OVD_LDO6}	+52.4	+80.0	+107.6	mV	(36h) LDO6_OVD_UVD = 11b
OVD Detecting Offset Voltage(*1) LDO7	V_{OVD_LDO7}	+52.4	+80.0	+107.6	mV	(36h) LDO7_OVD_UVD = 11b
UVD Detecting Offset Voltage(*1) LDO5	V_{UVD_LDO5}	-54.3	-40.0	-25.7	mV	(36h) LDO5_OVD_UVD = 11b
UVD Detecting Offset Voltage(*1) LDO6	V_{UVD_LDO6}	-107.6	-80.0	-52.4	mV	(36h) LDO6_OVD_UVD = 11b
UVD Detecting Offset Voltage(*1) LDO7	V_{UVD_LDO7}	-107.6	-80.0	-52.4	mV	(36h) LDO7_OVD_UVD = 11b
SHDWN Detecting Voltage LDOx	V_{SHDWN_LDOx}	-	0.1	-	V	(x: 5 to 7)

(*1) Delta against the VOUT voltage including DC accuracy from register setting voltage.

Duty Limitation of Peak Output Current

The duty limitation of the peak output current depends on the continuous output current (Idc) and the duty of peak current. The duty limitation of the peak output current is calculated in the following equation.

For BUCK1 and BUCK2 single mode.
(The duty limitation is 100 % at Ipeak = 2 A.)

$$Duty\ limitation\ of\ the\ peak\ output\ current\ \left(=\frac{Tp}{T}\right) \leq \frac{(2^2 - Idc^2)}{(Ipeak^2 - Idc^2)}$$

where:
Tp is the time width of one peak output current (maximum time of Tp is 10 ms).
T is the one cycle time of the peak output current.
Idc is the continuous output current.
Ipeak is the peak output current. (maximum current of Ipeak is 2.4 A)

For BUCK1 and BUCK2 dual phase mode.
(The duty limitation is 100 % at Ipeak = 4 A.)

$$Duty\ limitation\ of\ the\ peak\ output\ current\ \left(=\frac{Tp}{T}\right) \leq \frac{(4^2 - Idc^2)}{(Ipeak^2 - Idc^2)}$$

where:
Tp is the time width of one peak output current (maximum time of Tp is 10 ms).
T is the one cycle time of the peak output current.
Idc is the continuous output current.
Ipeak is the peak output current. (maximum current of Ipeak is 4.8 A)

For BUCK3 and BUCK4 single phase mode.
(The duty limitation is 100 % at Ipeak = 4 A.)

$$Duty\ limitation\ of\ the\ peak\ output\ current\ \left(=\frac{Tp}{T}\right) \leq \frac{(4^2 - Idc^2)}{(Ipeak^2 - Idc^2)}$$

where:
Tp is the time width of one peak output current (maximum time of Tp is 10 ms).
T is the one cycle time of the peak output current.
Idc is the continuous output current.
Ipeak is the peak output current. (maximum current of Ipeak is 4.8 A)

For BUCK3 and BUCK4 dual phase mode.
(The duty limitation is 100 % at Ipeak = 8 A.)

$$Duty\ limitation\ of\ the\ peak\ output\ current\ \left(=\frac{Tp}{T}\right) \leq \frac{(8^2 - Idc^2)}{(Ipeak^2 - Idc^2)}$$

where:
Tp is the time width of one peak output current (maximum time of Tp is 10 ms).
T is the one cycle time of the peak output current.
Idc is the continuous output current.
Ipeak is the peak output current. (maximum current of Ipeak is 9.6 A)

State Machine

Main State Machine

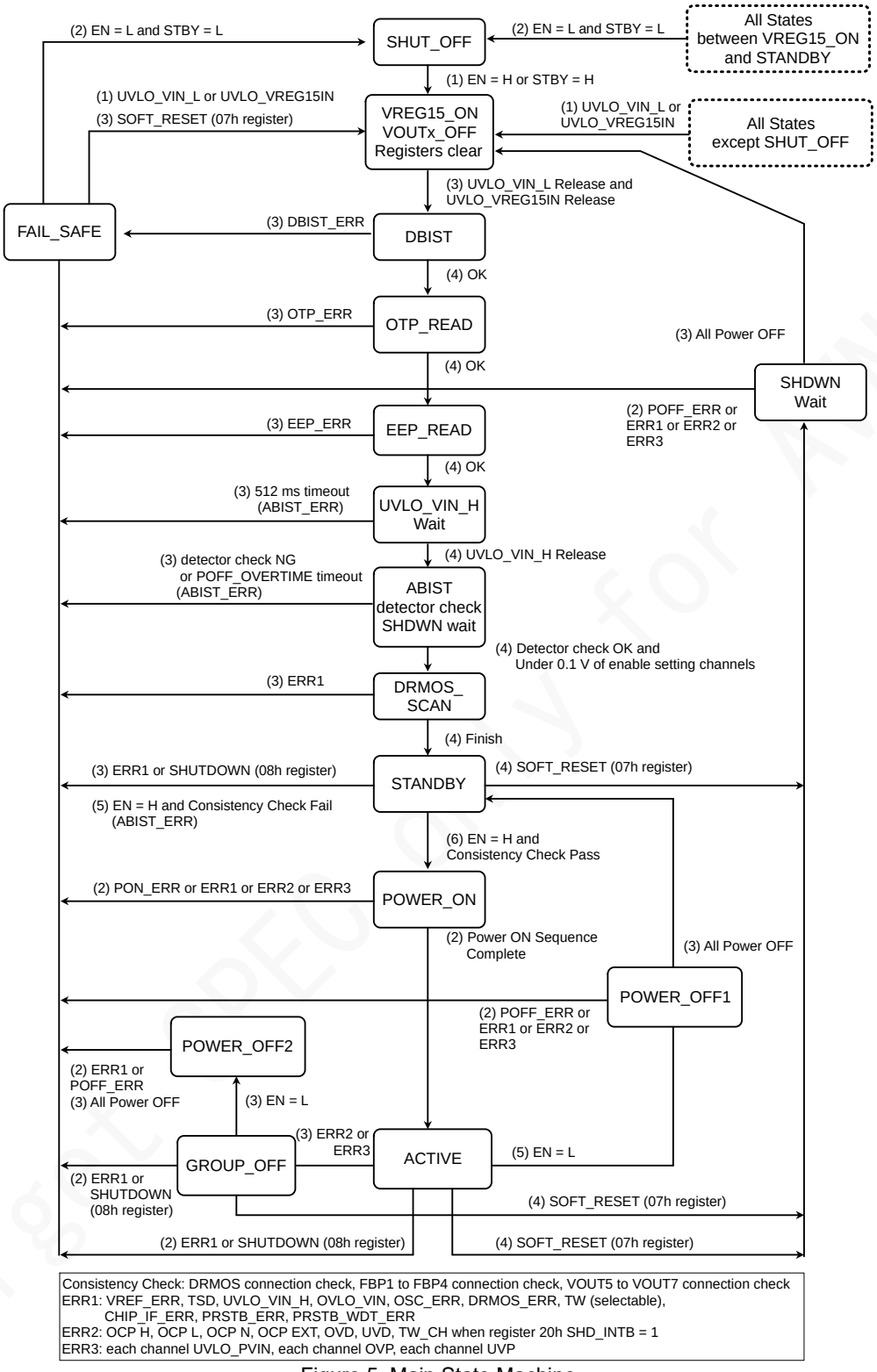


Figure 5. Main State Machine

Block	SHUT_OFF to STANDBY	POWER_ON	ACTIVE	POWER_OFF1, POWER_OFF2	GROUP_OFF	FAIL_SAFE
BUCK1	OFF	Sequential ON by register setting	ON	Sequential OFF by register setting	Group Control by register setting	OFF
BUCK2	OFF		ON			OFF
BUCK3	OFF		ON			OFF
BUCK4	OFF		ON			OFF
LDO5	OFF		ON			OFF
LDO6	OFF		ON			OFF
LDO7	OFF		ON			OFF

State Machine – continued

ADD_EN1 and ADD_EN2 function state machine.

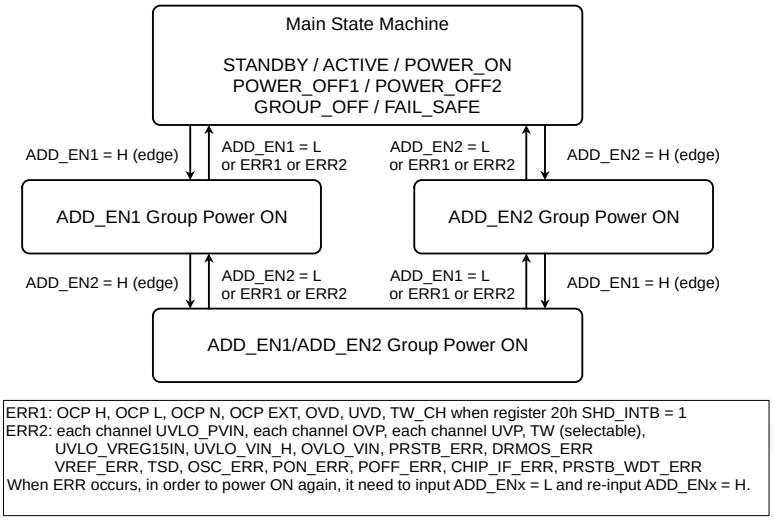


Figure 6. ADD_EN1, ADD_EN2 State Machine

ADD_EN1 or ADD_EN2 channels are controlled without main state machine power sequence.
ADD_EN1 channels have to be set same group in the (1Dh to 20h) XXX_SHD_GROUP register.
ADD_EN2 channels have to be set same group in the (1Dh to 20h) XXX_SHD_GROUP register.
(XXX: BUCK1 to BUCK4, LDO5 to LDO7, and PRSTB)

Sequencer and Chip Combination

General Description

For each power rail, there are two sequence timing registers which are the power-on timing (the XXX_DELAY_PON register) and power-off timing (the XXX_DELAY_POFF register). (XXX: BUCK1 to BUCK4, LDO5 to LDO7, and PRSTB)
The timing can be configured in a wide range, between 2 µs and 136 ms. Refer to register map (Sequence).
All configured times are defined with the transition of the EN signal. Power-on timing is defined as the delay time from the EN signal H assertion, and the power-off timing is defined as the delay time from the EN signal L de-assertion.
When first EN is H asserted before STANDBY state, power-on delay count will start after STANDBY state transition.

Multi PMIC Sequencing

If multiple PMICs will be used in an application, there is the possibility to synchronize the total power sequence.
In this case, one PMIC should be defined as Main-PMIC via the register 03h DEVICE_ID (refer to register map), and it will provide the System Clock. Also other PMICs should be defined as Sub-PMICs via the same register.
The Main-PMIC will provide the System Clock signal to Sub-PMICs IF1_ADDEN1 pin. The power-on and power-off sequence will be controlled via IF1 and IF2. The time that state shift to STANDBY after the internal LDO (VREG15) power-on is maximum 5 ms without EEPROM reading process, and plus maximum 3 ms x number of multi with EEPROM reading process. Note that these times do not include the BIST time of Driver MOS. In case of Driver MOS using, maximum 3.5 ms is added. Even if 2 pcs of DRMOS using, the time is same. In case of Driver MOS not using, maximum 1 ms is added. When first EN is H asserted before STANDBY state, power-on delay count will start after STANDBY state transition.

Chip Combination

BD96801Qxx-C and BD96802Qxx-C can be connected via the IF1_ADDEN1/IF2 pins.
The combination is set by the OTP register 03h SYSTEM_NUMBER.
And Main-PMIC or Sub-PMIC is set by DEVICE_ID.
The combination is shown in below table.

Table 6. Combination

SYSTEM_ NUMBER[7:4]	BD96801Qxx-C		BD96802Qxx-C					
	Main-PMIC0 ID = 0	Sub-PMIC0 ID = 1	Main-PMIC1 ID = 2	Sub-PMIC1 ID = 3	Sub-PMIC2 ID = 4	Sub-PMIC3 ID = 5	Sub-PMIC4 ID = 6	Sub-PMIC5 ID = 7
0	Chip 1	-	-	-	-	-	-	-
1	-	-	Chip 1	-	-	-	-	-
2	Chip 1	-	-	Chip 2	-	-	-	-
3	Chip 1	Chip 2	-	-	-	-	-	-
4	Chip 1	-	-	Chip 2	Chip 3	-	-	-
5	Chip 1	Chip 2	-	Chip 3	-	-	-	-
6	Chip 1	-	-	Chip 2	Chip 3	Chip 4	-	-
7	Chip 1	Chip 2	-	Chip 3	Chip 4	-	-	-
8	Chip 1	-	-	Chip 2	Chip 3	Chip 4	Chip 5	
9	Chip 1	Chip 2	-	Chip 3	Chip 4	Chip 5	-	-
A	Chip 1	-	-	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6
B	Chip 1	Chip 2	-	Chip 3	Chip 4	Chip 5	Chip 6	-

EEPROM Reading

When the extarnal EEPROM which the data is set in is connected via I^{2}C, the data will be automatically read in the EEP_READ state. The EEPROM I^{2}C device address have to be A0/A1 (8bit description write/read mode). And the size of data is 2k bits.
For the SYSTEM_NUMBER is 8 or more, 1 word address 4k or 8k bits EEPROM is needed. The second EEPROM I^{2}C device address have to be A2/A3 (8bit description write/read mode).
The figure below shows the data storage.

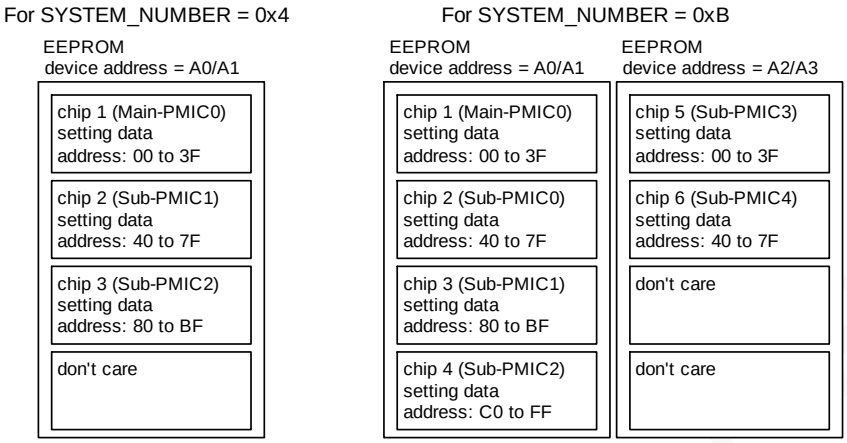
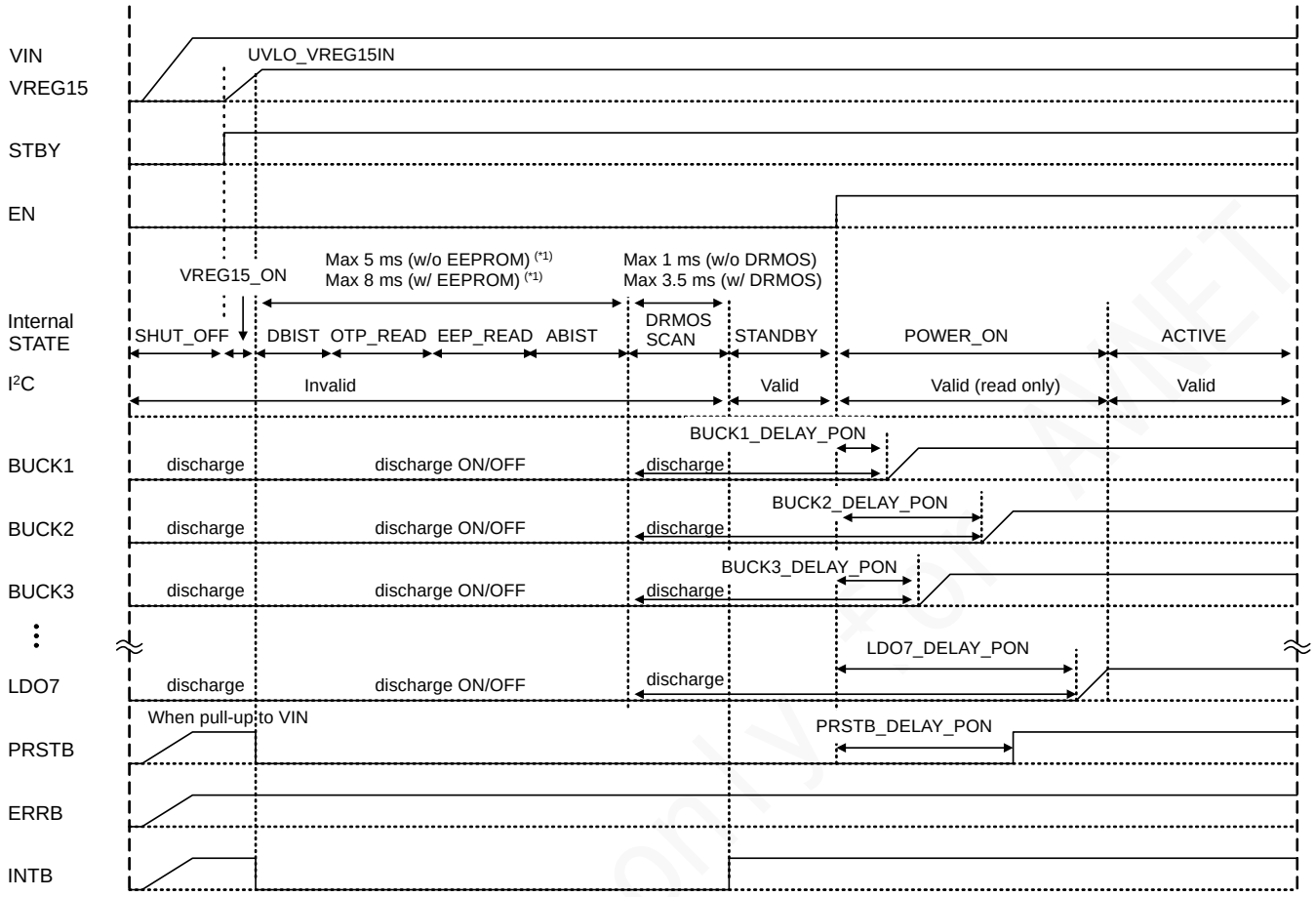


Figure 7. EEPROM Data

Timing Chart

ON Sequence (An example)



(*1) This 5 ms and 8 ms time does not include waiting time. In ABIST state, PMIC waits all channel which is set to enable becomes under 0.1 V. In this time, discharge function is enabled. Discharge resistor is set by register setting. If discharge function setting is OFF, the channel is excluded from under 0.1 V checking.

Figure 8. ON Sequence1

Timing Chart – continued

OFF Sequence EN (An example)

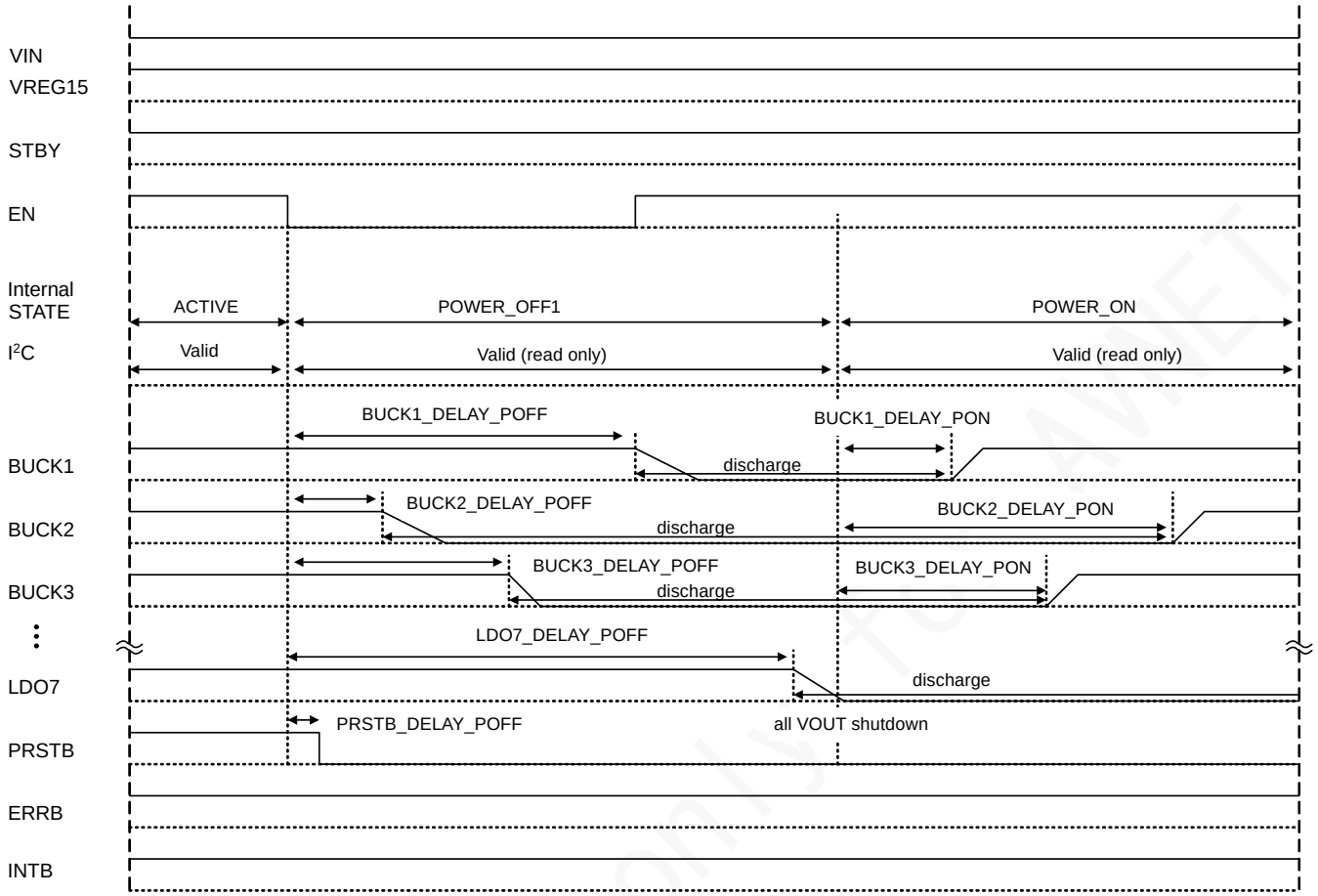


Figure 9. OFF Sequence1

Timing Chart – continued

OFF Sequence with an ERROR (An example)

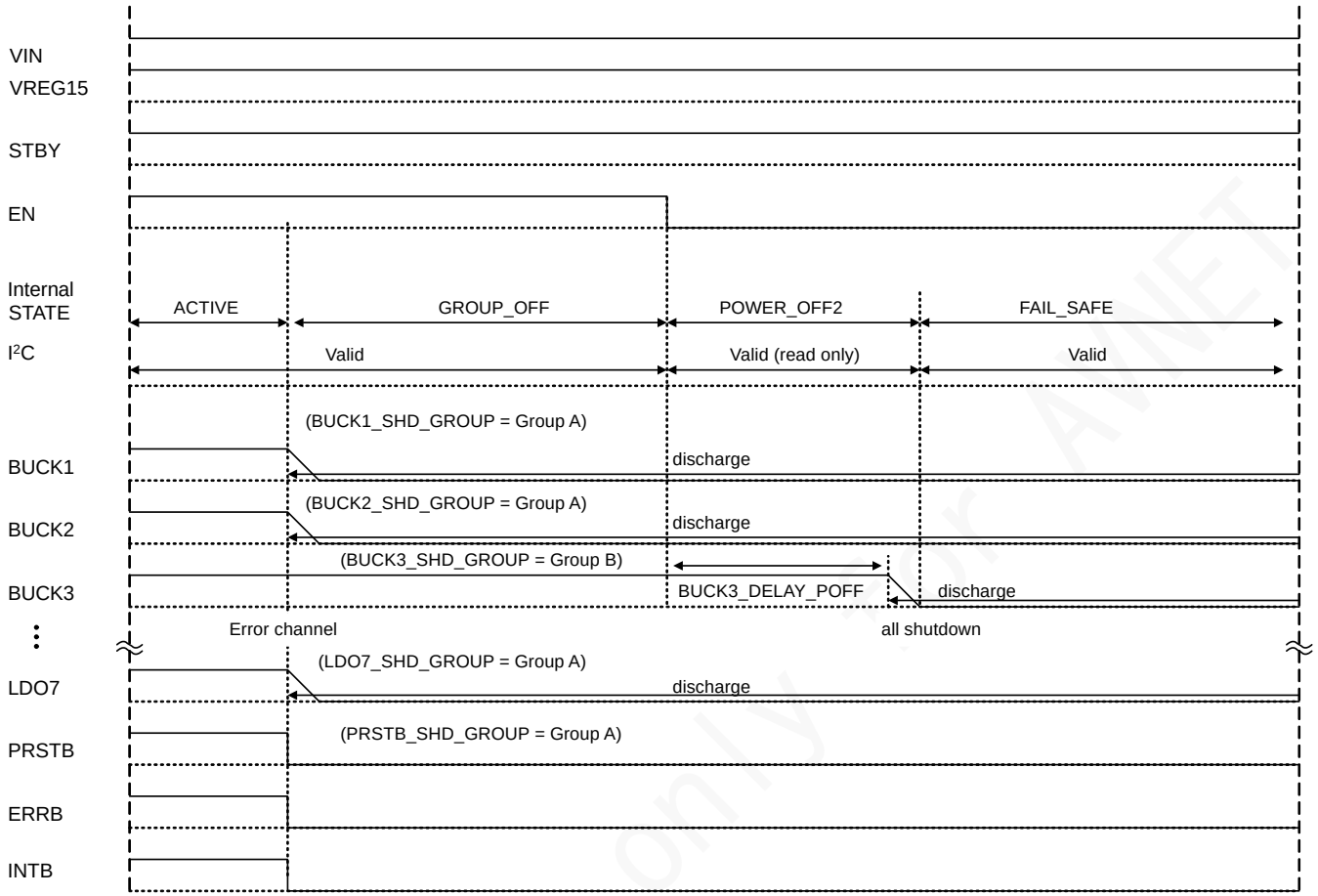


Figure 10. OFF Sequence2

Timing Chart – continued

OFF Sequence with VIN UVLO (An example)

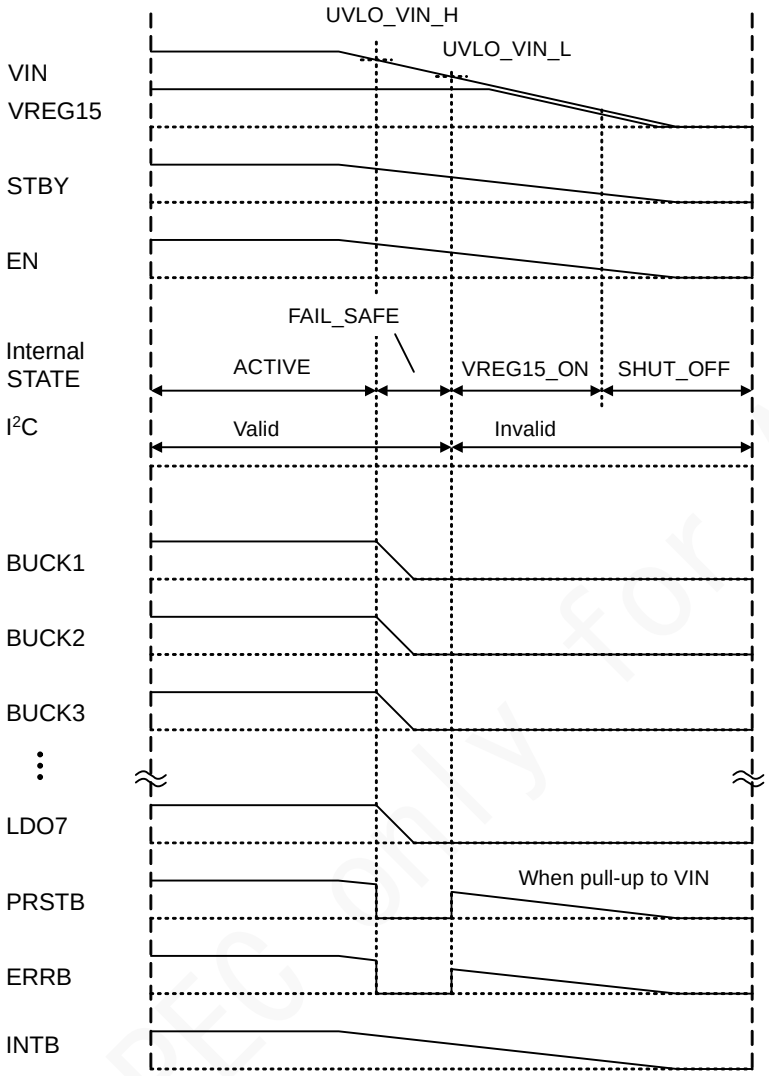
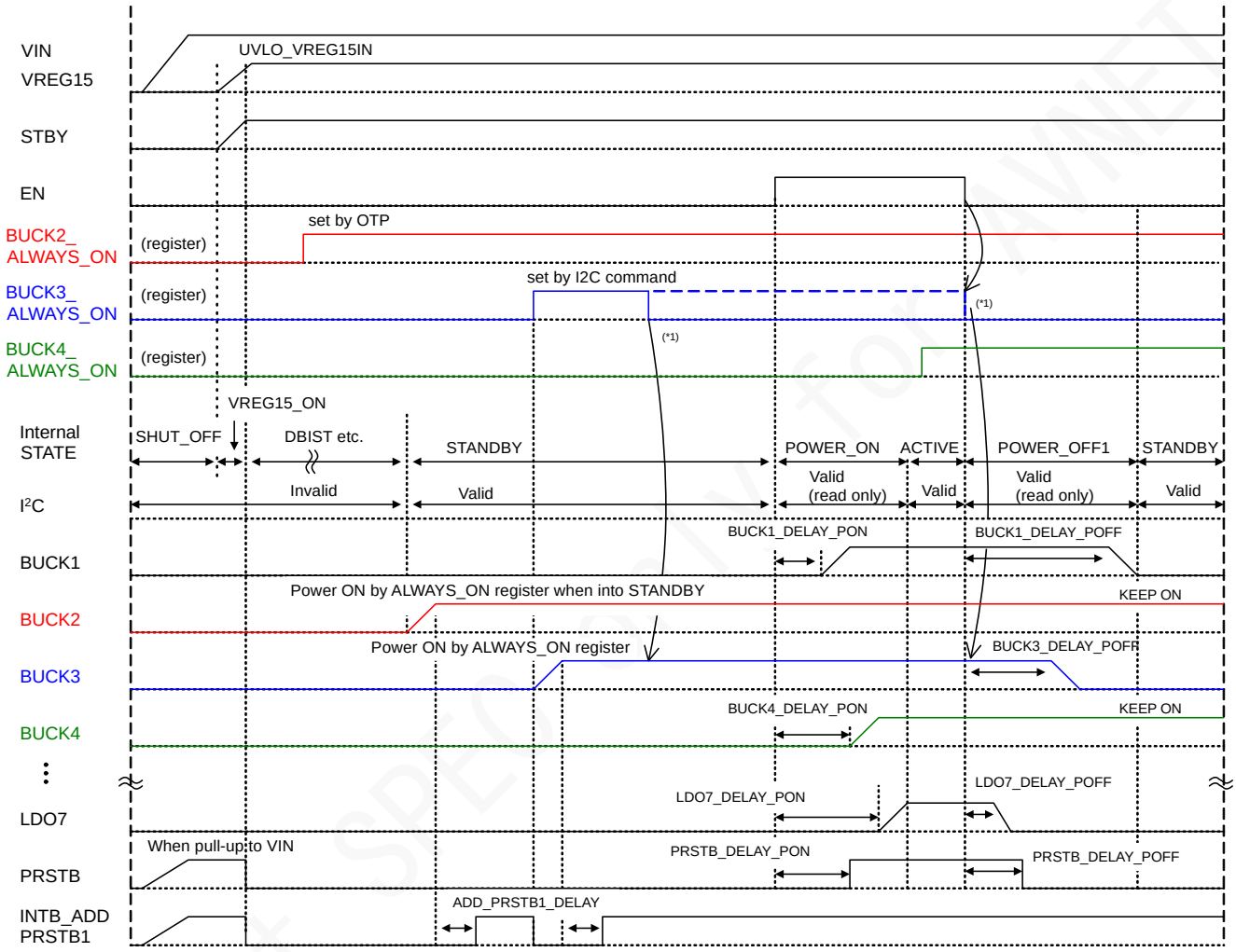


Figure 11. OFF Sequence3

Timing Chart – continued

ALWAYS_ON Power ON/OFF Sequence (An example)

Each channel can power ON by the (3Ch) ALWAYS_ON register.
The register can be set via OTP, EEPROM, or I²C command. About I²C command, it can be set in only STANDBY state or ACTIVE state. When the ALWAYS_ON register be set to 1, the channel power ON in STANDBY state. Even if the register be set to 0 after 1 setting, the channel does not OFF, but controlled by the EN signal in power OFF sequence. When the register be set to 1 in ACTIVE state, the channel does not OFF in power OFF sequence.
Below shows the sequence using the ALWAYS_ON register. As a prerequisite, the (3Dh) ADD_PRSTB1 register is set 01 (ALWAYS_ON channel PRSTB mode).



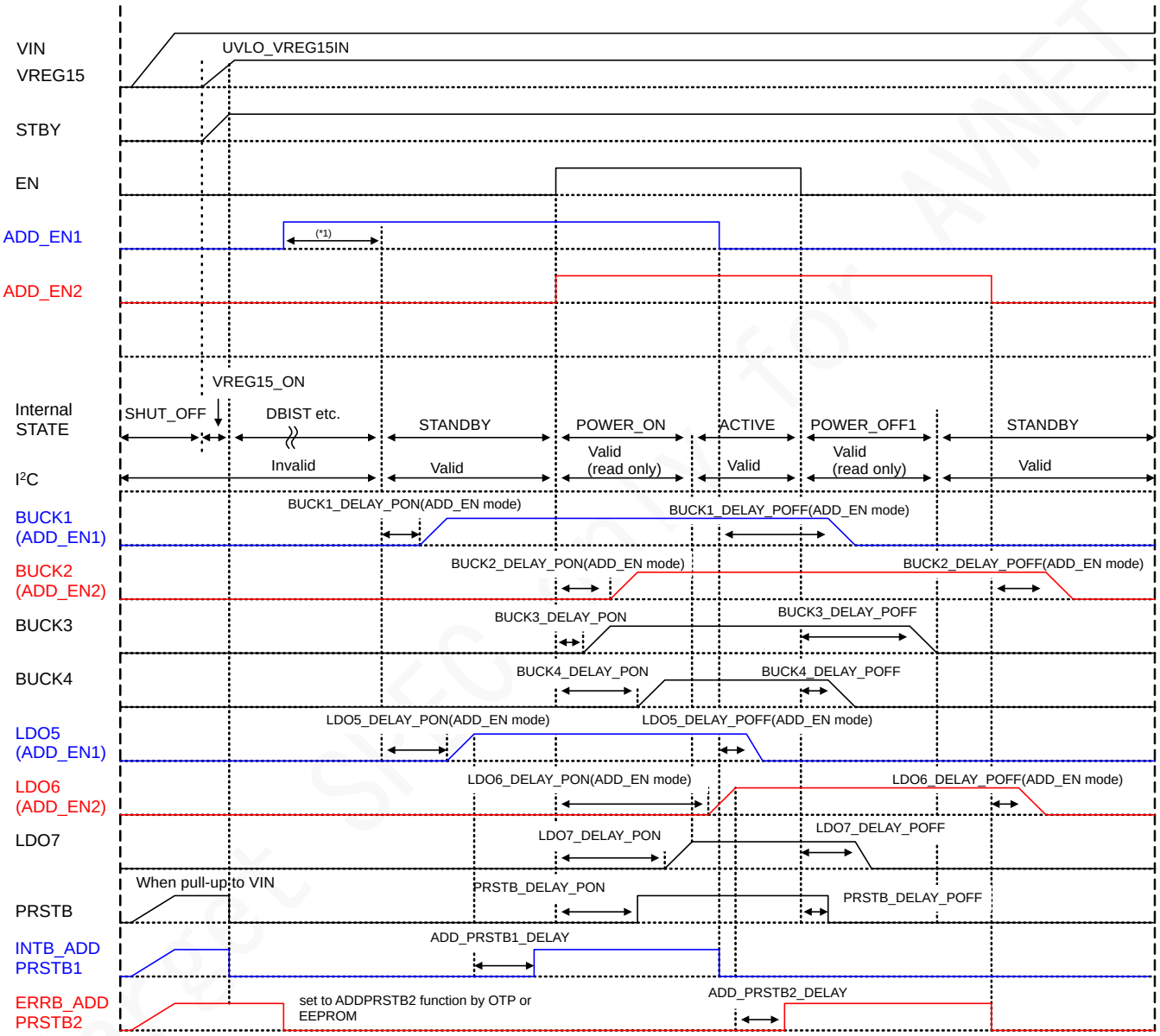
(*1) Even if BUCK3_ALWAYS_ON is set to 0 after 1 setting, BUCK3 does not OFF in this time.
When POWER_OFF1 state, BUCK3 is controlled by the EN signal.

Figure 12. ALWAYS_ON Power ON/OFF Sequence

Timing Chart – continued

ADD_EN Power ON/OFF Sequence (An example)

ADD_EN function can be set by only OTP or EEPROM. It is set by the (3Eh) ADD_EN1 or (3Fh) ADD_EN2 register. When any one of the (3Eh) ADD_EN1 registers is 1, the IF1_ADDEN1 pin functions as the ADD_EN1 function. When any one of the ADD_EN2 registers is 1, the SYNC_ADDEN2 pin functions as the ADD_EN2 function. When ADD_EN1 or ADD_EN2 is active, the DELAY_ON and DELAY_OFF time is ADD_EN mode setting which is not same delay time of basic EN mode.
Below shows the ADD_EN1 and ADD_EN2 sequence. As a prerequisite, BUCK1 and LDO5 are assigned to ADD_EN1, BUCK2 and LDO6 are assigned to ADD_EN2. The ADD_PRSTB1 is related to ADD_EN1 channel and the ADD_PRSTB2 is related to ADD_EN2 channel.



(*1) When the ADD_EN H assertion is earlier than STANDBY state, the ADD_EN channel power ON delay count start after into STANDBY state.

Figure 13. ADD_EN Power ON/OFF Sequence

Register Map

The default value is the value loaded after OTP_READ. OTP/EEP/I²C description in below table.
The registers of OTP = “O” is reflected OTP setting at OTP_READ state.
The registers of EEP = “E” can be overwritten by EEPROM setting.
The registers of I²C = “RW” can be overwritten by I²C command.
The registers of I²C = “RWS” can be overwritten by I²C command in only STANDBY and GROUP_OFF state.
The registers of I²C = “RWSA” can be overwritten by I²C command in only STANDBY, ACTIVE and GROUP_OFF state.
The registers of I²C = “RWSAF” can be overwritten by I²C command in only STANDBY, ACTIVE, GROUP_OFF and FAIL_SAFE state.
The registers of I²C = “RO” is read only.

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
00h	Vendor_ Code	VENDOR[7:0]								-/-/ RO	DBh
01h	Product Code	PRODUCT[7:0]								O/-/ RO	30h
02h	Product Revision	REVISION[7:0]								-/-/ RO	A2h
03h	Device Identification	SYSTEM_NUMBER[3:0]				-	DEVICE_ID[2:0]			O/-/ RO	00h
04h	Write Protect	WRITE_PROTECT[7:0]								-/-/ RW	00h
05h	CRC ON	CRC_ON[7:0]								-/-/ RW	00h
06h	PRSTB_ CONTROL	PRSTB_L_ MASK	-	-	PRSTB_L_ HIST	-	-	-	PRSTB_L	-/-/ RW	01h
07h	SOFT_ RESET	SOFT_RESET[7:0]								-/-/ RWSAF	00h
08h	SHUTDOWN	SHUTDOWN[7:0]								-/-/ RW	00h
09h	SSCG	-	SSCG_WIDTH[2:0]			-	SSCG_FREQ[2:0]			O/E/ RWS	00h
0Ah	MODE_SET	-	-	LDO7_ LDSW	LDO7_ EXTSW	BUCK2_ IntFET	BUCK1_ IntFET	BUCK34_ MULTI	BUCK12_ MULTI	O/E/ RWS	0Ch
0Bh	DISABLE_ SET	-	LDO7_ DISABLE	LDO6_ DISABLE	LDO5_ DISABLE	BUCK4_ DISABLE	BUCK3_ DISABLE	BUCK2_ DISABLE	BUCK1_ DISABLE	O/E/ RWS	00h
0Ch	PRSTB_ WDT/ SW_FREQ	PRSTB_WDT[1:0]		PRSTB_WDT _TO	PRSTB_WDT_TO_SEL[2:0]			SW_FREQ[1:0] (I²C = RWS)		O/E/ RWSA	00h
0Dh	BUCK1_ DELAY_PON	BUCK1_DELAY_PON[7:0]								O/E/ RWS	20h
0Eh	BUCK2_ DELAY_PON	BUCK2_DELAY_PON[7:0]								O/E/ RWS	30h
0Fh	BUCK3_ DELAY_PON	BUCK3_DELAY_PON[7:0]								O/E/ RWS	10h
10h	BUCK4_ DELAY_PON	BUCK4_DELAY_PON[7:0]								O/E/ RWS	70h
11h	LDO5_ DELAY_PON	LDO5_DELAY_PON[7:0]								O/E/ RWS	40h
12h	LDO6_ DELAY_PON	LDO6_DELAY_PON[7:0]								O/E/ RWS	50h
13h	LDO7_ DELAY_PON	LDO7_DELAY_PON[7:0]								O/E/ RWS	60h
14h	PRSTB_ DELAY_PON	PRSTB_DELAY_PON[7:0]								O/E/ RWS	80h
15h	BUCK1_ DELAY_POFF	BUCK1_DELAY_POFF[7:0]								O/E/ RWS	60h
16h	BUCK2_ DELAY_POFF	BUCK2_DELAY_POFF[7:0]								O/E/ RWS	50h
17h	BUCK3_ DELAY_POFF	BUCK3_DELAY_POFF[7:0]								O/E/ RWS	70h

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
18h	BUCK4_ DELAY_POFF	BUCK4_DELAY_POFF[7:0]								O/E/ RWS	10h
19h	LDO5_ DELAY_POFF	LDO5_DELAY_POFF[7:0]								O/E/ RWS	40h
1Ah	LDO6_ DELAY_POFF	LDO6_DELAY_POFF[7:0]								O/E/ RWS	30h
1Bh	LDO7_ DELAY_POFF	LDO7_DELAY_POFF[7:0]								O/E/ RWS	20h
1Ch	PRSTB_ DELAY_POFF	PRSTB_DELAY_POFF[7:0]								O/E/ RWS	00h
1Dh	SHD_ GROUP1	-	BUCK2_SHD_GROUP[2:0]			-	BUCK1_SHD_GROUP[2:0]			O/E/ RWS	00h
1Eh	SHD_ GROUP2	-	BUCK4_SHD_GROUP[2:0]			-	BUCK3_SHD_GROUP[2:0]			O/E/ RWS	00h
1Fh	SHD_ GROUP3	-	LDO6_SHD_GROUP[2:0]			-	LDO5_SHD_GROUP[2:0]			O/E/ RWS	00h
20h	SHD_ GROUP4	SHD_INTB	PRSTB_SHD_GROUP[2:0]			-	LDO7_SHD_GROUP[2:0]			O/E/ RWS	00h
21h	BUCK1_ INI_VOUT	BUCK1_INI_VOUT[7:0]								O/E/ RWS	CEh
22h	BUCK2_ INI_VOUT	BUCK2_INI_VOUT[7:0]								O/E/ RWS	AAh
23h	BUCK3_ INI_VOUT	BUCK3_INI_VOUT[7:0]								O/E/ RWS	64h
24h	BUCK4_ INI_VOUT	BUCK4_INI_VOUT[7:0]								O/E/ RWS	ECh
25h	LDO5_ INI_VOUT	LDO5_INI_VOUT[7:0]								O/E/ RWS	24h
26h	LDO6_ INI_VOUT	LDO6_INI_VOUT[7:0]								O/E/ RWS	58h
27h	LDO7_ INI_VOUT	LDO7_INI_VOUT[7:0]								O/E/ RWS	78h
28h	BUCK1_ VOUT	BUCK1_SR[1:0]		-	BUCK1_TUNE[4:0]					O/E/ RW	40h
29h	BUCK2_ VOUT	BUCK2_SR[1:0]		-	BUCK2_TUNE[4:0]					O/E/ RW	40h
2Ah	BUCK3_ VOUT	BUCK3_SR[1:0]		-	BUCK3_TUNE[4:0]					O/E/ RW	40h
2Bh	BUCK4_ VOUT	BUCK4_SR[1:0]		-	BUCK4_TUNE[4:0]					O/E/ RW	40h
2Ch	LDO5_ VOUT	LDO5_RDIS	LDO5_SR	-	LDO5_UVLO_ LVL	-	LDO5_MODE[1:0] (writeable in STANDBY)		LDO5_VOL_ LVL	O/E/ RW	10h
2Dh	LDO6_ VOUT	LDO6_RDIS	LDO6_SR	-	LDO6_UVLO_ LVL	-	LDO6_MODE[1:0] (writeable in STANDBY)		LDO6_VOL_ LVL	O/E/ RW	00h
2Eh	LDO7_ VOUT	LDO7_RDIS	LDO7_SR	-	LDO7_UVLO_ LVL	-	LDO7_MODE[1:0] (writeable in STANDBY)		LDO7_VOL_ LVL	O/E/ RW	00h
2Fh	DISCHG	BUCK4_RDIS[1:0]		BUCK3_RDIS[1:0]		BUCK2_RDIS[1:0]		BUCK1_RDIS[1:0]		O/E/ RW	65h
30h	OVP1	BUCK4_OVP[1:0]		BUCK3_OVP[1:0]		BUCK2_OVP[1:0]		BUCK1_OVP[1:0]		O/E/ RWS	FFh
31h	OVP2	-	-	LDO7_OVP[1:0]		LDO6_OVP[1:0]		LDO5_OVP[1:0]		O/E/ RWS	3Fh
32h	INTR_ OCPH	BUCK2_EXTR_OCP[1:0]		BUCK2_INTR_OCPH[1:0]		BUCK1_EXTR_OCP[1:0]		BUCK1_INTR_OCPH[1:0]		O/E/ RWS	ABh
33h	OCPH1	-	-	BUCK4_OCPH[1:0]		-	-	BUCK3_OCPH[1:0]		O/E/ RWS	23h
34h	-	-	-	-	-	-	-	-	-	-	2Ah
35h	OVD_UVD1	BUCK4_OVD_UVD[1:0]		BUCK3_OVD_UVD[1:0]		BUCK2_OVD_UVD[1:0]		BUCK1_OVD_UVD[1:0]		O/E/ RWS	FFh

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
36h	OVD_UVD2	-	-	LDO7_OVD_UVD[1:0]		LDO6_OVD_UVD[1:0]		LDO5_OVD_UVD[1:0]		O/E/ RWS	3Fh
37h	LDSW_ UVD_UVP	-	UVP_LDSW[2:0]			-	UVD_LDSW[2:0]			O/E/ RWS	42h
38h	MASK_ CNT1	OVD_MASK_TIME[3:0]				UVD_MASK_TIME[3:0]				O/E/ RWS	22h
39h	MASK_ CNT2	PRSTB_ERR_ OFF	CHIP_IF_ SHD_OFF	-	-	TW_MASK_TIME[3:0]				O/E/ RWS	82h
3Ah	POFF_ OVERTIME	-	PON_OVERTIME[2:0]			-	POFF_OVERTIME[2:0]			O/E/ RWS	11h
3Bh	PIN BIST	EN_STAT (read only)	EN_CTRL_SEL	EN_CTRL_ON	INTB_ MANUAL	PRSTB_ MANUAL	PRSTB_ MANUAL_ MASK	-	BIST_ON_ DEMAND	-/-/ RW	18h
3Ch	ALWAYS_ ON	PRSTB_ ALWAYS_ON	LDO7_ ALWAYS_ ON	LDO6_ ALWAYS_ ON	LDO5_ ALWAYS_ ON	BUCK4_ ALWAYS_ ON	BUCK3_ ALWAYS_ ON	BUCK2_ ALWAYS_ ON	BUCK1_ ALWAYS_ ON	O/E/ RWSA	00h
3Dh	ADD_ PRSTB	ADD_PRSTB2_DELAY[1:0]		ADD_PRSTB2[1:0]		ADD_PRSTB1_ DELAY[1:0]		ADD_PRSTB1[1:0]		O/E/ RO	00h
3Eh	ADD_EN1	PRSTB_ ADD_EN1	LDO7_ ADD_EN1	LDO6_ ADD_EN1	LDO5_ ADD_EN1	BUCK4_ ADD_EN1	BUCK3_ ADD_EN1	BUCK2_ ADD_EN1	BUCK1_ ADD_EN1	O/E/ RO	00h
3Fh	ADD_EN2	PRSTB_ ADD_EN2	LDO7_ ADD_EN2	LDO6_ ADD_EN2	LDO5_ ADD_EN2	BUCK4_ ADD_EN2	BUCK3_ ADD_EN2	BUCK2_ ADD_EN2	BUCK1_ ADD_EN2	O/E/ RO	00h
40h	WDT_SET1	-	FAST_TO[2:0]			-	-	RATIO_TO[1:0]		-/-/ RW	02h
41h	WDT_SET2	-	-	-	WDT_ SLOWMD	WDT_ PRSTB_ INTB	WDT_TYPE	WDT_EN[1:0]		-/-/ RW	00h
42h	WDT_SET3	-	-	-	-	-	-	-	WDT_IFRST	-/-/ RW	00h
43h	WDT_ FCSET	WDT_FC[3:0] (read only)				-	-	WDT_FCSET[1:0]		-/-/ RW	02h
44h	WDT_QA_ SEED	-	-	-	WDT_SEED[4:0]					-/-/ RW	00h
45h	WDT_QA_QCF G	-	-	-	WDT_QCFG[4:0]					-/-/ RW	00h
46h	WDT_QUESTI ON	-	-	-	WDT_Q[4:0]					-/-/ RO	00h
47h	WDT_ANSWE R	WDT_A[7:0]								-/-/ RW	00h
48h	WDT_ANSWE R_TYPE	-	-	-	-	-	-	WDT_ANSTYPE[1:0]		-/-/ RW	00h
49h	WDT_FLAG_ CLEAR	-	-	-	-	-	-	WDT_FC_ CLEAR	WDT_FLAG_ CLEAR	-/-/ RW	00h
4Ah	WDT_STAT	-	-	ST_WDT_ ANSNG	ST_WDT_ SLOW	ST_WDT_ FAST	ST_WDT_ OPEN	ST_WDT_ ERR	ST_WDT_ BE_DET	-/-/ RO	00h
4Bh	-	-	-	-	-	-	-	-	-	-	-
4Ch	INTB_GPO/ ERRB_GPO	-	-	-	ERRB_GPO	-	-	-	INTB_GPO	-/-/ RW	00h
4Dh	-	-	-	-	-	-	-	-	-	-	-
4Eh	-	-	-	-	-	-	-	-	-	-	-
4Fh	INTERNAL_ STATE	-	-	-	-	INTERNAL_STATE[3:0]				-/-/ RO	00h
50h	STATUS_ CHIP_ERRB	SUB_ PMIC5_ STAT	SUB_ PMIC4_ STAT	SUB_ PMIC3_ STAT	SUB_ PMIC2_ STAT	SUB_ PMIC1_ STAT	MAIN_ PMIC1_ STAT	SUB_ PMIC0_ STAT	MAIN_ PMIC0_ STAT	-/-/ RW	00h
51h	STATUS_ PART_ INTB_ERRB	LDO7_ STAT	LDO6_ STAT	LDO5_ STAT	BUCK4_ STAT	BUCK3_ STAT	BUCK2_ STAT	BUCK1_ STAT	SYSTEM_ STAT	-/-/ RO	00h
52h	STATUS_ SYSTEM_ ERRB_1	SUB_PMIC_ ERR_STAT	DRMOS2_ ERR_STAT	DRMOS1_ ERR_STAT	PRSTB_ ERR_STAT	ABIST_ ERR_STAT	EEP_ ERR_STAT	DBIST_ ERR_STAT	OTP_ ERR_STAT	-/-/ RW	00h
53h	STATUS_ SYSTEM_ ERRB_2	CMD_SHDN_ STAT	POFF_ERR_ STAT	PON_ERR_ STAT	OSC_ERR_ STAT	OVLO_VIN_ STAT	UVLO_VIN_ STAT	TSD_STAT	VREF_ERR_ STAT	-/-/ RW	00h
54h	STATUS_ SYSTEM_ ERRB_3	SYS_INT_ SHD	-	-	-	CHIP_IF_ ERR_STAT	-	-	PRSTB_WDT_ ERR_STAT	-/-/ RW	00h

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
55h	STATUS_ BUCK1_ ERRB	BUCK1_INT_ SHD	-	-	-	-	BUCK1_ UVP_STAT	BUCK1_ OVP_STAT	UVLO_ PVIN1_STAT	-/-/ RW	00h
56h	STATUS_ BUCK2_ ERRB	BUCK2_INT_ SHD	-	-	-	-	BUCK2_ UVP_ STAT	BUCK2_ OVP_ STAT	UVLO_ PVIN2_STAT	-/-/ RW	00h
57h	STATUS_ BUCK3_ ERRB	BUCK3_INT_ SHD	-	-	-	-	BUCK3_ UVP_ STAT	BUCK3_ OVP_ STAT	UVLO_ PVIN3_STAT	-/-/ RW	00h
58h	STATUS_ BUCK4_ ERRB	BUCK4_INT_ SHD	-	-	-	-	BUCK4_ UVP_ STAT	BUCK4_ OVP_ STAT	UVLO_ PVIN4_STAT	-/-/ RW	00h
59h	STATUS_ LDO5_ ERRB	LDO5_INT_ SHD	-	-	-	-	LDO5_ UVP_ STAT	LDO5_ OVP_ STAT	UVLO_ PVIN5_STAT	-/-/ RW	00h
5Ah	STATUS_ LDO6_ ERRB	LDO6_INT_ SHD	-	-	-	-	LDO6_ UVP_ STAT	LDO6_ OVP_ STAT	UVLO_ PVIN6_STAT	-/-/ RW	00h
5Bh	STATUS_ LDO7_ ERRB	LDO7_INT_ SHD	-	-	-	-	LDO7_ LDSW7_UVP_ STAT	LDO7_ OVP_ STAT	UVLO_ PVIN7_STAT	-/-/ RW	00h
5Ch	STATUS_ SYSTEM_ INTB	-	-	-	-	CHIP_IF_ INT_ STAT	I2C_INT_ STAT	WDT_ INT_STAT	TW_STAT	-/-/ RW	00h
5Dh	STATUS_ BUCK1_ INTB	-	-	BUCK1_TW_ CH_STAT	BUCK1_UVD_ STAT	BUCK1_ OVD_ STAT	BUCK1_ OCPN_OCPEX T_STAT	BUCK1_ OCPL_ STAT	BUCK1_ OCPH_ STAT	-/-/ RW	00h
5Eh	STATUS_ BUCK2_ INTB	-	-	BUCK2_TW_ CH_STAT	BUCK2_UVD_ STAT	BUCK2_ OVD_ STAT	BUCK2_ OCPN_OCPEX T_STAT	BUCK2_ OCPL_ STAT	BUCK2_ OCPH_ STAT	-/-/ RW	00h
5Fh	STATUS_ BUCK3_ INTB	-	-	BUCK3_TW_ CH_STAT	BUCK3_UVD_ STAT	BUCK3_ OVD_ STAT	BUCK3_ OCPN_ STAT	BUCK3_ OCPL_ STAT	BUCK3_ OCPH_ STAT	-/-/ RW	00h
60h	STATUS_ BUCK4_ INTB	-	-	BUCK4_TW_ CH_STAT	BUCK4_UVD_ STAT	BUCK4_ OVD_ STAT	BUCK4_ OCPN_ STAT	BUCK4_ OCPL_ STAT	BUCK4_ OCPH_ STAT	-/-/ RW	00h
61h	STATUS_ LDO5_ INTB	-	-	-	LDO5_UVD_ STAT	LDO5_ OVD_ STAT	-	-	LDO5_ OCPH_ STAT	-/-/ RW	00h
62h	STATUS_ LDO6_ INTB	-	-	-	LDO6_UVD_ STAT	LDO6_ OVD_ STAT	-	-	LDO6_ OCPH_ STAT	-/-/ RW	00h
63h	STATUS_ LDO7_ INTB	-	-	-	LDO7_ LDSW7_ UVD_STAT	LDO7_ OVD_ STAT	-	-	LDO7_ OCPH_ STAT	-/-/ RW	00h
64h	-	-	-	-	-	-	-	-	-	-	-
65h	-	-	-	-	-	-	-	-	-	-	-
66h	-	-	-	-	-	-	-	-	-	-	-
67h	-	-	-	-	-	-	-	-	-	-	-
68h	-	-	-	-	-	-	-	-	-	-	-
69h	MASK_ SYSTEM_ ERRB_1	SUB_PMIC_ ERR_MASK	DRMOS2_ ERR_MASK	DRMOS1_ ERR_MASK	PRSTB_ERR_ MASK	ABIST_ERR_ MASK	EEP_ERR_ MASK	DBIST_ ERR_ MASK	OTP_ERR_ MASK	-/-/ RW	00h
6Ah	MASK_ SYSTEM_ ERRB_2	CMD_SHDN_ MASK	POFF_ ERR_MASK	PON_ ERR_MASK	OSC_ ERR_MASK	OVLO_ VIN_ MASK	UVLO_VIN_ MASK	TSD_ MASK	VREF_ERR_ MASK	-/-/ RW	00h
6Bh	MASK_ SYSTEM_ ERRB_3	SYS_INT_ SHD_MASK	-	-	-	CHIP_IF_ ERR_ MASK	-	-	PRSTB_WDT_ ERR_MASK	-/-/ RW	00h
6Ch	MASK_ BUCK1_ ERRB	BUCK1_INT_ SHD_MASK	-	-	-	-	BUCK1_ UVP_ MASK	BUCK1_ OVP_ MASK	UVLO_ PVIN1_STAT_ MASK	-/-/ RW	00h
6Dh	MASK_ BUCK2 _ERRB	BUCK2_INT_ SHD_MASK	-	-	-	-	BUCK2_ UVP_ MASK	BUCK2_ OVP_ MASK	UVLO_ PVIN2_STAT_ MASK	-/-/ RW	00h
6Eh	MASK_ BUCK3_ ERRB	BUCK3_INT_ SHD_MASK	-	-	-	-	BUCK3_ UVP_ MASK	BUCK3_ OVP_ MASK	UVLO_ PVIN3_STAT_ MASK	-/-/ RW	00h
6Fh	MASK_ BUCK4_ ERRB	BUCK4_INT_ SHD_MASK	-	-	-	-	BUCK4_ UVP_ MASK	BUCK4_ OVP_ MASK	UVLO_ PVIN4_STAT_ MASK	-/-/ RW	00h
70h	MASK_ LDO5_ ERRB	LDO5_INT_ SHD_MASK	-	-	-	-	LDO5_ UVP_ MASK	LDO5_ OVP_ MASK	UVLO_ PVIN5_STAT_ MASK	-/-/ RW	00h
71h	MASK_ LDO6_ ERRB	LDO6_INT_ SHD_MASK	-	-	-	-	LDO6_UVP_ MASK	LDO6_ OVP_ MASK	UVLO_ PVIN6_STAT_ MASK	-/-/ RW	00h
72h	MASK_ LDO7_ ERRB	LDO7_INT_ SHD_MASK	-	-	-	-	LDO7_ LDSW7_UVP_ MASK	LDO7_ OVP_ MASK	UVLO_ PVIN7_STAT_ MASK	-/-/ RW	00h
73h	MASK_ SYSTEM_ INTB	-	-	-	-	CHIP_IF_ INT_ MASK	I2C_INT_ MASK	WDT_ INT_ MASK	TW_MASK	-/-/ RW	00h
74h	MASK_ BUCK1_ INTB	-	-	BUCK1_TW_ CH_MASK	BUCK1_UVD_ MASK	BUCK1_ OVD_ MASK	BUCK1_ OCPN_ OCPEXT MASK	BUCK1_ OCPL_ MASK	BUCK1_ OCPH_ MASK	-/-/ RW	00h

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
75h	MASK_ BUCK2_ INTB	-	-	BUCK2_TW_ CH_MASK	BUCK2_UVD_ MASK	BUCK2_ OVD_ MASK	BUCK2_ OCPN_ OCPEXT_ MASK	BUCK2_ OCPL_ MASK	BUCK2_ OCPH_ MASK	-/-/ RW	00h
76h	MASK_ BUCK3_ INTB	-	-	BUCK3_TW_ CH_MASK	BUCK3_UVD_ MASK	BUCK3_ OVD_ MASK	BUCK3_ OCPN_ MASK	BUCK3_ OCPL_ MASK	BUCK3_ OCPH_ MASK	-/-/ RW	00h
77h	MASK_ BUCK4_ INTB	-	-	BUCK4_TW_ CH_MASK	BUCK4_UVD_ MASK	BUCK4_ OVD_ MASK	BUCK4_ OCPN_ MASK	BUCK4_ OCPL_ MASK	BUCK4_ OCPH_ MASK	-/-/ RW	00h
78h	MASK_ LDO5_INTB	-	-	-	LDO5_UVD_ MASK	LDO5_ OVD_ MASK	-	-	LDO5_ OCPH_ MASK	-/-/ RW	00h
79h	MASK_ LDO6_INTB	-	-	-	LDO6_UVD_ MASK	LDO6_ OVD_ MASK	-	-	LDO6_ OCPH_ MASK	-/-/ RW	00h
7Ah	MASK_ LDO7_INTB	-	-	-	LDO7_ LDSW7_ UVD_ MASK	LDO7_ OVD_ MASK	-	-	LDO7_ OCPH_ MASK	-/-/ RW	00h

Register Map – continued

The default value is the value loaded after OTP_READ. OTP/EEP/I²C description in below table.
The registers of OTP = “O” is reflected OTP setting at OTP_READ state.
The registers of EEP = “E” can be overwritten by EEPROM setting.
The registers of I²C = “RW” can be overwritten by I²C command.
The registers of I²C = “RWS” can be overwritten by I²C command in only STANDBY and GROUP_OFF state.
The registers of I²C = “RWSA” can be overwritten by I²C command in only STANDBY, ACTIVE, and GROUP_OFF state.
The registers of I²C = “RWSAF” can be overwritten by I²C command in only STANDBY, ACTIVE, GROUP_OFF, and FAIL_SAFE state.
The registers of I²C = “RO” is read only.

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
00h	Vendor_ Code	VENDOR[7:0]								-/-/ RO	DBh
01h	Product Code	PRODUCT[7:0]								O/-/ RO	30h
02h	Product Revision	REVISION[7:0]								-/-/ RO	A2h
03h	Device Identification	SYSTEM_NUMBER[3:0]				-	DEVICE_ID[2:0]			O/-/ RO	00h

VENDOR To identify ROHM vendor ID.
PRODUCT To identify product ID. It be set by OTP.
REVISION To identify revision ID.
SYSTEM_NUMBER Combination setting by OTP, refer to Table 6.
DEVICE_ID Combination setting by OTP, refer to Table 6.

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
04h	Write Protect	WRITE_PROTECT[7:0]								-/-/ RW	00h

WRITE_PROTECT All registers are locked. When write 0x9D, registers become writeable.
0x9D Writeable
Other Locked

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
05h	CRC ON	CRC_ON[7:0]								-/-/ RW	00h

CRC_ON
0xD6 I²C Data CRC mode
0xD9 I²C ALL CRC mode
Other Normal mode (without CRC)

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
06h	PRSTB_ CONTROL	PRSTB_L_ MASK	-	-	PRSTB_L_ HIST	-	-	-	PRSTB_L	-/-/ RW	01h

PRSTB_L_MASK In (39h) PRSTB_ERR_OFF = 0 (PRSTB_ERR detection is active), when PRSTB_L be set, PRSTB_ERR will be detected.
This mask has to be set to prevent this error.
0 Mask Disable
1 PRSTB_ERR Mask Enable

PRSTB_L_HIST Software RESET history
0 No detection of PRSTB_L = 0
1 When PRSTB_L = 0, latched to 1. When write 1, the bit is cleared.

PRSTB_L Software RESET
0 When “0” is written, PRSTB becomes L between 5 ms. After finish, it returns “1” automatically.
1 Normal working

Register Map – continued

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
07h	SOFT_ RESET	SOFT_RESET[7:0]								-/-/ RWSAF	00h
08h	SHUTDOWN	SHUTDOWN[7:0]								-/-/ RW	00h

SOFT_RESET 0x35 Software Reset. Refer to Figure 5.
Other No Software Reset

SHUTDOWN 0x57 Software Shutdown. Refer to Figure 5.
Other No Software Shutdown

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
09h	SSCG	-	SSCG_WIDTH[2:0]			-	SSCG_FREQ[2:0]			O/E/ RWS	00h

SSCG_WIDTH Spread Spectrum Clock Generator WIDTH
000 0.4 %
001 2 %
010 4 %
011 6 %
100 8 %
101 10 %
110,111 Reserved

SSCG_FREQ Spread Spectrum Clock Generator Frequency
000 SSCG OFF
001 0.1 kHz
010 0.5 kHz
011 1.0 kHz
100 2.5 kHz
101 5.0 kHz
110,111 Reserved

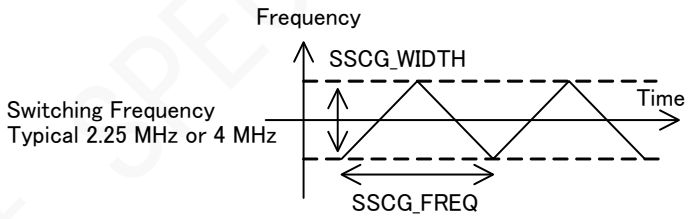


Figure 14. SSCG

Register Map – continued

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
0Ah	MODE_SET	-	-	LDO7_ LDSW	LDO7_ EXTSW	BUCK2_ IntFET	BUCK1_ IntFET	BUCK34_ MULTI	BUCK12_ MULTI	O/E/ RWS	0Ch

Setting for BUCK / LDO mode.

LDO7_LDSW
- 0 LDO mode
- 1 Load SW mode

LDO7_EXTSW When LDO7_LDSW = 0, this setting is ignored. In LDO mode, Internal only.
- 0 Internal FET mode
- 1 External FET mode

BUCK1_IntFET / BUCK2_IntFET
- 0 Driver MOS mode
- 1 Internal FET mode

BUCK12_MULTI / BUCK34_MULTI
- 0 Single (1 phase)
- 1 Dual (2 phases)

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
0Bh	DISABLE_ SET	-	LDO7_ DISABLE	LDO6_ DISABLE	LDO5_ DISABLE	BUCK4_ DISABLE	BUCK3_ DISABLE	BUCK2_ DISABLE	BUCK1_ DISABLE	O/E/ RWS	00h

Enable / Disable setting for each channel.
- 0 Enable
- 1 Disable

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
0Ch	PRSTB_ WDT/ SW_FREQ	PRSTB_WDT[1:0]		PRSTB_WDT_ TO	PRSTB_WDT_TO_SEL[2:0]			SW_FREQ[1:0] (I²C = RWS)		O/E/ RWSA	00h

PRSTB_WDT Selection of PRSTB which is used for timeout.
And setting of association of reset signal to be output when WDT_ERR occurs.
When (41h) WDT_PRSTB_INTB = 1, this PRSTB will be L asserted.
- 00 PRSTB
- 01 ADD_PRSTB1
- 10,11 ADD_PRSTB2

PRSTB_WDT_TO Timeout setting of WDT enable from PRSTB H de-assertion.
If a control device cannot control WDT enable with in timeout time from PRSTB H de-assertion, PRSTB_WDT_ERR will be detected.
- 0 OFF
- 1 ON

PRSTB_WDT_TO_SEL The time setting of timeout from PRSTB H de-assertion.
- 000 100 ms
- 001 200 ms
- 010 400 ms
- 011 600 ms
- 100 800 ms
- 101 1,000 ms
- 110 1,200 ms
- 111 1,400 ms

SW_FREQ Switching frequency for BUCK
- 00 2.25 MHz
- 01 4 MHz
- 10,11 Prohibit

Register Map – continued

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
0Dh	BUCK1_ DELAY_PON	BUCK1_DELAY_PON[7:0]								O/E/ RWS	20h
0Eh	BUCK2_ DELAY_PON	BUCK2_DELAY_PON[7:0]								O/E/ RWS	30h
0Fh	BUCK3_ DELAY_PON	BUCK3_DELAY_PON[7:0]								O/E/ RWS	10h
10h	BUCK4_ DELAY_PON	BUCK4_DELAY_PON[7:0]								O/E/ RWS	70h
11h	LDO5_ DELAY_PON	LDO5_DELAY_PON[7:0]								O/E/ RWS	40h
12h	LDO6_ DELAY_PON	LDO6_DELAY_PON[7:0]								O/E/ RWS	50h
13h	LDO7_ DELAY_PON	LDO7_DELAY_PON[7:0]								O/E/ RWS	60h
14h	PRSTB_ DELAY_PON	PRSTB_DELAY_PON[7:0]								O/E/ RWS	80h
15h	BUCK1_ DELAY_POFF	BUCK1_DELAY_POFF[7:0]								O/E/ RWS	60h
16h	BUCK2_ DELAY_POFF	BUCK2_DELAY_POFF[7:0]								O/E/ RWS	50h
17h	BUCK3_ DELAY_POFF	BUCK3_DELAY_POFF[7:0]								O/E/ RWS	70h
18h	BUCK4_ DELAY_POFF	BUCK4_DELAY_POFF[7:0]								O/E/ RWS	10h
19h	LDO5_ DELAY_POFF	LDO5_DELAY_POFF[7:0]								O/E/ RWS	40h
1Ah	LDO6_ DELAY_POFF	LDO6_DELAY_POFF[7:0]								O/E/ RWS	30h
1Bh	LDO7_ DELAY_POFF	LDO7_DELAY_POFF[7:0]								O/E/ RWS	20h
1Ch	PRSTB_ DELAY_POFF	PRSTB_DELAY_POFF[7:0]								O/E/ RWS	00h

These registers are shared for basic EN, additional ADD_EN1, and ADD_EN2 power ON/OFF sequence.
When the (3Eh) ADD_EN1 or (3Fh) ADD_EN2 register is set, the channel's delay registers become ADD_EN mode.

In case of EN mode:

Delay time setting from the EN signal for ON sequence or OFF sequence.
The EN pin debounce time typical 10 µs is added to this delay time.

0x00	2 µs
0x01 to 0x80	128 µs to 16.384 ms (128 µs step)
0x80 to 0xA0	16.384 ms to 24.576 ms (256 µs step)
0xA0 to 0xC0	24.576 ms to 40.960 ms (512 µs step)
0xC0 to 0xE0	40.960 ms to 73.728 ms (1.024 ms step)
0xE0 to 0xFF	73.728 ms to 137.216 ms (2.048 ms step)

In case of ADD_EN mode:

Delay time setting from the ADD_EN signal for ON sequence or OFF sequence.
The IF1_ADDEN1 / SYNC_ADDEN2 pin debounce time typical 10 µs is added to this delay time.

Bit[7] to Bit[4]	Ignored
0x0	2 µs
0x1 to 0xF	1.024 ms to 15.360 ms (1.024 ms step)

Register Map – continued

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
1Dh	SHD_ GROUP1	-	BUCK2_SHD_GROUP[2:0]			-	BUCK1_SHD_GROUP[2:0]			O/E/ RWS	00h
1Eh	SHD_ GROUP2	-	BUCK4_SHD_GROUP[2:0]			-	BUCK3_SHD_GROUP[2:0]			O/E/ RWS	00h
1Fh	SHD_ GROUP3	-	LDO6_SHD_GROUP[2:0]			-	LDO5_SHD_GROUP[2:0]			O/E/ RWS	00h
20h	SHD_ GROUP4	SHD_INTB	PRSTB_SHD_GROUP[2:0]			-	LDO7_SHD_GROUP[2:0]			O/E/ RWS	00h

XXX_SHD_GROUP (XXX: BUCK1 to BUCK4, LDO5 to LDO7, and PRSTB)
When the event (refer to Table 4) is detected and error CH becomes OFF,
also other CHs in the same group channels can become OFF by group setting of shutdown group.
0x0 A Group
0x1 B Group
0x2 C Group
0x3 D Group
0x4 E Group
0x5 F Group
0x6 G Group
0x7 H Group (individual shutdown. For example if BUCK1 and BUCK2 are in this group and BUCK1 has an error, BUCK1 will shutdown and BUCK2 will not shutdown.)

SHD_INTB When each interrupt event is detected, it is selectable in either CONTINUE or OFF.
0 CONTINUE, INTB notification only
1 OFF, INTB notification and shutdown

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
21h	BUCK1_ INI_VOUT	BUCK1_INI_VOUT[7:0]								O/E/ RWS	CEh
22h	BUCK2_ INI_VOUT	BUCK2_INI_VOUT[7:0]								O/E/ RWS	AAh
23h	BUCK3_ INI_VOUT	BUCK3_INI_VOUT[7:0]								O/E/ RWS	64h
24h	BUCK4_ INI_VOUT	BUCK4_INI_VOUT[7:0]								O/E/ RWS	ECh

Voltage setting for BUCK
0x00 to 0xC8 0.5 V to 1.5 V (5 mV step)
0xC9 to 0xEC 1.55 V to 3.3 V (50 mV step)
0xED to 0xFF 3.3 V

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
25h	LDO5_ INI_VOUT	LDO5_INI_VOUT[7:0]								O/E/ RWS	24h
26h	LDO6_ INI_VOUT	LDO6_INI_VOUT[7:0]								O/E/ RWS	58h
27h	LDO7_ INI_VOUT	LDO7_INI_VOUT[7:0]								O/E/ RWS	78h

Voltage setting for LDO
0x00 to 0x78 0.3 V to 3.3 V (25 mV step)
0x79 to 0xFF 3.3 V

Register Map – continued

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
28h	BUCK1_VOUT	BUCK1_SR[1:0]		-	BUCK1_TUNE[4:0]					O/E/RW	40h
29h	BUCK2_VOUT	BUCK2_SR[1:0]		-	BUCK2_TUNE[4:0]					O/E/RW	40h
2Ah	BUCK3_VOUT	BUCK3_SR[1:0]		-	BUCK3_TUNE[4:0]					O/E/RW	40h
2Bh	BUCK4_VOUT	BUCK4_SR[1:0]		-	BUCK4_TUNE[4:0]					O/E/RW	40h

BUCK1_SR / BUCK2_SR / BUCK3_SR / BUCK4_SR

Slew rate for boot up and for voltage shift of tuning.

00 1 V/ms
01 5 V/ms
10 10 V/ms
11 20 V/ms

BUCK1_TUNE / BUCK2_TUNE / BUCK3_TUNE / BUCK4_TUNE

Voltage tuning from initial voltage setting.
Even if this setting is changed, OVP threshold is not changed.
There is possibility OVP is detected, when low voltage channel is changed.

0x00 BUCKx_INI_VOUT (x: 1 to 4) +0 mV
0x01 BUCKx_INI_VOUT (x: 1 to 4) +10 mV
…
0x0F BUCKx_INI_VOUT (x: 1 to 4) +150 mV
0x10 BUCKx_INI_VOUT (x: 1 to 4) -150 mV
0x11 BUCKx_INI_VOUT (x: 1 to 4) -140 mV
…
0x1E BUCKx_INI_VOUT (x: 1 to 4) -10 mV
0x1F BUCKx_INI_VOUT (x: 1 to 4) -0 mV

Register Map – continued

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
2Ch	LDO5_ VOUT	LDO5_RDIS	LDO5_SR	-	LDO5_UVLO_ LVL	-	LDO5_MODE[1:0] (writeable in STANDBY)		LDO5_VOL_ LVL	O/E/ RW	10h
2Dh	LDO6_ VOUT	LDO6_RDIS	LDO6_SR	-	LDO6_UVLO_ LVL	-	LDO6_MODE[1:0] (writeable in STANDBY)		LDO6_VOL_ LVL	O/E/ RW	00h
2Eh	LDO7_ VOUT	LDO7_RDIS	LDO7_SR	-	LDO7_UVLO_ LVL	-	LDO7_MODE[1:0] (writeable in STANDBY)		LDO7_VOL_ LVL	O/E/ RW	00h

LDO5_RDIS / LDO6_RDIS / LDO7_RDIS
Discharge resistance setting
0 55 Ω
1 Disable

LDO5_SR / LDO6_SR / LDO7_SR
Slew rate setting for boot up and voltage shift.
0 Slew rate = 1 V/ms when (25h to 27h) LDOx (x: 5 to 7) = 0x00 to 0x16, 0.300 V to 0.850 V setting
Slew rate = 2 V/ms when (25h to 27h) LDOx (x: 5 to 7) = 0x17 to 0x36, 0.875 V to 1.650 V setting
Slew rate = 4 V/ms when (25h to 27h) LDOx (x: 5 to 7) = 0x37 to 0xFF, 1.675 V to 3.300 V setting

1 Slew rate = 2 V/ms when (25h to 27h) LDOx (x: 5 to 7) = 0x00 to 0x16, 0.300 V to 0.850 V setting
Slew rate = 4 V/ms when (25h to 27h) LDOx (x: 5 to 7) = 0x17 to 0x36, 0.875 V to 1.650 V setting
Slew rate = 8 V/ms when (25h to 27h) LDOx (x: 5 to 7) = 0x37 to 0xFF, 1.675 V to 3.300 V setting

LDO5_UVLO_LVL / LDO6_UVLO_LVL / LDO7_UVLO_LVL
UVLO level for PVINx (x: 5 to 7)
If LDO7 is load SW mode, this setting has to be 0.
0 2.3 V
1 1.6 V

LDO5_MODE / LDO6_MODE / LDO7_MODE
Mode of LDO
If LDO7 is load SW mode, this setting is ignored.
00 LDOx_INI_VOUT (x: 5 to 7) voltage
01 SD_MODE (3.3 V or 1.8 V selected by LDOx_VOL_LVL (x: 5 to 7))
10 LPDDR5_VTT_MODE (0.5 V or 0.3 V selected by LDOx_VOL_LVL (x: 5 to 7))
11 Prohibit

LDO5_VOL_LVL / LDO6_VOL_LVL / LDO7_VOL_LVL
Select voltage level
If LDO7 is load SW mode, this setting is ignored.
0 When LDOx_MODE (x: 5 to 7) = 00b LDOx_INI_VOUT (x: 5 to 7)
When LDOx_MODE (x: 5 to 7) = 01b 3.3 V
When LDOx_MODE (x: 5 to 7) = 10b 0.5 V

1 When LDOx_MODE (x: 5 to 7) = 00b LDOx_INI_VOUT (x: 5 to 7)
When LDOx_MODE (x: 5 to 7) = 01b 1.8 V
When LDOx_MODE (x: 5 to 7) = 10b 0.3 V

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
2Fh	DISCHG	BUCK4_RDIS[1:0]		BUCK3_RDIS[1:0]		BUCK2_RDIS[1:0]		BUCK1_RDIS[1:0]		O/E/ RW	65h

Discharge resistance for BUCK
00 55 Ω
01 30 Ω
10 22 Ω
11 Disable

Register Map – continued

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
30h	OVP1	BUCK4_OVP[1:0]		BUCK3_OVP[1:0]		BUCK2_OVP[1:0]		BUCK1_OVP[1:0]		O/E/ RWS	FFh
31h	OVP2	-	-	LDO7_OVP[1:0]		LDO6_OVP[1:0]		LDO5_OVP[1:0]		O/E/ RWS	3Fh

OVP threshold

00	Prohibit
01	9 %
10	15 %
11	20 %

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
32h	INTR_ OCPH	BUCK2_EXTR_OCP[1:0]		BUCK2_INTR_OCPH[1:0]		BUCK1_EXTR_OCP[1:0]		BUCK1_INTR_OCPH[1:0]		O/E/ RWS	ABh
33h	OCPH1	-	-	BUCK4_OCPH[1:0]		-	-	BUCK3_OCPH[1:0]		O/E/ RWS	23h
34h	-	-	-	-	-	-	-	-	-	O/E/ RWS	2Ah

BUCK1_EXTR_OCP / BUCK2_EXTR_OCP

OCP threshold voltage of DRMOS using (refer to Table 3,OCP EXT block)

00	819 mV
01	947 mV
10	1075 mV
11	1203 mV

BUCK1_INTR_OCPH / BUCK2_INTR_OCPH

OCP threshold of internal FET using for BUCK1 and BUCK2

00	1.5 A
01	2.4 A
10	3.3 A
11	4.2 A

BUCK3_OCPH / BUCK4_OCPH

OCP threshold for BUCK3 and BUCK4

00	3.00 A
01	4.33 A
10	5.66 A
11	7.00 A

Register Map – continued

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
35h	OVD_UVD1	BUCK4_OVD_UVD[1:0]		BUCK3_OVD_UVD[1:0]		BUCK2_OVD_UVD[1:0]		BUCK1_OVD_UVD[1:0]		O/E/ RWS	FFh
36h	OVD_UVD2	-	-	LDO7_OVD_UVD[1:0]		LDO6_OVD_UVD[1:0]		LDO5_OVD_UVD[1:0]		O/E/ RWS	3Fh
37h	LDSW_ UVD_UVP	-	UVP_LDSW[2:0]			-	UVD_LDSW[2:0]			O/E/ RWS	42h

BUCK1_OVD_UVD / BUCK2_OVD_UVD / BUCK3_OVD_UVD / BUCK4_OVD_UVD
OVD and UVD threshold for BUCK
The value is delta voltage against the VOUT voltage including DC accuracy from register setting voltage.
00 Prohibit
01 Prohibit
10 -/+15 mV (accuracy -/+10 mV)
11 -/+20 mV (accuracy -/+10 mV)

LDO5_OVD_UVD / LDO6_OVD_UVD / LDO7_OVD_UVD
OVD and UVD threshold for LDO
The value is delta voltage against the VOUT voltage including DC accuracy from register setting voltage.

When LDOx_INI_VOUT (x: 5 to 7) = 0x00 to 0x16 (0.300 V to 0.850 V)
00 Prohibit
01 Prohibit
10 -/+15 mV (accuracy -/+10 mV)
11 -/+20 mV (accuracy -/+10 mV)

When LDOx_INI_VOUT (x: 5 to 7) = 0x17 to 0x36 (0.875 V to 1.650 V)
00 Prohibit
01 -/+18 mV (accuracy -/+14.3 mV)
10 -/+30 mV (accuracy -/+14.3 mV)
11 -/+40 mV (accuracy -/+14.3 mV)

When LDOx_INI_VOUT (x: 5 to 7) = 0x37 to 0xFF (1.675 V to 3.300 V)
00 Prohibit
01 -/+36 mV (accuracy -/+27.6 mV)
10 -/+60 mV (accuracy -/+27.6 mV)
11 -/+80 mV (accuracy -/+27.6 mV)

UVP_LDSW
UVP setting when LDO7 is load SW mode. Int is internal FET mode, Ext is external FET mode.
000 150 mV (Int), 50 mV (Ext)
001 150 mV (Int), 60 mV (Ext)
010 200 mV (Int), 70 mV (Ext)
011 200 mV (Int), 80 mV (Ext)
100 250 mV (Int), 90 mV (Ext)
101 250 mV (Int), 100 mV (Ext)
110 250 mV (Int), 110 mV (Ext)
111 250 mV (Int), 120 mV (Ext)

UVD_LDSW
UVD setting when LDO7 is load SW mode. Int is internal FET mode, Ext is external FET mode.
000 50 mV (Int), 30 mV (Ext)
001 50 mV (Int), 40 mV (Ext)
010 100 mV (Int), 50 mV (Ext)
011 100 mV (Int), 60 mV (Ext)
100 150 mV (Int), 70 mV (Ext)
101 150 mV (Int), 80 mV (Ext)
110 200 mV (Int), 90 mV (Ext)
111 200 mV (Int), 100 mV (Ext)

Register Map – continued

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
38h	MASK_ CNT1	OVD_MASK_TIME[3:0]				UVD_MASK_TIME[3:0]				O/E/ RWS	22h
39h	MASK_ CNT2	PRSTB_ERR_ OFF	CHIP_IF_ SHD_OFF	-	-	TW_MASK_TIME[3:0]				O/E/ RWS	82h

OVD_MASK_TIME, UVD_MASK_TIME, TW_MASK_TIME

When over voltage, under voltage, or thermal warning is detected longer than this mask time, the XXX_OVD_STAT, XXX_UVD_STAT, YYY_TW_CH_STAT, or TW_STAT register becomes 1 and it is informed from the INTB_ADDPRSTB1 pin. (XXX: BUCK1 to BUCK4 and LDO5 to LDO7, YYY: BUCK1 to BUCK4)

0x0 to 0xF 4 µs to 64 µs (4 µs step)

In case of LDSW7 mode, UVD_MASK_TIME setting is following.

0x0 Prohibit
0x1 to 0xF 4 µs to 32 µs (2 µs step)

PRSTB_ERR_OFF The mask of shutdown when PRSTB_ERR is detected.

0 Shutdown when PRSTB_ERR
1 Not shutdown

CHIP_IF_SHD_OFF The mask of shutdown when IF1 and IF2 function communication error occurs.

0 Shutdown when IF communication error
1 Not shutdown

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
3Ah	POFF_ OVERTIME	-	PON_OVERTIME[2:0]			-	POFF_OVERTIME[2:0]			O/E/ RWS	11h

PON_OVERTIME, POFF_OVERTIME

Setting of time over for power ON or power OFF.
When power ON sequence time or power OFF sequence time is over this time, PON_ERR or POFF_ERR occurs.

0x0 to 0x7 64 ms to 512 ms (64 ms step)

Register Map – continued

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
3Bh	PIN BIST	EN_STAT (read only)	EN_CTRL_SEL	EN_CTRL_ON	INTB_ MANUAL	PRSTB_ MANUAL	PRSTB_ MANUAL_ MASK	-	BIST_ON_ DEMAND	-/-/ RW	18h

EN_STAT — The EN pin input value read back.
- 0 The EN pin is low voltage.
- 1 The EN pin is high voltage.

EN_CTRL_SEL — When EN_CTRL_ON = 1, Power ON/OFF sequence is controlled by EN_CTRL_SEL instead of the EN pin input.
- 0 Start OFF sequence
- 1 Start ON sequence

EN_CTRL_ON — EN_CTRL_SEL function enable / disable.
- 0 EN_CTRL_SEL Disable
- 1 EN_CTRL_SEL Enable

INTB_MANUAL, PRSTB_MANUAL — Control the INTB_ADDPRSTB1 pin or the PRSTB pin manually for system BIST.
- 0 The pin is forced L.
- 1 Normal

PRSTB_MANUAL_MASK — In (39h) PRSTB_ERR_OFF = 0 (PRSTB_ERR detection is active), when PRSTB_MANUAL be set, PRSTB_ERR will be detected. This mask has to be set to prevent this error.
- 0 Mask Disable
- 1 PRSTB_ERR Mask Enable

BIST_ON_DEMAND — Analog BIST (OVD/UVD/TW detection comparator check) run.
- 0 No action
- 1 ABIST run. After finish, it returns “0” automatically.

Register Map – continued

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
3Ch	ALWAYS_ ON	PRSTB_ ALWAYS_ON	LDO7_ ALWAYS_ON	LDO6_ ALWAYS_ON	LDO5_ ALWAYS_ ON	BUCK4_ ALWAYS_ ON	BUCK3_ ALWAYS_ ON	BUCK2_ ALWAYS_ ON	BUCK1_ ALWAYS_ ON	O/E/ RWSA	00h
3Dh	ADD_ PRSTB	ADD_PRSTB2_DELAY[1:0]		ADD_PRSTB2[1:0]		ADD_PRSTB1_ DELAY[1:0]		ADD_PRSTB1[1:0]		O/E/ RO	00h
3Eh	ADD_EN1	PRSTB_ ADD_EN1	LDO7_ ADD_EN1	LDO6_ ADD_EN1	LDO5_ ADD_EN1	BUCK4_ ADD_EN1	BUCK3_ ADD_EN1	BUCK2_ ADD_EN1	BUCK1_ ADD_EN1	O/E/ RO	00h
3Fh	ADD_EN2	PRSTB_ ADD_EN2	LDO7_ ADD_EN2	LDO6_ ADD_EN2	LDO5_ ADD_EN2	BUCK4_ ADD_EN2	BUCK3_ ADD_EN2	BUCK2_ ADD_EN2	BUCK1_ ADD_EN2	O/E/ RO	00h

XXX_ALWAYS_ON (XXX: BUCK1 to BUCK4, LDO5 to LDO7, and PRSTB)
Always ON setting.
0 Normal ON / OFF sequence
1 Forced Power ON

ADD_PRSTB1_DELAY / ADD_PRSTB2_DELAY
The power ON delay time setting from final channel boot-up for ADD_PRSTB1 or ADD_PRSTB2.
For power OFF delay time, it is fixed 2 µs.
00 2 µs
01 1.211 ms
10 4.845 ms
11 9.690 ms

ADD_PRSTB2 Selection of the ERRB_ADDPRSTB2 pin function.
00 ERRB (ADD_PRSTB2_DELAY = 00b, 01b, 10b)
or ERRB_GPO (ADD_PRSTB2_DELAY = 11b)
01 ADD_PRSTB2 function for ALWAYS_ON channel
10 ADD_PRSTB2 function for ADD_EN1 channel
11 ADD_PRSTB2 function for ADD_EN2 channel

ADD_PRSTB1 Selection of the INTB_ADDPRSTB1 pin function.
00 INTB (ADD_PRSTB1_DELAY = 00b, 01b, 10b)
or INTB_GPO (ADD_PRSTB1_DELAY = 11b)
01 ADD_PRSTB1 function for ALWAYS_ON channel
10 ADD_PRSTB1 function for ADD_EN1 channel
11 ADD_PRSTB1 function for ADD_EN2 channel

XXX_ADD_EN1 (XXX: BUCK1 to BUCK4, LDO5 to LDO7, and PRSTB)
Setting the boot channel associated with the ADD_EN1 function.
When any one of the ADD_EN1 registers becomes 1, the IF1_ADDEN1 pin functions as the ADD_EN1 function.
This setting can be used when SYSTEM_NUMBER is 0 (standalone mode).
In other SYSTEM_NUMBER setting, don't set this register, the IF1_ADDEN1 pin is used for IF1 function.
0 Normal ON / OFF sequence
1 Power ON/OFF controlled by the IF1_ADDEN1 pin.

XXX_ADD_EN2 (XXX: BUCK1 to BUCK4, LDO5 to LDO7, and PRSTB)
Setting the boot channel associated with the ADD_EN2 function.
When any one of the ADD_EN2 registers becomes 1, the SYNC_ADDEN2 pin functions as the ADD_EN2 function.
0 Normal ON / OFF sequence
1 Power ON/OFF controlled by the SYNC_ADDEN2 pin.

Register Map – continued

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
40h	WDT_SET1	-	FAST_TO[2:0]			-	-	RATIO_TO[1:0]		-/-/ RW	02h
41h	WDT_SET2	-	-	-	WDT_ SLOWMD	WDT_ PRSTB_ INTB	WDT_TYPE	WDT_EN[1:0]		-/-/ RW	00h
42h	WDT_SET3	-	-	-	-	-	-	-	WDT_IFRST	-/-/ RW	00h

FAST_TO Fast time out setting for WDT.
About the fast and slow timetable, refer to Table 8.
0x0 1 ms
0x1 2 ms
0x2 4 ms
0x3 8 ms
0x4 16 ms
0x5 32 ms
0x6 64 ms
0x7 128 ms

RATIO_TO Ratio setting of slow time out for WDT.
About the fast and slow timetable, refer to Table 8.
0x0 Fast : Slow = 1 : 2
0x1 Fast : Slow = 1 : 4
0x2 Fast : Slow = 1 : 8
0x3 Fast : Slow = 1 : 16

WDT_SLOWMD Time counter mode setting when over the slow time limit.
0 Time counter is not cleared.
Also in this setting, if slow time out is detected again, fail counter will be added +2.
1 Time counter is cleared to 0, and re-count.

WDT_PRSTB_INTB Indication setting when WDT_ERR is detected.
0 L assert to INTB
1 L assert to INTB
and also L assert PRSTB which is selected by (0Ch) PRSTB_WDT register for 5 ms.

WDT_TYPE Select of WDT time judge
0 Window Type (Fast Timeout and Slow Timeout)
1 Timeout Type (Slow Timeout only)

WDT_EN Enable of WDT
This register can be set after PRSTB signal H de-assertion.
The signal is selected in the (0Ch) PRSTB_WDT register.
This register is cleared when the signal is L asserted.
00 Disable
01 WDT_IF_EN: Enable for IF access WDT
10,11 WDT_QA_EN: Enable for Q&A WDT

WDT_IFRST Reset for WDT counter when IF access WDT mode (WDT_EN = 01b).
0 No function
1 Clear counter. This bit returns to “0” automatically.

Register Map – continued

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
43h	WDT_ FCSET	WDT_FC[3:0] (read only)				-	-	WDT_FCSET[1:0]		-/-/ RW	02h

WDT_FC Read back fail counter value.
0x0 to 0xF Fail counter value

WDT_FCSET Maximum fail counter value. When fail counter reaches this value, WDT_ERR occurs.
00 1
01 3
10 7
11 13

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
44h	WDT_QA_ SEED	-	-	-	WDT_SEED[4:0]					-/-/ RW	00h
45h	WDT_QA_QCF G	-	-	-	WDT_QCFG[4:0]					-/-/ RW	00h
46h	WDT_QUESTI ON	-	-	-	WDT_Q[4:0]					-/-/ RO	00h
47h	WDT_ANSWE R	WDT_A[7:0]								-/-/ RW	00h
48h	WDT_ANSWE R_TYPE	-	-	-	-	-	-	WDT_ANSTYPE[1:0]		-/-/ RW	00h

WDT_SEED Seed Value for WDT_Q. For the detail, refer to Figure 27 and Figure 28.
0x00 to 0x1F

WDT_QCFG WDT Question Configuration Setting. For the detail, refer to Figure 27 and Figure 28.
0x00 to 0x1F

WDT_Q WDT Question
0x00 to 0x1F

WDT_A WDT Answer for QA type WDT
Write 8-bit answer which is calculated by Figure 29.

WDT_ANSTYPE WDT Answer Type selection. For the detail, refer to Figure 29.
0x0 to 0x3

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
49h	WDT_FLAG_ CLEAR	-	-	-	-	-	-	WDT_FC_ CLEAR	WDT_FLAG_ CLEAR	-/-/ RW	00h

WDT_FC_CLEAR Clear (43h) WDT_FC register which is fail counter.
0 No function
1 Clear. This bit returns to “0” automatically.

WDT_FLAG_CLEAR Clear (4Ah) ST_WDT_SLOW, ST_WDT_FAST, ST_WDT_BE_DET register.
0 No function
1 Clear. This bit returns to “0” automatically.

Register Map – continued

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
4Ah	WDT_STAT	-	-	ST_WDT_ ANSNG	ST_WDT_ SLOW	ST_WDT_ FAST	ST_WDT_ OPEN	ST_WDT_ ERR	ST_WDT_ BE_DET	-/-/ RO	00h
4Bh	-	-	-	-	-	-	-	-	-	-	-

ST_WDT_ANSNG Status register which WDT answer is not correct.
0 No detected
1 Detected

ST_WDT_SLOW Status register of WDT slow timeout.
0 No detected
1 Detected

ST_WDT_FAST Status register of WDT fast timeout.
0 No detected
1 Detected

ST_WDT_OPEN Status register of time counter.
0 Time counter is under fast timeout, or over slow timeout.
1 Time counter is between fast timeout and slow timeout.

ST_WDT_ERR Status register of WDT error.
0 No detected
1 Detected

ST_WDT_BE_DET Status register of bad event.
Bad event is WDT_ANSNG, WDT_SLOW, and WDT_FAST.
0 No detected
1 Detected

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
4Ch	INTB_GPO/ ERRB_GPO	-	-	-	ERRB_GPO	-	-	-	INTB_GPO	-/-/ RW	00h

ERRB_GPO Output Low or High-Z to the ERRB_ADDPRSTB2 pin when GPO mode.
(ADD_PRSTB2_DELAY = 11b and ADD_PRSTB2 = 00b).
0 Low output
1 High-Z output

INTB_GPO Output Low or High-Z to the INTB_ADDPRSTB1 pin when GPO mode.
(ADD_PRSTB1_DELAY = 11b and ADD_PRSTB1 = 00b).
0 Low output
1 High-Z output

Register Map – continued

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
4Fh	INTERNAL_ STATE	-	-	-	-	INTERNAL_STATE[3:0]				-/-/ RO	00h

INTERNAL_STATE Internal state read back.

0x0 to 0x8	Reserved
0x9	STANDBY
0xA	POWER_ON
0xB	ACTIVE
0xC	POWER_OFF1
0xD	GROUP_OFF
0xE	POWER_OFF2
0xF	FAIL_SAFE

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
50h	STATUS_ CHIP_ERRB	SUB_ PMIC5_ STAT	SUB_ PMIC4_ STAT	SUB_ PMIC3_ STAT	SUB_ PMIC2_ STAT	SUB_ PMIC1_ STAT	MAIN_ PMIC1_ STAT	SUB_ PMIC0_ STAT	MAIN_ PMIC0_ STAT	-/-/ RW	00h

Main-PMIC and Sub-PMIC ERROR status register
1 is set when each Main-PMIC or Sub-PMIC device detects ERRB event (Not included INTB event).
When write 1, the bit is cleared.

0	No detected
1	Detected

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
51h	STATUS_ PART_ INTB_ERRB	LDO7_ STAT	LDO6_ STAT	LDO5_ STAT	BUCK4_ STAT	BUCK3_ STAT	BUCK2_ STAT	BUCK1_ STAT	SYSTEM_ STAT	-/-/ RO	00h

Each channel status register read back.
SYSTEM_STAT = OR of each bit of 52h, 53h, 54h, and 5Ch.
BUCK1_STAT = OR of each bit of 55h and 5Dh.
BUCK2_STAT = OR of each bit of 56h and 5Eh.
BUCK3_STAT = OR of each bit of 57h and 5Fh.
BUCK4_STAT = OR of each bit of 58h and 60h.
LDO5_STAT = OR of each bit of 59h and 61h.
LDO6_STAT = OR of each bit of 5Ah and 62h.
LDO7_STAT = OR of each bit of 5Bh and 63h.

Register Map – continued

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
52h	STATUS_ SYSTEM_ ERRB_1	SUB_PMIC_ ERR_STAT	DRMOS2_ ERR_STAT	DRMOS1_ ERR_STAT	PRSTB_ ERR_STAT	ABIST_ ERR_STAT	EEP_ ERR_STAT	DBIST_ ERR_STAT	OTP_ ERR_STAT	-/-/ RW	00h
53h	STATUS_ SYSTEM_ ERRB_2	CMD_SHDN_ STAT	POFF_ERR_ STAT	PON_ERR_ STAT	OSC_ERR_ STAT	OVLO_VIN_ STAT	UVLO_VIN_ STAT	TSD_STAT	VREF_ERR_ STAT	-/-/ RW	00h
54h	STATUS_ SYSTEM_ ERRB_3	SYS_INT_ SHD	-	-	-	CHIP_IF_ ERR_STAT	-	-	PRSTB_WDT_ ERR_STAT	-/-/ RW	00h

System error status register
1 is set if any ERRB event is detected. When write 1, the bit is cleared.

SUB_PMIC_ERR_STAT Sub-PMIC detects errors.
CMD_SHDN_STAT (08h) SHUTDOWN done.
SYS_INT_SHD (5Ch) TW_STAT was detected for 512 µs when (20h) SHD_INTB = 1 and system shutdown.

For other error event detail, refer to Table 3.

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
55h	STATUS_ BUCK1_ ERRB	BUCK1_INT_ SHD	-	-	-	-	BUCK1_ UVP_STAT	BUCK1_ OVP_STAT	UVLO_ PVIN1_STAT	-/-/ RW	00h
56h	STATUS_ BUCK2_ ERRB	BUCK2_INT_ SHD	-	-	-	-	BUCK2_ UVP_ STAT	BUCK2_ OVP_ STAT	UVLO_ PVIN2_STAT	-/-/ RW	00h
57h	STATUS_ BUCK3_ ERRB	BUCK3_INT_ SHD	-	-	-	-	BUCK3_ UVP_ STAT	BUCK3_ OVP_ STAT	UVLO_ PVIN3_STAT	-/-/ RW	00h
58h	STATUS_ BUCK4_ ERRB	BUCK4_INT_ SHD	-	-	-	-	BUCK4_ UVP_ STAT	BUCK4_ OVP_ STAT	UVLO_ PVIN4_STAT	-/-/ RW	00h
59h	STATUS_ LDO5_ ERRB	LDO5_INT_ SHD	-	-	-	-	LDO5_ UVP_ STAT	LDO5_ OVP_ STAT	UVLO_ PVIN5_STAT	-/-/ RW	00h
5Ah	STATUS_ LDO6_ ERRB	LDO6_INT_ SHD	-	-	-	-	LDO6_ UVP_ STAT	LDO6_ OVP_ STAT	UVLO_ PVIN6_STAT	-/-/ RW	00h
5Bh	STATUS_ LDO7_ ERRB	LDO7_INT_ SHD	-	-	-	-	LDO7_ LDSW7_UVP_ STAT	LDO7_ OVP_ STAT	UVLO_ PVIN7_STAT	-/-/ RW	00h

Each channel error status register
1 is set if any ERRB event is detected. When write 1, the bit is cleared.

XXX_INT_SHD (XXX: BUCK1 to BUCK4 and LDO5 to LDO7)
Each channel interrupt event (5Dh to 63h) is detected for 512 µs when (20h) SHD_INTB = 1 and the channel and same group channel shutdown.

For other error event detail, refer to Table 3.

Register Map – continued

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
5Ch	STATUS_ SYSTEM_ INTB	-	-	-	-	CHIP_IF_ INT_ STAT	I2C_INT_ STAT	WDT_ INT_ STAT	TW_STAT	-/-/ RW	00h
5Dh	STATUS_ BUCK1_ INTB	-	-	BUCK1_TW_ CH_STAT	BUCK1_UVD_ STAT	BUCK1_ OVD_ STAT	BUCK1_ OCPN_ OCPEXT_STA T	BUCK1_ OCPL_ STAT	BUCK1_ OCPH_ STAT	-/-/ RW	00h
5Eh	STATUS_ BUCK2_ INTB	-	-	BUCK2_TW_ CH_STAT	BUCK2_UVD_ STAT	BUCK2_ OVD_ STAT	BUCK2_ OCPN_ OCPEXT_STA T	BUCK2_ OCPL_ STAT	BUCK2_ OCPH_ STAT	-/-/ RW	00h
5Fh	STATUS_ BUCK3_ INTB	-	-	BUCK3_TW_ CH_STAT	BUCK3_UVD_ STAT	BUCK3_ OVD_ STAT	BUCK3_ OCPN_ STAT	BUCK3_ OCPL_ STAT	BUCK3_ OCPH_ STAT	-/-/ RW	00h
60h	STATUS_ BUCK4_ INTB	-	-	BUCK4_TW_ CH_STAT	BUCK4_UVD_ STAT	BUCK4_ OVD_ STAT	BUCK4_ OCPN_ STAT	BUCK4_ OCPL_ STAT	BUCK4_ OCPH_ STAT	-/-/ RW	00h
61h	STATUS_ LDO5_ INTB	-	-	-	LDO5_UVD_ STAT	LDO5_ OVD_ STAT	-	-	LDO5_ OCPH_ STAT	-/-/ RW	00h
62h	STATUS_ LDO6_ INTB	-	-	-	LDO6_UVD_ STAT	LDO6_ OVD_ STAT	-	-	LDO6_ OCPH_ STAT	-/-/ RW	00h
63h	STATUS_ LDO7_ INTB	-	-	-	LDO7_LDSW7_ UVD_ STAT	LDO7_ OVD_ STAT	-	-	LDO7_ OCPH_ STAT	-/-/ RW	00h

System and each channel error status register
1 is set if any INTB event is detected. When write 1, the bit is cleared.

For error event detail, refer to Table 3.

Register Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	OTP /EEP /I²C	Default
69h	MASK_ SYSTEM_ ERRB_1	SUB_PMIC_ ERR_MASK	DRMOS2_ ERR_MASK	DRMOS1_ ERR_MASK	PRSTB_ERR_ MASK	ABIST_ERR_ MASK	EEP_ERR_ MASK	DBIST_ ERR_ MASK	OTP_ERR_ MASK	-/-/ RW	00h
to											
7Ah	MASK_ LDO7_INTB	-	-	-	LDO7_ LDSW7_ UVD_ MASK	LDO7_ OVD_ MASK	-	-	LDO7_ OCPH_ MASK	-/-/ RW	00h

These registers are indication MASK register.
For example when OTP_ERR is detected, system shutdown even if OTP_ERR_MASK = 1.

0 Indication to the ERRB_ADDPRSTB2 pin or the INTB_ADDPRSTB1 pin
1 No indication

I²C Protocol Description

I²C Protocol Basic

1ch I²C Interface is implemented.

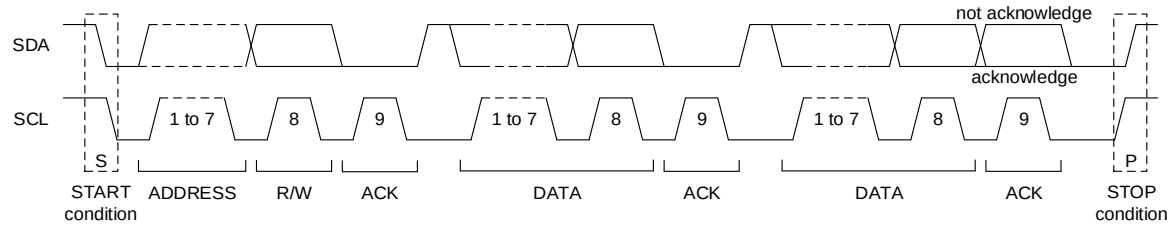


Figure 15. I²C SDA / SCL

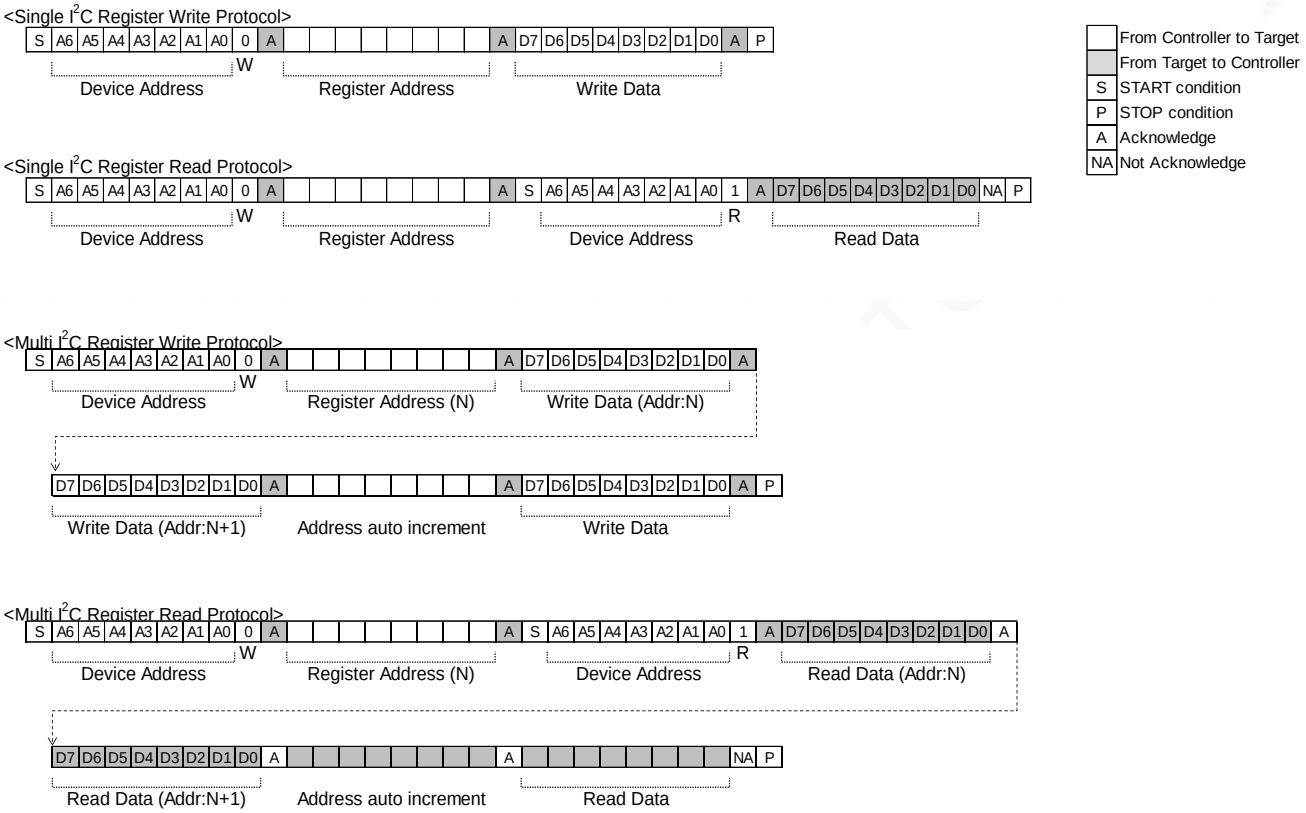


Figure 16. I²C Command Configure

Device Address
Support 7bit Address mode
Device Address: 0x60 (When 8bit description, it is 0xC0 in Write mode and 0xC1 in Read mode.)

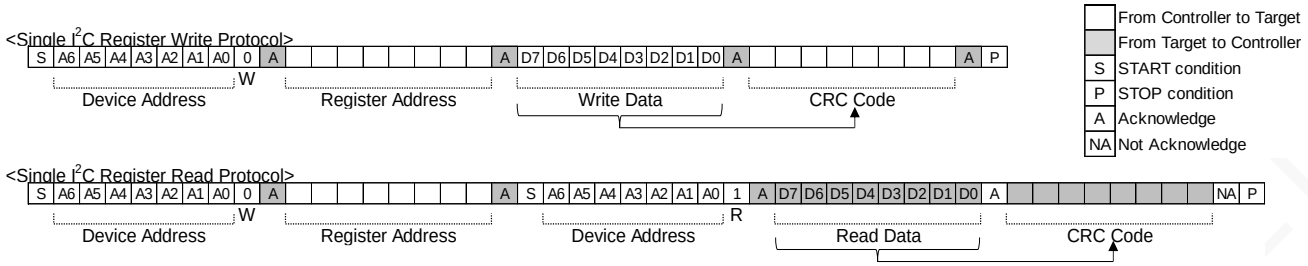
Speed Mode	Frequency
(1) Fast mode	(1) Fast mode: Max 400 kHz
(2) Fast mode plus	(2) Fast mode plus: Max 1MHz

I²C Protocol Description – continued

I²C Protocol with CRC

DATA CRC Mode

DATA CRC Single Mode



DATA CRC Burst Mode

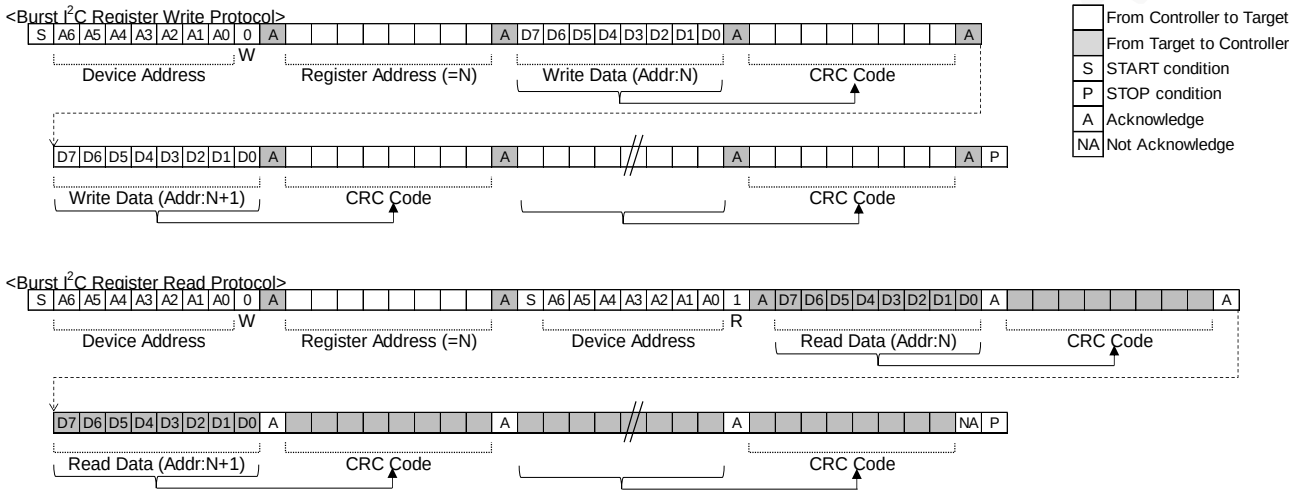
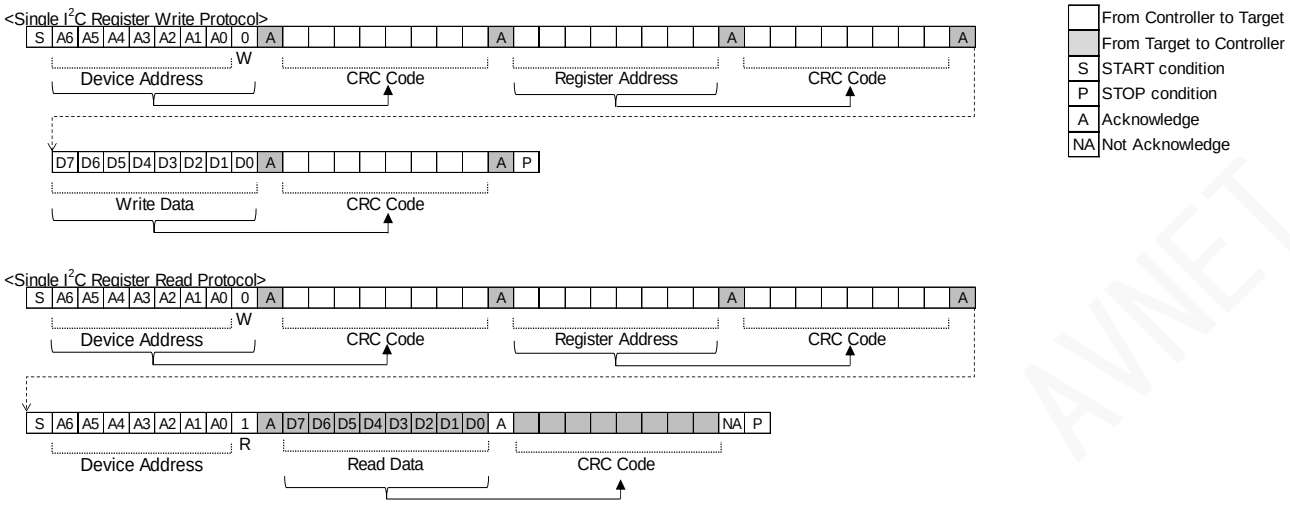


Figure 17. DATA CRC Mode

I²C Protocol Description – continued

ALL CRC Mode

ALL CRC Single Mode



ALL CRC Burst Mode

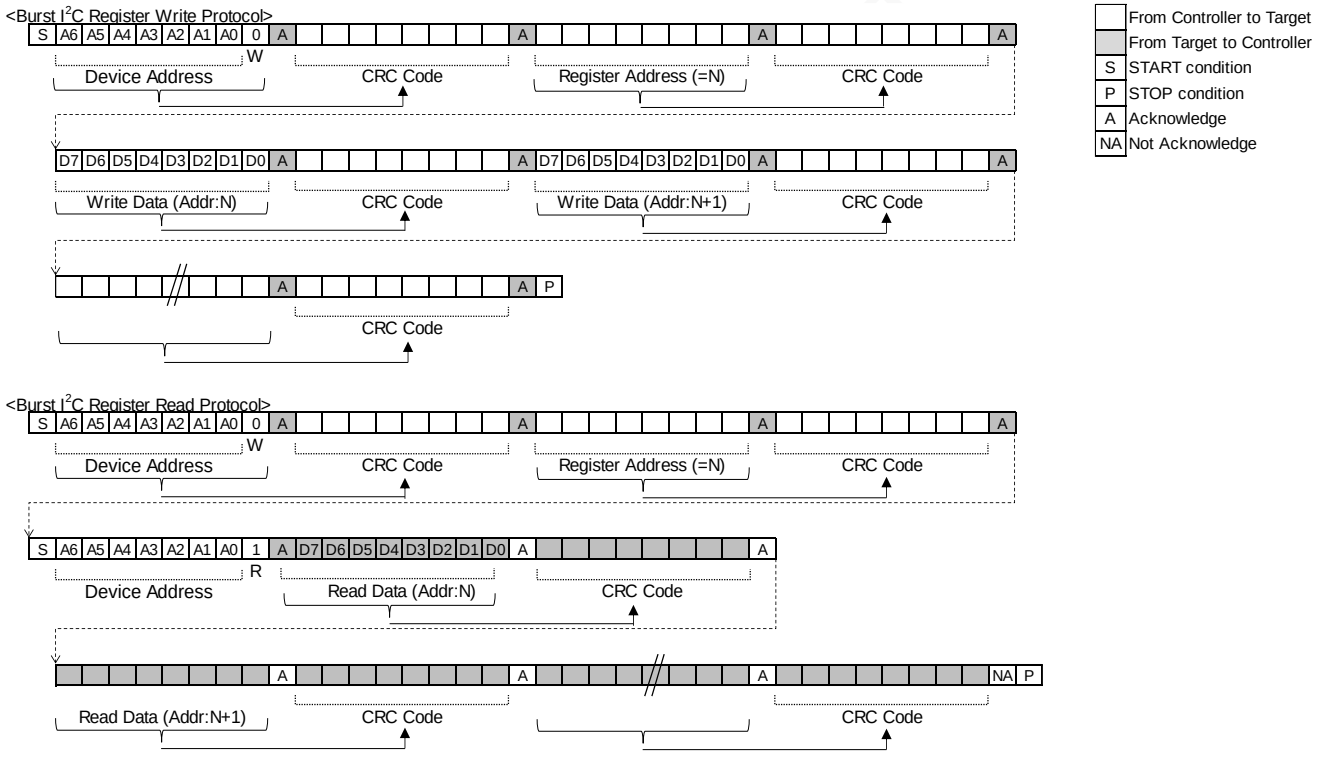


Figure 18. ALL CRC Mode

I²C Protocol Description – continued

CRC Calculation for EEPROM and I²C

CRC Polynomial: $X^8 + X^5 + X^4 + 1$
Default Value: 0x00
Bit Order: MSB

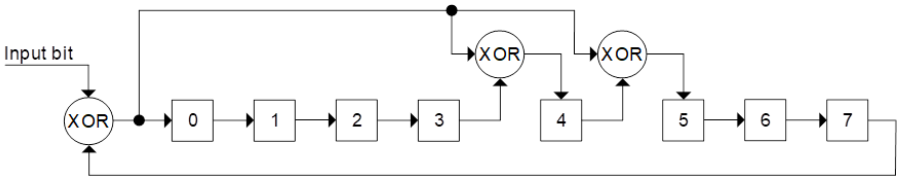


Figure 19. CRC Calculation

I²C Protocol Description – continued

Timing diagram and Electric Characteristics

SDA / SCL have timing constraints as shown below.

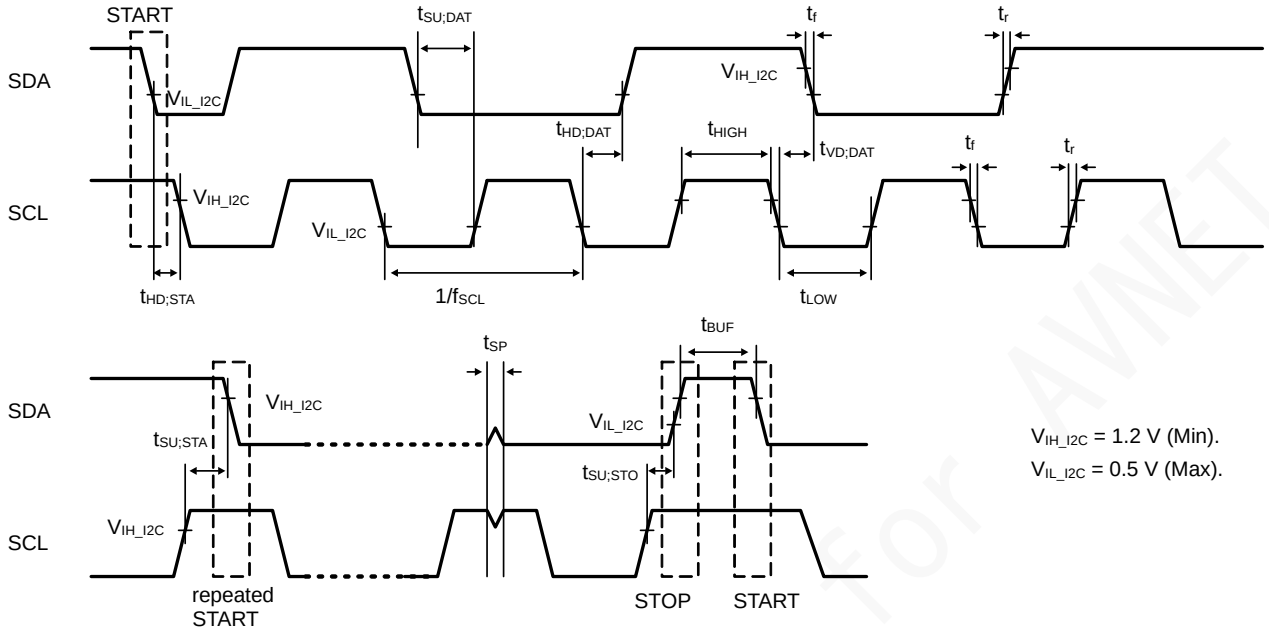


Figure 20. SDA / SCL Timing

Table 7. Electric Characteristics of I2C Protocol

Parameter	Symbol	Min	Typ	Max	Unit
<I²C BUS format>					
SCL clock frequency	f_{SCL}	-	-	1000	kHz
Hold time (repeated) START condition After this period, the first clock is generated	$t_{HD;STA}$	0.26	-	-	µs
Low period of the SCL clock	t_{LOW}	0.5	-	-	µs
High period of the SCL clock	t_{HIGH}	0.26	-	-	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	0.26	-	-	µs
Data hold time	$t_{HD;DAT}$	0	-	-	µs
Data set-up time	$t_{SU;DAT}$	50	-	-	ns
Rise time of SDA and SCL	t_r	-	-	120	ns
Fall time of SDA and SCL	t_f	-	-	120	ns
Set-up time for STOP condition	$t_{SU;STO}$	0.26	-	-	µs
Bus free time between a STOP and START condition	t_{BUF}	0.5	-	-	µs
Data valid time	$t_{VD;DAT}$	-	-	0.45	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	-	-	50	ns

Watch Dog Timer Protocol Description

Watch Dog Timer Enable Timeout and Automatically OFF

If a control device cannot control WDT enable, WDT cannot detect error. To prevent this situation, there is timeout function from PRSTB signal H de-assertion. This function is enabled by (0Ch) the PRSTB_WDT_TO register. If WDT enable is not set with in the time from PRSTB signal H de-assertion, PRSTB_WDT_ERR is detected and system shutdown. Register unlock (04h WRITE_PROTECT = 0x9D) and WDT_EN have to be set before the timeout.
PRSTB signal is selected from PRSTB, ADD_PRSTB1, or ADD_PRSTB2 by the PRSTB_WDT register.
The time of timeout is selected between 100 ms and 1400 ms by the PRSTB_WDT_TO_SEL register.
When PRSTB signal is L asserted, also WDT enable is set OFF automatically regardless PRSTB_WDT_TO setting.
This is including also software reset which is in the (06h) PRSTB_L register and system pin BIST which is in the (3Bh) PRSTB_MANUAL register. After software reset or system pin BIST, WDT enable have to be set again.
If PRSTB_WDT is ADD_PRSTB1 or ADD_RSTB2 setting, WDT enable is not set OFF by PRSTB_L or PRSTB_MANUAL.
To OFF after WDT enabled in this mode, the way is to set PRSTB_WDT_TO = 0 first and to set WDT_EN = 00b.

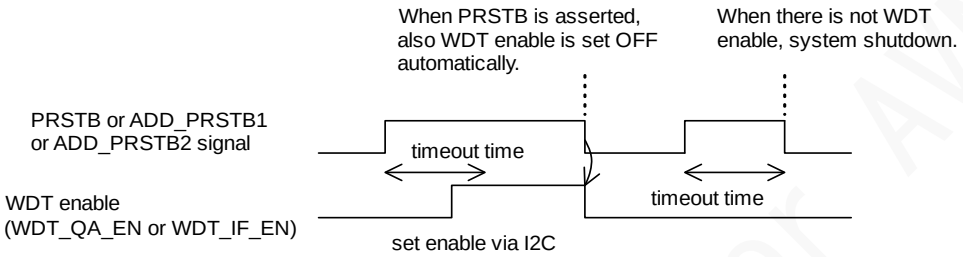


Figure 21. WDT Enable Timeout

Watch Dog Timer Protocol

Watch Dog Timer (WDT) function is enabled by the register setting (41h) WDT_EN. This function is valid after H de-assertion of PRSTB which is selected by (0Ch) PRSTB_WDT register.

By WDT_IF_EN = H setting, IF type WDT is enabled. WDT monitors the duration of the I^2C write command to the WDT_IFRST register.
By WDT_QA_EN = H setting, QA type WDT is enabled. WDT monitors the duration of the I^2C write command to the WDT_A[7:0] register and the correctness of the value of WDT_A[7:0].
Regarding the calculation of WDT Correct Answer, refer to Figure 27 to Figure 29.

There are 2 types regarding the duration of WDT, Window Type and Timeout Type.
Window Type monitors Fast Timeout and Slow Timeout. Timeout Type monitors Slow Timeout only.
Regarding the Fast Timeout and Slow Timeout definition, refer to Figure 22 and Figure 23.
The range of Fast Timeout and Slow Timeout is selected by RATIO_TO[1:0] and FAST_TO[2:0].
For the detail, refer to Table 8.

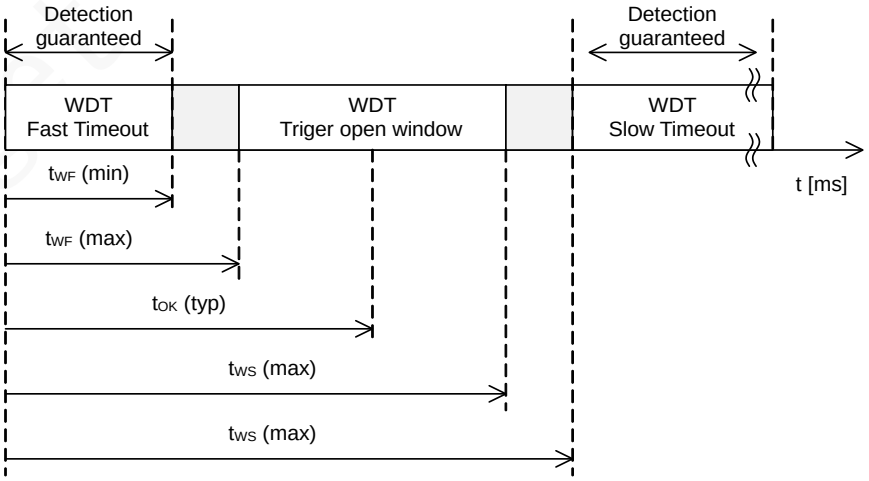


Figure 22. WDT Detection Range

Watch Dog Timer Protocol - continued

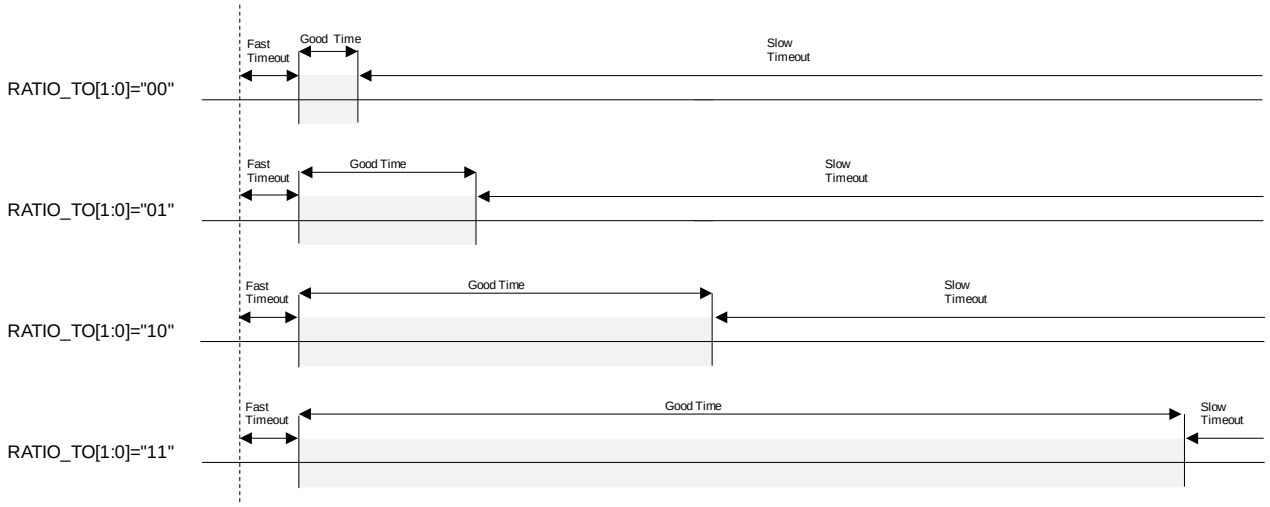


Figure 23. WDT RATIO

Table 8. WDT Detection Time

RATIO_TO[1:0]	FAST_TO[2:0]	Fast Timeout Detection [ms]		t_{OK} [ms] (Typ)	Slow Timeout Detection [ms]	
		t_{WF} (Min)	t_{WF} (Max)		t_{WS} (Min)	t_{WS} (Max)
00	000	0.9	1.1	1.45	1.8	2.2
	001	1.8	2.2	2.9	3.6	4.4
	010	3.6	4.4	5.8	7.2	8.8
	011	7.2	8.8	11.6	14.4	17.6
	100	14.4	17.6	23.2	28.8	35.2
	101	28.8	35.2	46.4	57.6	70.4
	110	57.6	70.4	92.8	115.2	140.8
	111	115.2	140.8	185.6	230.4	281.6
01	000	0.9	1.1	2.35	3.6	4.4
	001	1.8	2.2	4.7	7.2	8.8
	010	3.6	4.4	9.4	14.4	17.6
	011	7.2	8.8	18.8	28.8	35.2
	100	14.4	17.6	37.6	57.6	70.4
	101	28.8	35.2	75.2	115.2	140.8
	110	57.6	70.4	150.4	230.4	281.6
	111	115.2	140.8	300.8	460.8	563.2
10	000	0.9	1.1	4.15	7.2	8.8
	001	1.8	2.2	8.3	14.4	17.6
	010	3.6	4.4	16.6	28.8	35.2
	011	7.2	8.8	33.2	57.6	70.4
	100	14.4	17.6	66.4	115.2	140.8
	101	28.8	35.2	132.8	230.4	281.6
	110	57.6	70.4	265.6	460.8	563.2
	111	115.2	140.8	531.2	921.6	1126.4
11	000	0.9	1.1	7.75	14.4	17.6
	001	1.8	2.2	15.5	28.8	35.2
	010	3.6	4.4	31.0	57.6	70.4
	011	7.2	8.8	62.0	115.2	140.8
	100	14.4	17.6	124.0	230.4	281.6
	101	28.8	35.2	248.0	460.8	563.2
	110	57.6	70.4	496.0	921.6	1126.4
	111	115.2	140.8	992.0	1843.2	2252.8

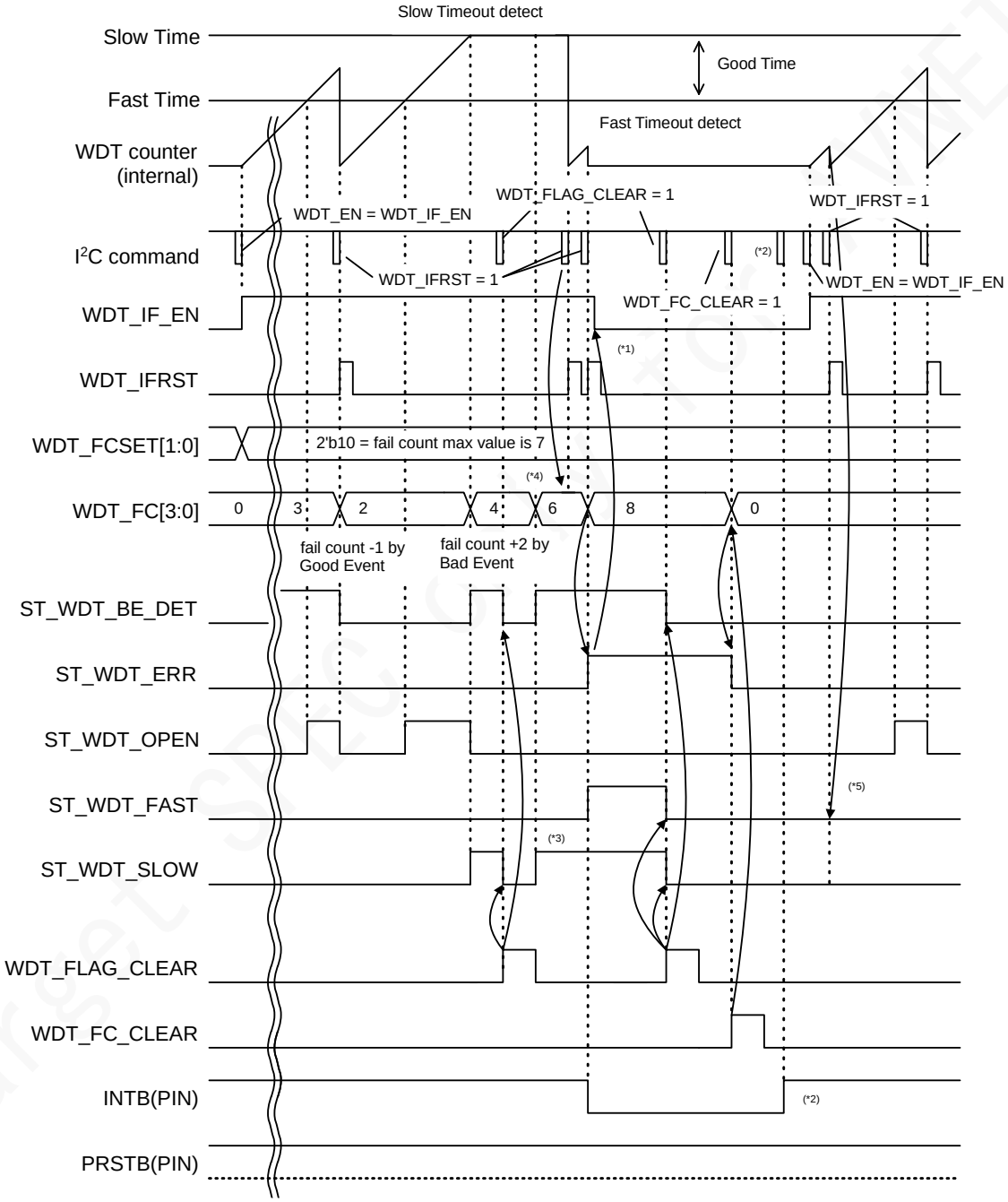
Watch Dog Timer Protocol Description – continued

There are 2 types (IF type and QA type) of the Watch Dog Timer.

IF Type WDT

In IF type, WDT counter is cleared by WDT_IFRST register via I^2C command. When the reset timing is in good time, the failure counter is decremented -1. When the reset timing is not in good time, the failure counter is incremented +2. If the failure counter reaches max value which is set by WDT_FCSET, WDT_ERR occurs.

<Condition>
WDT_TYPE = "0" (Window Type)
WDT_PRSTB_INTB = "0" (When WDT_ERR occurs, only INTB = L assert, No PRSTB = L assert)
WDT_SLOWMD = "0" (When slow timeout detects, No Counter Clear)

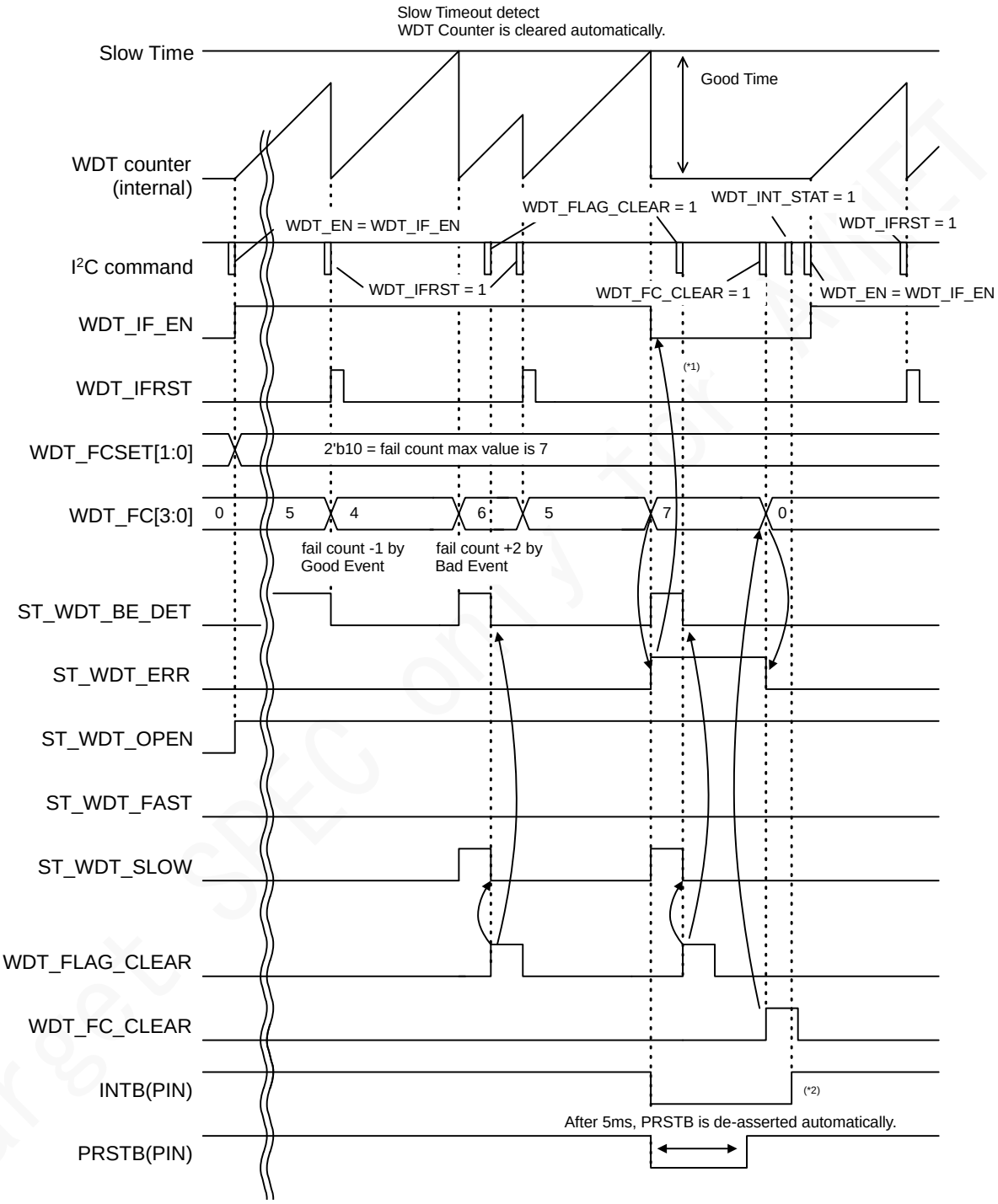


(*1) By Watch Dog Timer Error detection, WDT enable setting is cleared automatically.
(*2) Writing WDT_INT_STAT = 1. INTB is de-asserted by WDT_INT_STAT register clear.
(*3) After slow timeout detection, when there is not WDT_IFRST writing, next slow timeout is detected.
(*4) Fail counter is not decremented by WDT_IFRST after slow timeout detection.
(*5) When first WDT_IFRST timing is Fast Timeout after WDT_IF_EN = H, it is ignored.

Figure 24. IF WDT Window Type

Watch Dog Timer Protocol Description – continued

<Condition>
WDT_TYPE = "1" (Timeout Type)
WDT_PRSTB_INTB = "1" (When WDT_ERR occurs, INTB and also PRSTB = L assert)
WDT_SLOWMD = "1" (When slow timeout detects, Counter Clear)



(*1) By Watch Dog Timer Error detection, WDT Enable setting is cleared automatically.
(*2) Writing WDT_INT_STAT = 1. INTB is de-asserted by WDT_INT_STAT register clear.

Figure 25. IF WDT Timeout Type

Watch Dog Timer Protocol Description – continued

QA Type WDT

In QA type, WDT counter is cleared by WDT_A register via - command. When the answer timing is correct in good time, the failure counter is decremented -1. When the answer timing is not in good time or the answer is incorrect, the failure counter is incremented +2. If the failure counter reaches max value which is set by WDT_FCSET, WDT_ERR occurs.

<Condition>
WDT_TYPE = "0" (Window Type)
WDT_PRSTB_INTB = "1" (When WDT_ERR occurs, INTB and also PRSTB = L assert)
WDT_SLOWMD = "0" (When slow timeout detects, No Counter Clear)

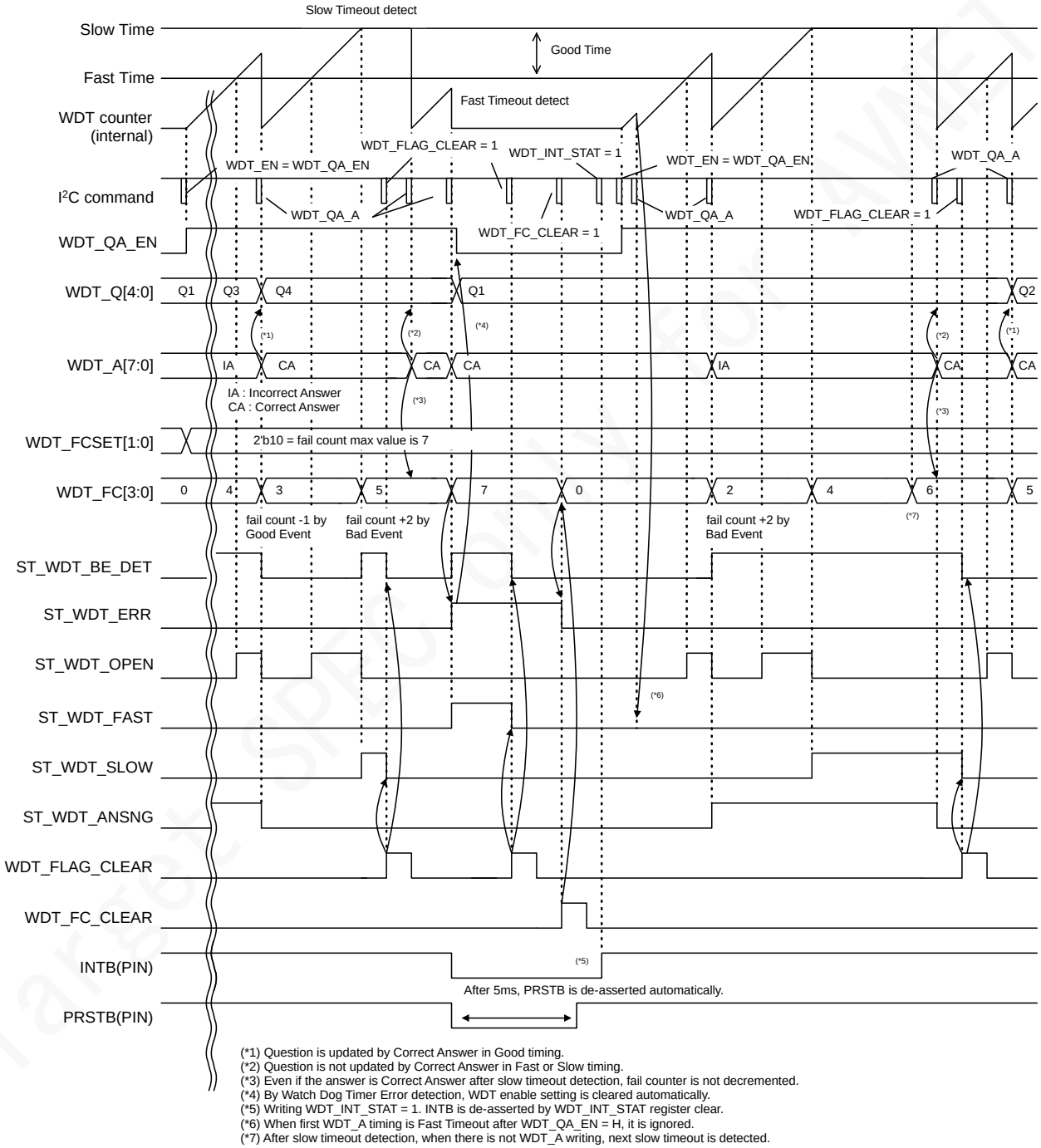


Figure 26. Q&A WDT Window Type

Watch Dog Timer Protocol Description – continued

Watch Dog Timer Correct Answer[7:0] is determined by the calculation below.

At first, X_1 to X_5 is determined by WDT_SEED[4:0] as described in the figure below.
WDT has 5 bit linear feedback shift register (LFSR), and it is used for the generation of WDT_Q[4:0].
The LFSR value is shifted by one and updated every good event.

Overview of Question generator circuit

Feedback Polynomial: X^5+X^3+1 (31cycles)
Default Value: 0x00
Bit Order: LSB

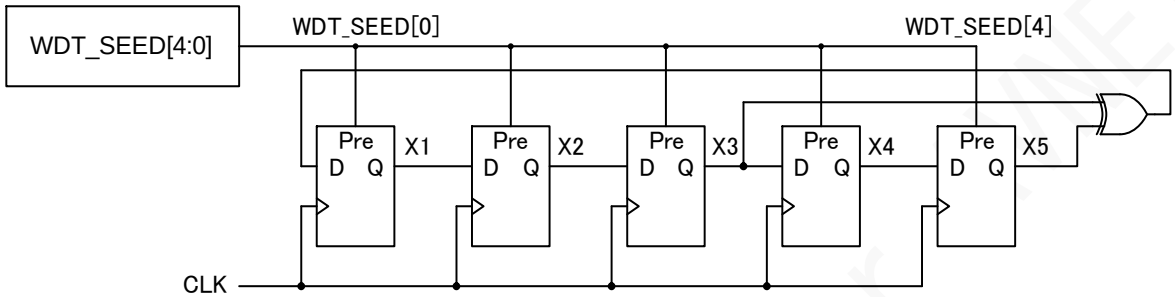


Figure 27. Question Generator1

Second, WDT_Q[4:0] is calculated by X_1 to X_5 and WDT_QCFG[4:0] as described in the figure below.

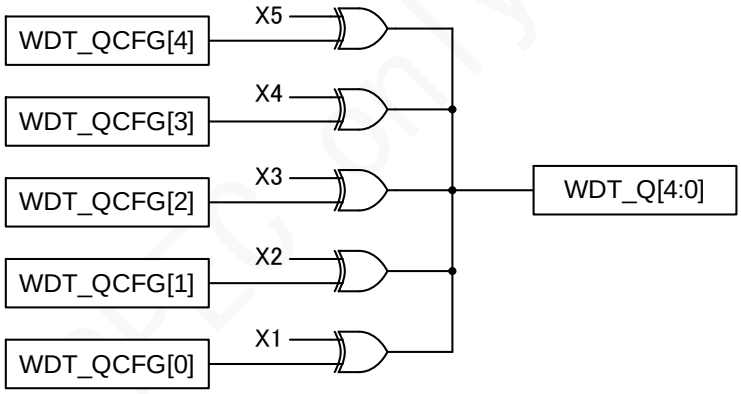


Figure 28. Question Generator2

Watch Dog Timer Protocol Description – continued

At last, Correct Answer[7:0] is selected by WDT_Q[4:0] and WDT_ANSTYPE[1:0] as described in the figure below.

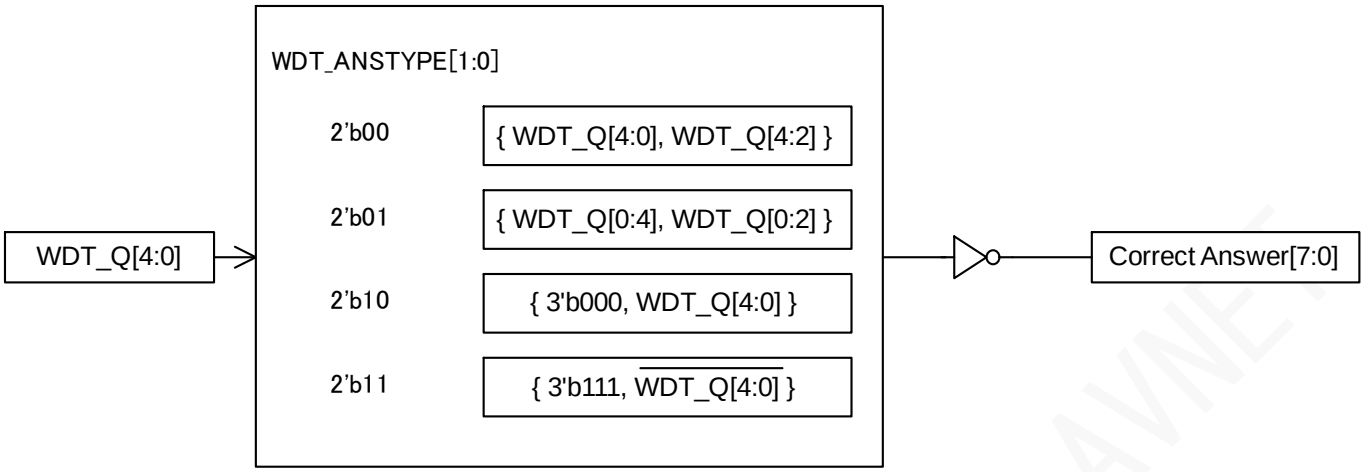


Figure 29. Answer Generator

When WDT_A[7:0] is equal to Correct Answer[7:0], it is judged as a Good Event. By Good Event, WDT_Q[4:0] is updated and Fail Count will add -1.
When WDT_A[7:0] is not equal to Correct Answer[7:0], it is judged as a Bad Event. By Bad Event, WDT_Q[4:0] is not updated and Fail Count will add +2.
WDT_ERR is detected when WDT_FC[3:0] exceed or equal to Maximum Fail Count selected by WDT_FCSET[1:0].

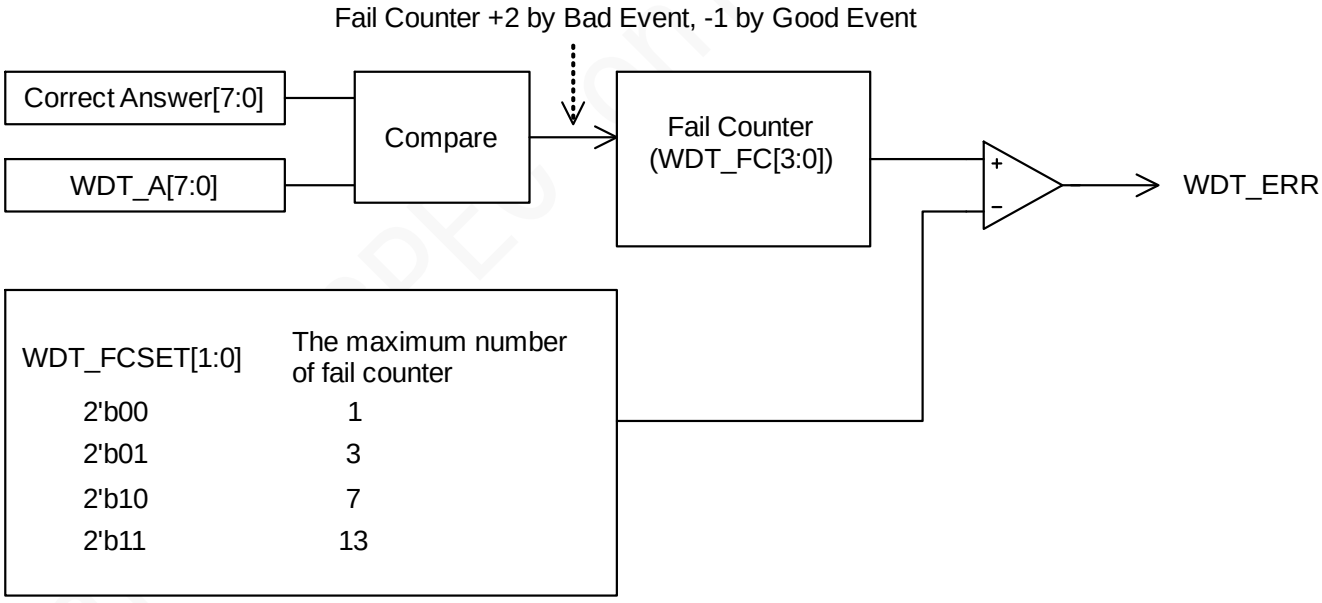


Figure 30. WDT_ERR

Application Example

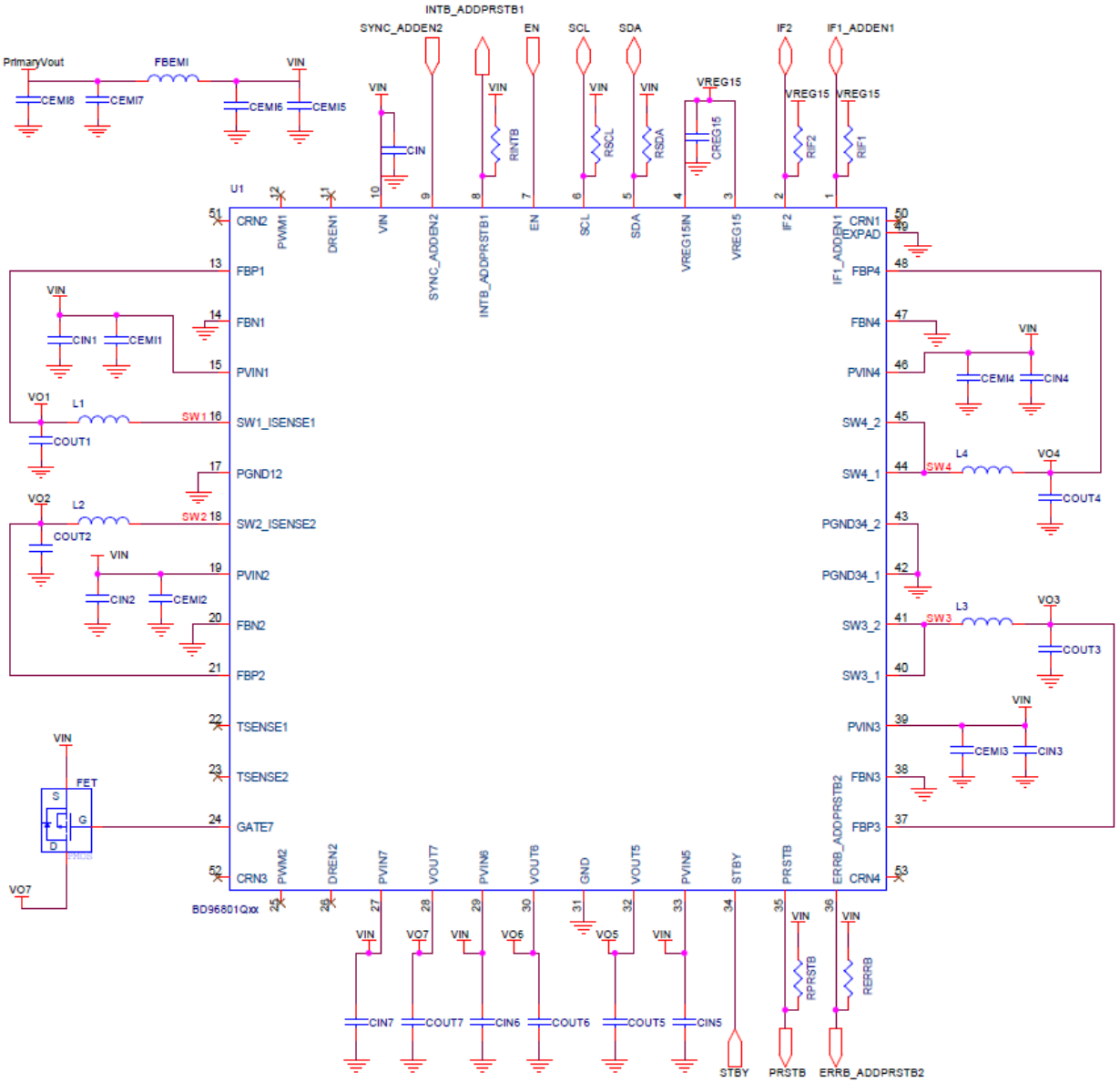


Figure 31. Application Example

Table 9. Application Example Circuit Components List

Parts name	Parameters	Manufacturer	Parts Number	Size (mm)
CIN, CIN5, CIN6, CIN7, CREG15	1 µF	Murata	GCM155C71A105KE38	1005
CIN1, CIN2, CIN3, CIN4	10 µF	TDK	CGA4J1X7S1C106K125AC	2012
CEMI1, CEMI2, CEMI3, CEMI4 (Optional)	0.1 µF	TDK	CGA2B1X7R1C104K050BC	1005
L1, L2, L3, L4	0.47 µH	TDK	TFM252012ALMAR47MTAA	2520
COUT1, COUT2, COUT3, COUT4	22 µF x N (1 or more)	TDK	CGA4J1X7T0J226M125AC	2012
COUT5, COUT6, COUT7	4.7 µF	Murata	GCM155D70G475ME36	1005
FET (Optional)	PMOS	ROHM	RQ1A070ZPHZG	3028
RIF1, RIF2 (Optional)	470 Ω (2 PMICs connection)	ROHM	MCR01 Series	1005
RSCL, RSDA	1 kΩ	ROHM	MCR01 Series	1005
RINTB, RPRSTB, RERRB	10 kΩ	ROHM	MCR01 Series	1005
FBEMI (Optional)	Ferrite Beads	Murata	BLE18PS080SH1D	1608
CEMI5, CEMI7 (Optional)	0.01 µF	TDK	CGA2B2X7R1E103K050BA	1005
CEMI6, CEMI8 (Optional)	0.47 µF	TDK	CGA2B3X7S1A474K050BB	1005

Selection of Components Externally Connected

1. Selection of the inductor Lx value

Basically use the value in the table below for the inductor value. The internal phase compensation is OTP set based on the inductor value and output capacitor value. In addition, there is a constraint that the DCR is 100 mΩ or less.

MODE	Frequency	Inductor value	Recommended parts number
Internal FET mode for BUCKs	2.25 MHz	0.47 µH	TFM252012ALMAR47MTAA
	4 MHz	0.22 µH to 0.47 µH	TFM252012ALMAR22MTAA TFM252012ALMAR47MTAA
Driver MOS mode for BUCK1 and BUCK2	2.25 MHz	0.1 µH	XEL4030-101ME
	4 MHz	0.1 µH	XEL4030-101ME

2. Selection of the output capacitors

Basically use the value in the table below for the capacitor value. The internal phase compensation is OTP set based on the inductor value and output capacitor value.

Channel	capacitor value	Recommended parts number
BUCKs	22 µF x N pcs or more (1 pcs per 2 A)	CGA4J1X7T0J226M125AC
Driver MOS	22 µF x N pcs or more (1 pcs per 2 A)	CGA4J1X7T0J226M125AC
LDOs	1 µF x 2 pcs or more or 4.7 µF or more	GCM155C71A105KE38 or GCM155D70G475ME36
VREG15	1 µF	GCM155C71A105KE38

For LDO output capacitor, if output capacitor value that cannot be charged with a maximum current of 300 mA is connected, startup failure will occur.

Slew rate setting 2Ch, 2Dh, 2Eh LDOx_SR (x = 5 to 7)	Output voltage setting 25h, 26h, 27h	The slew rate set by setting	Maximum output capacitor
0	0x00 to 0x16 (0.300 V to 0.850 V)	1 V/ms	100 µF
	0x17 to 0x36 (0.875 V to 1.650 V)	2 V/ms	100 µF
	0x37 to 0xFF (1.675 V to 3.300 V)	4 V/ms	75 µF
1	0x00 to 0x16 (0.300 V to 0.850 V)	2 V/ms	100 µF
	0x17 to 0x36 (0.875 V to 1.650 V)	4 V/ms	75 µF
	0x37 to 0xFF (1.675 V to 3.300 V)	8 V/ms	37.5 µF

3. Selection of the input capacitors

Basically use the value in the table below for the capacitor value. For disabled channel PVIN, input capacitor is not needed.

Channel	capacitor value	Recommended parts number
VIN	1 µF	GCM155C71A105KE38
PVIN1 to PVIN4	10 µF or more	CGA4J1X7S1C106K125AC
Driver MOS PVIN	22 µF x 2 pcs or more	CGA4J1X7T0J226M125AC
	0.47 µF x 2 pcs	CGA2B3X7S1A474K050BB
	0.01 µF x 2 pcs	CGA2B3X7R1H103K050BB
PVIN5 to PVIN7	1 µF	GCM155C71A105KE38

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

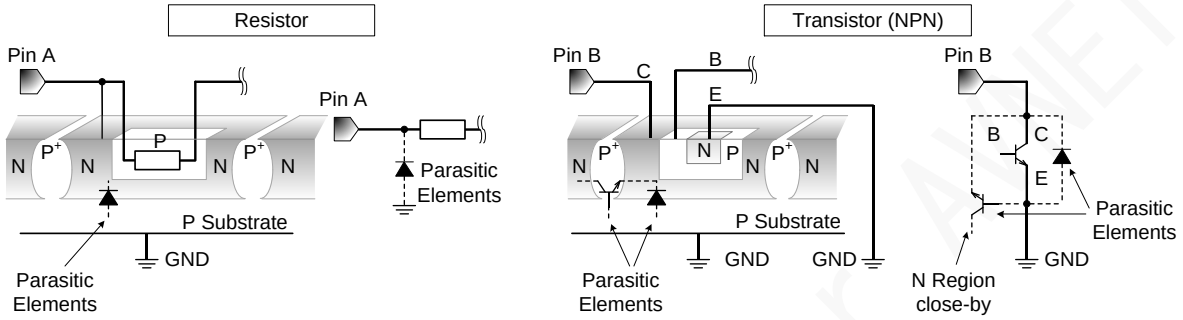


Figure 32. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. The IC should be powered down and turned ON again to resume normal operation because the TSD circuit keeps the outputs at the OFF state even if the Tj falls below the TSD threshold.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

14. Functional Safety

"ISO 26262 Process Compliant to Support ASIL-*"
A product that has been developed based on an ISO 26262 design process compliant to the ASIL level described in the datasheet.

"Safety Mechanism is Implemented to Support Functional Safety (ASIL-*)"
A product that has implemented safety mechanism to meet ASIL level requirements described in the datasheet.

"Functional Safety Supportive Automotive Products"
A product that has been developed for automotive use and is capable of supporting safety analysis with regard to the functional safety.

Note: "ASIL-*" is stands for the ratings of "ASIL-A", "-B", "-C" or "-D" specified by each product's datasheet.

Ordering Information

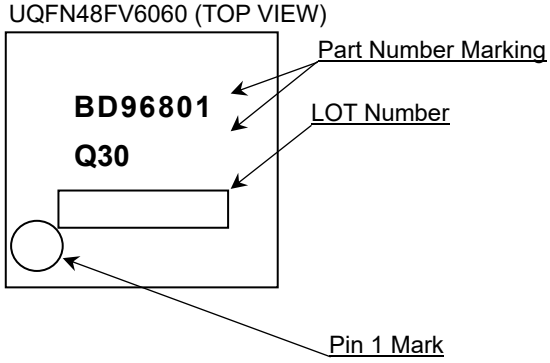
B	D	9	6	8	0	1	Q	3	0	-	CE 2

Part Number

Product Rank
C: for Automotive
Packaging and forming specification
E2: Embossed tape and reel

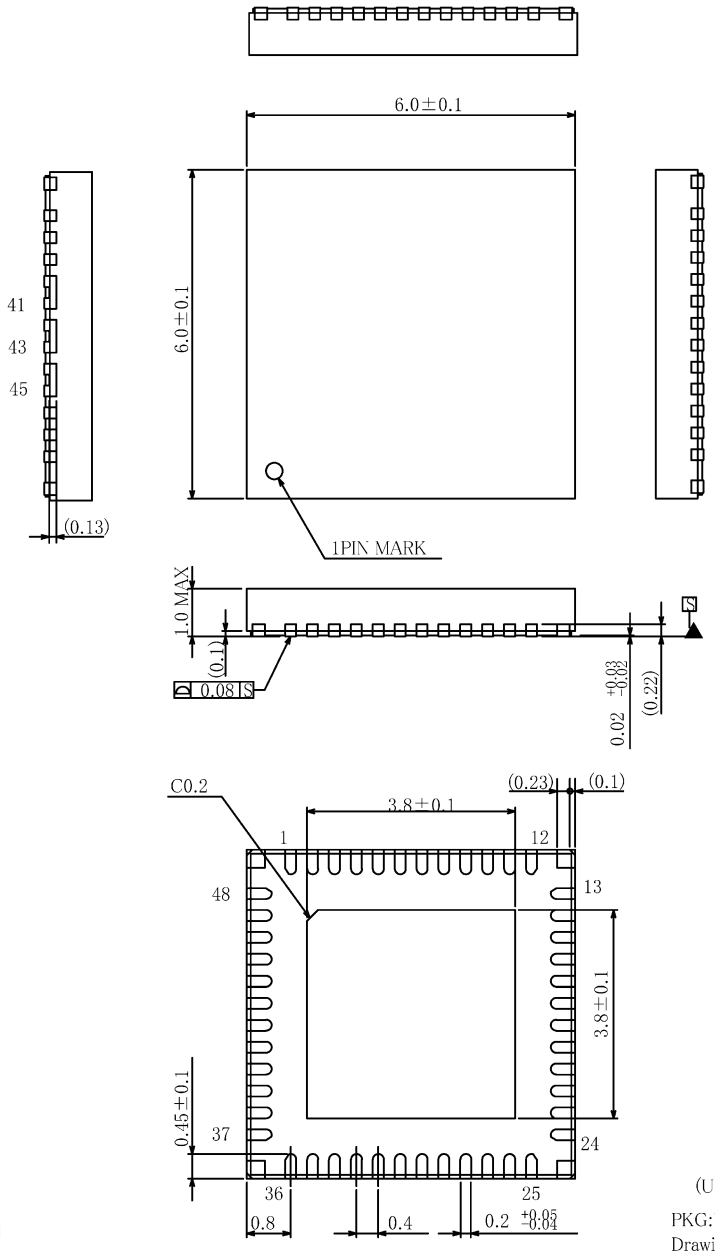
Marking Diagram

UQFN48FV6060 (TOP VIEW)



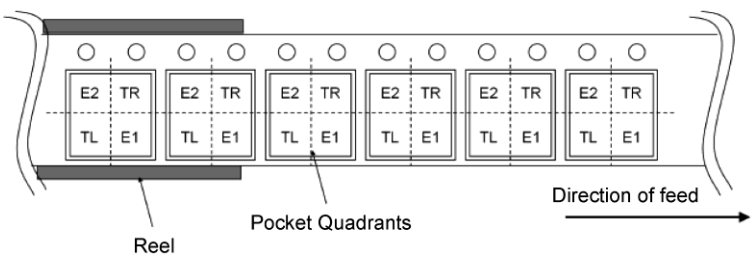
Physical Dimension and Packing Information

Package Name	UQFN48FV6060



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
5.Apr.2024	001	New Release