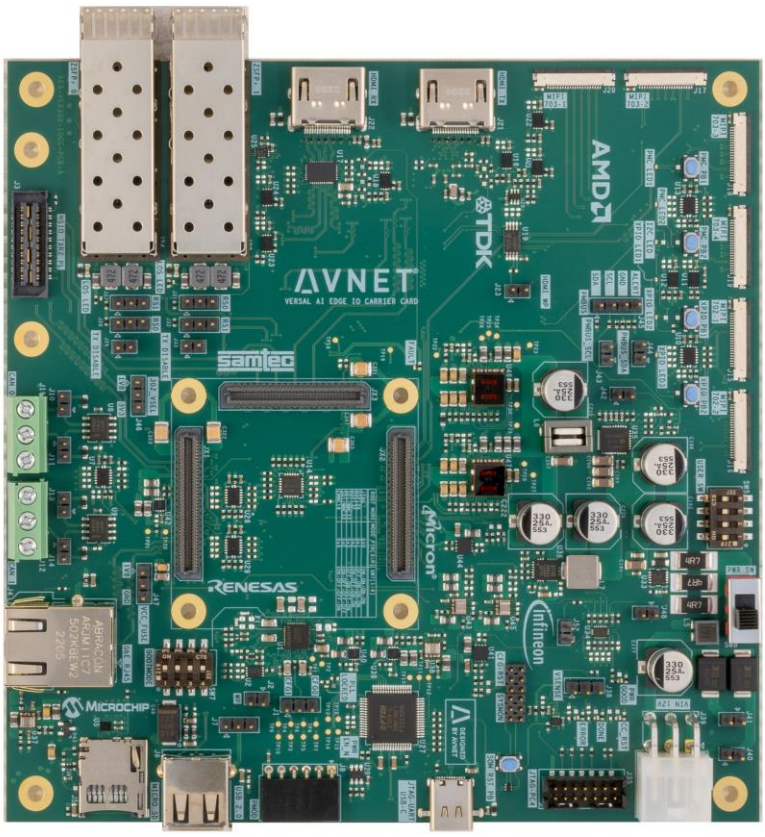

Versal™ AI Edge Carrier Card Hardware User Guide

Version 1.2

LIT# VE2302-IOCC-UG-V1P2

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1 Document Control

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2 Version History

Version	Date	Comment
1.0	6/13/2025	Initial Release
1.1	6/30/2025	Master JX Table Correction
1.2	8/5/2025	Master JX Table Correction

3 Introduction

The Versal™ AI Edge Carrier Card is a development board designed to be used by customers for rapid proof-of-concept and prototype development efforts using the Tria Technologies VE2032 System-On-Module (SOM). Leveraging the Tria Technologies VE2302 Development Kit (which includes the VE2302 SOM and the Versal™ AI Edge Carrier Card) greatly reduces time to market and hardware risk by decreasing target application development time on a reliable hardware platform.

The Versal™ AI Edge Carrier Card provides the VE2302 SOM necessary power regulation and sequencing, system clocks, reset control, and I/O accessibility through the JX1, JX2, and JX3 Micro Headers along with providing industry standard interfaces such as GbE and USB 2.0.

The Versal™ AI Edge Carrier Card provides two debug interfaces – FTDI JTAG (USB Type-C) and PC-4 JTAG header. The PC-4 requires a debug module such as the Digilent® HS3 dongle. Both debug interfaces are provided to assist with VE2302 SOM application development.

This document details the specific features, operation, and configuration of the Versal™ AI Edge Carrier Card. Please visit **http://avnet.me/ve2302-dk** for the latest product information on the VE2032 Development Kit which includes the VE2302 SOM and the Versal™ AI Edge Carrier Card.

4 Architecture and Features

The Versal™ AI Edge Carrier Card provides a hardware environment for developing designs targeting the AMD Versal™ AI Edge XCVE2302-1LSESFVA784. The Versal™ AI Edge Carrier Card provides features common to many systems such as TX/RX HDMI Interfaces, MIPI CSI/DSI, Gigabit Ethernet, USB2.0, general purpose I/O, and UART interfaces. The details for the Versal™ AI Edge Carrier Card features are described in Functional Description sections that follow.

4.1 List of Features

The Versal™ AI Edge Carrier Card supports the following features:

- Connections to the VE2302 SOM:
  - Three 160-pin JX Connectors (JX1, JX2, JX3)
  - Samtec 0.635 mm HD High-Density 4-Row Terminal
  - Part Number: **ADM6-40-01.5-L-4-0-A**
- High-Speed IO (HSIO) Board-to-Board Connector
  - Samtec Q-Strip High Performance 40-Pin 0.5mm Differential Pair Array
  - Part Number: **QTH-020-01-F-D-DP-A-K-TR**
- x4 MIPI CSI2 or MIPI DSI 22-pin Connectors
  - Molex Conn, 22 Position FFC, FPC 0.50mm SMT, RA (MIPI)
  - Part Number: **545482272**
- HDMI TX and RX Interfaces
  - Molex Conn RCPT HDMI V2.1 19Pos SMD RA
  - Part Number: **2086581061**
- x2 CAN Interfaces
  - Wurth Elektronik Pluggable Terminal Blocks
  - Part Number: **69111710003**
- x2 SFP28 Interfaces
  - TE Connectivity SFP112 Receptacle Connector
  - Part Number: **2378765-1**
- Gigabit Ethernet RJ45 Connector
  - Abracon LLC 1000 Base-T Magnetics Module

    - Part Number: **ARJM11C7-502-KB-EW2**
- USB 2.0
    - Samtec USB Type A Single Through-hole Connector
    - Part Number: **USB-A-S-F-B-TH**
- microSD Card Connector
    - Molex 1.10mm Pitch microSD Memory Card Connector
    - Part Number: **5025700893**
- USB Type-C
    - USB 3.1 TYPE C 5G Mid Mount
    - Part Number: **E8124-010-01**
- JTAG Connector
    - 14P SMD PB FREE SHRD
    - Part Number: **87832-1420**
- Clock Generation
    - Renesas FemtoClock™ NG Universal Frequency Translator
    - Part Number: **8T49N241-998NLGI**
- x6 GPIO LEDs
    - Everlight Electronics Co Ltd Led Red Diffused 2SMD
    - Part Number: **EAST0603RA0**
- x4 Push Buttons
    - C&K Switch Tactile SPST-NO 0.05A 16V
    - Part Number: **PTS810 SJG 250 SMTR LFS**
- 4-Pos Dip Switch
    - CTS Electronic Components Series 219 4 Positions SMD DIP Switch
    - Part Number: **219-4MSTR**
- Boot Mode Dip Switch
    - CTS Electronic Components Series 219 4 Positions SMD DIP Switch
    - Part Number: **219-4MSTR**
- Voltage Regulators
    - LDO Voltage Regulators
    - Part Number: **AP7361-FGE-7**
    - Infineon Technologies Switching Regulator / Converter
    - Part Number: **IR3899AMTRPBFXUMA1**
    - Part Number: **TDA387250000AUMA1**
    - TDK Buck Regulator / Converter
    - Part Number: **FS1406-0600-AS**
- Power Load Switch
    - Onsemi Controlled Load Switch with Low RON
    - Part Number: **NCP45524IMNTWG-H**
- Power Sequencer
    - Renesas GreenPak™ Custom Power Sequencer
    - Part Number: **SLG7AV46723V**

The following table is a glossary of acronyms that will be used in description of the Versal™ AI Edge Carrier Card.

Term	Definition
PS	Adaptive SoC Processing System
PL	Adaptive SoC Programmable Logic
MIO	Multiplexed Input Output Pins
LPD	Low Power Domain
PMC	Platform Manager Controller
PLM	Platform Loader and Manager
POR	Power On Reset
APU	Application Processing Unit
RPU	Real-time Processing Unit
GPU	Graphics Processing Unit
SYSMON	System Monitor
ADC	Analog-to-Digital Converter
HDIO	High Density PL I/O Pins
XPIO	High Performance PL I/O Pins
PMBus	Power Management Bus
PDM	Power Design Manager
OOB	Out-of-Box

Table 1 – Glossary

4.2 Additional Information

Additional information and documentation on the AMD Versal™ Adaptive SoC can be found Here: **https://www.amd.com/en/products/adaptive-socs-and-fpgas/versal.html**

Additional information and documentation on the Tria Technologies VE2302 SOM product line can be found here: **http://avnet.me/ve2302-som**

Additional information and documentation on the Tria Technologies VE2302 Development Kit can be found here: **http://avnet.me/ve2302-dk**

4.3 Block Diagram

The following figure is a high-level block diagram of the Versal™ AI Edge Carrier Card and the peripherals attached to the VE2302 SOM.

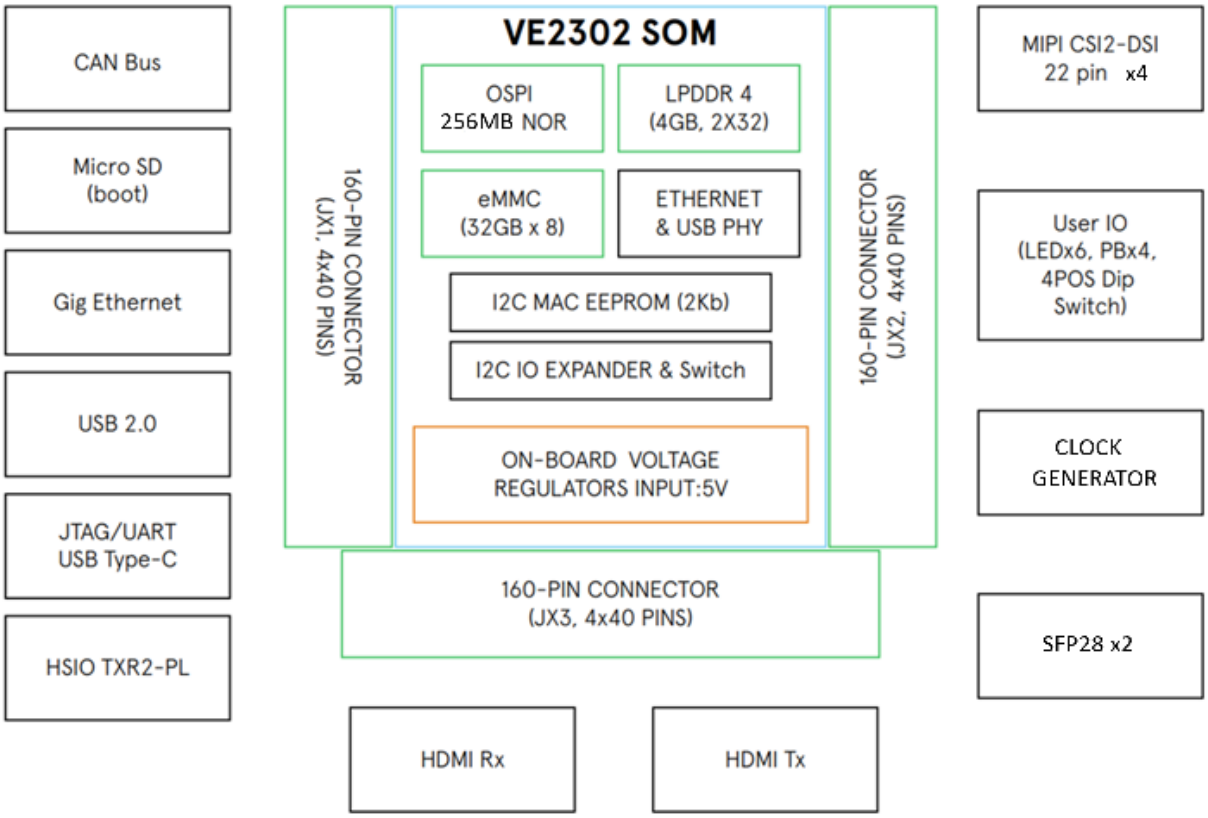

Figure 1 – Versal™ AI Edge Carrier Card Block Diagram

5 Functional Description

The following sections provide brief descriptions of each feature provided on the Versal™ AI Edge Carrier Card.

5.1 Interfaces and Connectors

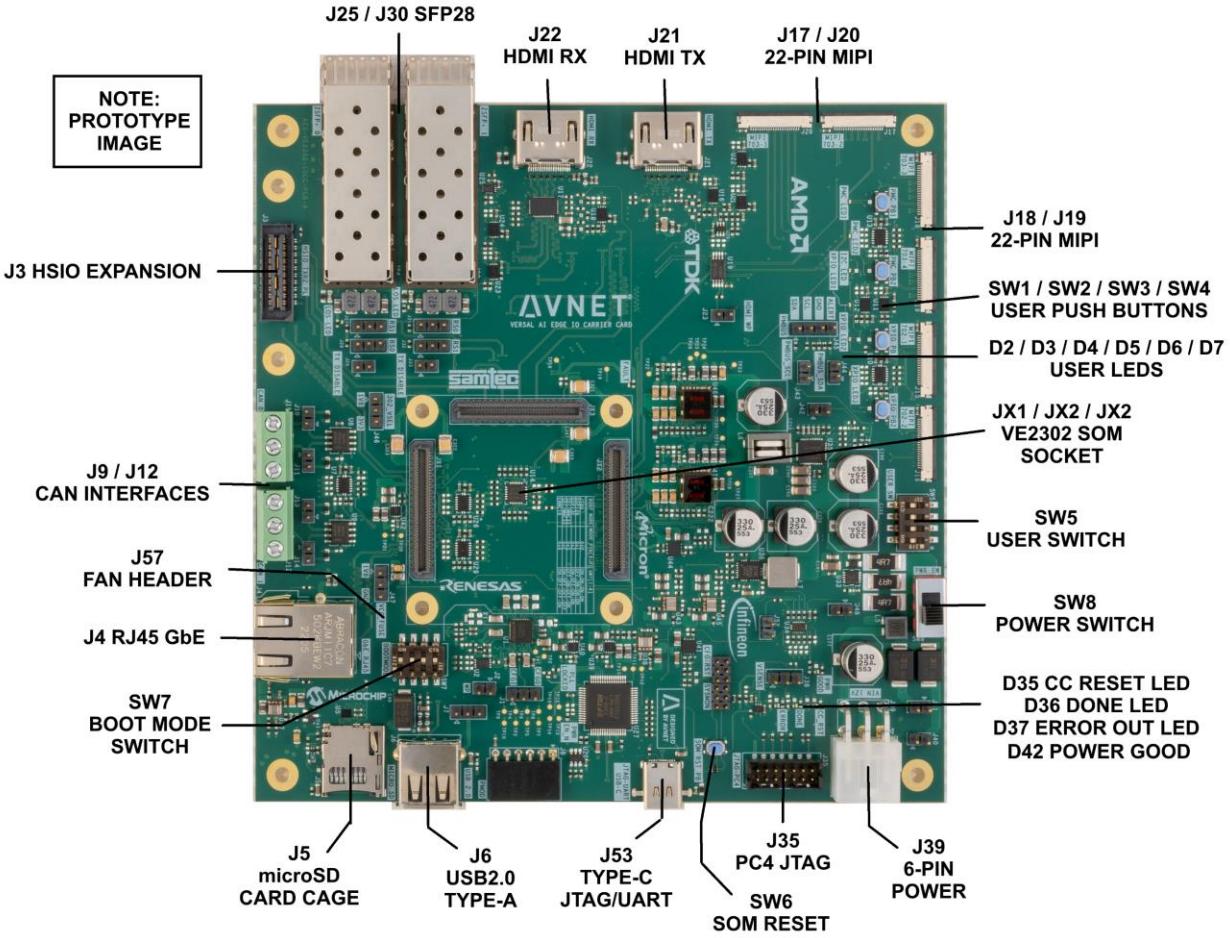

Figure 2 – Interfaces and Connectors (Preliminary)

5.2 Powering the Versal™ AI Edge Carrier Card

The Versal™ AI Edge Carrier Card requires a 12V / 5A or better power supply to power the solution at a minimum. Some designs that fully utilize the available resource in the Versal™ AI Edge device may require a larger power supply such as an available 12V / 10A supply. The power supply requires a 6-pin connector that plugs into the 6-pin power receptacle (**J39**) to supply the +12V power source to Versal™ AI Edge Carrier Card.

CAUTION! Do NOT plug a PC ATX power supply or PCIe power supply 6-pin connector into the Versal™ AI Edge power connector **J39**. The PC ATX or PCIe power supply 6-pin connectors have different pinouts than **J39**. Connecting one of these 6-pin connectors into **J39** can damage the board and will void the board warranty.

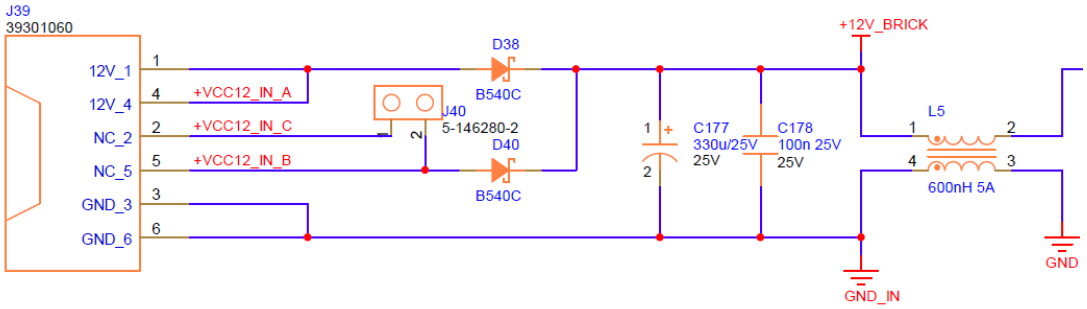

Figure 3 – 6-pin Power Receptacle Pinout

To power up the Versal™ AI Edge Carrier Card, a user must switch the **SW8** Power Switch to the ON position to get power sequencing on to the board.

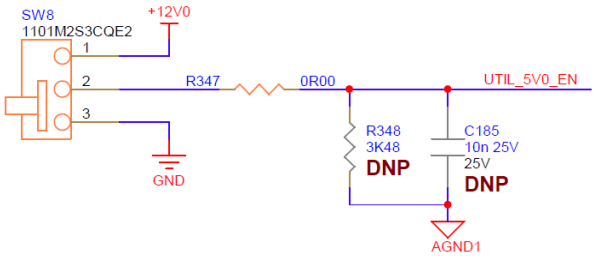

Figure 4 – Power Switch

To power down the Versal™ AI Edge Carrier Card a user must switch the **SW8** Power Switch to the OFF position to turn being sequencing power off the board.

The Versal™ AI Edge Carrier Card provides the power supply rails and control necessary to ensure the appropriate power sequencing, device power budgets, and interface power budgets are met. The following is a brief description of the power supply sequence.

- The Versal™ AI Edge Carrier Card has an on-board regulator that generates a 5V supply and provides power to other voltage regulators and the VE2302 SOM.
- The VE2302 SOM power rail (+VIN) is powered by the 5V supply.
- The VE2302 SOM on-board power-on sequencing starts after always-on regulators are stable with the assertion of **SOM_PWR_ENB_IN**.
- The Versal™ AI Edge Carrier Card and VE2302 SOM handshake the intermediate control of supply +VCCO_702 using **VCCO_702_ENB_OUT** and **VCCO_702_PG_IN**.
- The VE2302 SOM indicates to the Versal™ AI Edge Carrier Card that it has completed its power sequence with the assertion of **SOM_PG_OUT**. The carrier card may then complete its power sequence for the remaining regulators.
- Power good indicator LED **D42** will illuminate indicated power up success.

The Versal™ AI Edge Carrier Card supplies power to I/O peripherals as specified by the following interface specifications.

- **USB2.0** – The USB2.0 interface port can deliver a 5V supply to the attached I/O peripherals with up to 500mA. The port is protected against an over-current event through a current-limiting high-side power-switch on the VE2302 SOM.

- **microSD Card** – The microSD card is support by the 3.3V supply voltage. The supply to this interface is not limited.

- **High-Speed I/O (HSIO) Interface** – The HSIO interface is supplied with 3.3V from an on-board utility regulator as well as with 1.8V or 3.3V from +VCCO_302. The +VCCO_302 voltage is passed from the selection of the voltage rail by shunting jumper **J46** appropriately. 1.8V for +VCCO_302 is generated from an on-board 1.8V regulator and 3.3V for +VCCO_302 is generated from an on-board 3.3V regulator.

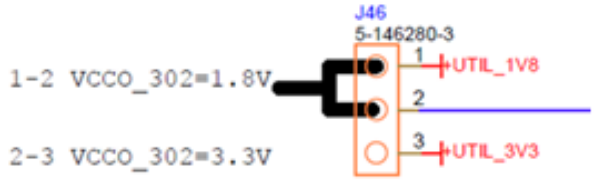

Figure 5 – VCCO_302 Voltage Select

- **CAN Interfaces** – There are two CAN interface on the Versal™ AI Edge Carrier Card. Each interface is supplied with 5V and 3.3V. The supplies to these interfaces are delivered by the +UTIL_5V power supply and the 3.3V +UTIL_3V3 power supply.

- **MIPI DSI Interface** – There is a 3-pin header used to power MIPI DSI Displays with 5V. The supply to this header is delivered by the +UTIL_5V power supply.

- **HDMI TX Interface** – There is a small power supply used to provide the HDMI TX connector interface with 5V. The supply to this header is delivered by the +UTIL_5V power supply.

- **SFP28 Interfaces –** The SFP28 interfaces get powered by the +UTIL_3V3 on-board regulator.

- **JTAG Interface** – The JTAG interface gets powered by the +UTIL_3V3 on-board regulator.

5.3 Power-On and Processor Subsystem Resets

The Versal™ AI Edge APSoC processing system supports an external power-on reset signal, **POR_B**. The power-on reset signal is the master reset of the Versal™ AI Edge APSoC device. The power-on reset signal resets every register in the device capable of being reset. On the Versal™ AI Edge Carrier Card this reset signal is labelled **SOM_RESET_IN_B** and it is connected to a push button, **SW6**.

To stall the Versal™ AI Edge APSoC boot-up, this reset signal should be held low. Pressing **SW6** will cause the **CC_RESET_B** LED **D35** to turn-on.

The power-on reset signal **SOM_RESET_IN_B** resets several interfaces on the Versal™ AI Edge Carrier Card when it is returned from the VE2302 SOM as **CC_RESET_OUT_B**. The microSD card interface, I2C bus switch, and the IO Expander interface are reset upon **CC_RESET_OUT_B** being pulled low by **SOM_RESET_IN_B**. The **SOM_RESET_IN_B** is an active-low input signal to the **JX** Connector (**JX2-B32**).

The **SOM_RESET_IN_B** signal is a combination of voltage rail monitoring, manual assertion (**SW6**), JTAG reset, and FTDI reset. The **SOM_RESET_IN_B** on the Versal™ AI Edge Carrier Card is implemented as OPEN-DRAIN output. The **SOM_RESET_IN_B** is pulled up on the VE2302 SOM.

Header **J37** can be utilized to add in the PC4 connector reset signal and / or the FTDI reset signal to the OPEN-DRAIN output of **SOM_RESET_IN_B.**

Pin Shunted (J37)	Operation Mode
1 - 2	SOM_RESET_IN_B driven by push-button only
3 - 4	SOM_RESET_IN_B connected to FTDI_POR_B
5 - 6	SOM_RESET_IN_B connected to PC4_POR_B (JTAG connector)

Table 2 – SOM RESET Header Configurations

A small push switch is used to manually assert the **SOM_RESET_IN_B** signal on the Versal™ AI Edge Carrier Card and send it to the **JX2** connector.

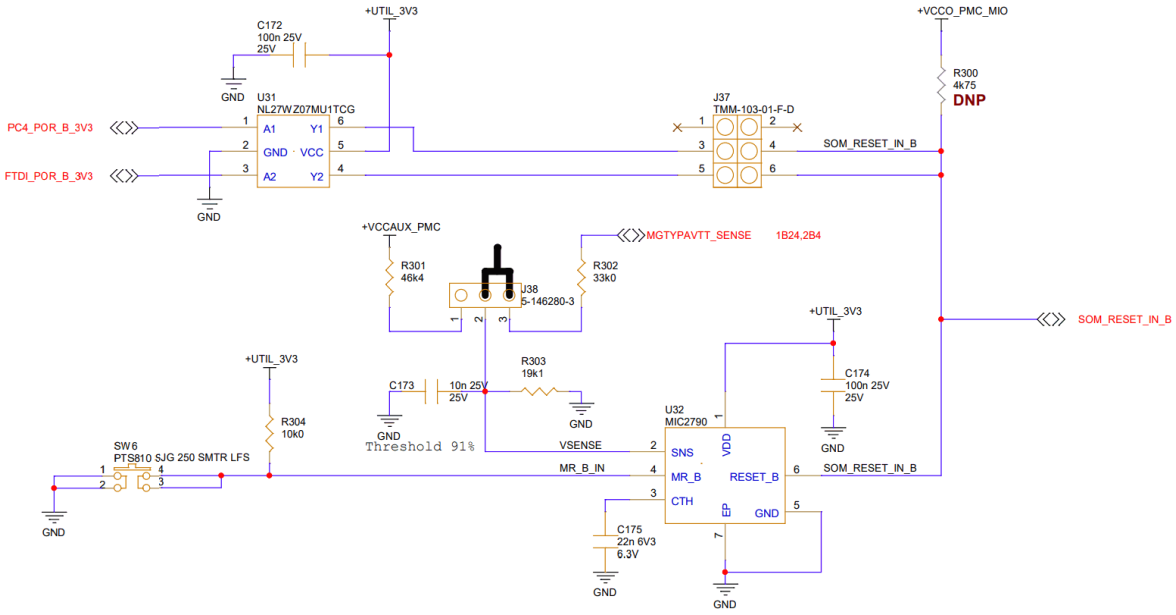

Figure 6 – RESET Structure Schematic

The Push Button (**SW6**) generates a master reset signal when asserted along with voltage monitoring to a supervisor device (**U32**) that generates the **SOM_RESET_IN_B** output. The voltage monitoring is connected to one of two pins of the **JX2** Connector based on the configuration of the Header **J38**. The voltage monitoring header **J38** selects one two voltages depending on the power up sequence and the time when **POR_B** can be released. The earliest **POR_B** can be released is after **+VCCAUX_PMC** voltage rail is stable. The latest **POR_B** can be released is after the system power is good which is indicated by the **+MGTYPAVTT** voltage rail is stable.

- Manufacturer: Micrel
- Part Number: **MIC2790**
- Supervisor with High-Accuracy
- Ultra-Fast Propagation Delay
- Capacitor-Programmable Reset Delay

Pin Shunted (J38)	Signal Name	JX Connector Pin Number
1 - 2	+VCCAUX_PMC	JX2-A32
2 - 3	MGTYPAVTT_SENSE	JX2-D20

Table 3 – Voltage Monitoring Configuration Header

NOTE: On the Versal™ AI Edge Carrier Card implements an orange LED (**D35**) is connected to the **CC_RESET_OUT_B** signal. The jumper **J54** should be shunted otherwise LED **D35** not be utilized.

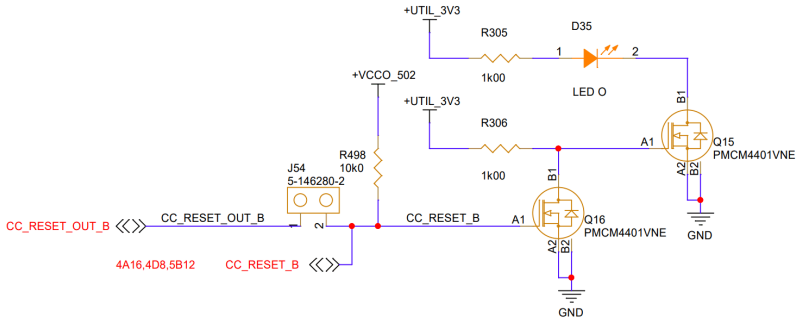

Figure 7 – CC_RESET_OUT_B LED Schematic

5.4 Status LEDs

There are several status LEDs on the Versal™ AI Edge Carrier Card. The available status LEDs are BLUE **DONE_OUT** LED indicator - **D36**, RED **ERROR_OUT** LED indicator – **D37**, ORANGE **CC_RESET_OUT_B** LED indicator – **D35**, ORANGE SFP28 Loss of Signal LED indicators – **D32** and **D33**, ORANGE JTAG Power Enable LED indicator – **D34,** a GREEN System Power Good LED indicator – **D42**, and finally a RED FS1525 Fault LED indicator – **D44**.

Net Name	LED Ref Des	Color	Function
DONE_OUT	D36	BLUE	Configuration Complete
ERROR_OUT	D37	RED	Boot Process Failure
CC_RESET_OUT_B	D35	ORANGE	Power-On-Reset / SW Reset via SOM
SFP0 LOS	D32	ORANGE	SFP0 Port Loss of Signal
SFP1 LOS	D33	ORANGE	SFP1 Port Loss of Signal
PWR_EN_B	D34	ORANGE	JTAG Powered
SYSTEM_PG_IN	D42	GREEN	System Power Good
FAULT	D44	RED	FS1525 Fault Indicator

Table 4 – Status LED Indicators

As an example, the Versal™ AI Edge Carrier Card implements a Blue Diffused 2SMD LED (**D36**) indicating the configuration complete. The **DONE_OUT** signal is a 1.8V signal and care must be taken to ensure that the LED illuminates properly.

- Manufacturer: Everlight Electronics Co Ltd
- Part Number: **EAST0603BA0**
- +3.3 V

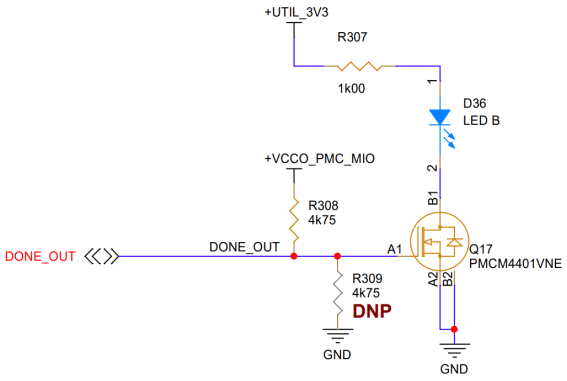

Figure 8 – DONE_OUT LED Schematic

I/O Net Name	JX Connector
DONE_OUT	JX1-D28

Table 5 – DONE_OUT LED Pin Assignment

Similarly, the Versal™ AI Edge Carrier Card implements an **ERROR_OUT** Red Diffused 2SMD LED (**D37**). The **ERROR_OUT** signal is a 1.8V signal and care must be taken to ensure that the LED illuminates properly.

- Manufacturer: Everlight Electronics Co Ltd
- Part Number: **EAST0603RA0**
- +3.3 V

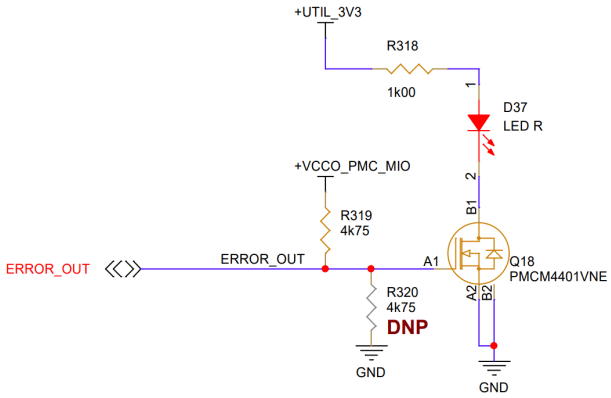

Figure 9 – ERROR_OUT LED Schematic

I/O Net Name	JX Connector
ERROR_OUT	JX1-D13

Table 6 – ERROR_OUT LED Pin Assignment

5.5 System Monitor Connector

The Versal™ AI Edge Carrier Card supports System Monitor functionality through the SYSMON header (**J36**). The SMON_V_P and SMON_V_N pins on the board are connected to the **JX1** Connector.

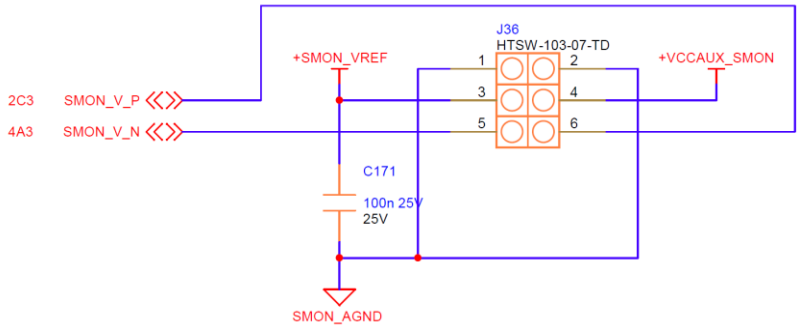

Figure 10 – SYSMON Voltage Reference Select

I/O Net Name	JX1 Connector
+SMON_VREF	JX1-A40
SMON_V_P	JX1-B40
SMON_V_N	JX1-C40
+VCCAUX_SMON	JX1-D40
SMON_AGND	JX1-A39 / JX1-B39 JX1-C39 / JX1-D39

Table 7 – SYSMON Signals Pin Assignment

5.6 Encryption Key Backup Circuit

The Versal™ AI Edge Carrier Card includes an encryption key backup battery circuit. The circuit is design to support a rechargeable 1.5V lithium button-type battery, **B1**, that is to be soldered to the board with the positive output connected to the Connector **JX1** VCC_BATT pin D27. **B1** is charged from the **+UTIL_1V8** +1.8V rail through a series diode and a 4.75 kΩ current limit resistor.

NOTE: Do to shipping restrictions, the rechargeable battery, **B1**, is not included with the platform, and it is expected that an end-user that requires use of the encryption key backup feature would procure and properly install the rechargeable battery.

- Manufacturer: Seiko Semiconductors
- Part Number: **TS621E-FL11E**
- Style: 1.5V Coin Cell Battery

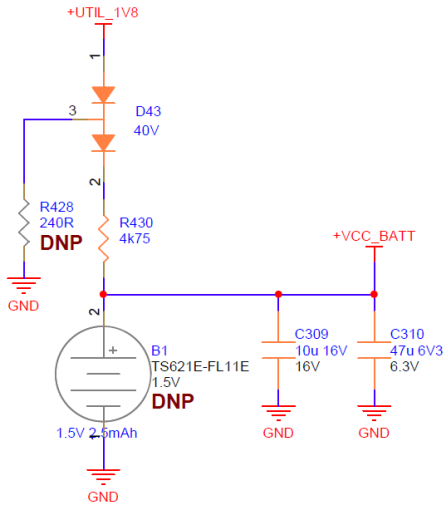

Figure 11 – Encryption Key Backup Circuit

5.7 Clock Sources

The Versal™ AI Edge Carrier Card shares four clock sources with the VE2302 SOM. The first is a programmable clock source (**U1**) for the HDMI TX interface and three LVDS Oscillators (**U48, U49,** and **U70**). The VE2302 SOM provides one HDMI recovered clock to the Versal™ AI Edge Carrier Card. These clocks are shared via the **JX** connectors.

NOTE: The clock sources related to the HDMI RX and HDMI TX interfaces are described in detail in the HDMI sections of this document. Those clock sources are associated with **GTYP_103_REFLCLK0_P/N, GTYP_104_REFCLK0_P/N, GTYP_104_REFCLK1_P/N,** and **XPIO_702_L23_P/N_CLKIN_CG**.

Connector (JX) Pin	Schematic Net Name	I/O Standard	Clock Ref	Pin	Description
JX3-C7	GTYP_103_REFCLK0_P	LVDS	U70	4	400MHz Reference Clock for GT (HDMI FRL)
JX3-C8	GTYP_103_REFCLK0_N	LVDS		5	
JX3-D10	GTYP_103_REFCLK1_P	LVDS	U71	11	Select between 156.25MHz (U48) or HSIO GT REFCLK
JX3-D11	GTYP_103_REFCLK1_P	LVDS		10	
JX3-B10	GTYP_104_REFCLK1_P	LVDS	U1	22	Programmable HDMI Reference Clock for GT
JX3-B11	GTYP_104_REFCLK1_N	LVDS		23	
JX3-A7	GTYP_104_REFCLK0_P	LVDS	-	-	HDMI RX Reference Clock from Connector
JX3-A8	GTYP_104_REFCLK0_P	LVDS		-	
JX1-D14	SYSCLK_P	LVDS	U49	4	200.00MHz System Reference Clock
JX1-D15	SYSCLK_N	LVDS		5	
JX2-B33	XPIO_702_L23_P_CLKIN_CG	LVDS	U1	16	HDMI RX Recovered Clock
JX2-B34	XPIO_702_L23_N_CLKIN_CG	LVDS		17	

Table 8 – Board Clock Sources

5.7.1 System Clock Source

The Versal™ AI Edge Carrier Card implements a +3.3V LVDS 200MHz Oscillator (**U49**). It generates a signal pair that is sent to the **JX1** connector to drive the programmable logic on the VE2302 SOM.

- Manufacturer: ECS
- Part Number: **ECX-L33CN-200.000-TR**
- LVDS Oscillator 200.00 MHz

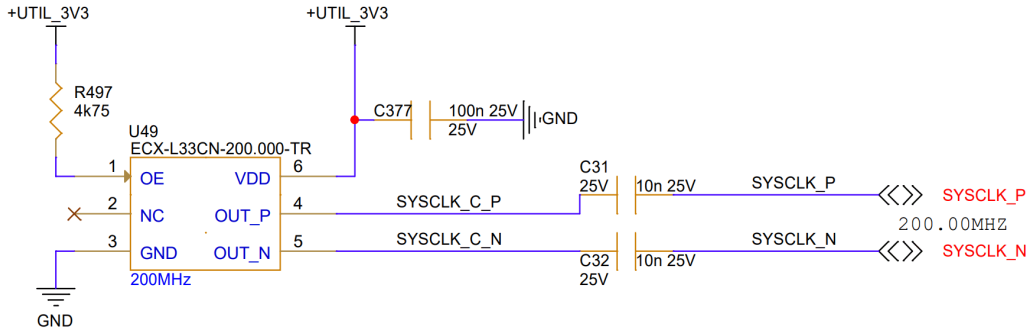

Figure 12 – System Clock Oscillator Schematic

5.7.2 Shared GTYP 103 Reference Clock

The Versal™ AI Edge Carrier Card provides a shared reference clock to GTYP quad 103 reference clock port 1, **GTYP_103_REFCLK1_P/N**. There are two sources of this are the implementation of an **ECX2-LMV** Low Jitter LVDS Oscillator (**U48**) named **GTYP_156P25MHZ_P/N** and the HSIO GT reference clock from the HSIO connector, **J3,** named **GTYP_HSIO_REFCLK_P/N**. These two clocks are selected by a clock multiplexer, **U71**, and the clock is selected by the position of jumper **J58.** This allows flexibility in the selection of the clock dependent on the interface that is being utilized within the GTYP quad.

- Manufacturer: ECS
- Part Number: **ECX2-LMV-2CN-156.250-TR**
- LVDS Oscillator 156.250 MHz

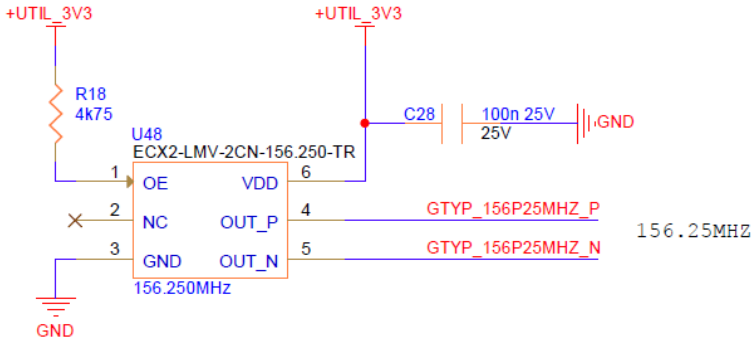

Figure 13 – GTYP Oscillator Schematic

As you can see from the following figure, shunting jumper **J58** will pull the **U71** clock select to ground and select **GTYP_HSIO_REFCLK_P/N** to **GTYP_103_REFCLK1_P/N**. Removing the shunt from jumper **J58** will pull up the **U71** clock select and select **GTYP_156P25MHZ_P/N** to **GTYP_103_REFCLK1_P/N**.

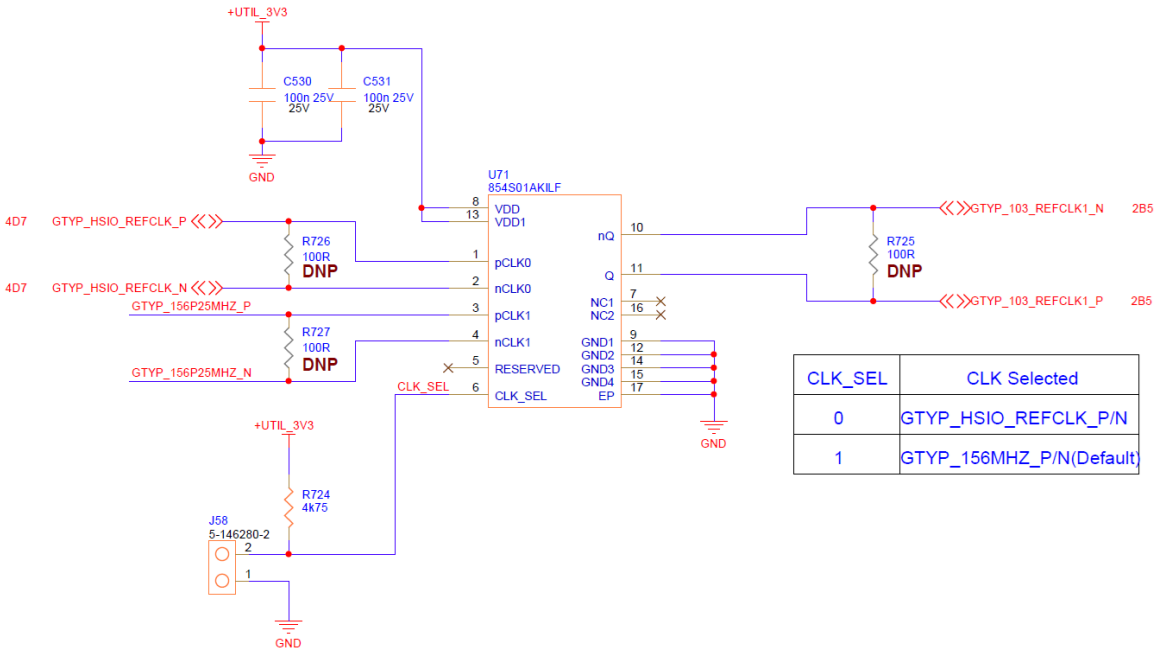

Figure 14 – Clock Multiplexer Schematic

5.8 VE2302 System-On-Module

Versal™ AI Edge Carrier Card features a socket for the VE2302 SOM.

The VE2302 SOM socket features the following resources:

- 80 User High Performance I/O (XPIO)
- 22 User High Density I/O (HDIO)
- 12 User LPD MIO Pins
- 13 User PMC MIO Pins
- 8 GTYP Transceivers
- 4 GTYP Reference Clock Inputs
- I2C I/O Expander GPIO – 2 bits
- PMC JTAG Interface
- PMC SYSMON interface
- USB 2.0 Connector Interface
- Gigabit Ethernet RJ45 Connector Interface
- PMBus Interface
- Carrier Card I2C Interface
- SOM +VCC_BATT Battery Input
- SOM Reset Input
- Carrier Card Interrupt Input
- Carrier Card Reset Output
- SOM Power Good Output
- SOM to Carrier Card Ground Pins
- SOM Input Voltages and Output Sense Pins

5.8.1 Vivado Board Definition File

The VE2302 SOM is enabled in the Vivado Design Suite through the Vivado Board Flow functionality. Vivado Board Flow enables a level of hardware abstraction that automatically configures peripherals fixed on the VE2302 SOM (e.g., LPDDR4), defines associated timing constraints, and presents the customizable physical I/O available on the VE2302 SOM connector(s). It is expected that this Vivado board file will be utilized as the starting point for any design targeting the Versal™ AI Edge Carrier Card.

The Vivado VE2302 SOM board model will be made available through the Vivado installation process as well as on the Vivado board file GitHub repository. The following VE2302 SOM Vivado board files are available:

- **AES-VE2302-SOM: Commercial grade production SOM**

For additional information on using the Vivado tools and the Vivado board flow, refer to the Vivado Design Suite User Guide: System-Level Design Entry **(UG895)**.

5.9 Boot Source and Storage Devices

The VE2302 SOM includes a non-volatile storage boot device in the form of OSPI flash memory. The Versal™ AI Edge Carrier Card provides a secondary boot device via a SD card interface on the carrier card.

The VE2302 SOM included with the K24 Development Kit does include a secondary non-volatile storage but it cannot be used as a boot source. A user must rely on the microSD card or OSPI flash as the primary boot devices.

The Versal™ AI Edge Carrier Card and VE2302 SOM supports the following boot modes:

- Master SPI flash memory using the onboard Octal SPI flash memory.
- microSD card memory using the carrier card microSD card cage.
- JTAG using a Type-C USB cable for connecting the host PC to the Versal™ AI Edge Carrier Card via configuration port **J52** or via a PC4 connector **J35** which requires the use of a third-party programming dongle.

NOTE: The only way to utilize the debug UART is via the Type-C USB cable. When the debug UART functionality is required, the end-user cannot utilize the PC4 connector for JTAG functionality.

The configuration interface corresponds to one or more boot modes and bus widths. The default mode setting is **M[3:0] = 1000**, which selects the Master SPI flash memory at board power-on.

BOOT Mode	M[3:0]	SW7[4:1]
Master SPI Flash Memory	1000	OFF-ON-ON-ON
microSD Card Memory	0011	ON-ON-OFF-OFF
JTAG	0000	ON-ON-ON-ON

Table 9 – Available Boot Modes

The Versal™ AI Edge Carrier Card allows the APSoC Boot Mode to be selected by setting the Boot Mode Switch, **SW7** to the appropriate values. The Boot Mode Switch, **SW7**, is placed on the bottom right-hand corner of the Versal™ AI Edge Carrier Card. The proper APSoC Boot Mode should be set prior to board power-on for proper operation.

The Versal™ AI Edge Carrier Card implements a small 4-position DIP switch for the Boot Mode pins (**SW7**) and routes the Boot Mode pins to a **JX** connector

- Manufacturer: CTS Electronic Components
- Part Number: **219-4MSTR**
- SMD DIP 4-POS Switch

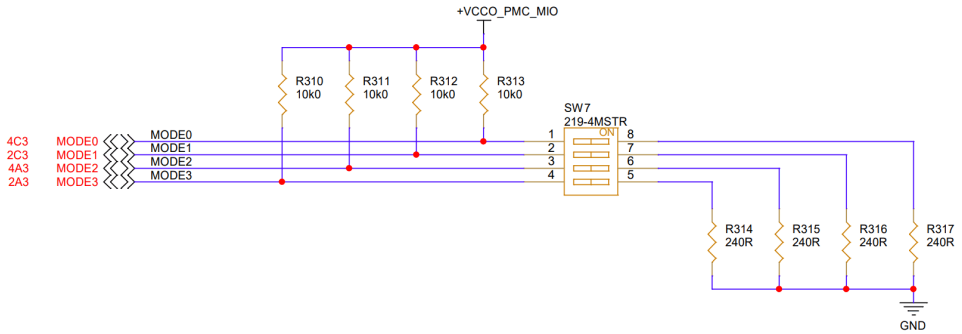

Figure 15 – Carrier Card BOOT Mode Switch Schematic

Net Name	JX Connector
MODE0	JX1-A35
MODE1	JX1-B35
MODE2	JX1-C35
MODE3	JX1-D35

Table 10 – BOOT Mode Pin Assignment

5.10 VE2302 SOM OSPI Interface

The VE2302 SOM includes a 2048Mb (256MB) OSPI flash memory device. It supports interface clocks speeds up to 200 MHZ and can be used as the primary boot device for the APSoC processing subsystem. The OSPI device contains an Out-of-Box design that boots to a Petalinux command prompt from the factory.

The Octal-SPI Flash connects to the Versal™ APSoC OSPI interface. This requires connection to specific pins in MIO Bank 500, specifically MIO[0:10] and MIO[12] as outlined in the Versal™ APSoC TRM (Technical Reference Manual, **AM011**). See the **VE2302 Hardware User Guide** for more information on the implementation of the OSPI interface on the VE2302 SOM.

MIO BANK 500	MIO PIN NAME	APSoC Package Pin
PMC_MIO0	OSPI_CLK	AA1
PMC_MIO1	OSPI_IO0	AB1
PMC_MIO2	OSPI_IO1	AD1
PMC_MIO3	OSPI_IO2	AE1
PMC_MIO4	OSPI_IO3	AF1
PMC_MIO5	OSPI_IO4	AG1
PMC_MIO6	OSPI_DS	AH2
PMC_MIO7	OSPI_IO5	AG2
PMC_MIO8	OSPI_IO6	AE2
PMC_MIO9	OSPI_IO7	AD2
PMC_MIO10	OSPI_CS_B	AC2
PMC_MIO12	OSPI_RST_B	AA3

Table 11 – OSPI Interface Pin Map

5.11 microSD Card Interface

The Versal™ AI Edge Carrier Card provides a microSD card interface for use as a boot device and / or for user storage. The VE2302 SOM exposes PMC MIO[38-45] and PMC MIO[49] on the JX1 connector and these PMC MIO pins are used to interface to the microSD card cage that is operated at 3.3V. The PMC MIO bank on the VE2302 SOM has its voltage set to 1.8V. The Versal™ AI Edge Carrier Card implements a Level Shifter for SD3.0 card applications with auto-direction sensing so that it can translate the signals between the 1.8V and 3.3V voltages.

The microSD interface is implemented with **U4**, **U5** and the connector **J5** from manufacturer Molex. It provides access to the microSD to boot or store data.

- Manufacturer: Molex
- Part Number: **5025700893**
- Style: Push-Push

The microSD interface is connected to the **JX1** connector through the level shifter **NVT4857UKAZ** device **U5**.

- Manufacturer: NXP USA, Inc
- Part Number: **NVT4857UKAZ**

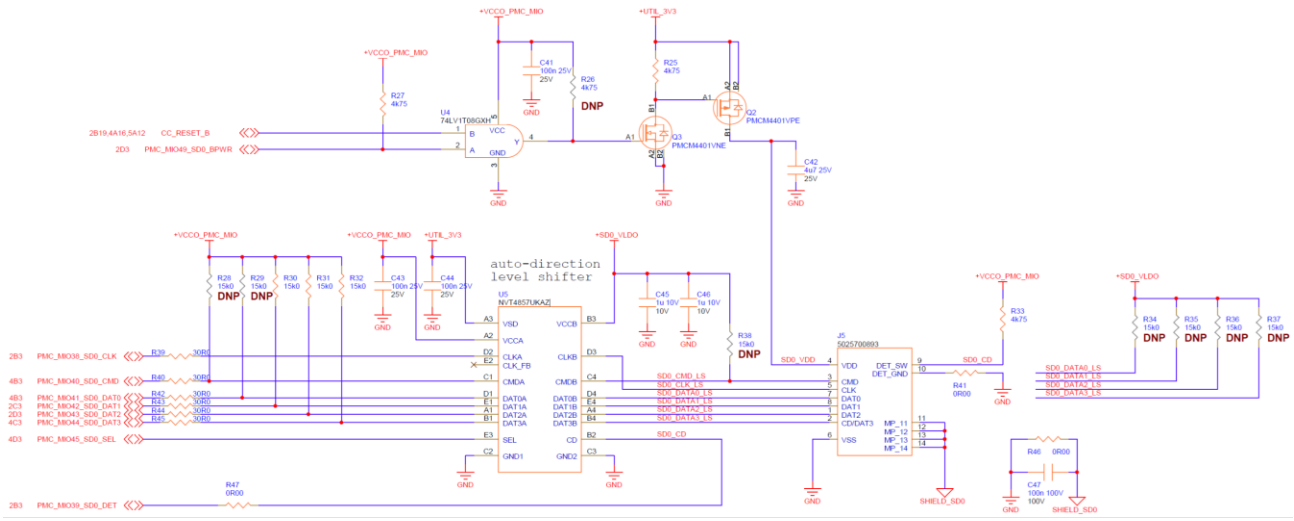

Figure 16 – microSD Card Interface

Carrier Card Net Name	U5 Signal Name	JX1 Pin Name (Number)	APSoC Package Pin
PMC_MIO38_SD0_CLK	SD0_CLK_LS	PMC_MIO38 (D24)	AE8
PMC_MIO39_SD0_DET	SD0_CD	PMC_MIO39 (D23)	AC8
PMC_MIO40_SD0_CMD	SD0_CMD_LS	PMC_MIO40 (C27)	AB8
PMC_MIO41_SD0_DAT0	SD0_DATA0_LS	PMC_MIO41 (C26)	AA8
PMC_MIO42_SD0_DAT1	SD0_DATA1_LS	PMC_MIO42 (B23)	AA9
PMC_MIO43_SD0_DAT2	SD0_DATA2_LS	PMC_MIO43 (B22)	AC9
PMC_MIO44_SD0_DAT3	SD0_DATA3_LS	PMC_MIO44 (A23)	AD9
PMC_MIO45_SD0_SEL	SD0_SEL	PMC_MIO45 (A22)	AE9
PMC_MIO49_SD0_BPWR	SD0_BPWR	PMC_MIO49 (B19)	AC10

Table 12 – microSD Card Interface Pin Map

5.12 USB-to-JTAG Interface

JTAG configuration is provided through an onboard USB-to-JTAG configuration device (**U27**), in which a host computer accesses the Versa™ AI Edge Carrier Card JTAG chain through a type-A or type-C (host side) to type-C (Versal™ AI Edge Carrier Card **J53**) USB cable. The USB-to-JTAG configuration device can be used for PL configuration, OSPI flash programming, as well as software debugging.

This USB-to-JTAG bridge device is shared with the device that also provides the USB-to-UART interface functionality.

The JTAG interface is translated from 3.3V to 1.8V for use by the VE2302 SOM. The VE2302 SOM has access to the JTAG interface via the **JX1** connector.

LED indicator **D34** will illuminate when a USB Type-C cable is properly attached between a host device and the **J53** port on the Versal™ AI Edge Carrier Card.

Carrier Card Net Name	JX1 Pin Name (Number)	APSoC Package Pin
JTAG_TCK	JTAG_TCK (A37)	AH10
JTAG_TDI	JTAG_TDI (C37)	AG10
JTAG_TDO	JTAG_TDO (D37)	AF8
JTAG_TMS	JTAG_TMS (B37)	AH9

Table 13 – JTAG Interface Pin Map

- Manufacturer: Pulse Electronics
- Part Number: **E8124-010-01**
- USB 3.1 TYPE C 5G Mid Mount

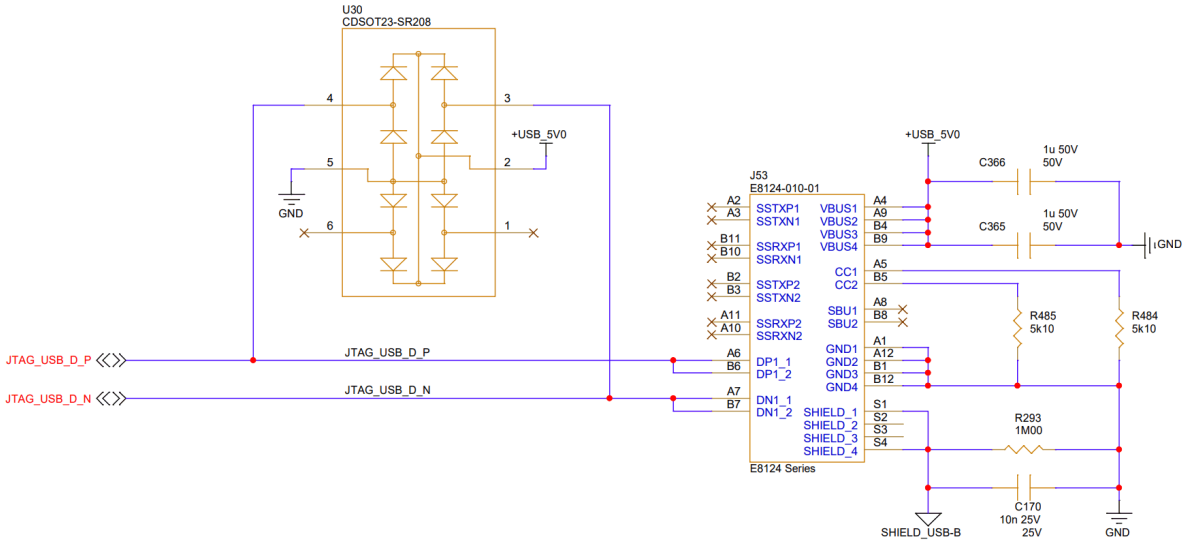

Figure 17 – USB Type-C Connector

The USB Type-C signals **JTAG_USB_D_P/N** goes through a FTDI Quad High-Speed USB to Multipurpose UART/MPSSE IC (**U27**) before being redirected to the **JX1** Connectors.

- Manufacturer: FTDI
- Part Number: **FT2232HL-REEL**
- USB Interface IC USB HS to Quad UART/ SPI/JTAG/I2C LQFP-6

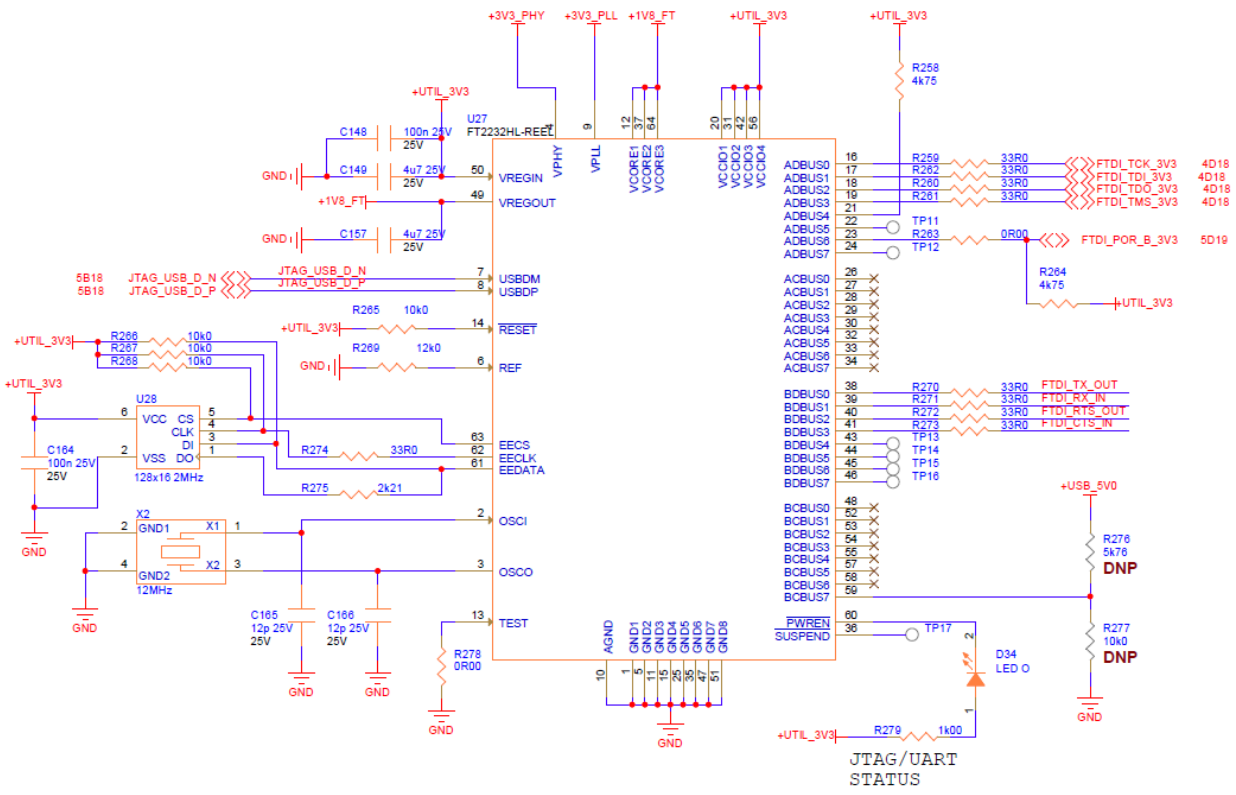

Figure 18 – USB JTAG-UART Schematic

NOTE: Two voltage translators, **U26** and **U29**, exist to translate signal levels between **+UTIL_3V3** and **+VCCO_PMC_MIO** that are not depicted in this document. These two translators convert the JTAG interface and the UART interface to signal levels suitable for the VE2302 SOM.

FT4232HL (U27) Pin Number	FT4232HL (U27) Pin Name	Schematic Net Name	JX1 Pin Number
16	ADBUS0	FTDI_TCK_3V3	A37
17	ADBUS1	FTDI _TDI_3V3	C37
18	ADBUS2	FTDI _TDO_3V3	D37
19	ADBUS3	FTDI _TMS_3V3	B37
38	BDBUS0	FTDI_TX_OUT (LPD_MIO16_UART0_RXD)	D18
39	BDBUS1	FTDI_RX_IN (LPD_MIO17_UART0_TXD)	D17
40	BDBUS2	FTDI_RTS_OUT (LPD_MIO18_UART0_CTS)	C22
41	BDBUS3	FTDI_CTS_IN (LPD_MIO19_UART0_RTS)	C21

Table 14 – FTDI To JX Signals Mapping

A 2mm JTAG header (**J35**) is also provided in parallel for access by JTAG download cables. JTAG configuration is allowed at any time regardless of the settings. This is a traditional programming header for AMD devices and requires a third-part programming dongle.

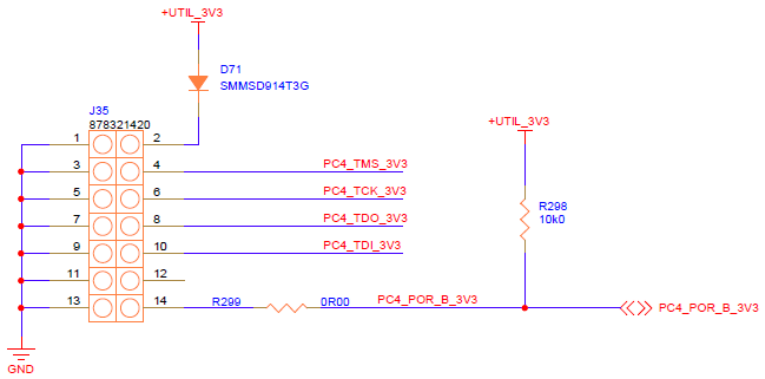

Figure 19 – PC4 JTAG Header

NOTE: Plugging in the Type-C cable selects the FTDI device as the programming solution as referenced by the multiplexer select signal below. When desiring to utilize the PC4 JTAG header, you must not have a Type-C cable plugged into the Versal™ AI Edge Carrier Card.

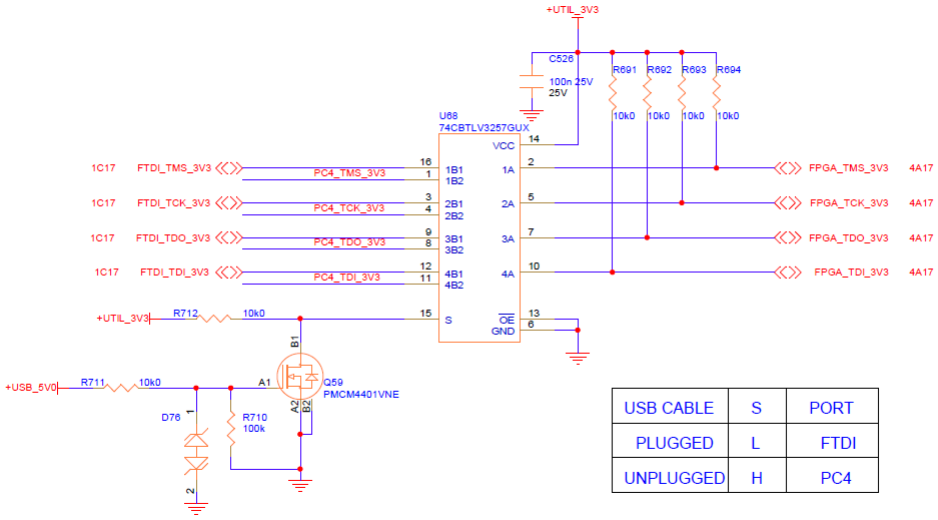

Figure 20 – JTAG Interface Select

NOTE: The only way to utilize the debug UART is via the Type-C USB cable. When the debug UART functionality is required, the end-user cannot utilize the PC4 connector for JTAG functionality.

5.13 USB-to-UART Interface

UART communication interface is provided through an onboard USB-to-UART configuration device (**U27**), in which a host computer accesses the Versal™ AI Edge Carrier Card UART interface through a type-A or type-C (host side) to type-C (Versal™ AI Edge Carrier Card side **J53**) USB cable. This USB-to-UART bridge device is shared with the device that also provides the USB-to-JTAG interface functionality.

NOTE: Device **U27** is not self-powered by the USB 5V provided by the host PC USB cable. It is powered by an on-board +3V3 power rail.

NOTE: The VCP (Virtual COM Port) device drivers must be installed on the host PC prior to establishing communications with the Versal™ AI Edge Carrier Card.

The UART interface is translated from 3.3V to 1.8V for use by the VE2302 SOM. The VE2302 SOM has access to the UART interface via the **JX1** connector.

JX1 Pin Number	Schematic Net Name	I/O Name	APSoC Package Pin
JX1-D18	LPD_MIO16_UART0_RXD	FTDI_TX_OUT	U5
JX1-D17	LPD_MIO17_UART0_TXD	FTDI_RX_IN	V5
JX1-C22	LPD_MIO19_UART0_RTS	FTDI_CTS_IN	Y6
JX1-C21	LPD_MIO18_UART0_CTS	FTDI_RTS_OUT	W5

Table 15 – UART Interfaces Pin Map

NOTE: The only way to utilize the debug UART is via the Type-C USB cable. When the debug UART functionality is required, the end-user cannot utilize the PC4 connector for JTAG functionality.

5.14 JX Micro Headers

The Versal™ AI Edge Carrier Card has 3 Micro Headers for connection to the VE2302 SOM. The three Micro Headers consist of 160-pin connectors from Samtec, ADM6-40-01.5-L-4-0-A. These connectors are Samtec 0.635mm AcceleRate® HD High Density 4-Row Sockets with 160 Positions and have stack heights options from 5mm and 16mm, making it easy to connect to a variety of expansion or system boards depending on the end-user requirements. By default, the mating solution with the VE2302 SOM is set to 5mm. Each pin can carry 1.340A of current and support I/O speeds more than what the AMD Versal™ AI Edge device can deliver with performance up to 64Gbps PAM4.

The JX Micro Header connectors on the VE2302 SOM have a default height of 3.5mm. The height of the mating JX receptacles on the Versal™ AI Edge Carrier Card is selected such that the stack height combination is <= 12mm when the VE2302 SOM is attached (this requirement must be met to meet the 32Gbps data rate for the GTYP transceivers connected to the JX3 connector). Also, the stack height combination has a minimum requirement that is dependent on circuit implementation on the bottom of the VE2302 SOM and any circuitry that could be implemented on the end-user carrier card under the VE2302 SOM. Care must be taken to avoid shorting components when implementing short stacking height via the end-user carrier card.

The JX1 connector is the main interface to MIO and HDIO signals for the end-user carrier card. The JX1 provides access to dedicated JTAG signals, various power rails, voltage sense signals, PMBUS interface, and control signals. Lastly, the JX1 connector also host signals for the Gigabit Ethernet and USB 2.0 connectors.

The JX2 connector is the main interface for the XPIO signals for the end-user carrier card. The JX2 signal also provides access to various power rails, voltage sense signals, and control signals.

The JX3 connector interfaces to the GTYP MGTs, GTYP Reference Clocks, and GTYP power supplies. The JX3 connector also contains various power rail as well as voltage sense signals for the end-user carrier card power supply feedback.

The following table summarizes connections to the VE2302 SOM JX Micro Header Connectors.

Micro Header JX1			
Interface	**Signal Name**	**Source**	**Pins**
PMC	Bank 502 PMC MIO	Bank 502	12
	Bank 501 PMC MIO	Bank 501	13
	JTAG_TMS, JTAG_TCK, JTAG_TDI, JTAG_TDO ERROR_OUT DONE_OUT MODE[0:3]	Bank 503	10
PL I/O	Bank 302 Differential Pair I/Os	Bank 302	22
	SYSCLK_P/N	Bank 702	2
Comms	I2C_P6_GPIO, I2C_P7_GPIO	I2C Expander	2
	USB2.0 PHY Interface	USB PHY	4
	Gigabit Ethernet PHY Interface	ETH PHY	10
SYSMON	SMON_V_P, SMON_V_N SMON_VREF VCCAUX_SMON GND_SMON	Bank 500	8
Control	PMBus	I2C Switch	3
	CC I2C BUS	I2C Switch	3
	SOM_PG_OUT	VE2302 SOM	1
Power	GND	Carrier Card	39
	+VCC_BATT		1
	+VCC_FUSE		1
	+VCC_RAM and VCC_RAM_SENSE		2
	+VCCO_302REF and VCCO_302_SENSE		3
	+VCCO_502	VE2302 SOM	1
	+VCCO_PMC_MIO	VE2302 SOM	1
	VCCINT_SENSE and GND_SENSE	VE2302 SOM	2
	+VCCINT	Carrier Card	20

Table 16 – Micro Header JX1 Summary

Micro Header JX2			
Interface	**Signal Name**	**Source**	**Pins**
PL	Bank 702 Differential Pair I/Os	Bank 702	28
	Bank 702 – DDRMC Do Not Connect	Bank 702	24
	Bank 703 Differential Pair I/Os	Bank 703	52
Control	SOM_RESET_IN_B, SOM_PWR_ENB_IN, VCCO_702_PG_IN	Carrier Card	3
	VCCO_702_ENB_OUT, CC_RESET_OUT_B	VE2302 SOM	2

Micro Header JX2			
Interface	**Signal Name**	**Source**	**Pins**
Power	GND	Carrier Card	28
	+VCCO_702		2
	+VCCO_703		2
	+MGTYPAVCC		3
	+MGTYPVCCAUX		2
	+VCCAUX_PMC	VE2302 SOM	1
	VCCO_702_SENSE, VCCO_702_SENSE, MGTYPVCCAUX_SENSE, MGTYPAVCC_SENSE, MGTYPAVTT_SENSE		5
	+VCCINT	Carrier Card	8

Table 17 – Micro Header JX2 Summary

Micro Header JX3			
Interface	**Signal Name**	**Source**	**Pins**
GTYP	Bank 103 Differential Pair I/Os	Bank 103	20
	Bank 104 Differential Pair I/Os	Bank 104	20
Power	GND	Carrier Card	92
	+MGTYPAVTT		3
	VIN_SENSE	VE2302 SOM	1
	+VIN	Carrier Card	12
	+VCCINT		12

Table 18 – Micro Header JX3 Summary

5.14.1 JX Connector Master Table

The following tables list the VE2302 SOM JX Micro Header connections in master tables targeting each connector:

- Pins in **Orange** are DDRMC dedicated and are not available to be used
- Pins in **Pink** are Power, Ground, or Sense signals
- Pins in **Blue** are dedicated signals
- Pins in **Black** are multi-function/general-purpose pins
- Pins in **Black** with **_HDGC** designators inputs are clock capable pins in a HDIO bank
- Pins in **Black** with **_XCC** designators can accept a strobe to capture data
- Pins in **Black** with _**GC** and _**XCC** these pins can act as Global Clocks and/or XCCs inputs
- **PMC_MIO** stands for Platform Management Controller Multiplexed I/O
- **LPD_MIO** stands for Low Power Domain Multiplexed I/O
- **HDIO** stands for I/O from bank 302
- **XPIO** stands for I/O from bank 702 or bank 703
- **GTYP** stands for I/O from quad 103 or quad 104

XCVE2302 Pin #	Signal Name	JX1 Pin #		Signal Name	XCVE2302 Pin #
Many	+VCCINT	A1	B1	+VCCINT	Many
	+VCCINT	A2	B2	+VCCINT	
	+VCCINT	A3	B3	+VCCINT	
	+VCCINT	A4	B4	+VCCINT	
	+VCCINT	A5	B5	+VCCINT	
N/A	GND	A6	B6	GND	N/A
B13	HDIO_302_L10_P	A7	B7	HDIO_302_L9_P	B12
A14	HDIO_302_L10_N	A8	B8	HDIO_302_L9_N	A13
N/A	GND	A9	B9	GND	N/A
C14	HDIO_302_L1_P	A10	B10	HDIO_302_L2_P	E13
C13	HDIO_302_L1_N	A11	B11	HDIO_302_L2_N	D14
D13, F13	+VCCO_302	A12	B12	+VCCO_302	D13, F13
E12	HDIO_302_L3_P	A13	B13	HDIO_302_HDGC_L5_P	D11
D12	HDIO_302_L3_N	A14	B14	HDIO_302_HDGC_L5_N	C12
N/A	GND	A15	B15	GND	N/A
Y7	LPD_MIO23	A16	B16	LPD_MIO21	U6
T6	LPD_MIO22	A17	B17	LPD_MIO20	W6
N/A	GND	A18	B18	+VCC_FUSE	V15
AF10	PMC_MIO47	A19	B19	PMC_MIO49	AC10
AF9	PMC_MIO46	A20	B20	PMC_MIO48	AD10
N/A	GND	A21	B21	GND	N/A
AE9	PMC_MIO45	A22	B22	PMC_MIO43	AC9
AD9	PMC_MIO44	A23	B23	PMC_MIO42	AA9
U7, U8, V7, W8, V9, W9	+VCCO_PMC_MIO	A24	B24	GND	N/A
N/A	CC_INT_B	A25	B25	CC_SCL	N/A
N/A	PMBUS_ALERT_B	A26	B26	GND	N/A
N/A	VCCO_302_SENSE	A27	B27	VCC_RAM_SENSE	N/A
N/A	GND	A28	B28	PMBUS_SDA	N/A
N/A	ETH_ACT	A29	B29	SOM_PG_OUT	N/A
N/A	ETH_LINK	A30	B30	USB_ID	N/A
N/A	GND	A31	B31	GND	N/A
N/A	ETH_MD4_P	A32	B32	ETH_MD3_P	N/A
N/A	ETH_MD4_N	A33	B33	ETH_MD3_N	N/A
N/A	GND	A34	B34	GND	N/A

XCVE2302 Pin #	Signal Name	JX1 Pin #		Signal Name	XCVE2302 Pin #
AG8	MODE0	A35	B35	MODE1	AG7
N/A	GND	A36	B36	GND	N/A
AH10	JTAG_TCK	A37	B37	JTAG_TMS	AH9
N/A	GND	A38	B38	GND	N/A
R18	SMON_AGND	A39	B39	SMON_AGND	R18
U17	+SMON_VREF	A40	B40	SMON_V _P	T17
Many	+VCCINT	C1	D1	+VCCINT	Many
	+VCCINT	C2	D2	+VCCINT	
	+VCCINT	C3	D3	+VCCINT	
	+VCCINT	C4	D4	+VCCINT	
	+VCCINT	C5	D5	+VCCINT	
N/A	GND	C6	D6	GND	N/A
B11	HDIO_302_L8_P	C7	D7	HDIO_302_L7_P	B10
A11	HDIO_302_L8_N	C8	D8	HDIO_302_L7_N	A10
N/A	GND	C9	D9	GND	N/A
D10	HDIO_302_HDGC_L6_P	C10	D10	HDIO_302_L4_P	F11
C10	HDIO_302_HDGC_L6_N	C11	D11	HDIO_302_L4_N	E11
P20, T20	+VCC_RAM	C12	D12	+USB_VBUS	N/A
F14	HDIO_302_L0_P	C13	D13	ERROR_OUT	AH5
E14	HDIO_302_L0_N	C14	D14	SYSCLK_P	N23
N/A	GND	C15	D15	SYSCLK_N	N24
F10	VCCINT_SENSE	C16	D16	GND	N/A
F9	GND_SENSE	C17	D17	LPD_MIO17	V5
N/A	I2C_P6_GPIO	C18	D18	LPD_MIO16	U5
N/A	I2C_P7_GPIO	C19	D19	GND	N/A
N/A	GND	C20	D20	LPD_MIO15	T5
Y6	LPD_MIO19	C21	D21	LPD_MIO14	T4
W5	LPD_MIO18	C22	D22	+VCCO_502	T8, T9
V4	LPD_MIO13	C23	D23	PMC_MIO39	AC8
W4	LPD_MIO12	C24	D24	PMC_MIO38	AE8
N/A	GND	C25	D25	GND	N/A
AA8	PMC_MIO41	C26	D26	PMC_MIO37	AE7
AB8	PMC_MIO40	C27	D27	+VCC_BATT	W15
N/A	GND	C28	D28	DONE_OUT	AF5
N/A	CC_SDA	C29	D29	USB_D_P	N/A

XCVE2302 Pin #	Signal Name	JX1 Pin #		Signal Name	XCVE2302 Pin #
N/A	PMBUS_SCL	C30	D30	USB_D_N	N/A
N/A	GND	C31	D31	GND	N/A
N/A	ETH_MD2_P	C32	D32	ETH_MD1_P	N/A
N/A	ETH_MD2_N	C33	D33	ETH_MD1_N	N/A
N/A	GND	C34	D34	GND	N/A
AG6	MODE2	C35	D35	MODE3	AG5
N/A	GND	C36	D36	GND	N/A
AG10	JTAG_TDI	C37	D37	JTAG_TDO	AF8
N/A	GND	C38	D38	GND	N/A
R18	SMON_AGND	C39	D39	SMON_AGND	R18
U18	SMON_V_N	C40	D40	+VCCAUX_SMON	R17

Table 19 – JX1 Connector Master Pin-out

XCVE2302 Pin #	Signal Name	JX2 Pin #		Signal Name	XCVE2302 Pin #
Many	+VCCINT	A1	B1	+VCCINT	Many
	+VCCINT	A2	B2	+VCCINT	
A25	XPIO_703_L10_P	A3	B3	XPIO_703_XCC_L3_P	E27
A26	XPIO_703_L10_N	A4	B4	XPIO_703_XCC_L3_N	E28
N/A	GND	A5	B5	GND	N/A
B26	XPIO_703_L11_P	A6	B6	XPIO_703_GC_XCC_L9_P	C25
B27	XPIO_703_L11_N	A7	B7	XPIO_703_GC_XCC_L9_N	B25
AE21, AF20, AF21	+VCCO_702	A8	B8	+VCCO_702	AE21, AF20, AF21
C23	XPIO_703_L16_P	A9	B9	XPIO_702_L26_P	N25
B23	XPIO_703_L16_N	A10	B10	XPIO_702_L26_N	M25
N/A	GND	A11	B11	GND	N/A
D24	XPIO_703_XCC_L15_P	A12	B12	XPIO_703_L17_P	A23
C24	XPIO_703_XCC_L15_N	A13	B13	XPIO_703_L17_N	A24
AA24, AA25, AB25	+VCCO_703	A14	B14	+VCCO_703	AA24, AA25, AB25
B20	XPIO_703_XCC_L21_P	A15	B15	XPIO_703_L22_P	A20
C21	XPIO_703_XCC_L21_N	A16	B16	XPIO_703_L22_N	A21
N/A	GND	A17	B17	GND	N/A
D20	XPIO_703_L20_P	A18	B18	XPIO_703_L23_P	C22

XCVE2302 Pin #	Signal Name	JX2 Pin #		Signal Name	XCVE2302 Pin #
D21	XPIO_703_L20_N	A19	B19	XPIO_703_L23_N	B22
N/A	VCCO_702_SENSE	A20	B20	VCCO_703_SENSE	N/A
G21	XPIO_703_XCC_L18_P	A21	B21	XPIO_703_L19_P	E20
H22	XPIO_703_XCC_L18_N	A22	B22	XPIO_703_L19_N	F21
N/A	GND	A23	B23	GND	N/A
R27	XPIO_702_L1_P	A24	B24	XPIO_702_L2_P	P27
T28	XPIO_702_L1_N	A25	B25	XPIO_702_L2_N	R28
L7, N7	+MGTYPAVCC	A26	B26	+MGTYPAVCC	L7, N7
N28	XPIO_702_XCC_L3_P	A27	B27	XPIO_702_XCC_L0_P	U27
M28	XPIO_702_XCC_L3_N	A28	B28	XPIO_702_XCC_L0_N	U28
N/A	GND	A29	B29	GND	N/A
K27	XPIO_702_L5_P	A30	B30	XPIO_702_L4_P	M27
K28	XPIO_702_L5_N	A31	B31	XPIO_702_L4_N	L28
W12, W14	+VCCAUX_PMC	A32	B32	SOM_RESET_IN_B	N/A
K21	XPIO_702_XCC_L22_P	A33	B33	XPIO_702_L23_P	J21
L22	XPIO_702_XCC_L22_N	A34	B34	XPIO_702_L23_N	J22
N/A	GND	A35	B35	GND	N/A
T21	XPIO_702_L20_P	A36	B36	XPIO_702_XCC_L21_P	N21
R22	XPIO_702_L20_N	A37	B37	XPIO_702_XCC_L21_N	M21
N/A	GND	A38	B38	GND	N/A
R21	XPIO_702_L19_P	A39	B39	XPIO_702_XCC_L18_P	V21
P22	XPIO_702_L19_N	A40	B40	XPIO_702_XCC_L18_N	U22
Many	+VCCINT	C1	D1	+VCCINT	Many
	+VCCINT	C2	D2	+VCCINT	
D27	XPIO_703_L4_P	C3	D3	XPIO_703_L5_P	C27
C28	XPIO_703_L4_N	C4	D4	XPIO_703_L5_N	B28
N/A	GND	C5	D5	GND	N/A
H27	XPIO_703_L1_P	C6	D6	XPIO_703_L2_P	G27
G28	XPIO_703_L1_N	C7	D7	XPIO_703_L2_N	F28
N/A	VCCO_702_ENB_OUT	C8	D8	VCCO_702_PG_IN	N/A
F23	XPIO_703_GC_XCC_L24_P	C9	D9	XPIO_703_XCC_L0_P	J27
F24	XPIO_703_GC_XCC_L24_N	C10	D10	XPIO_703_XCC_L0_N	H28
N/A	GND	C11	D11	GND	
D25	XPIO_703_L26_P	C12	D12	XPIO_703_L25_P	E24
D26	XPIO_703_L26_N	C13	D13	XPIO_703_L25_N	F25

XCVE2302 Pin #	Signal Name	JX2 Pin #		Signal Name	XCVE2302 Pin #
N/A	CC_RESET_OUT_B	C14	D14	MGTYPVCCAUX_SENSE	N/A
G25	XPIO_703_L7_P	C15	D15	XPIO_703_L8_P	F26
G26	XPIO_703_L7_N	C16	D16	XPIO_703_L8_N	E26
N/A	GND	C17	D17	GND	N/A
E22	XPIO_703_L14_P	C18	D18	XPIO_703_GC_XCC_L6_P	H25
E23	XPIO_703_L14_N	C19	D19	XPIO_703_GC_XCC_L6_N	J26
N/A	MGTYPAVCC_SENSE	C20	D20	MGTYPAVTT_SENSE	N/A
H23	XPIO_703_GC_XCC_L12_P	C21	D21	XPIO_703_L13_P	F22
H24	XPIO_703_GC_XCC_L12_N	C22	D22	XPIO_703_L13_N	G23
N/A	GND	C23	D23	GND	N/A
M26	XPIO_702_L10_P	C24	D24	XPIO_702_L11_P	J25
L26	XPIO_702_L10_N	C25	D25	XPIO_702_L11_N	K26
L7, N7	+MGTYPAVCC	C26	D26	+MGTYPVCCAUX	G7, J7
L23	XPIO_702_L16_P	C27	D27	XPIO_702_GC_XCC_L9_P	P26
K24	XPIO_702_L16_N	C28	D28	XPIO_702_GC_XCC_L9_N	N27
N/A	GND	C29	D29	GND	N/A
K23	XPIO_702_L17_P	C30	D30	XPIO_702_XCC_L15_P	M22
J24	XPIO_702_L17_N	C31	D31	XPIO_702_XCC_L15_N	M23
N/A	SOM_PWR_ENB_IN	C32	D32	+MGTYPVCCAUX	G7, J7
P25	XPIO_702_L8_P	C33	D33	XPIO_702_L7_P	T25
R26	XPIO_702_L8_P	C34	D34	XPIO_702_L7_N	T26
N/A	GND	C35	D35	GND	N/A
U25	XPIO_702_GC_XCC_L6_P	C36	D36	XPIO_702_L13_P	T23
U26	XPIO_702_GC_XCC_L6_N	C37	D37	XPIO_702_L13_N	R24
N/A	GND	C38	D38	GND	N/A
U23	XPIO_702_GC_XCC_L12_P	C39	D39	XPIO_702_L14_P	R23
T24	XPIO_702_GC_XCC_L12_N	C40	D40	XPIO_702_L14_N	P24

Table 20 – JX2 Connector Master Pin-out

XCVE2302 Pin #	Signal Name	JX3 Pin #		Signal Name	XCVE2302 Pin #
Many	+VCCINT	A1	B1	+VCCINT	Many
	+VCCINT	A2	B2	+VCCINT	
	+VCCINT	A3	B3	+VCCINT	
N/A	GND	A4	B4	GND	N/A

XCVE2302 Pin #	Signal Name	JX3 Pin #		Signal Name	XCVE2302 Pin #
N/A	VIN_SENSE	A5	B5	+MGTYPAVTT	L9, M9, N9
N/A	GND	A6	B6	GND	N/A
H7	GTYP_104_REFCLK0_P	A7	B7	GND	N/A
H6	GTYP_104_REFCLK0_N	A8	B8	GND	N/A
N/A	GND	A9	B9	GND	N/A
N/A	GND	A10	B10	GTYP_104_REFCLK1_P	F7
N/A	GND	A11	B11	GTYP_104_REFCLK1_N	F6
N/A	GND	A12	B12	GND	N/A
N/A	GND	A13	B13	GND	N/A
D8	GTYP_104_TX1_P	A14	B14	GND	N/A
D7	GTYP_104_TX1_N	A15	B15	GND	N/A
N/A	GND	A16	B16	GND	N/A
N/A	GND	A17	B17	GTYP_104_TX3_P	B8
N/A	GND	A18	B18	GTYP_104_TX3_N	B7
N/A	GND	A19	B19	GND	N/A
C5	GTYP_104_TX2_P	A20	B20	GND	N/A
C4	GTYP_104_TX2_N	A21	B21	GND	N/A
N/A	GND	A22	B22	GND	N/A
N/A	GND	A23	B23	GTYP_104_TX0_P	E5
N/A	GND	A24	B24	GTYP_104_TX0_N	E4
N/A	GND	A25	B25	GND	N/A
G5	GTYP_103_TX3_P	A26	B26	GND	N/A
G4	GTYP_103_TX3_N	A27	B27	GND	N/A
N/A	GND	A28	B28	GND	N/A
N/A	GND	A29	B29	GTYP_103_TX2_P	J5
N/A	GND	A30	B30	GTYP_103_TX2_N	J4
N/A	GND	A31	B31	GND	N/A
L5	GTYP_103_TX1_P	A32	B32	GND	N/A
L4	GTYP_103_TX1_N	A33	B33	GND	N/A
N/A	GND	A34	B34	GND	N/A
N/A	GND	A35	B35	GTYP_103_TX0_P	N5
N/A	GND	A36	B36	GTYP_103_TX0_N	N4
N/A	GND	A37	B37	GND	N/A
N/A	+VIN	A38	B38	+VIN	N/A
N/A	+VIN	A39	B39	+VIN	N/A

XCVE2302 Pin #	Signal Name	JX3 Pin #		Signal Name	XCVE2302 Pin #
N/A	+VIN	A40	B40	+VIN	N/A
Many	+VCCINT	C1	D1	+VCCINT	Many
	+VCCINT	C2	D2	+VCCINT	
	+VCCINT	C3	D3	+VCCINT	
N/A	GND	C4	D4	GND	N/A
L9, M9, N9	+MGTYPAVTT	C5	D5	+MGTYPAVTT	L9, M9, N9
N/A	GND	C6	D6	GND	N/A
M7	GTYP_103_REFCLK0_P	C7	D7	GND	N/A
M6	GTYP_103_REFCLK0_N	C8	D8	GND	N/A
N/A	GND	C9	D9	GND	N/A
N/A	GND	C10	D10	GTYP_103_REFCLK1_P	K7
N/A	GND	C11	D11	GTYP_103_REFCLK1_N	K6
N/A	GND	C12	D12	GND	N/A
N/A	GND	C13	D13	GND	N/A
A5	GTYP_104_RX3_P	C14	D14	GND	N/A
A4	GTYP_104_RX3_N	C15	D15	GND	N/A
N/A	GND	C16	D16	GND	N/A
N/A	GND	C17	D17	GTYP_104_RX2_P	B2
N/A	GND	C18	D18	GTYP_104_RX2_N	B1
N/A	GND	C19	D19	GND	N/A
D2	GTYP_104_RX1_P	C20	D20	GND	N/A
D1	GTYP_104_RX1_N	C21	D21	GND	N/A
N/A	GND	C22	D22	GND	N/A
N/A	GND	C23	D23	GTYP_104_RX0_P	F2
N/A	GND	C24	D24	GTYP_104_RX0_N	F1
N/A	GND	C25	D25	GND	N/A
H2	GTYP_103_RX3_P	C26	D26	GND	N/A
H1	GTYP_103_RX3_N	C27	D27	GND	N/A
N/A	GND	C28	D28	GND	N/A
N/A	GND	C29	D29	GTYP_103_RX2_P	K2
N/A	GND	C30	D30	GTYP_103_RX2_N	K1
N/A	GND	C31	D31	GND	N/A
M2	GTYP_103_RX1_P	C32	D32	GND	N/A
M1	GTYP_103_RX1_N	C33	D33	GND	N/A
N/A	GND	C34	D34	GND	N/A

XCVE2302 Pin #	Signal Name	JX3 Pin #		Signal Name	XCVE2302 Pin #
N/A	GND	C35	D35	GTYP_103_RX0_P	P2
N/A	GND	C36	D36	GTYP_103_RX0_N	P1
N/A	GND	C37	D37	GND	N/A
N/A	+VIN	C38	D38	+VIN	N/A
N/A	+VIN	C39	D39	+VIN	N/A
N/A	+VIN	C40	D40	+VIN	N/A

Table 21 – JX3 Connector Master Pin-out

5.14.2 JX Connector Carrier Card Connections

The following figures depict the actual signal connections to the VE2302 SOM JX Micro Headers. Each symbol represents two rows of a four-row connector. For example, JX1A symbol plus JX1B symbol make up the entire JX1 connector. JX1A contains JX1 row A and JX1 row B signals. JX1B contains JX1 row C and JX1 row D signals.

While these figures depict the physical connections to each JX connector, the functional descriptions of each interface will also document the individual connections to the various JX connectors.

NOTE: The NO CONNECTs on JX2 are indicative of the locations on the DDRMC signals that can not be utilized by carrier card designs.

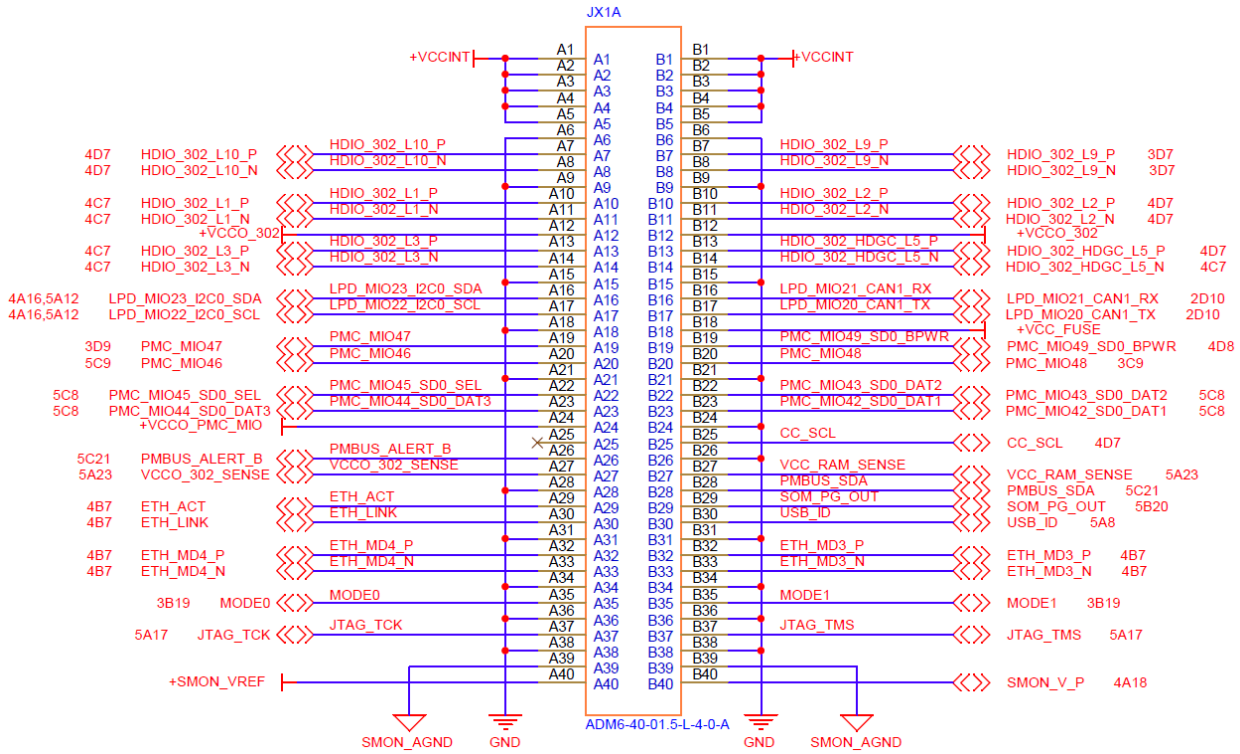

Figure 21 – JX1 Row A/B Carrier Card Pinout

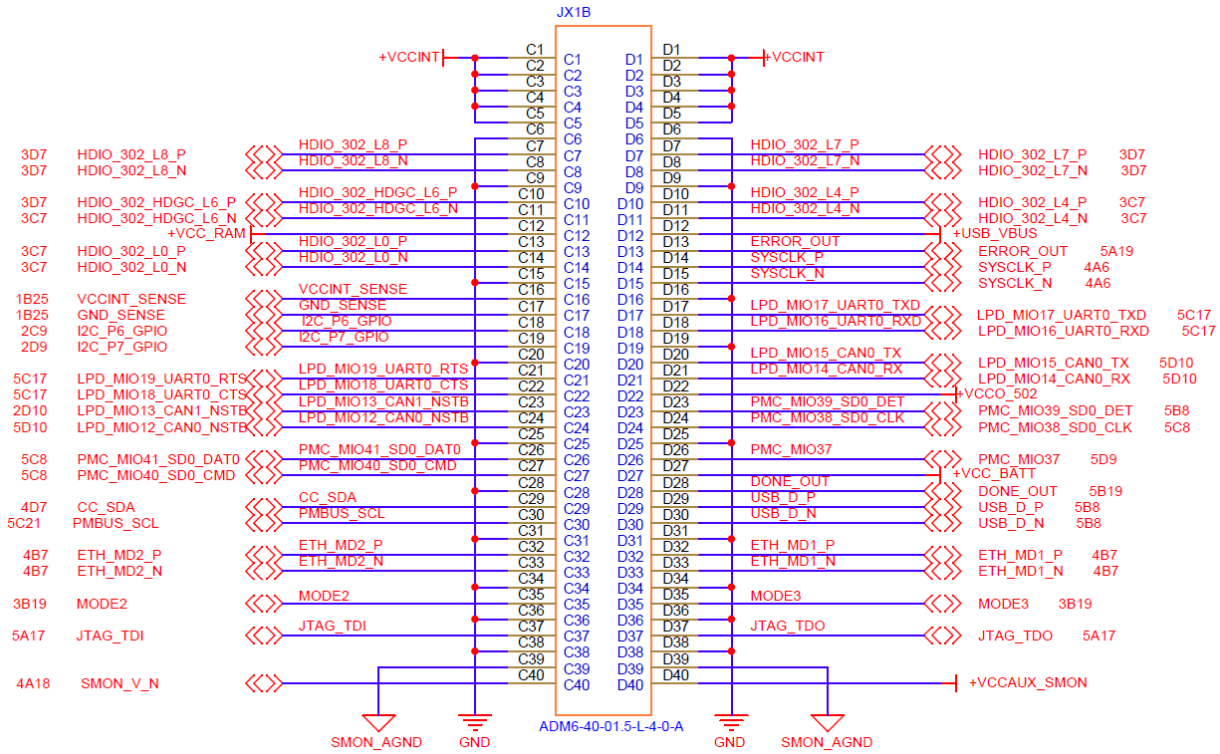

Figure 22 – JX1 Row C/D Carrier Card Pinout

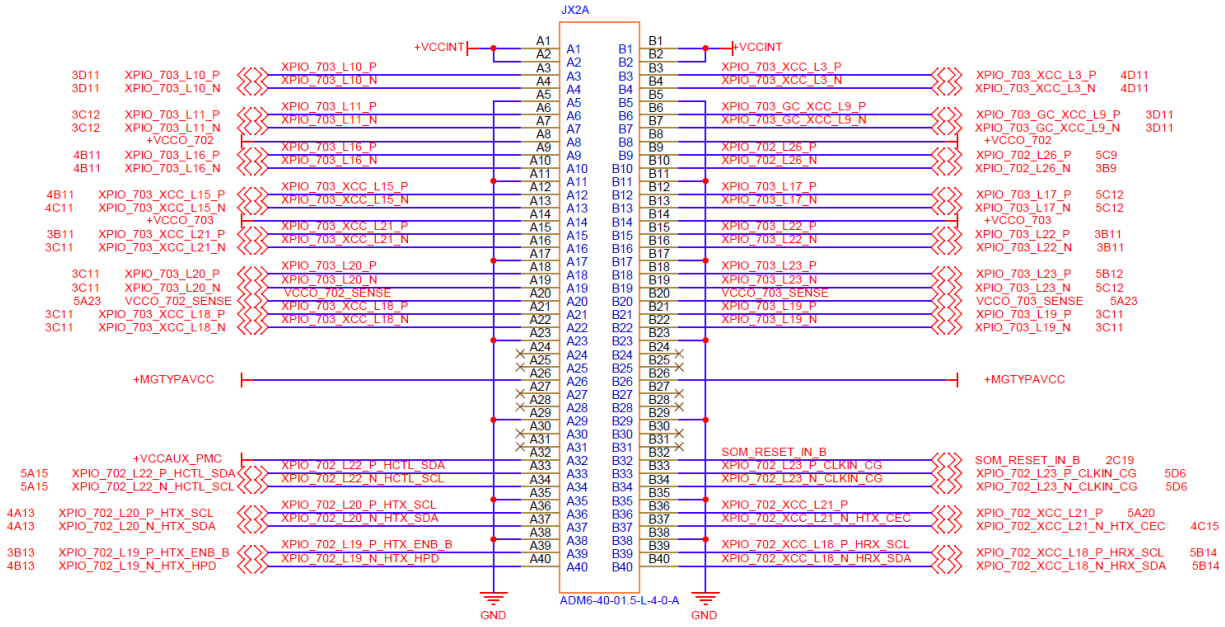

Figure 23 – JX2 Row A/B Carrier Card Pinout

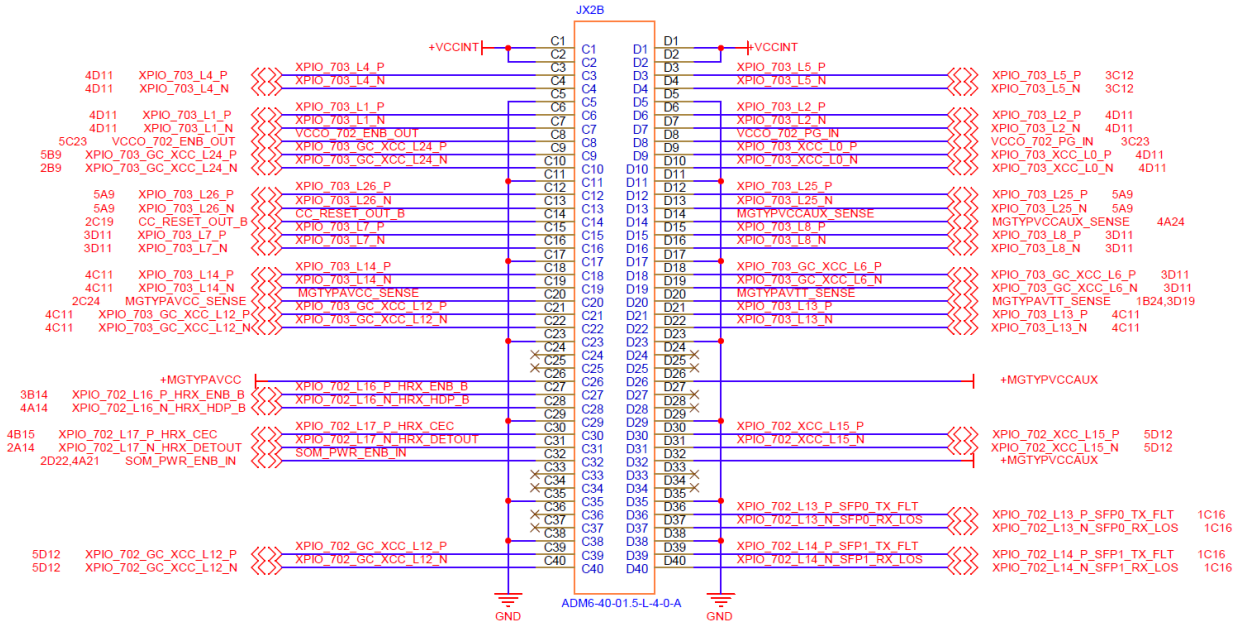

Figure 24 – JX2 Row C/D Carrier Card Pinout

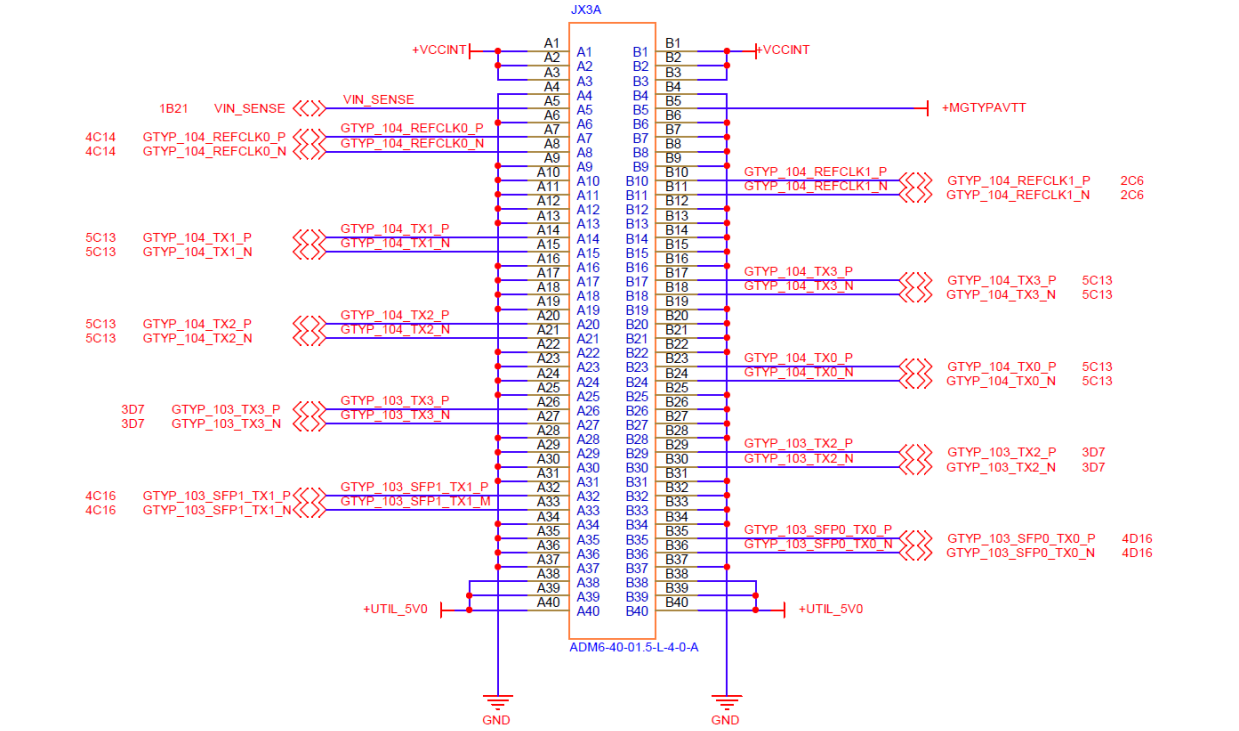

Figure 25 – JX3 Row A/B Carrier Card Pinout

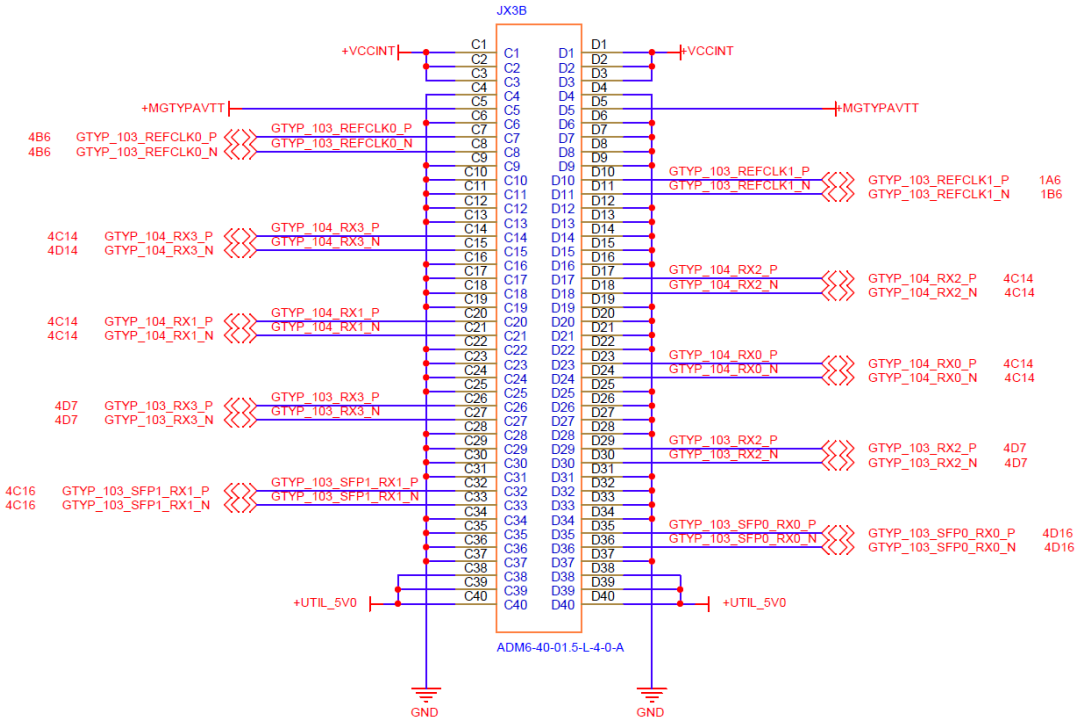

Figure 26 – JX3 Row C/D Carrier Card Pinout

5.15 Dual SFP28 Interfaces

The Versal™ AI Edge Carrier Card provides two SFP28 interfaces. Two small form factor pluggable (SFP28) connectors (**J25** and **J30**) and two cage assemblies (**J24** and **J29**) can accept SFP, SFP+, and SFP28 connections. The following figures show one of the two SFP28 interfaces schematic implementation.

NOTE: Several control signal from the SFP28 interface get translated from SFP28 interface voltage to the Versal™ bank voltage that supports the SFP28 interface. In this case, it translates to **+VCCO_702** for bank 702 pins.

- Manufacturer: TE Connectivity AMP Connectors
- Part Number: **2378765-1**

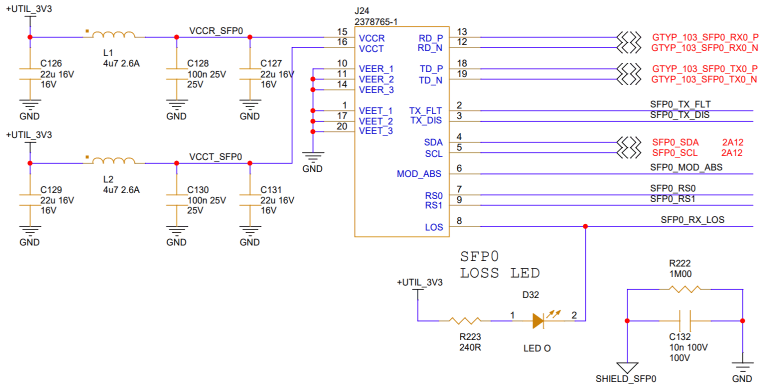

Figure 27 – SFP28 Interface Connector Schematic

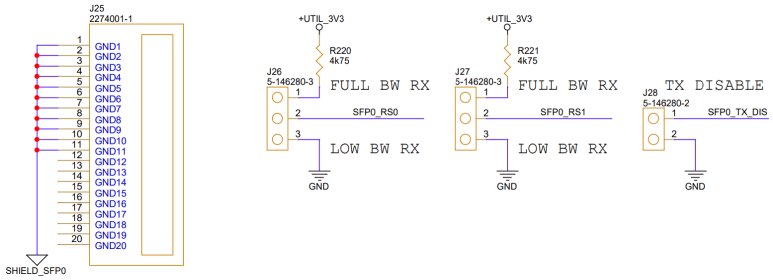

Figure 28 – SFP28 Cage and Jumpers Schematic

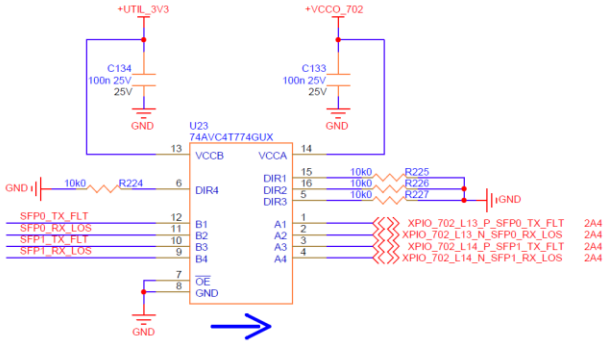

Figure 29 – SFP28 Voltage Translation

JX Connector	Connector Pin Number	Schematic Net Name	APSoC Package Pin	SFP28 Pin
JX3	D35 / D36	GTYP_103_SFP0_RX0_P/N	P2 / P1	J24.13 / J24.12
JX3	B35 / B36	GTYP_103_SFP0_TX0_P/N	N5 / N4	J24.18 / J24.19
JX2	D36	SFP0_TX_FLT (XPIO_702_L13_P_SFP0_TX_FLT)	D36	J24.2
JX1	A16 /A17	SFP0_TX_DIS	-	J24.3
JX1	A16	SFP0_SDA	Y7	J24.4
JX1	A17	SFP0_SCL	T6	J24.5
JX1	A16 /A17	SFP0_MOD_ABS	-	J24.6
J26	2	SFP0_RS0	-	J24.7
J27	2	SFP0_RS1	-	J24.9
JX2	D37	SFP0_RX_LOS (XPIO_702_L13_N_SFP0_RX_LOS)	D37	J24.8
JX3	C32 / C33	GTYP_103_SFP1_RX1_P/N	M2 / M1	J29.13 / J29.12
JX1	A32 / A33	GTYP_103_SFP1_TX1_P/N	L5 / L4	J29.18 / J29.19
JX2	D39	SFP1_TX_FLT (XPIO_702_L14_P_SFP1_TX_FLT)	D39	J29.2

JX1	A16 /A17	SFP1_TX_DIS	-	J29.3
JX1	A16	SFP1_SDA	Y7	J29.4
JX1	A17	SFP1_SCL	T6	J29.5
JX1	A16 /A17	SFP1_MOD_ABS	-	J29.6
J31	2	SFP1_RS0	-	J29.7
J32	2	SFP1_RS1	-	J29.9
JX2	D40	SFP1_RX_LOS (XPIO_702_L13_N_SFP0_RX_LOS)	D40	J29.8

Table 22 – SFP28 Interface Connections

The table below lists the SFP28 module control and status connections (High = [1-2], Low = [2-3]).

SFP28 Signal Name	Board Connection
SFP0_RS0	**Jumper J26** High = SFP0 Full Receiver Bandwidth Low = SFP0 Reduced Receiver Bandwidth
SFP0_RS1	**Jumper J27** High = SFP0 Full Transmitter Bandwidth Low = SFP0 Reduced Transmitter Bandwidth
SFP0_TX_DIS	**Jumper J28** Shunted = SFP0 TX Laser Disable Open = SFP0 TX Laser Enabled
SFP1_RS0	**Jumper J31** High = SFP1 Full Receiver Bandwidth Low = SFP1 Reduced Receiver Bandwidth
SFP1_RS1	**Jumper J32** High = SFP1 Full Transmitter Bandwidth Low = SFP1 Reduced Transmitter Bandwidth
SFP1_TX_DIS	**Jumper J33** Shunted = SFP1 TX Laser Disable Open = SFP1 TX Laser Enabled

Table 23 – SFP28 Interface Mode Select Jumpers

NOTE: There is a 156.25MHz GTYP reference clock that is provided on the Versal™ AI Edge Carrier Card to support the SFP28 interfaces. The 156.36MHz clock is an input to a clock multiplexer solution that allows for multiple GTYP reference clocks to be the source for the **GTYP_103_REFCLK1_P/N** pins on the Versal™ AI Edge device. Please see the **Clock Sources** section of this document for a better understanding of the selection of the 156.25MHz GTYP reference clock as the source for the second GTYP reference clock on quad 103.

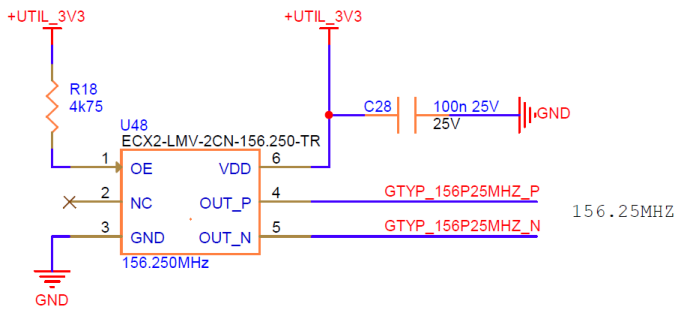

Figure 30 – SFP28 GTYP Reference Clock

OSC Pin Number	JX Connector Pin Name	JX Connector Pin Number
U48-4	GTYP_156P25MHZ_P	JX3-D10
U48-5	GTYP_156P25MHZ_N	JX3-D11

Table 24 – SFP28 GTYP Reference Clock JX3 Mapping

The SFP28 156.25MHz reference is from a SMD crystal oscillator (**X1**).

- Manufacturer: ECS
- Part Number: **ECX2-LMV-2CN-156.250-TR**
- Crystal 156.250MHz LVDS XO -40C +85C

5.15.1 SFP28 I2C I/O Expander

The **signals SFP0_TX_DIS, SFP0_MOD_ABS, SFP1_TX_DIS** and **SFP1_MOD_ABS** are connected to the GPIO[0-3] output of an I2C I/O Expander **U25**, that is controlled by an I2C interface from the VE2302 SOM. The I2C interface is made up of signals **LPD_MIO22_I2C0_SCL** and **LPD_MIO23_I2C0_SDA** which comes from the JX connector.

- Manufacturer: Onsemi / Fairchild
- Part Number: **FXL6408UMX**
- I/O Expanders 8-Bit I2C-Controlled GPIO Expander
- I2C Address: **0x88**

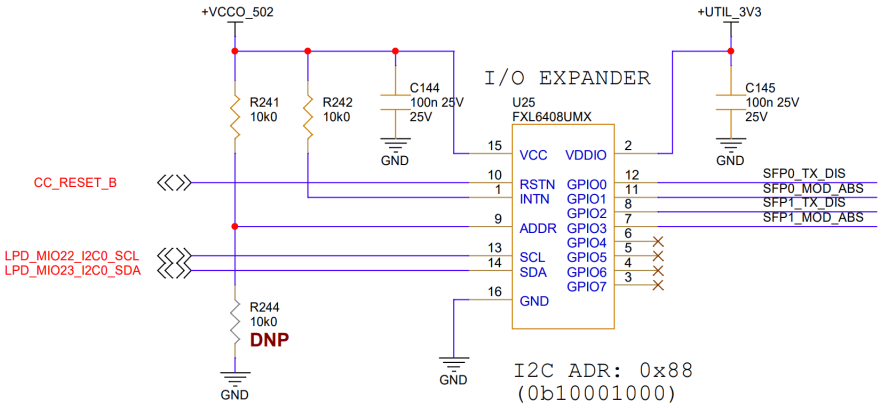

Figure 31 – I2C IO Expander Schematic

NOTE: The outputs of the I2C I/O expander are pulled up on the Versal™ AI Edge Carrier Card to the **+UTIL_3V3** voltage rail. The signals **CC_RESET_B, LPD_MIO22_I2C0_SCL,** and **LPD_MIO23_I2C0_SDA** are all pulled up to the **+VCCO_502** voltage rail.

5.16 SFP28 Interface – Shared I2C Bus Switch

Each SFP28 interface has an I2C bus that is connected to an I2C Bus Switch (**PI4MSD5V9548AZDEX**) **U14**, that is controlled by an I2C interface from the VE2302 SOM. The I2C interface is made up of signals **LPD_MIO22_I2C0_SCL** and **LPD_MIO23_I2C0_SDA** which comes from the JX1 connector.

- Manufacturer: Diodes Incorporated
- Part Number: **PI4MSD5V9548AZDEX**
- I2C 8-Channel Switch / MUX
- I2C Address: **0x70**

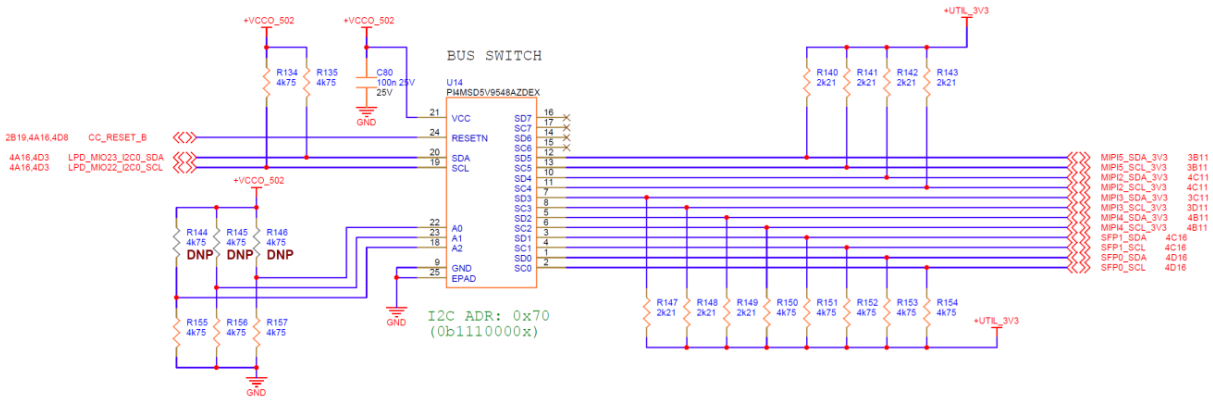

Figure 32 – SFP28 Shared I2C Bus Switch Schematic

IO NAME	IO PIN	FUNCTION	NET NAME	JX Connector	APSoC Pin
SD0	1	SERIAL DATA 0	SFP0_SDA	-	
SC0	2	SERIAL CLOCK 0	SFP0_SCL	-	
SD1	3	SERIAL DATA 1	SFP1_SDA	-	
SC1	4	SERIAL CLOCK 1	SFP1_SCL	-	
SDA		I2C DATA	LPD_MIO23_I2C0_SDA	JX1-A16	Y7
SCL		I2C CLOCK	LPD_MIO22_I2C0_SCL	JX1-A17	T6

Table 25 – SFP28 I2C Bus Switch Pin Mapping

5.17 MIPI Connectors x4

The Versal™ AI Edge Carrier Card features an impressive configuration with four MIPI-CSI2 / MIPI-DSI 22-pin connectors (**J17 through J20**). These connectors emphasize the substantial capacity for connecting a mix of multiple cameras and / or displays to the system.

- Manufacturer: Molex
- Part Number: **545482272**
- 22-position FFC/FPC Connector – Bottom Contacts

- Number of Pin Positions: 22
- Pitch: 0.5 mm

The implementation of the four MIPI Connectors is described in the following figures and tables.

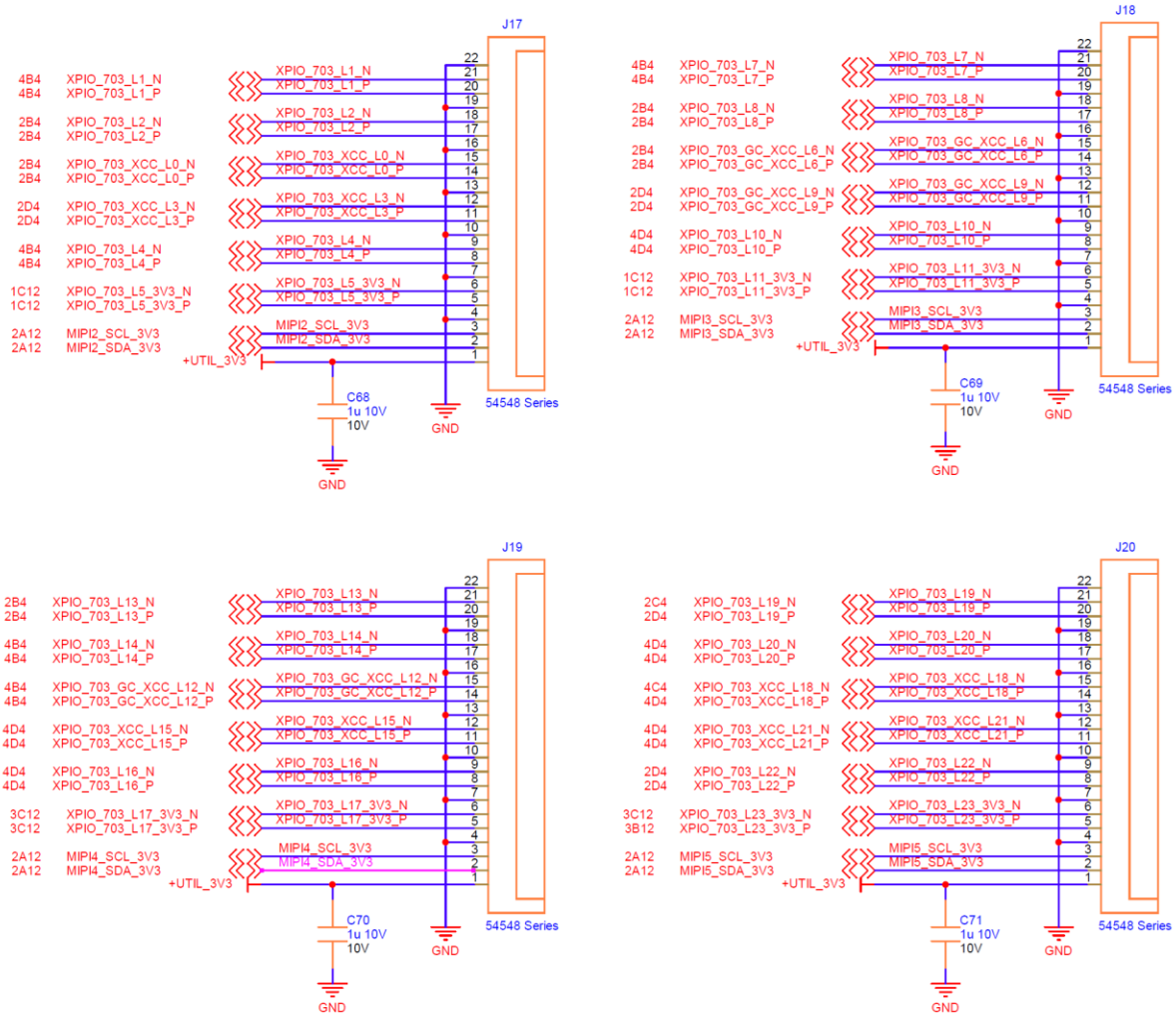

Figure 33 – MIPI Connectors

NOTE: There are two GPIO signals with ***_3V3_P/N** for each MIPI connector that get voltage translated from +3.3V to the respective bank voltage, XPIO bank 703, before reaching the JX2 Connector.

MIPI Conn	MIPI Pin Number	Schematic Name	JX Conn	JX Pin Name
J17	20/21	XPIO_703_L1_P/N	JX2	C6 / C7
J17	17/18	XPIO_703_L2_P/N	JX2	D6 / D7
J17	14/15	XPIO_703_XCC_L0_P/N	JX2	D9 / D10
J17	11/12	XPIO_703_XCC_L3_P/N	JX2	B3 / B4

J17	8/9	XPIO_703_L4_P/N	JX2	C3 / C4
J17	5/6	XPIO_703_L5_3V3_P/N	JX2	D3 / D4
J17	3	MIPI2_SCL_3V3	U14	LPD_MIO22_I2C0_SCL
J17	2	MIPI2_SDA_3V3	U14	LPD_MIO23_I2C0_SDA
J18	20/21	XPIO_703_L7_P/N	JX2	C15 / C16
J18	17/18	XPIO_703_L8_P/N	JX2	D15 / D16
J18	14/15	XPIO_703_GC_XCC_L6_P/N	JX2	D18 / D19
J18	11/12	XPIO_703_GC_XCC_L9_P/N	JX2	B6 / B7
J18	8/9	XPIO_703_L10_P/N	JX2	A3 / A4
J18	5/6	XPIO_703_L11_3V3_P/N	JX2	A6 / A7
J18	3	MIPI3_SCL_3V3	U14	LPD_MIO22_I2C0_SCL
J18	2	MIPI3_SDA_3V3	U14	LPD_MIO23_I2C0_SDA
J19	20/21	XPIO_703_L13_P/N	JX2	D21 / D22
J19	17/18	XPIO_703_L14_P/N	JX2	C18 / C19
J19	14/15	XPIO_703_GC_XCC_L12_P/N	JX2	C21 / C22
J19	11/12	XPIO_703_XCC_L15_P/N	JX2	A12 / A13
J19	8/9	XPIO_703_L16_P/N	JX2	A9 / A10
J19	5/6	XPIO_703_L17_3V3_P/N	JX2	B12 / B13
J19	3	MIPI4_SCL_3V3	U14	LPD_MIO22_I2C0_SCL
J19	2	MIPI4_SDA_3V3	U14	LPD_MIO23_I2C0_SDA
J20	20/21	XPIO_703_L19_P/N	JX2	B21 / B22
J20	17/18	XPIO_703_L20_P/N	JX2	A18 / A19
J20	14/15	XPIO_703_XCC_L18_P/N	JX2	A21 / A22
J20	11/12	XPIO_703_XCC_L21_P/N	JX2	A15 / A16
J20	8/9	XPIO_703_L22_P/N	JX2	B15 / B16
J20	5/6	XPIO_703_L23_3V3_P/N	JX2	B18 / B19
J20	3	MIPI5_SCL_3V3	U14	LPD_MIO22_I2C0_SCL
J20	2	MIPI5_SDA_3V3	U14	LPD_MIO23_I2C0_SDA

Table 26 – MIPI Connectors to JX2 Connector Mapping

NOTE: The following figure shows a conversion from the MIPI-22 pin connector solution to the MIPI-CSI2 15-pin or MIPI-DSI 15-pin connectors. It is important to understand that the MIPI-22 pin connector solution on the Versal™ AI Edge Carrier Card has bottom contacts on the connector. It is important to ensure that the way the connections between the two conversion connectors aligns with the utilized flex cable properly to ensure that the end-user does not short something unintended.

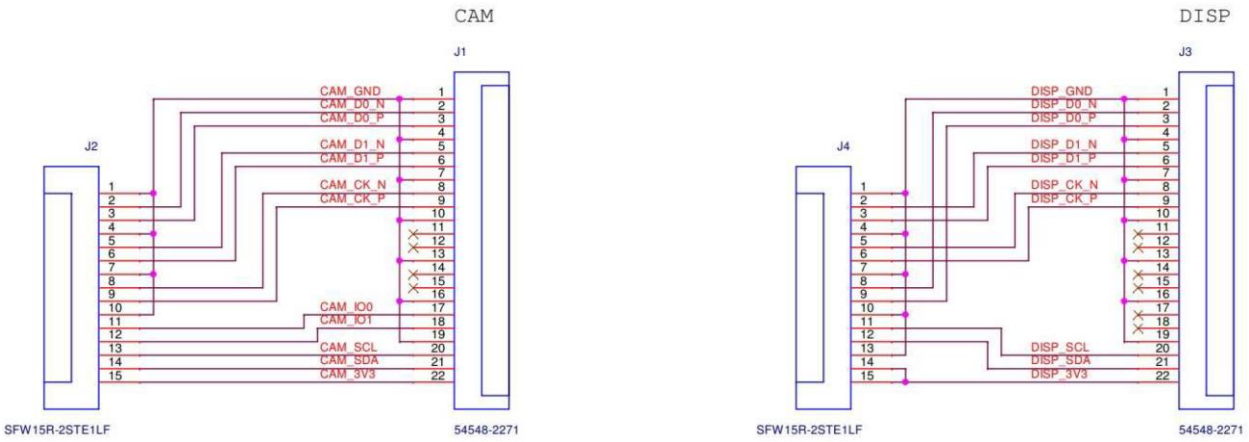

Figure 34 – MIPI 22-pin to 15-pin Conversions

5.18 MIPI Interface – Shared I2C Bus Switch

The last two pins of each MIPI Connector (**MIPI[2-5]_SCL_3V3** and **MIPI[2-5]_SDA_3V3**) are all connected to the output of an I2C Bus Switch (**PI4MSD5V9548AZDEX**) **U14**, that is controlled by an I2C interface from the VE2302 SOM. The I2C interface is made up of signals **LPD_MIO22_I2C0_SCL** and **LPD_MIO23_I2C0_SDA** which comes from the JX1 connector.

- Manufacturer: Diodes Incorporated
- Part Number: **PI4MSD5V9548AZDEX**
- I2C 8-Channel Switch / MUX
- I2C Address: **0x70**

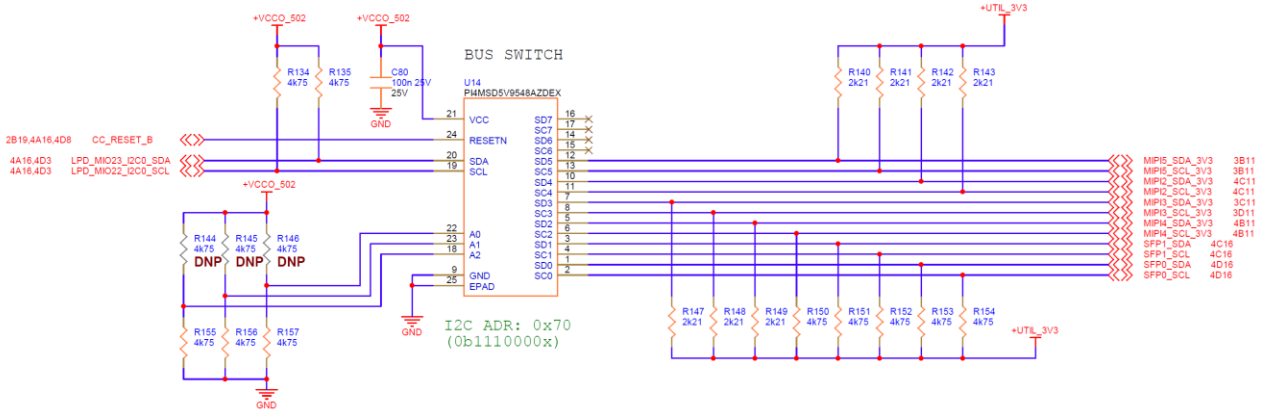

Figure 35 – MIPI Shared I2C Bus Switch Schematic

IO NAME	IO PIN	FUNCTION	NET NAME	JX Connector	APSoC Pin
SD2	5	SERIAL DATA 2	MIPI4_SDA_3V3	-	-
SC2	6	SERIAL CLOCK 2	MIPI4_SCL_3V3	-	-
SD3	7	SERIAL DATA 3	MIPI3_SDA_3V3	-	-
SC3	8	SERIAL CLOCK 3	MIPI3_SCL_3V3	-	-
SD4	10	SERIAL DATA 0	MIPI2_SDA_3V3	-	-
SC4	11	SERIAL CLOCK 0	MIPI2_SCL_3V3	-	-
SD5	12	SERIAL DATA 1	MIPI5_SDA_3V3	-	-
SC5	13	SERIAL CLOCK 1	MIPI5_SCL_3V3	-	-
SDA	20	I2C DATA	LPD_MIO23_I2C0_SDA	JX1-A16	Y7
SCL	19	I2C CLOCK	LPD_MIO22_I2C0_SCL	JX1-A17	T6

Table 27 – MIPI I2C Bus Switch Pin Mapping

5.19 HDMI RX and TX Interfaces

The Versal™ AI Edge Carrier Card provides HDMI video input and video output using 12-Gbps TMDS® and FRL HDMI™ hybrid redriver devices. The HDMI video input and video output is provided on Molex **2086581061** HDMI connectors (**J21** and **J22**). The HDMI hybrid redriver solution supports HDMI 2.1 data rates up to 12-Gbps but the resolution limitation will be set due to available IP and the Versal™ AI Edge device populated on the VE2302 SOM. As a result, the HDMI 2.1 data rate will be limited to 8-Gbps.

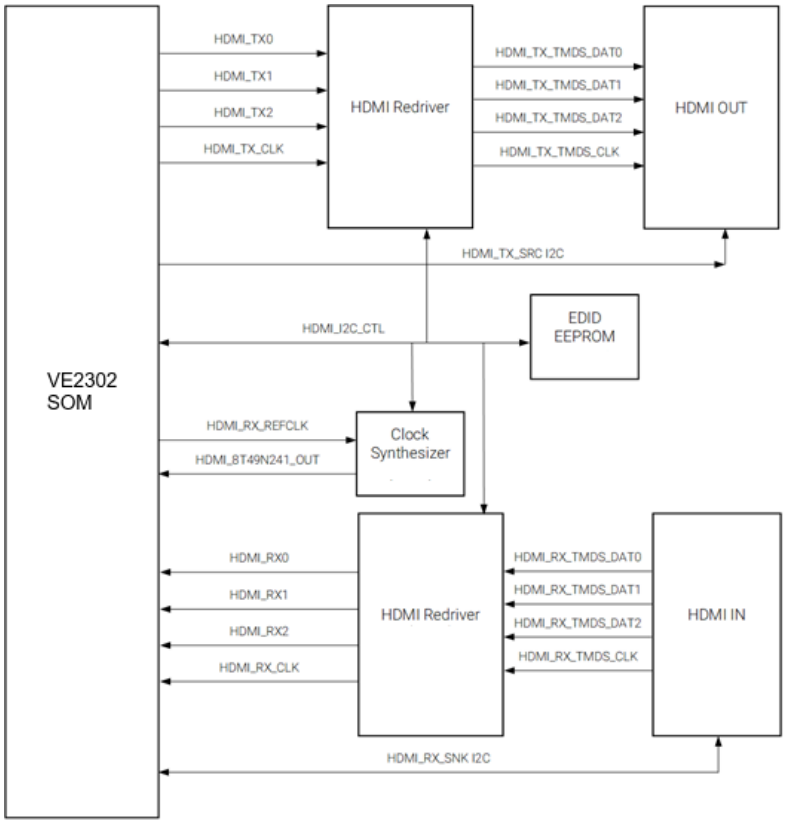

Figure 36 – HDMI Interface Block Diagram

5.19.1 HDMI Source Clock

The Versal™ AI Edge Carrier Card includes a 400 MHz FRL/DRU clock, **U70**, used as the reference for driving the Versal™ device logic and related circuit for HDMI.

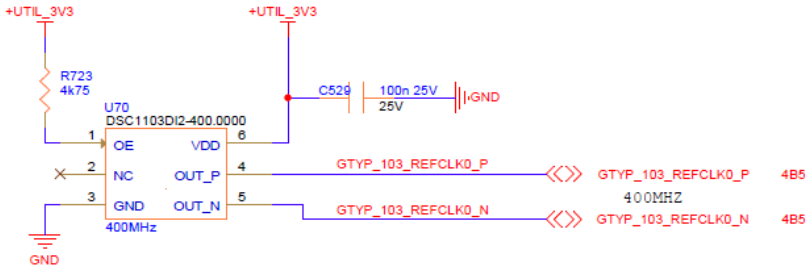

Figure 37 – HDMI 400MHz FRL/DRU Clock

OSC Pin Number	JX Connector Pin Name	JX Connector Pin Number	APSoC Pin Number
U70-4	GTYP_103_REFCLK0_P	JX3-C7	JX3-C7
U70-5	GTYP_103_REFCLK0_N	JX3-C8	JX3-C8

Table 28 – HDMI 400MHz FRL/DRU JX3 Mapping

5.19.2 HDMI Clock Recovery

The Versal™ AI Edge Carrier Card includes a programmable clock generator that is connected to the HDMI CTL I2C Bus. This programmable clock generator acts as a jitter attenuator. The VE2302 SOM can output a differential RX recovered clock (**CLKIN_P_CG / CLKIN_N_CG**) for jitter attenuation. The jitter attenuated clock (**GTYP_104_REFCLK1_P/N**) is routed as a reference clock to GTYP bank 104. The **8TN49N241** is used to generate the reference clock for the HDMI transmitter subsystem. When the HDMI transmitter is used in standalone mode (FRL/TMDS) or pass-through mode (FRL), the **8T49N241** clock synthesizer operates in free running mode and uses an external oscillator as reference. When the HDMI operation is in pass-through mode (TMDS), the **8T49N241** generates a jitter-attenuated reference clock to drive the HDMI transmitter subsystem with a phase-aligned version of the HDMI RX subsystem TMDS clock.

The programmable clock source, **U1**, is used to generate **GTYP_104_REFCLK1_P/N** clock signals and forward them to the **JX3** Connector. This programmable clock source is depicted in the HDMI Interface block diagram as **CLOCK SYNTHESIZER**.

- Manufacturer: Renesas Electronics
- Part Number: **8T49N241-998NLGI**
- Programmable clock generator
- Single-ended or Differential Outputs
- I2C Address: **0xD8**

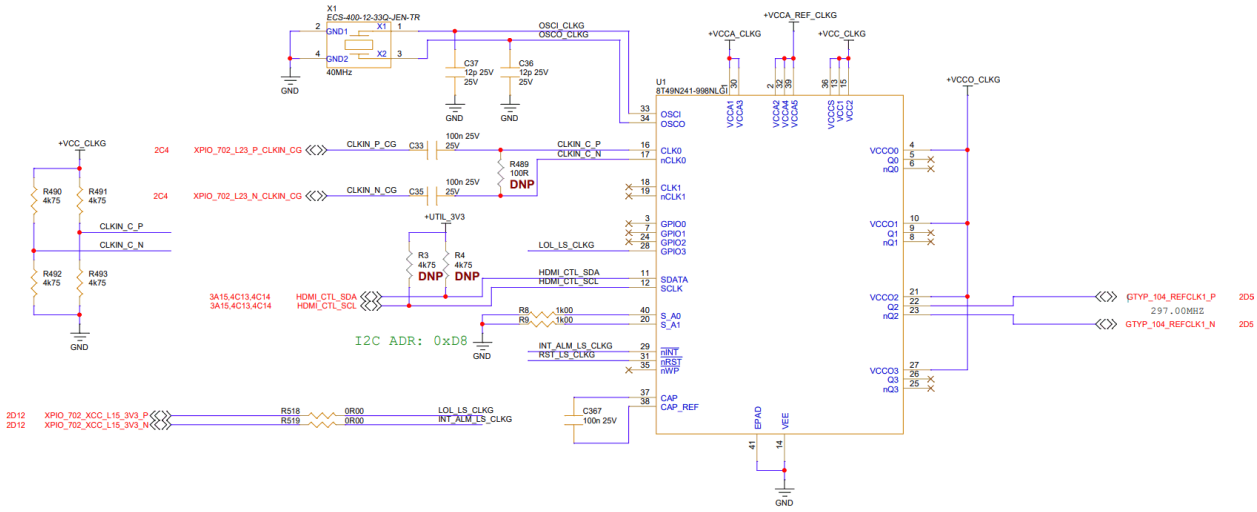

Figure 38 – HDMI Clock Recovery Schematic

The clock generator I2C programming interface is connected to **JX2** Connector at pin **A34** (**XPIO_702_L22_N_HCTL_SCL**) and pin A33 (**XPIO_702_L22_P_HCTL_SDA**).

NOTE: The signal with **_3V3_P/N** in the net name goes through a voltage translator before reaching the **JX** Connector.

Source	Pin Name	Schematic Net Name	8T49N241 (U1) Pin Name / No	APSoC Pin
X1	1	OSCI_CLKG	OSCI (33)	-
X1	3	OSCO_CLKG	OSCO (34)	-
JX2	B33	XPIO_702_L23_P_CLKIN_CG	CLK0 (16)	J21
JX2	B34	XPIO_702_L23_N_CLKIN_CG	nCLK0 (17)	J22
JX2	A34	HDMI_CTL_SCL (XPIO_702_L22_N_HCTL_SCL)	SDATA (11)	L22
JX2	A33	HDMI_CTL_SDA (XPIO_702_L22_P_HCTL_SDA)	SCLK (12)	K21
JX2	D30	LOL_LS_CLKG (XPIO_702_XCC_L15_3V3_P)	GPIO3 (28)	M22
JX2	D31	INT_ALM_LS_CLKG (XPIO_702_XCC_L15_3V3_N)	nINT (29)	M23
JX2	C39	RST_LS_CLKG (XPIO_702_GC_XCC_L12_3V3_P)	nRST (31)	U23
JX3	B10	GTYP_104_REFCLK1_P	Q2 (22)	F7
JX3	B11	GTYP_104_REFCLK1_N	nQ2 (23)	F6

Table 29 – HDMI Clock Recovery Pin Assignments

Only the third port of the 4 port clock generators LVDS output clocks is physically connected and its frequency is programmed via HDMI IP to support the expected resolution of the transmitted HDMI interface.

The clock generator receives 40.00MHz as reference from a SMD crystal oscillator (**X1**).

- Manufacturer: ECS
- Part Number: **ECS-400-12-33Q-JEN-TR**
- Crystals 40.000MHz 12pF AEC-Q200 -40C +85C

5.19.3 HDMI Transceiver Lanes

The HDMI data lanes are mapped to the GTYPs through the HDMI hybrid redriver devices (**U15** and **U17**). The signals are then sent to the JX Connectors.

- Manufacturer: Texas Instruments
- Part Number: **TMDS1204IRNQR**
- Display Interface IC 12-Gbps HDMI 2.1 hybrid redriver
- HDMI TX I2C Address: **0x5E** (**U15**)
- HDMI RX I2C Address: **0x5B** (**U17**)

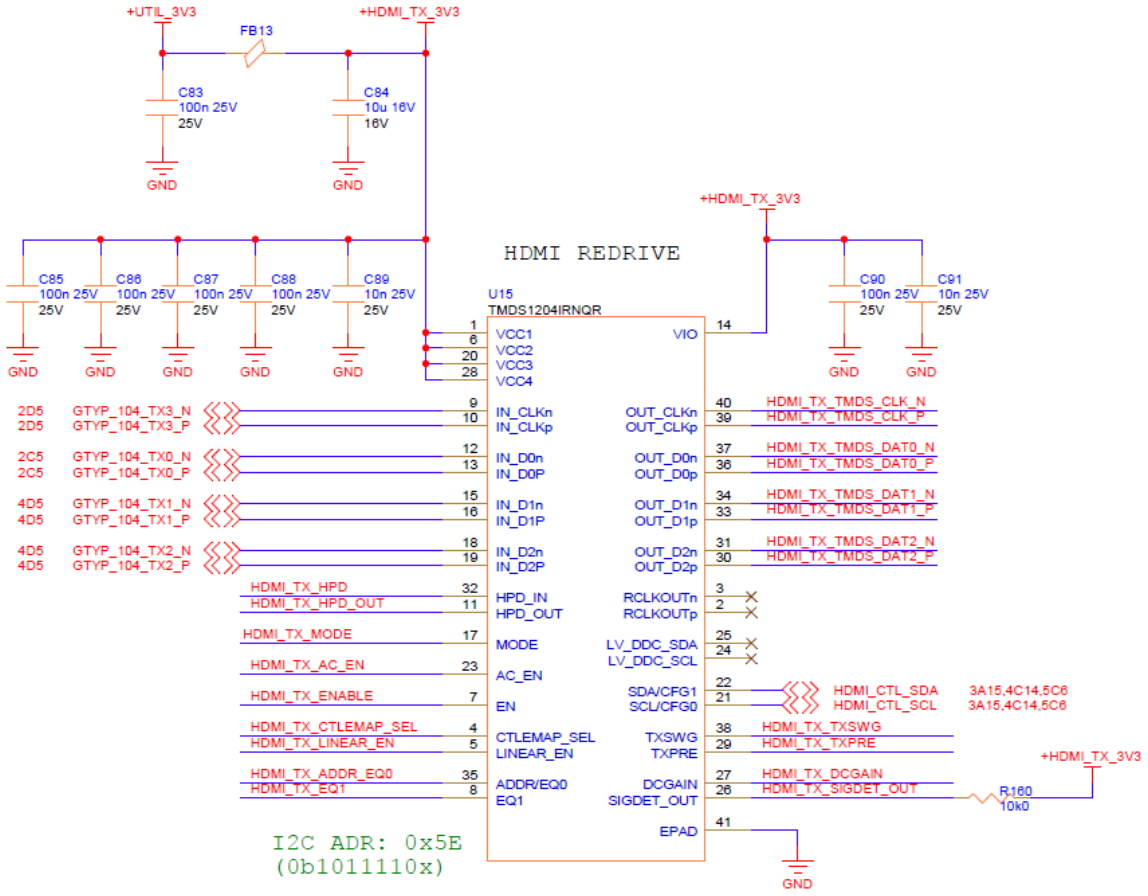

Figure 39 – HDMI TX Redriver Schematic

Redriver Chip Connection	JX Connector Pin Name	JX Connector Pin Number	APSoC Pin Number
HDMI_TX_TMDS_CLK_P	GTYP_104_TX3_P	JX3-B17	B8
HDMI_TX_TMDS_CLK_N	GTYP_104_TX3_N	JX3-B18	B7
HDMI_TX_TMDS_DAT2_P	GTYP_104_TX2_P	JX3-A20	C5
HDMI_TX_TMDS_DAT2_N	GTYP_104_TX2_N	JX3-A21	C4
HDMI_TX_TMDS_DAT 1_P	GTYP_104_TX1_P	JX3-A14	D8
HDMI_TX_TMDS_DAT 1_N	GTYP_104_TX1_N	JX3-A15	D7
HDMI_TX_TMDS_DAT 0_P	GTYP_104_TX0_P	JX3-B23	E5
HDMI_TX_TMDS_DAT 0_N	GTYP_104_TX0_N	JX3-B24	E4

Table 30 – HDMI TX Connector GTYP Pin JX3 Mapping

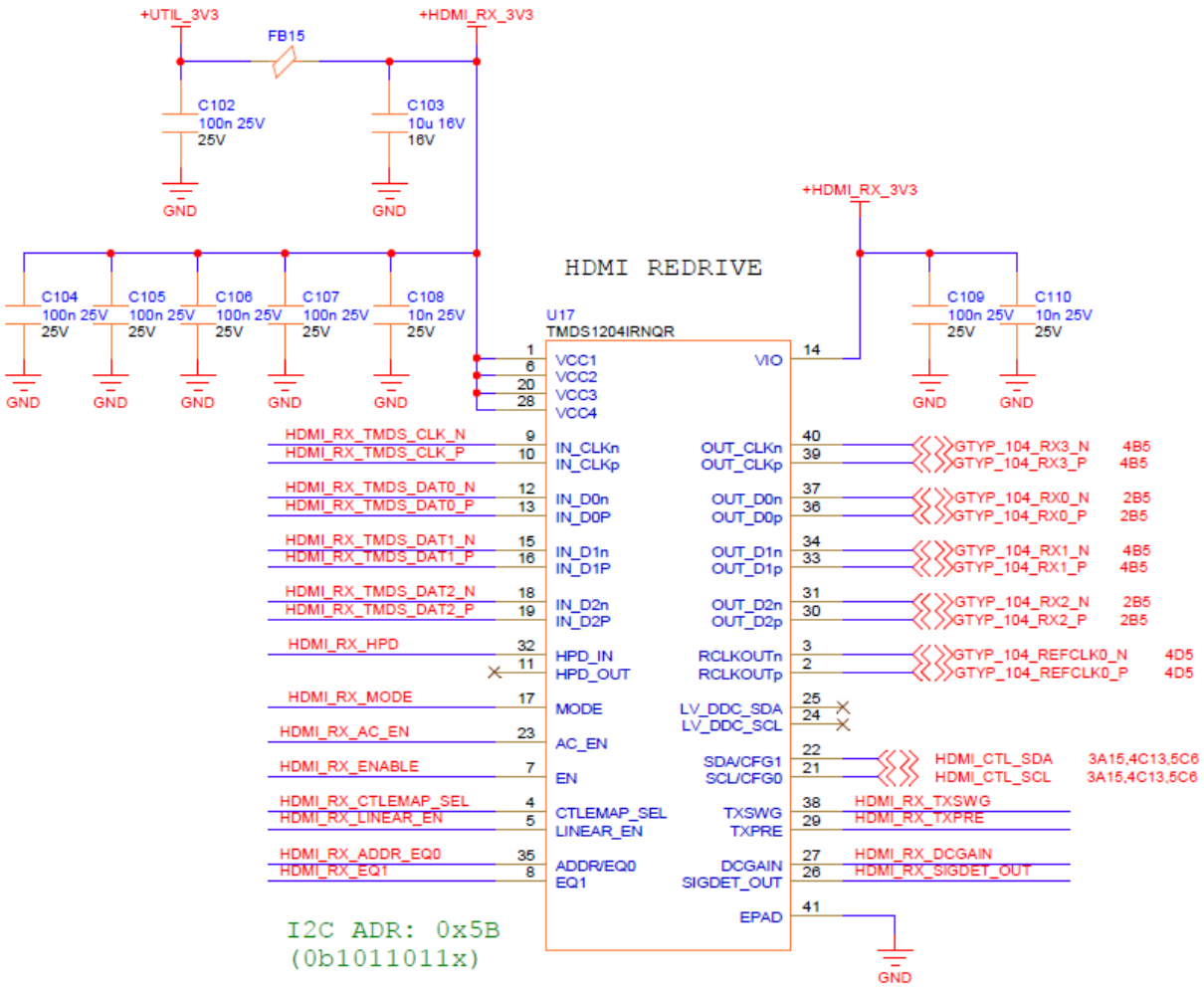

Figure 40 – HDMI RX Redriver Schematic

Redriver Chip Connection	JX Connector Pin Name	JX Connector Pin Number	APSoC Pin Number
HDMI_RX_TMDS_CLK_P	GTYP_104_RX3_P	JX3-C14	A5
HDMI_RX_TMDS_CLK_N	GTYP_104_RX3_N	JX3-C15	A4
HDMI_RX_TMDS_DAT2_P	GTYP_104_RX2_P	JX3-D17	B2
HDMI_RX_TMDS_DAT2_N	GTYP_104_RX2_N	JX3-D18	B1
HDMI_RX_TMDS_DAT 1_P	GTYP_104_RX1_P	JX3-C20	D2
HDMI_RX_TMDS_DAT 1_N	GTYP_104_RX1_N	JX3-C21	D1
HDMI_RX_TMDS_DAT 0_P	GTYP_104_RX0_P	JX3-D23	F2
HDMI_RX_TMDS_DAT 0_N	GTYP_104_RX0_N	JX3-D24	F1

Table 31 – HDMI RX Connector GTYP Pin JX3 Mapping

5.19.4 HDMI Control Signals

The HDMI RX and TX interface solutions requires control pins mapped to the Versal™ AI Edge device. The table below lists the 18 I/O required to implement the HDMI RX and HDMI TX control signals.

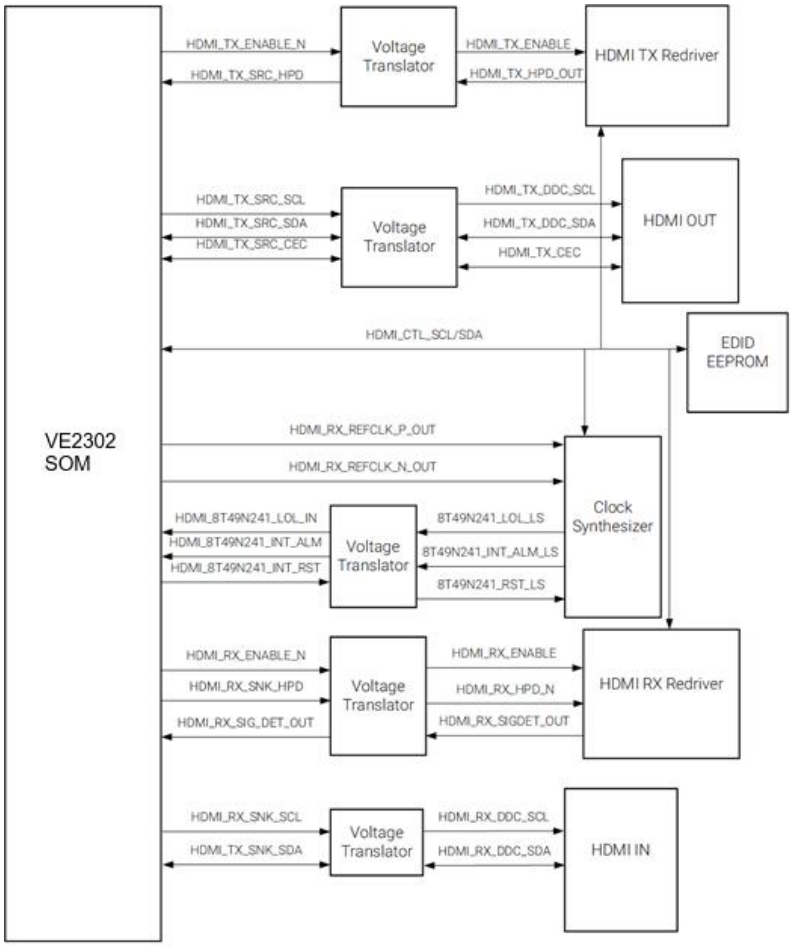

Figure 41 – HDMI Control Signals Block Diagram

NOTE: The signals in the table below are either voltage translated with a specific IC such as the case for I2C interfaces or utilize FETs to implement the voltage translation.

HDMI Redriver Net Name	JX Connector Pin Name	JX Connector Pin Number	APSoC Pin Number
HDMI_CTL_SCL	XPIO_702_L22_N_HCTL_SCL	JX2-A34	L22
HDMI_CTL_SDA	XPIO_702_L22_P_HCTL_SDA	JX2-A33	K21
HDMI_TX_CEC	XPIO_702_XCC_L21_N_HTX_CEC	JX2-B37	M21
HDMI_RX_CEC	XPIO_702_L17_P_HRX_CEC	JX2-C30	K23
HDMI_TX_DDC_SCL	XPIO_702_L20_P_HTX_SCL	JX2-A36	R21
HDMI_TX_DDC_SDA	XPIO_702_L20_N_HTX_SDA	JX2-A37	P22
HDMI_TX_HPD_OUT	XPIO_702_L19_N_HTX_HPD	JX2-A40	R22

HDMI_TX_ENABLE	XPIO_702_L19_P_HTX_ENB_B	JX2-A39	T21
HDMI_RX_DDC_SCL	XPIO_702_L18_P_HRX_SCL	JX2-B39	V21
HDMI_RX_DDC_SDA	XPIO_702_L18_N_HRX_SDA	JX2-B40	U22
HDMI_RX_HPD	XPIO_702_L16_N_HRX_HDP_B	JX2-C28	K24
HDMI_RX_ENABLE	XPIO_702_L16_P_HRX_ENB_B	JX2-C27	L23
HDMI_RX_SIGDET_OUT	XPIO_702_L17_N_HRX_DETOUT	JX2-C31	J24

Table 32 – HDMI Control Signals Pin Map

NOTE: The signals **HDMI_CTL_SCL** and **HDMI_CTL_SDA** are also connected to the EDID EEPROM **U19** (**M24128-BRDW6TP**) which is Write Protected by default. The protection can be disabled by closing the connected Jumper **J23**. The I2C Address of the EDID EEPROM **U19** is **0x50**.

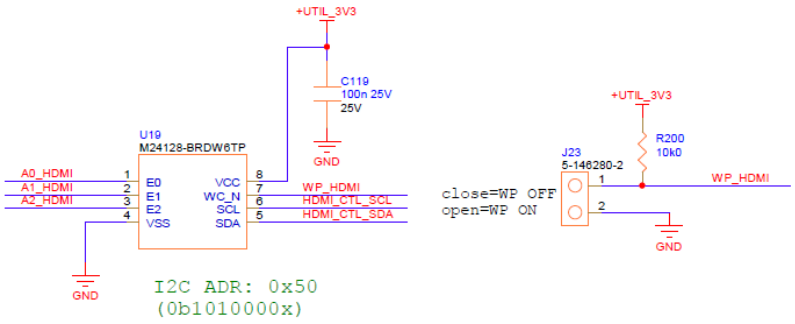

Figure 42 – HDMI EDID EEPROM Schematic

5.20 HSIO Expansion Interface

The Versal™ AI Edge Carrier Card offers a Samtec connector for HSIO (high-speed I/O) expansion interfaces. This interface contains a mix of GTYPs (multi-gigabit transceivers) and HDIO (high density) PL (programmable logic) I/Os. Samtec QSH-020-01-F-D-DP-A-K-TR connector is used to provide the high-speed site with GTYP transceivers which is also known as a TXR2 PLIO expansion interface.

NOTE: The multi-gigabit transceivers can be used to implement transceiver-based designs such as PCIe and additional SFP interfaces. Performance of the transceiver interfaces on this connector is highly dependent on the design of the mating HSIO board.

The I2C ports mapped to the HSIO expansion site is delivered via the I2C bus switch located on the SOM. Please review the I2C Bus Switch section of the **VE2302 SOM Hardware User Guide** document for more details on how the I2C pins from the HSIO expansion site are mapped to the I2C bus switch device.

NOTE: The GTYP reference clock that is provided from the mating HSIO board is an input to a clock multiplexer solution that allows for multiple GTYP reference clocks to be source the **GTYP_103_REFCLK1_P/N** pins on the Versal™ AI Edge device. Please see the **Clock Sources** section of this document for a better understanding of the selection of the mating HSIO board GTYP reference clock as the source for the second GTYP reference clock on quad 103.

- Manufacturer: Samtec
- Part Number: QSH-020-01-F-D-DP-A-K-TR
- 0.50mm / 40-position differential array connector

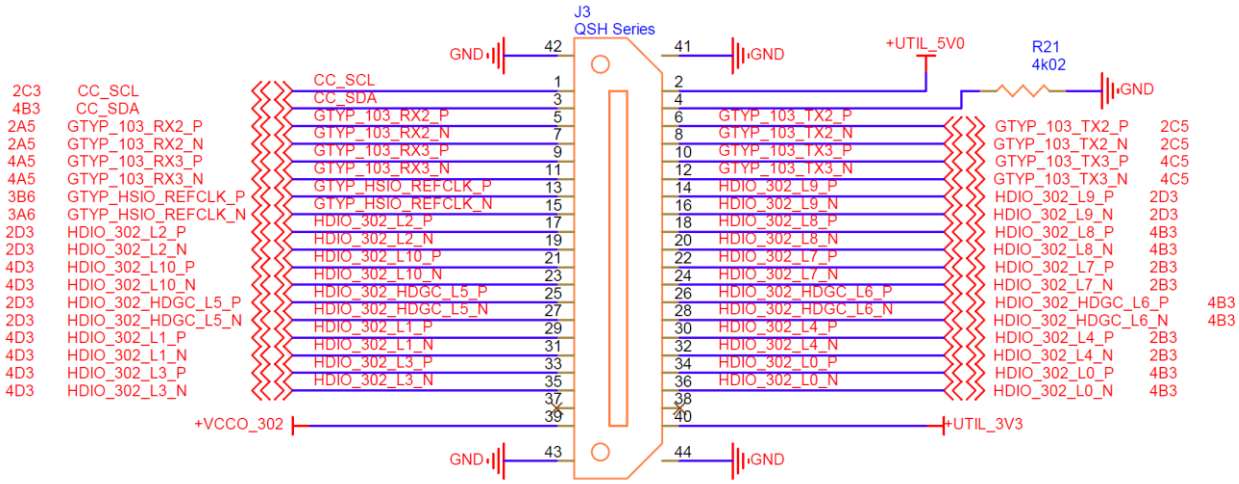

Figure 43 – HSIO Expansion Site Implementation

APSoC Pin Number (SOM)	SOM Connector Pin (CON1)	Schematic Net Name	HSIO Interface (J1) Pin Numbers
MIO50 / MIO51 (AB10 / AA10)	U14 6 /5 (Switch)	CC_SCL / CC_SDA	1 / 3
K2 / K1	JX3 D29 / D30	GTYP_103_RX2_P/N	5 / 7
J5 / J4	JX3 B29 / B30	GTYP_103_TX2_P/N	6 / 8
H2 / H1	JX3 C26 / C27	GTYP_103_RX3_P/N	9 / 11
G5 / G4	JX3 A26 / A27	GTYP_103_TX3_P/N	10 / 12
K7 / K6	JX3 D10 / D11	GTYP_HSIO_REFCLK_P/N	13 / 15
B12 / A13	JX1 B7 / B8	HDIO_302_L9_P/N	14 / 16
E13 / D14	JX1 B10 / B11	HDIO_302_L2_P/N	17 / 19
B11 / A11	JX1 C7 / C8	HDIO_302_L8_P/N	18 / 20
B13 / A14	JX1 A7 / A8	HDIO_302_L10_P/N	21 / 23
B10 / A10	JX1 D7 / D8	HDIO_302_L7_P/N	22 / 24
D11 / C12	JX1 B13 / B14	HDIO_302_HDGC_L5_P/N	25 / 27
D10 / C10	JX1 C10 / C11	HDIO_302_HDGC_L6_P/N	26 / 28
C14 / C13	JX1 A10 / A11	HDIO_302_L1_P/N	29 / 31
F11 / E11	JX1 D10 / D11	HDIO_302_L4_P/N	30 / 32
E12 / D12	JX1 A13 / A14	HDIO_302_L3_P/N	33 / 35
F14 / E14	JX1 C13 / C14	HDIO_302_L0_P/N	34 / 36

Table 33 – HSIO Expansion Site Connections to SOM

NOTE: **GTYP_HSIO_REFCLK_P/N** usage implies it is selected on clock multiplexer, **U71**, by shunting jumper **J58**.

5.21 Gigabit Ethernet RJ45 Connector

The VE2302 SOM provides gigabit ethernet PHY connections across the **JX1** connector to an Abracon RJ45 jack, **J4**, on the Versal™ AI Edge Carrier Card that support 10/100/1000 Base-T and AutoMDIX.

- Manufacturer: Abracon LLC
- Part Number: **ARJM11C7-502-KB-EW2**
- 1000 Mb/s RJ-45 Connector

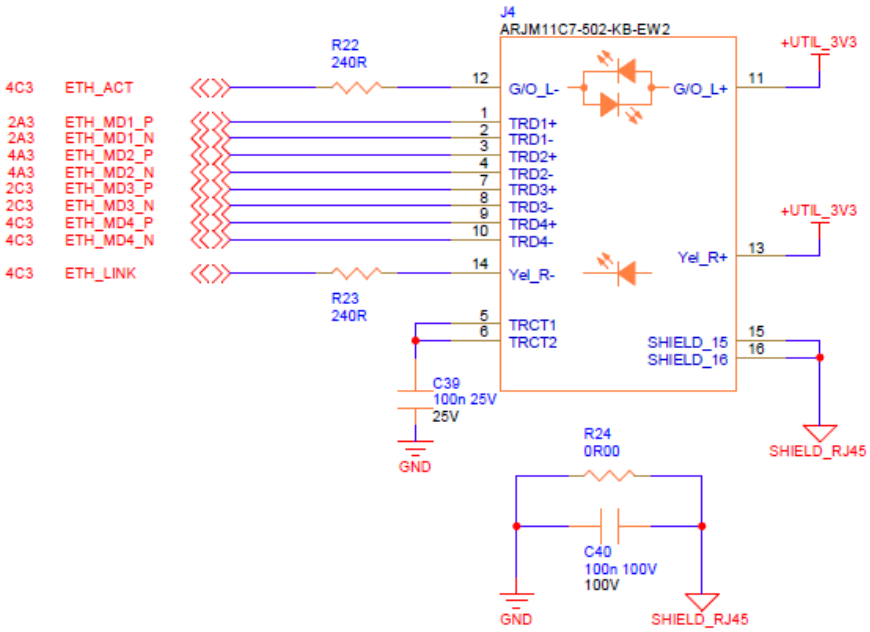

Figure 44 – RJ45 Jack Schematic

The Ethernet connections from the **JX1** connector to the Rj45 jack at **J4** are listed in the following table:

JX1 Pin Name	Schematic Net Name	ARJM11C7 (J4) Pin Name / No
A29	ETH_ACT	G/O_L- (12)
D32/D33	ETH_MD1_P/N	TRD1+/- (1/2)
C32/C33	ETH_MD2_P/N	TRD2+/- (3/4)
B32/B33	ETH_MD3_P/N	TRD3+/- (7/8)
A32/A33	ETH_MD4_P/N	TRD4+/- (9/10)
A30	ETH_LINK	Yel_R- (14)

Table 34 – Ethernet PHY JX1 Connections

There are two LED drivers, **ETH_ACT** (LED1) and **ETH_LINK** (LED2), that come from the Ethernet PHY on the VE2302 SOM that connects to the RJ45 Ethernet Jack (**J4**). The Microchip **KSZ9131** data sheet

contains details concerning the potential functions mapped to the LED1 and LED2 pins. For LED2, a LINK function is mapped to this pin. For LED1, an ACTIVITY function is mapped to this pin.

For implementation details on the RGMII side of the Ethernet PHY, please refer to the **VE2302 SOM Hardware User Guide**.

5.22 USB 2.0 Interface

The Versal™ AI Edge Carrier Card utilizes the USB PHY connection from the **JX1** connector to map to a Samtec USB Type-A Connector (**J6**).

- Manufacturer: Samtec
- Part Number: **USB-A-S-F-B-TH**
- USB 2.0 Type A Connector

JX1 Pin Name	Schematic Net Name	USB 2.0	USB Pin Name
D29	USB_D_P	3	D+
D30	USB_D_N	2	D-
B30	USB_ ID	Not Used	Not Used
D12	+USB_VBUS	1	VBUS

Table 35 – USB 2.0 PHY JX1 Connections

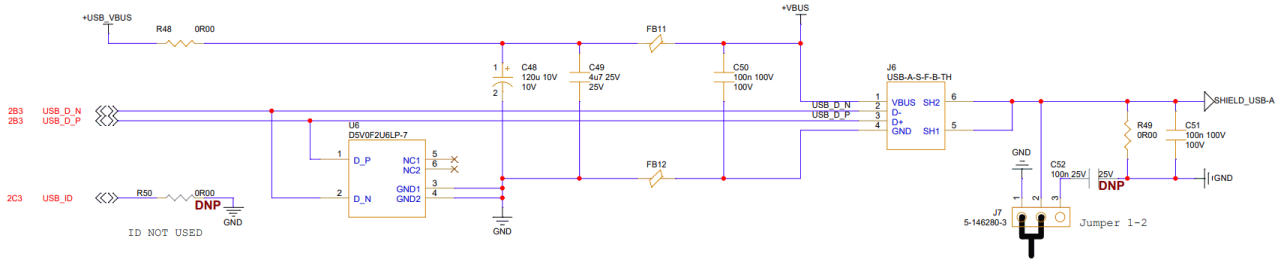

Figure 45 – USB 2.0 Schematic

NOTE: As shown in the figure, the shield for the USB 2.0 type-A connector (**J6**) is tied to GND by a jumper on header **J7** pins 1-2. The USB shield can optionally be connected through a capacitor to GND by inserting a jumper across pins 2-3 on header **J7**. By default, capacitor **C52** is not populated.

For implementation details on the ULPI side of the USB 2.0 interface, please refer to the **VE2302 SOM Hardware User Guide**.

5.23 CAN Interfaces

The Versal™ AI Edge Carrier Card implements two CAN interfaces (**U8** and **U9**). The two CAN interfaces are connected to the CAN transceivers via 6 LPD MIO pins on the **JX1** Connector. The CAN interfaces terminate to two wire-to-board terminal blocks, **J9** and **J12**. One of the two CAN interfaces is represented in the following tables.

- Manufacturer: NXP Semiconductors
- Part Number: **TJA1042BT/0Z**
- IC High-Speed CAN Transceiver

- Manufacturer: Wurth Elektronik
- Part Number: **691111710003**
- Pluggable Terminal Blocks WR-TBL 250VAC 15A 3P Straight

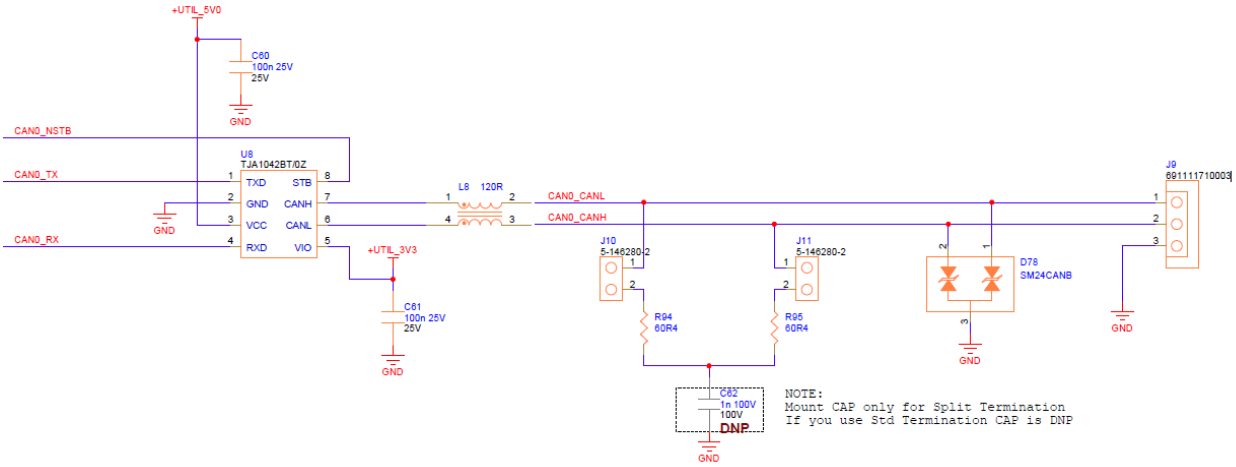

Figure 46 – CAN0 Interface Schematic

I/O Name	Terminal Block Pin
CAN0_CANL	J9-1
CAN0_CANH	J9-2
CAN1_CANL	J12-1
CAN1_CANH	J12-2

Table 36 – CAN Terminal Blocks Pin Map

The signals that get routed to the VE2302 SOM via the **JX1** connectors require voltage-level translation from **+UTIL_3.3V** to **+VCCO_502**.

Schematic Net Name	I/O Name	JX1 Pin Number	APSoC Pin Number
LPD_MIO12_CAN0_NSTB	CAN0_NSTB	C24	W4
LPD_MIO15_CAN0_TX	CAN0_TX	D20	T5
LPD_MIO14_CAN0_RX	CAN0_RX	D21	T4
LPD_MIO13_CAN1_NSTB	CAN1_NSTB	C23	V4
LPD_MIO20_CAN1_TX	CAN1_TX	B17	W6
LPD_MIO21_CAN1_RX	CAN1_RX	B16	U6

Table 37 – CAN Interfaces JX1 Mapping

The Versal™ AI Edge Carrier Card implements 4 Jumpers (**J10**, **J11**, **J13** and **J14**) to add the possibility to make the Carrier a Termination Point for the CAN Bus.

CAN Bus	Jumpers	Position	Carrier Option
CAN0	J10-J11	Shunted	Termination point
		Not shunted	Not a termination
CAN1	J13-J14	Shunted	Termination point
		Not shunted	Not a termination

Table 38 – CAN Termination Option Configuration

5.24 User Push Buttons

The Versal™ AI Edge Carrier Card provides two PMC active high user PUSH BUTTONs (**SW1** and **SW2**). These PUSH BUTTONs are connected to the MIO[37] and MIO[46] pin on the **JX** Connector and operated at proper bank voltage, **+VCCO_PMC_MIO**.

- Manufacturer: C&K
- Part Number: **PTS810SJG250SMTRLFS**
- Switch tactile SPST-NO 0.05A 16V

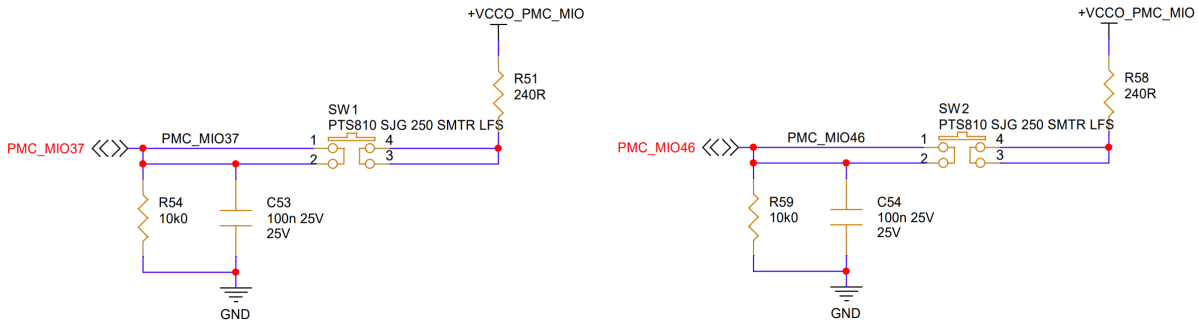

Figure 47 – PMC Push Buttons

Switch	I/O Net Name	JX Connector	APSoC Pin Number
SW1	PMC_MIO37	JX1-D26	AE7
SW2	PMC_MIO46	JX1-A20	AF9

Table 39 – PMC Push Buttons Pin Assignment

The Versal™ AI Edge Carrier Card also provides two XPIO active high user PUSH BUTTONs (**SW3** and **SW4**). These PUSH BUTTONs are connected to **XPIO_702_L26_P** and **XPIO_703_GC_XCC_L24_P** pins on the **JX** Connector and operated at proper bank voltage, **+VCCO_702** and **+VCCO_703** respectively.

- Manufacturer: C&K
- Part Number: **PTS810SJG250SMTRLFS**
- Switch tactile SPST-NO 0.05A 16V

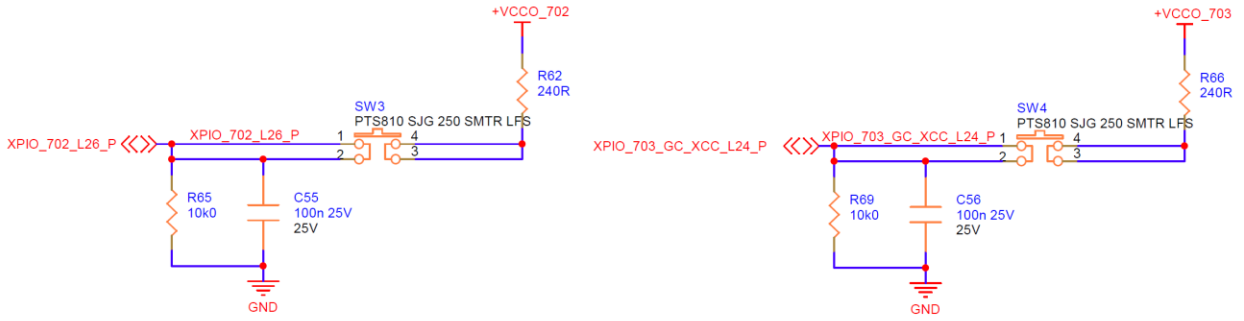

Figure 48 – XPIO Push Buttons

Switch	I/O Net Name	JX Connector	APSoC Pin Number
SW3	XPIO_702_L26_P	JX2-B9	N25
SW4	XPIO_703_GC_XCC_L24_P	JX2-C9	F23

Table 40 – XPIO Push Buttons Pin Assignment

5.25 User LEDs

The Versal™ AI Edge Carrier Card provides two PMC MIO driven active high user Red Diffused 2SMD LEDs (**D2** and **D4**). These USER LEDs are connected to PMC MIO pins on the **JX** Connector.

- Manufacturer: Everlight Electronics Co Ltd
- Part Number: **EAST0603RA0**

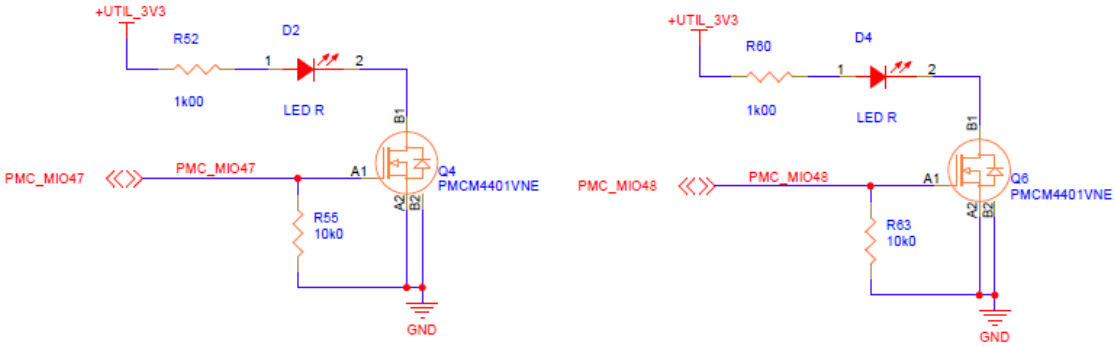

Figure 49 – PMC MIO LEDs Schematic

LED Component	I/O Net Name	JX Connector	APSoC Pin Number
D2	PMC_MIO47	JX1-A19	AF10
D4	PMC_MIO48	JX1-B20	AD10

Table 41 – PMC MIO LEDs Pin Assignment

The Versal™ AI Edge Carrier Card provides two XPIO driven active high user Red Diffused 2SMD LEDs (**D5** and **D6**). These USER LEDs are connected to XPIO pins on the **JX** Connector.

- Manufacturer: Everlight Electronics Co Ltd
- Part Number: **EAST0603RA0**

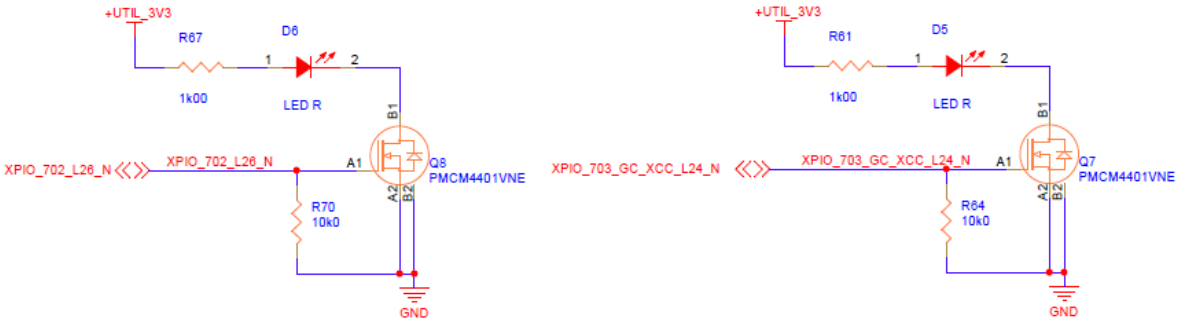

Figure 50 – XPIO LEDs Schematic

LED Component	I/O Net Name	JX Connector	APSoC Pin Number
D6	XPIO_702_L26_N	JX2-B10	M25
D5	XPIO_703_GC_XCC_L24_N	JX2-C10	F24

Table 42 – XPIO LEDs Pin Assignment

The Versal™ AI Edge Carrier Card provides two active high user RED LED (**D3** and **D7**) that are connector to I2C controlled GPIO pins on the **JX** connectors. Please review the **VE2302 SOM Hardware User Guide** for information on the I2C 8-bit IO Expander that controls these GPIO pins.

- Manufacturer: Everlight Electronics Co Ltd
- Part Number: **EAST0603RA0**

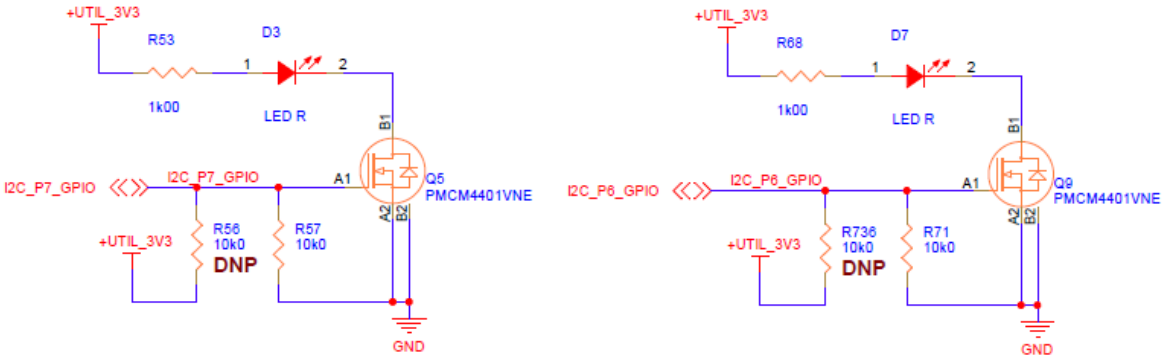

Figure 51 – I2C GPIO Expander LEDs Schematic

LED Component	I/O Net Name	JX Connector	APSoC Pin Number
D3	I2C_P7_GPIO	JX1-C19	PMC_I2C (AA10 / AB10)
D7	I2C_P6_GPIO	JX1-C19	PMC_I2C (AA10 / AB10)

Table 43 – I2C GPIO Expander LEDs Pin Assignment

5.26 User Switch

The Versal™ AI Edge Carrier Card provides an XPIO 4-POS Dip Switch (**SW5**). The Dip Switches are connected to the XPIO pins of the **JX2** Connector and operated at **+VCCO_703** voltage.

- Manufacturer: CTS Electronic Components
- Part Number: **219-4MSTR**
- SMD DIP 4-POS Switch

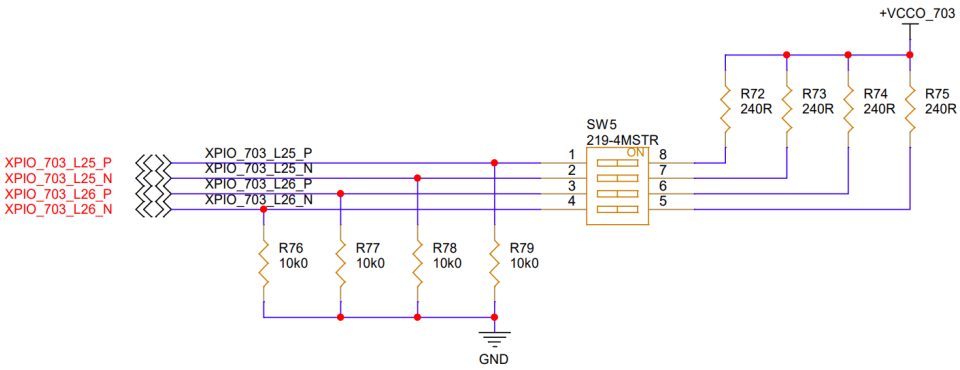

Figure 52 – XPIO Switch Schematic

SW5 Pin Number	I/O Net Name	JX Connector	APSoC Pin Number
1	XPIO_703_L25_P	JX2-D12	E24
2	XPIO_703_L25_N	JX2-D13	F25
3	XPIO_703_L26_P	JX2-C12	D25
4	XPIO_703_L26_N	JX2-C13	D26

Table 44 – XPIO Switch Pin Assignment

5.27 PMBus I2C Interface - SOM

The PMBus implementation on the Versal™ AI Edge Carrier Card connects to the primary voltage regulator, **+UTIL_5V0** (**U35**) and a 4-pin header (**J45**) which allows for a programming dongle from Infineon to mount to the carrier card. This type of solution allows for monitoring of the primary voltage regulator via the PMBus from the VE2302 SOM (with jumpers **J43** and **J44** shunted to provide connectivity). Otherwise, with **J43** and J44 jumpers not shunted, voltage monitoring and PMIC programming can be performed over the **J45** header.

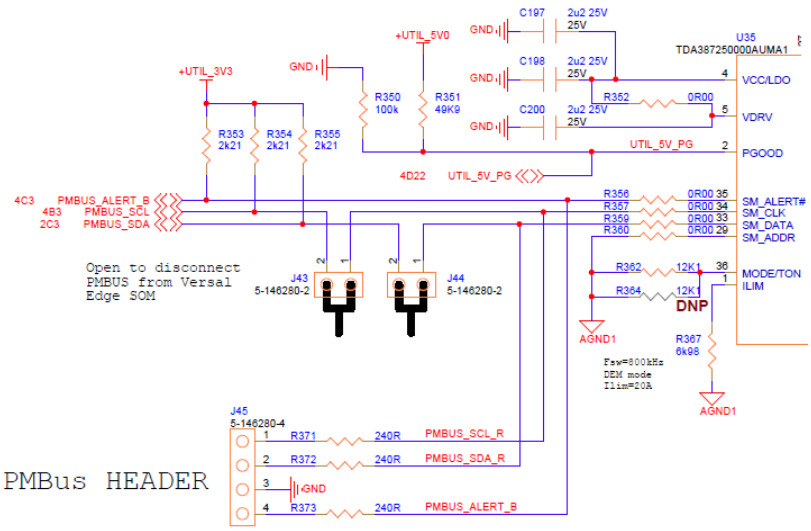

Figure 53 – PMBus I2C Interface

Voltage Regulator (U35) Pin Name	I/O Net Name	JX Connector	APSoC Pin Number
SM_ALERT#	PMBUS_ALERT_B	JX1-A26	PMC_I2C (AA10 / AB10)
SM_CLK	PMBUS_SCL	JX1-C30	PMC_I2C (AA10 / AB10)
SM_DATA	PMBUS_SDA	JX1-B28	PMC_I2C (AA10 / AB10)

Table 45 – PMBus I2C Interface Pin Assignment

The Versal™ AI Edge Carrier Card Power Management ICs (PMIC) can be accessed by attaching to the PMBus header, **J45**. To attach to this interface the customer may use a generic I2C dongle or an Infineon USB005 dongle with the proper Infineon programming software. Please refer to the Infineon website if access to XDP Designer power tool suite is required.

The PMBus Address of the attached Infineon Switching Voltage Regulators **U35** is **0x40**.

NOTE: After the initial programming of the PMBus voltage regulators, the SOM can use the PMBus to control/monitor the PMBus voltage regulator on the Versal™ AI Edge Carrier Card for the purpose of power management and/or measurements.

NOTE: The SCL and SDA signals can be disconnected from the SOM by opening the two Jumpers **J43** and **J44**.

J45 Pin Number	Signal
1	PMBUS_SCL
2	PMBUS_SDA
3	GND
4	PMBUS_ALERT_B

Table 46 – PMBus Header Pin Assignment

5.28 PMBus I2C Interface – Dongle Only

There is a secondary PMBus implementation on the Versal™ AI Edge Carrier Card that connects to the VE2302 SOMs core voltage regulators, **+VCCINT** (**U46** and **U47**) via a 4-pin header (**J55**) which allows for a generic I2C/PMBus programming dongle to mount to the carrier card. This type of solution allows for monitoring/programming of the **+VCCINT** voltage regulator via the PMBus.

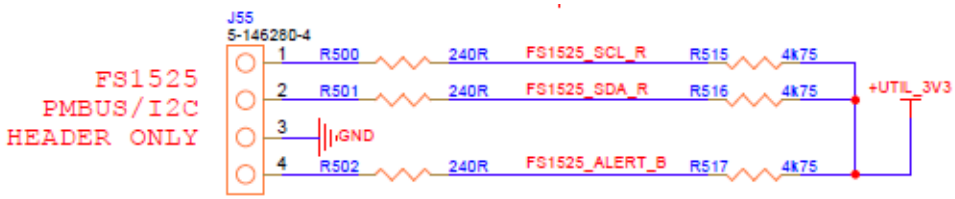

Figure 54 – PMBus I2C Interface – Dongle Only

The Versal™ AI Edge Carrier Card has two power supplies from TDK (**FS1525**) that can be accessed by attaching to the PMBus header, **J55**. To attach to this interface the customer must use a generic I2C/PMBus dongle with generic I2C/PMBus programming/monitoring software.

The PMBus Addresses of the attached TDK FS1525 Voltage Regulators are **U46** at **0x70** and **U47** at **0x71**.

J55 Pin Number	Signal
1	FS1525_SCL
2	FS1525_SDA
3	GND
4	FS1525_ALERT_B

Table 47 – PMBus Header Pin Assignment

5.28.1 Power Regulation

There is a combination of 13 regulators and load switches that reside on the Versal™ AI Edge Carrier Card that provides various voltages in proper sequence such as 0.70V, 0.80V, 0.92V, 1.2V, 1.5V, 1.8V, 3.3V, 5V, and 12V power rails. These voltages are used to power the peripheral devices as well as the VE2302 SOM.

The primary voltage used to power the VE2302 SOM as well as being the source voltage for the other regulators is the **+UTIL_5V0** regulator. This regulator is required to be stable before enabling power to the VE2302 SOM.

- +UTIL_5V0 +5.0V Infineon TDA38725

There are three voltage regulators on the carrier card that are considered utility regulators and used throughout the platform. These regulators are required to be stable before enabling power to the VE2302 SOM.

- +UTIL_3V3 +3.3V Infineon IR3899A
- +UTIL_1V8 +1.8V TDK FS1406
- +UTIL_1V2 +1.2V TDK FS1406

There are five voltages required by the by the VE2302 SOM to support its programmable logic functionality.

- +VCCINT +0.70V TDK FS1525 x 2-devices
- +VCC_RAM +0.80V Diodes Inc AP7361C
- +VCCO_702 +1.20V onsemi NCP45521
- +VCCO_703 +1.20V onsemi NCP45521
- +VCCO_302 Adjustable onsemi NCP45521
  - **J46** shunted 1-2 +1.80V
  - **J46** shunted 2-3 +3.30V

There are three voltages required by the FPGA to power the gigabit transceivers that each implemented with their own regulator.

- +MGTYPAVCC +0.92V TDK FS1406
- +MGTYPAVTT +1.2V TDK FS1406
- +MGTYPVCCAUX +1.5V Diodes Inc AP7361C

There are two additional voltages sent to the JX Connectors.

- +VCC_BATT +1.50V Seiko TS621E-FL11E
- +VCC_FUSE Selectable
  - **J47** shunted 1-2 +1.80V
  - **J47** shunted 2-3 GND

Here are VE2302 SOMs required power rails to be provided by the Versal™ AI Edge Carrier Card and the relative power sequence:

Power Rail Net Name	Voltage	AC Ripple	DC Tolerance	Power Sequence
+VCCO_702	+1.20V	3%	1%	SOM
+VCCO_703	+1.20V	3%	1%	1
+VCCO_302	+VADJ_302	2%	1%	2
+VCCINT	+0.70V	+/-17mV	1%	3
+VCC_RAM	+0.80V	+/-17mV	1%	4
+MGTYPAVCC	+0.92V	3%	1%	5
+MGTYPVCCAUX	+1.50V	3%	1%	6
+MGTYPAVTT	+1.20V	3%	1%	7

Table 48 – Programmable Logic Power Domain Power Supplies

5.28.2 Power Sequencing

The power-up and power-down sequencing of the VE2302 SOM and Versal™ AI Edge Carrier Card follows datasheet recommendations for the AMD Versal™ AI Edge Adaptive SoC device, **DS958**. The power architecture designed on the VE2302 SOM and the Versal™ AI Edge Carrier Card is a good example of a power architecture that follows the datasheet recommendations for power-up and power-down sequencing.

The PMC power domain must be powered first and remain on for all power modes except complete device power-down. During the PMC power domain power-on sequence, the **POR_B** input on the AMD Versal™

AI Edge device is asserted LOW and continues to be asserted for a minimum duration of **POR_B** (10uS) after all the required supplies of the PMC power domain (+**VCCO_500**, +**VCCO_501**, +**VCCO_503**, +**VCC_PMC**, +**VCCAUX_PMC**, and +**VCCAUX_SMON**) have reached minimum operating voltage levels.

After PMC power domain power-on, **POR_B** can de-asserted HIGH to complete the device power-on-reset (POR). If other power domains are powered with the PMC domain and are expected to be functional at initial power-on without additional power management, then the **POR_B** input on the AMD Versal™ AI Edge device is held LOW until all applicable power domain supplies have reached minimum voltage levels.

By design on the Versal™ AI Edge Carrier Card, a second **POR_B** de-assertion point is provided for targeting the end of the power-up sequence is provided. The header that monitors the **+VCCAUX_PMC** power rail can be changed to monitor the **+MGTYPAVTT_SENSE** signal to indicate the last power rail in the sequence is stable so that **POR_B** can be de-asserted HIGH to complete the device power-on-reset (POR).

The VE2302 SOM power sequencing requires several control signals to be utilized to sequence the VE2302 SOM and an end-user carrier card in the most appropriate manner. The signals from the VE2302 SOM that will be used as enable signals to the Versal™ AI Edge Carrier Card are called **VCCO_702_ENB_OUT**, and **SOM_PG_OUT**. The proper end-user carrier card voltage regulators should not be turned ON until the **VCCO_702_ENB_OUT** and **SOM_PG_OUT** signals are asserted. The control signals to the VE2302 SOM that are used are called **SOM_PWR_ENB_IN** and **VCCO_702_PG_IN**.

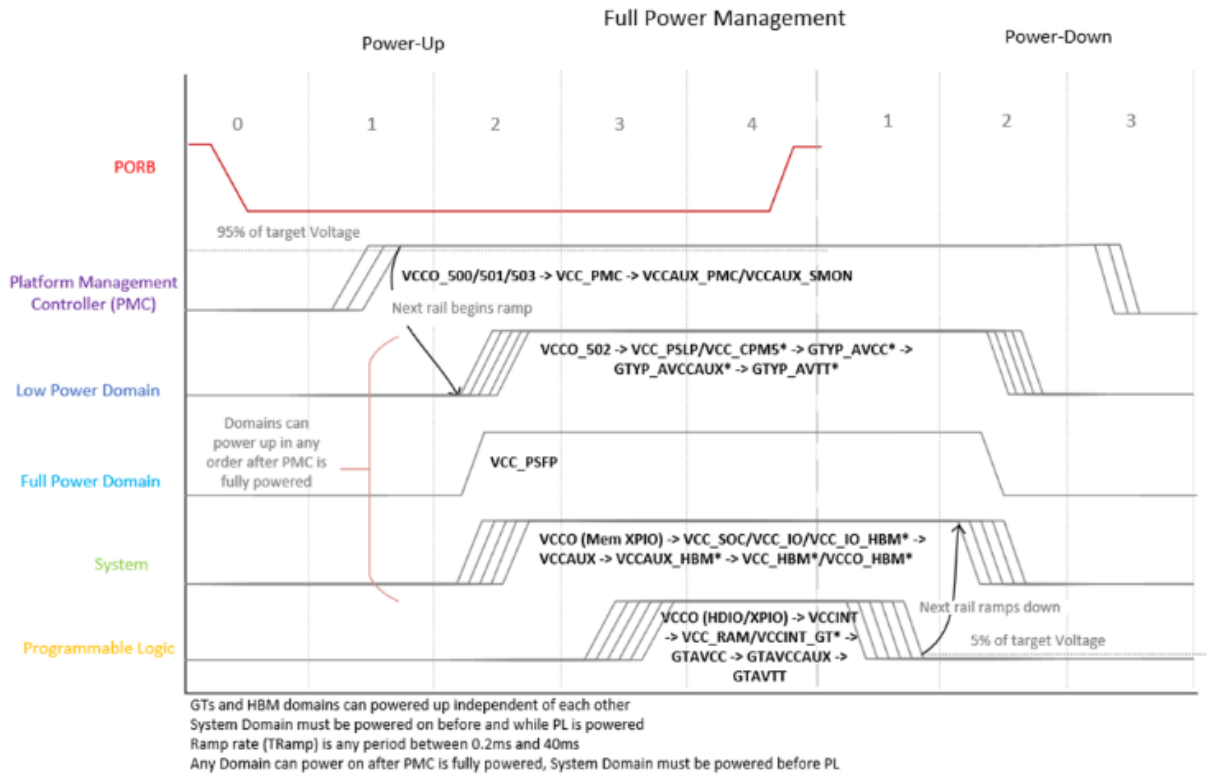

Figure 55 – Versal Power-On Sequence

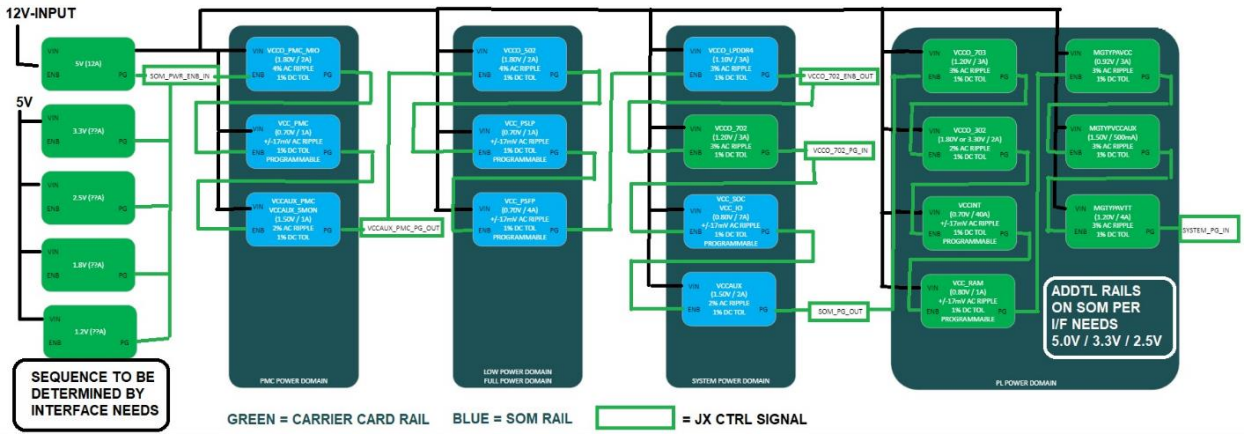

Figure 56 – Power Sequencing with End-User Carrier Card

To control the power sequencing for this power architecture, a custom power sequencer is implemented in a Renesas Greenpak device, base part number **SLG46620V**. The pre-programmed part number utilized is **SLG7A46723V** which is a custom designed power sequencer from Tria Technologies that can control the power-up and power-down sequence of up to 9 power supplies utilizing a single control signal. The power sequencer waits for the **SOM_PG_OUT** from the VE2302 SOM prior to starting the Versal™ AI Edge Carrier Card power-up sequence. If the **SOM_PG_OUT** signal from the VE2302 SOM is de-asserted, the power sequencer will begin bringing down the power supplies in the reverse order.

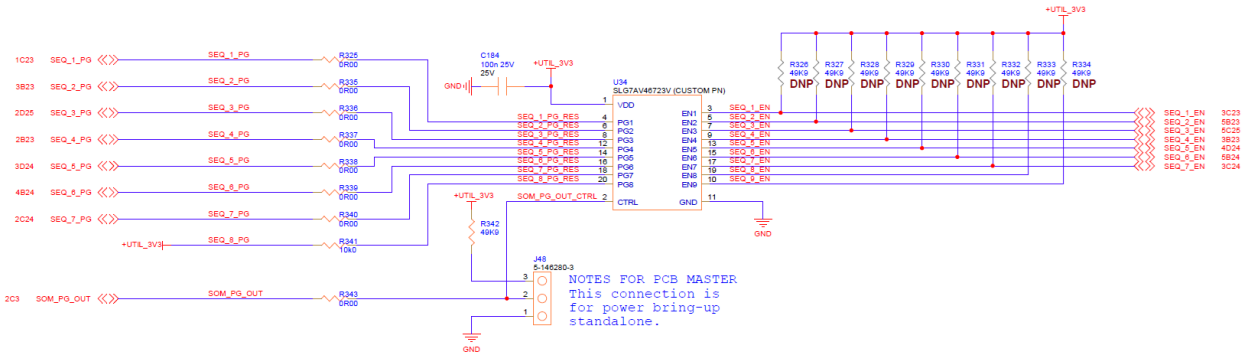

Figure 57 – Custom Power Sequencer Circuit

As you can see from the power sequencing figure above, as the power-up sequence progress, the VE2302 SOM will provide a **+VCCAUX_PMC** signal to the Versal™ AI Edge Carrier Card so it can be used to release the **POR_B** after the PMC power domain has been fully powered.

The VE2302 SOM power sequence progresses until it asserts the **VCCO_702_ENB_OUT** signal to the Versal™ AI Edge Carrier Card. **VCCO_702_ENB_OUT** is the signal from the VE2302 SOM to turn on the **+VCCO_702** rail. When the **+VCCO_702** rail is stable, it is expected that the Versal™ AI Edge Carrier Card will then assert the **VCCO_702_PG_IN** signal to tell the VE2302 SOM to complete its power-up sequence.

Once the VE2302 SOM completes its power-up sequence, it will assert the **SOM_PG_OUT** signal to the Versal™ AI Edge Carrier Card so that it can complete its power-up sequence. A good rule of thumb is to utilize an LED on an end-user carrier card to illuminate when the whole system power is valid.

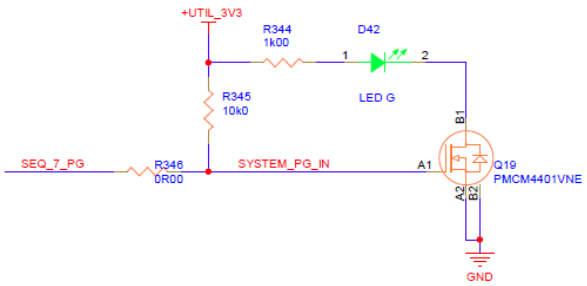

Figure 58 – System Power Good LED

Signal Name	Source	JX1 Pin Number	Description
SOM_PWR_ENB_IN	Carrier	JX2-C32	Power enable signal to SOM after +VIN is stable.
+VCCAUX_PMC	SOM	JX2-A32	Rail for monitoring for early release of POR_B.
VCCO_702_ENB_OUT	SOM	JX2-C8	Bank 702 enable signal to Carrier Card.
VCCO_702_PG_IN	Carrier	JX2-D8	Bank 702 power good signal to SOM.
SOM_PG_OUT	SOM	JX1-B29	SOM power good indicator to carrier card.

Table 49 – Power Sequencing Control Signals

NOTE: The end-user can initiate power on the Versal™ AI Edge Carrier Card in stand-alone mode. To do this without a VE2302 SOM installed, bypass the VE2302 SOM power supplies by closing the header **J48** on pins 2-3. This will simulate the VE2302 **SOM_PG_OUT** signal allowing the power sequencer to turn on the carrier card supplies. Only use this when the **VE2302 SOM is NOT INSTALLED**!

NOTE: By default, jumper **J56** is not shunted and the **+VCCO_702** voltage regulation is controlled by the VE2302 SOM using the **JX** connector control signals. To operate the Versal™ AI Edge Carrier Card in stand-alone mode (**VE2302 NOT INSTALLED**), close header **J56** pins 1-2. This will simulate the VE2302 **VCCO_702_ENB_OUT** signal allowing the **+VCCO_702** power supply to turn on properly.

5.29 Thermal Management

Depending on the end-user application, the performance of the VE2302 SOM will require a thermal solution to help maintain performance across temperature.

For the Versal™ AI Edge Development Kit, a thermal solution consisting of a 50mm heatsink and a fan assembly is utilized. This active arrangement is secured directly to the VE2302 SOM via hardware screws and nuts. An example heat-sink and fan assembly that has been tested is a skived 50mm copper BGA heat sink (**Boyd Laconia, LLC 342943**) and an active 12VDC square Fan **(Sanyo Denki America Inc 109P0512H701)** that are assembled and utilize an on-board fan header on the end-user carrier card that can provide active PWM control of the fan via from the AMD Versal™ AI Edge device.

It is expected that the end-user will be able to monitor the AMD Versal™ AI Edge device temperature via SYSMON and then actively speed up or slow down the fan speed to keep the desired temperature range. Please refer to the **VE2302 SOM Reference Design** webpage for an example design showing how to implement the control algorithm for the active-fan solution.

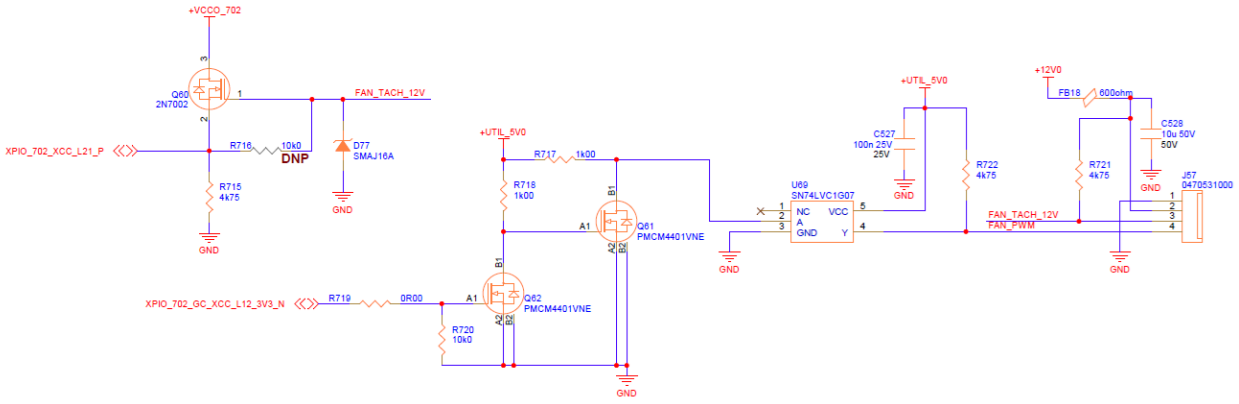

Figure 59 – Fan Control Header

Signal Name	JX1 Pin Number	APSoC Pin Number	Description
XPIO_702_XCC_L21_P	JX2-B36	N21	Fan Tachometer Control Signal
XPIO_702_GC_XCC_L12_N	JX2-C40	T24	Fan PWN Control Signal

Table 50 – Fan Control Signals

Under most circumstances this example 50mm heat-sink and fan assembly should provide adequate relief across temperature, but it cannot be guaranteed to support all environmental conditions due to lack of knowledge regarding end-user's thermal environment and the possible enclosure of the solution. For aggressive applications it is recommended that an accurate worst-case power analysis be performed to avoid the pitfalls of over designing or under designing your product's power and thermal management system.

NOTE: The operating temperature at the system level can be affected by carrier card design component selections, system enclosure, system air flow, etc. End-users should design a thermal management solution that is more conducive to the requirements of their system including alternative mounting techniques for the assembly which could enhance the thermal reliability of the system. It is recommended that necessary thermal system design tasks are completed prior to utilization of the SOM in the end-user application.

(TBD PHOTO)

Figure 60 – Example Heat Sink and Fan Assembly (TBD)

5.30 Recommended Operating Conditions

This section contains the recommended operating conditions for Versal™ AI Edge Carrier Card. Values listed are those available at the time of publication. Users may want to consult the latest device manufacturer's specifications if their application approaches any of the limits.

Parameter	Min	Max	Units	Notes
Operating Temperature	-20	65	C	Slide Switch -30C to 65C HDMI Connector -20C to 85C

Table 51 – Recommended Temperature Range

Parameter	Min	Max	Units	Notes
Input Voltage	11.4	12.6	V	12V 6-pin Power Supply

Table 52 – Recommended Input Voltage

5.30.1 Mechanical

The Versal™ AI Edge Carrier Card is designed to a form factor approximately two cell phones in size. The board measures 152.5mm x 152.5mm (approximately 6.00” x 6.00”).

Several factors can affect the maximum vertical dimension of the board including boards attached to expansion ports such as the HSIO Expansion site, the use of the PC4 JTAG connector, various cable attachments, or a thermal solution attached to the VE2302 SOM. A STEP model / DXF file of the PCB and its components can be made available to end-users that may require it.

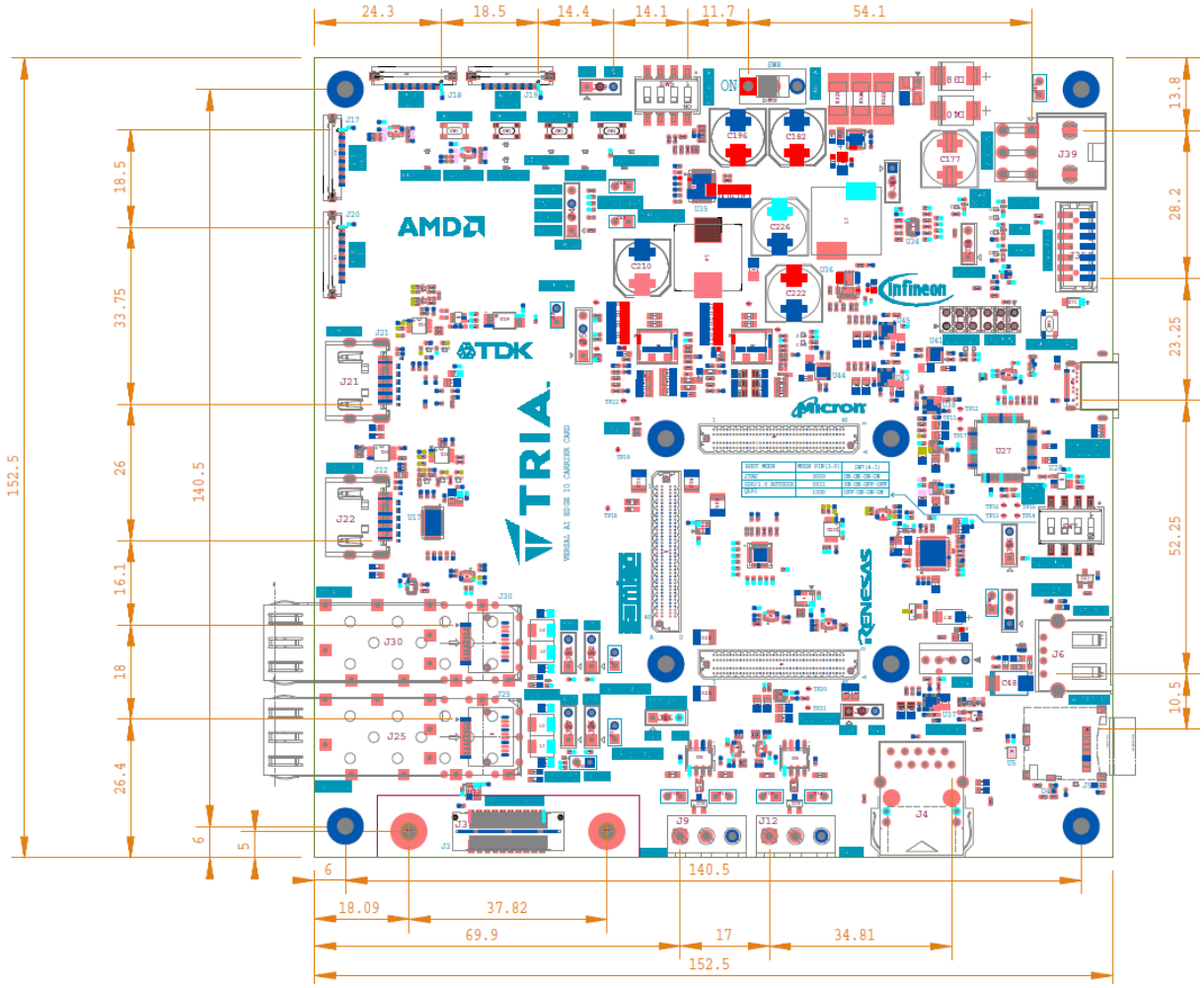

Figure 61 – Mechanical Dimensions

6 Getting Help and Support

If additional support is required, Tria Technologies has many avenues to search depending on your needs.

For general question regarding the Versal™ AI Edge Carrier Card, please visit our website at **http://avnet.me/ve2302-dk**. Here you can find any available documentation, technical specifications, videos and tutorials, reference designs and other support.

For more information regarding the VE2302 SOM, please visit our website at **http://avnet.me/ve2302-som**.

Detailed questions regarding VE2302 SOM hardware design, software application development, using AMD tools, training and other topics can be posted on the VE2302 SOM Support Forum at **http://avnet.me/ve2302-som-forum**. The Tria technical support team monitors the forum during normal business hours in North America.

Those interested in customization options on Versal™ AI Edge Carrier Card can send inquiries to **customize@avnet.com**.

7 General Information

Tria Technologies wants to highlight that the information presented in this user guide is subject to change, particularly due to the ongoing improvements in our product offerings. This document does not serve as a guarantee from Tria Technologies regarding the technical procedures outlined in the user guide or the product characteristics described therein. Tria Technologies holds no responsibility or liability for the use of the mentioned product(s), does not provide any licenses or rights related to patents, copyrights, or mask work rights for these products, and does not claim that these products are free from any infringements, unless explicitly stated. The applications showcased in this user guide are purely for illustrative purposes. Tria Technologies does not state that such applications are inherently suitable for the specified use without further testing or adjustments. It is essential to understand that this user guide offers a general overview of processes and instructions, which may not be universally applicable. If there are any uncertainties, please reach out to Tria Technologies.

https://tria-technologies.com

7.1 Intended Use

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You understand and agree that your use of Tria Technologies devices as a component in High-Risk Applications is entirely at your risk. To minimize the risks associated with your products and applications, you should provide adequate design and operating safeguards. You are solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning your products. You are responsible to ensure that your systems (and any Tria Technologies hardware or software components incorporated in your systems) meet all applicable requirements. Unless otherwise stated in the product documentation, the Tria Technologies device is not provided with error-tolerance capabilities and cannot therefore be deemed as being engineered, manufactured or setup to be compliant for implementation or for resale as device in High-Risk Applications. All application and safety related information in this document (including application descriptions, suggested safety measures, suggested Tria Technologies products, and other materials) is provided for reference only.

Handling and operation of the product is permitted only for trained personnel within a workplace that is access controlled. Follow the “General Safety Instructions” supplied with the product.

This product is not suited for storage or operation in corrosive environments, under exposure to sulfur and chlorine and their compounds. For information on how to harden electronics and mechanics against these stress conditions, contact Tria Technologies’ Support.

7.2 RoHS Compliance

The product is designed by using RoHS compliant components and manufactured on lead free production process to IPC-A-600(*) Class 2 standards.

7.3 Electrostatic Discharge

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, to ensure product integrity at all times.

Do not handle this product out of its protective packaging while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe workstations. Where a safe workstation is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

7.4 Warranty

At the following weblink you will find information regarding warranty, RoHS compliance, and expected lifecycle information regarding these products.

Warranty Terms: **WARRANTY-AND-LIFECYCLE**