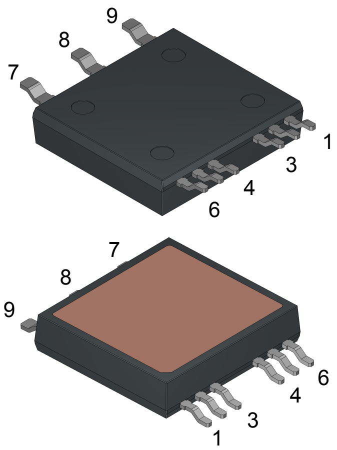
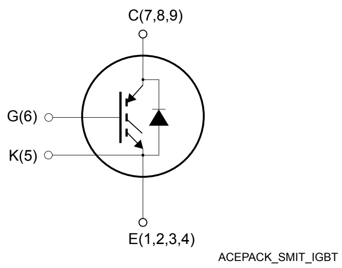
STGSB200M65DF2AG

Datasheet

Automotive-grade trench gate field-stop, 650 V, 200 A, low-loss M series IGBT in an ACEPACK SMIT package



ACEPACK SMIT



Product status link
STGSB200M65DF2AG

Product summary	
Order code	STGSB200M65DF2AG
Marking	GSB200M65DF2AG
Package	ACEPACK SMIT
Packing	Tape and reel

Features

- AEC-Q101 qualified
- 6 µs of minimum short-circuit withstand time
- $V_{CE(sat)}$ = 1.65 V (typ.) @ I_C = 200 A
- Tight parameter distribution
- Positive $V_{CE(sat)}$ temperature coefficient
- Low thermal resistance
- Maximum junction temperature: T_J = 175 °C
- Dice on direct bond copper (DBC) substrate
- Isolation rating of 3400 Vrms/min
- UL recognition: UL 1557 file E81734

Applications

- Traction inverter

Description

This device is an IGBT developed using an advanced proprietary trench gate field-stop structure. The device is part of the M series IGBTs, which represent an optimal balance between inverter system performance and efficiency where the low-loss and the short-circuit functionality is essential. Furthermore, the positive $V_{CE(sat)}$ temperature coefficient and the tight parameter distribution result in safer paralleling operation. Thanks to the DBC substrate, the ACEPACK SMIT surface mounting power package offers a low thermal resistance coupled with a electrical isolated top side thermal pad.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage (V_{GE} = 0 V)	650	V
I_C	Continuous collector current at T_C = 25 °C	216 [1]	A
	Continuous collector current at T_C = 100 °C	200	
I_{CP} [2][3]	Pulsed collector current	700	A
V_{GE}	Gate-emitter voltage	±20	V
	Transient gate-emitter voltage ($t_p \leq$ 10 μs)	±30	
I_F [1]	Continuous forward current at T_C = 25 °C	138	A
	Continuous forward current at T_C = 100 °C	138	
I_{FP} [2][3]	Pulse forward current	700	A
V_{ISO}	Isolation withstand voltage applied between each pin and heat sink plate (AC voltage 50/60 Hz, t = 60 s)	3400	Vrms
P_{TOT}	Total power dissipation at T_C = 25 °C	714	W
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range	-55 to 175	°C

1. *Limited by wires.*
2. *Specified by design, not tested in production.*
3. *Pulse width is limited by maximum junction temperature.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case, IGBT	0.21	°C/W
	Thermal resistance, junction-to-case, diode	0.36	

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 3. Static characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-emitter breakdown voltage	V_{GE} = 0 V, I_C = 1 mA	650			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{GE} = 15 V, I_C = 200 A	1.2	1.65	2.05	V
		V_{GE} = 15 V, I_C = 200 A, T_J = 125 °C		1.9		
		V_{GE} = 15 V, I_C = 200 A, T_J = 175 °C		2.1		
$V_{GE(th)}$	Gate threshold voltage	V_{CE} = V_{GE}, I_C = 1 mA	5	6	7	V
V_F	Forward on-voltage	I_F = 200 A	0.7	1.9	2.65	V
		I_F = 200 A, T_J = 125 °C		1.65		
		I_F = 200 A, T_J = 175 °C		1.55		
I_{CES}	Collector cut-off current	V_{GE} = 0 V, V_{CE} = 650 V			100	µA
I_{GES}	Gate-emitter leakage current	V_{CE} = 0 V, V_{GE} = ±20 V			±600	nA

Table 4. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies}	Input capacitance	V_{CE} = 25 V, f = 1 MHz, V_{GE} = 0 V	-	16	-	nF
C_{oes}	Output capacitance		-	1	-	nF
C_{res}	Reverse transfer capacitance		-	0.3	-	nF
Q_g	Total gate charge	V_{CC} = 520 V, I_C = 200 A, V_{GE} = 0 to 15 V (see Figure 27. Gate charge test circuit)	-	554	-	nC
Q_{ge}	Gate-emitter charge		-	127	-	nC
Q_{gc}	Gate-collector charge		-	229	-	nC

Table 5. Switching characteristics (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{CC} = 400 V, V_{GK} = -8 to 15 V, R_G = 4.7 Ω, I_C = 200 A (see Figure 26. Test circuit for inductive load switching and Figure 28. Switching waveform)		122	-	ns
t_r	Current rise time			54.4	-	ns
E_{on} (1)	Turn-on switching energy			3.82	-	mJ
$t_{d(off)}$	Turn-off delay time			250	-	ns
t_f	Current fall time			76.5	-	ns
E_{off} (2)	Turn-off switching energy			6.97	-	mJ
$t_{d(on)}$	Turn-on delay time	V_{CC} = 400 V, V_{GK} = -8 to 15 V, R_G = 4.7 Ω, I_C = 200 A, T_J = 175 °C (see Figure 26. Test circuit for inductive load switching and Figure 28. Switching waveform)		128	-	ns
t_r	Current rise time			65.6	-	ns
E_{on} (1)	Turn-on switching energy			7.4	-	mJ
$t_{d(off)}$	Turn-off delay time			266	-	ns
t_f	Current fall time			146.6	-	ns
E_{off} (2)	Turn-off switching energy			9.16	-	mJ
tsc	Short circuit withstand time	V_{CC} ≤ 400 V, V_{GE} = 15 V, R_G =4.7 Ω, T_{Jstart} = 150 °C	6		-	µs

1. *Including the reverse recovery of the diode.*
2. *Including the tail of the collector current.*

Table 6. Diode switching characteristics (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{rr}	Reverse recovery time	I_F = 200 A, V_R = 400 V, V_{GE} = -8 to 15 V, R_G =4.7 Ω (see Figure 29. Diode reverse recovery waveform)	-	174.5	-	ns
Q_{rr}	Reverse recovery charge		-	8.6	-	µC
I_{rrm}	Reverse recovery current		-	108.5	-	A
dI_{rr}/dt	Peak rate of fall of reverse recovery current during t_b		-	1503	-	A/µs
E_{rr}	Reverse recovery energy		-	2396	-	µJ
t_{rr}	Reverse recovery time	I_F = 200 A, V_R = 400 V, V_{GE} = -8 to 15 V, R_G =4.7 Ω, T_J = 175 °C (see Figure 29. Diode reverse recovery waveform)	-	264.3	-	ns
Q_{rr}	Reverse recovery charge		-	25.5	-	µC
I_{rrm}	Reverse recovery current		-	192.2	-	A
dI_{rr}/dt	Peak rate of fall of reverse recovery current during t_b		-	1247	-	A/µs
E_{rr}	Reverse recovery energy		-	7117	-	µJ

2.1 Electrical characteristics (curves)

Figure 1. Power dissipation vs case temperature

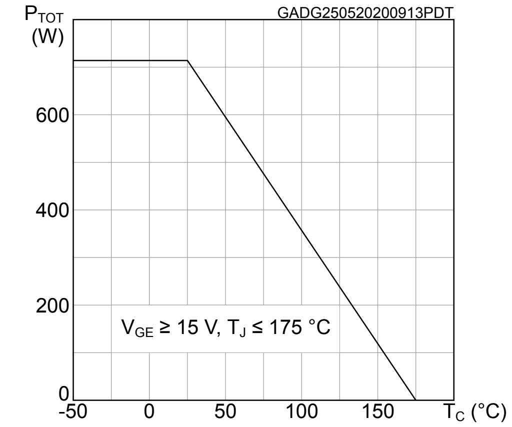


Figure 2. Collector current vs case temperature

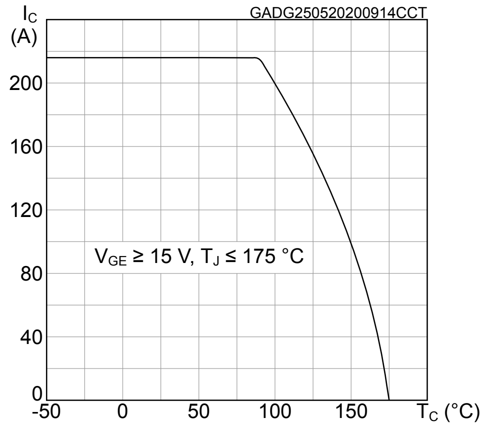


Figure 3. Output characteristics (T_J = 25 °C)

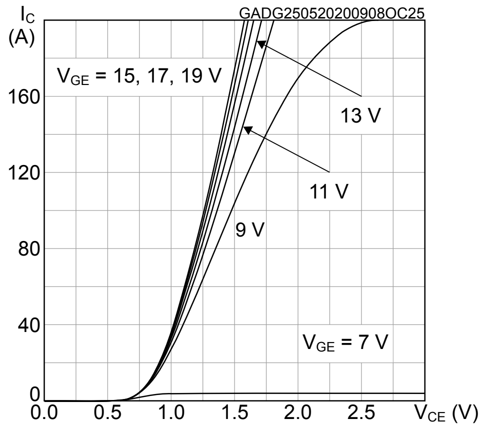


Figure 4. Output characteristics (T_J = 175 °C)

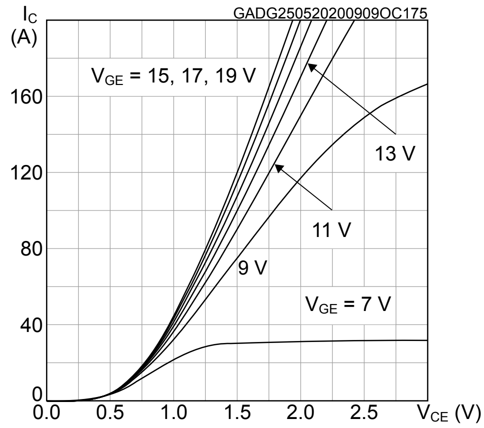


Figure 5. $V_{CE(sat)}$ vs junction temperature

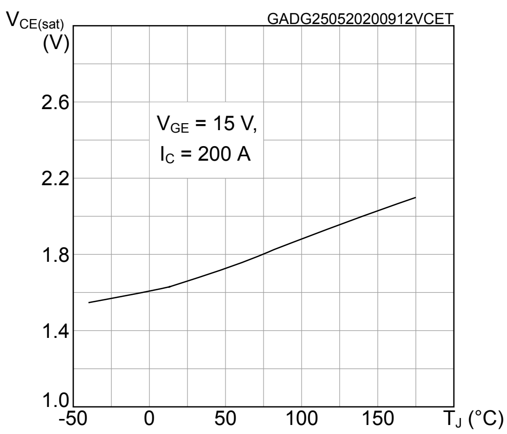


Figure 6. $V_{CE(sat)}$ vs collector current

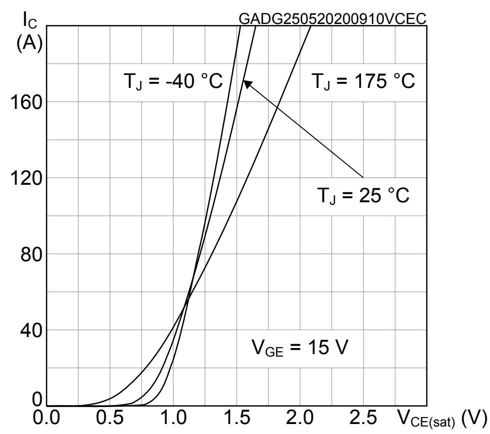


Figure 7. Collector current vs switching frequency

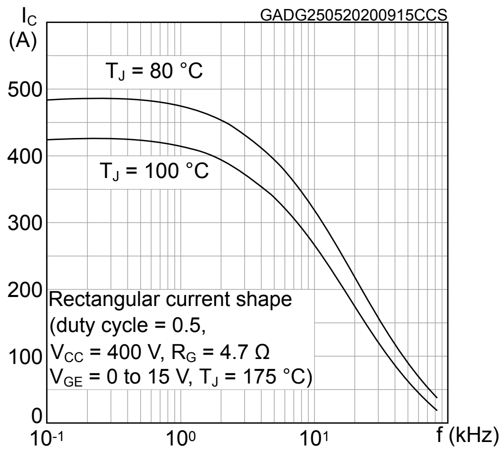


Figure 8. Forward bias safe operating area

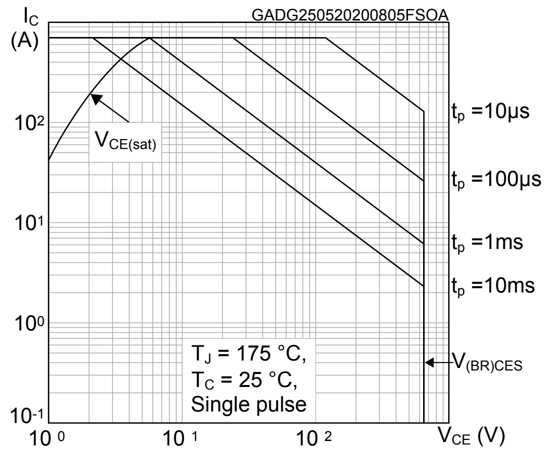


Figure 9. Transfer characteristics

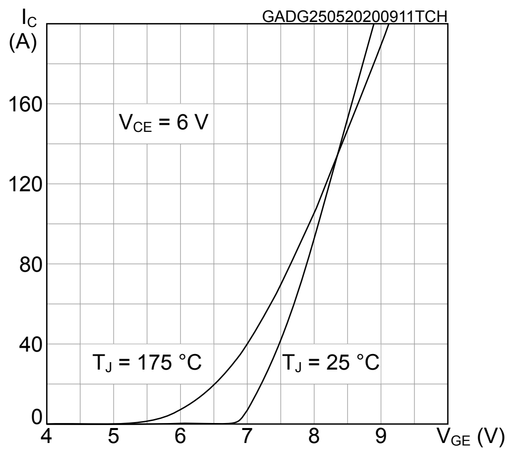


Figure 10. Diode V_F vs forward current

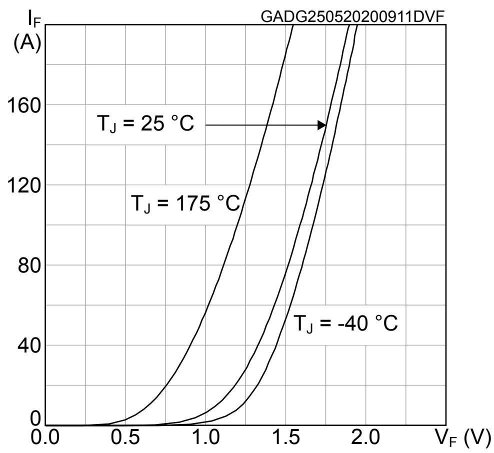


Figure 11. Normalized $V_{GE(th)}$ vs junction temperature

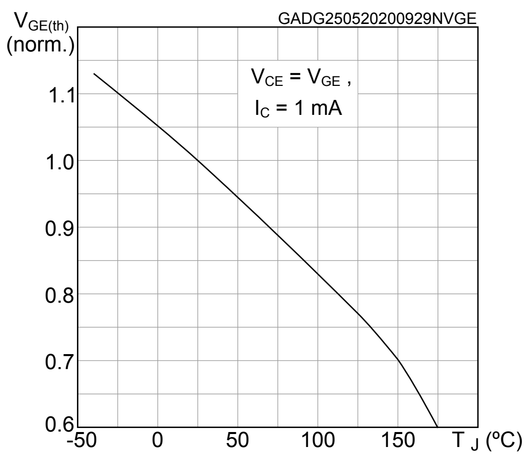


Figure 12. Normalized $V_{(BR)CES}$ vs junction temperature

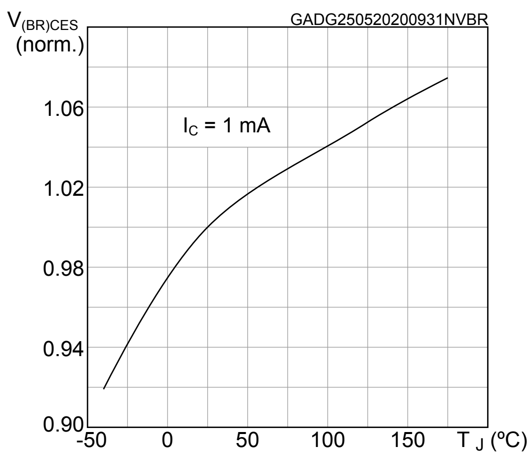


Figure 13. Capacitance variations

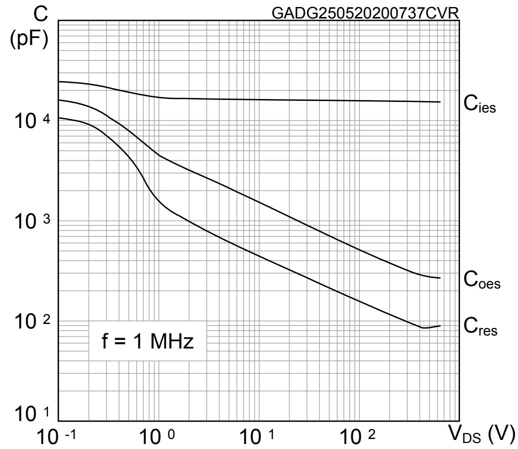


Figure 14. Gate charge vs gate-emitter voltage

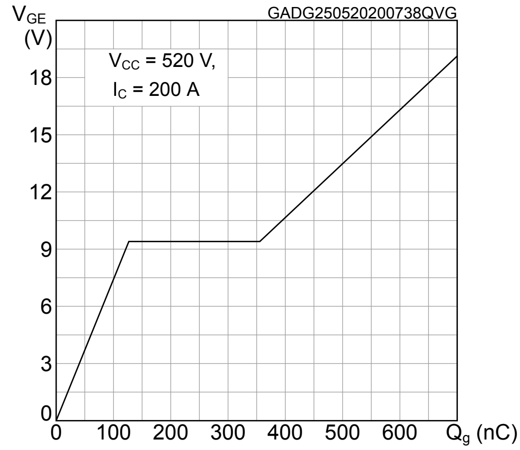


Figure 15. Switching energy vs collector current

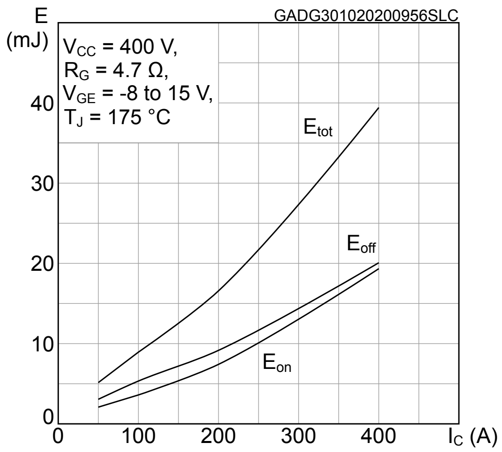


Figure 16. Switching energy vs gate resistance

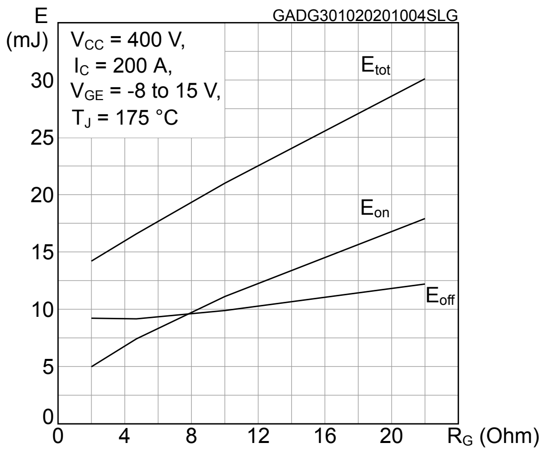


Figure 17. Switching energy vs temperature

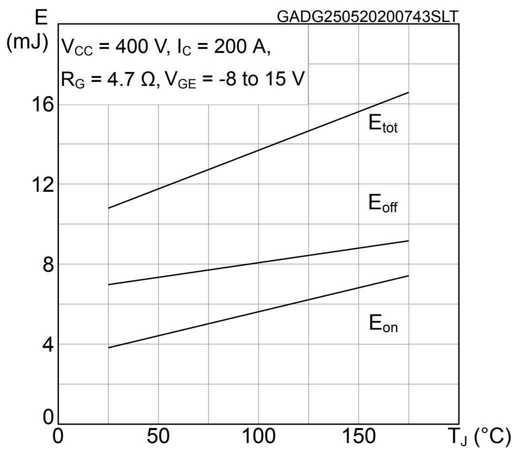


Figure 18. Switching energy vs collector emitter voltage

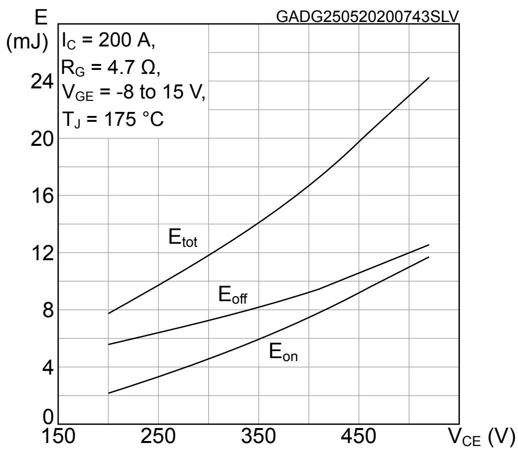


Figure 19. Switching times vs collector current

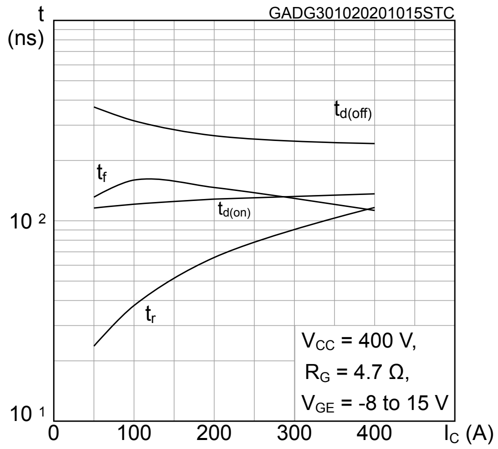


Figure 20. Switching times vs gate resistance

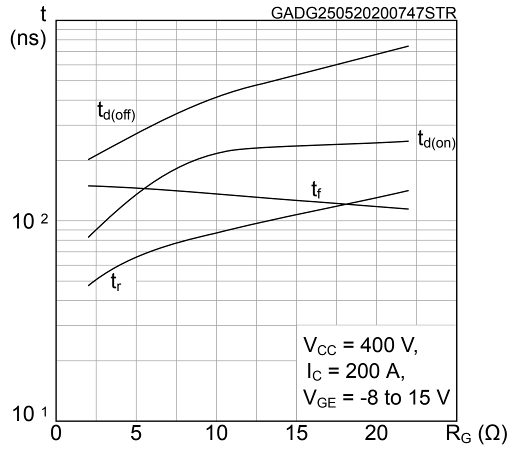


Figure 21. Reverse recovery current vs diode current slope

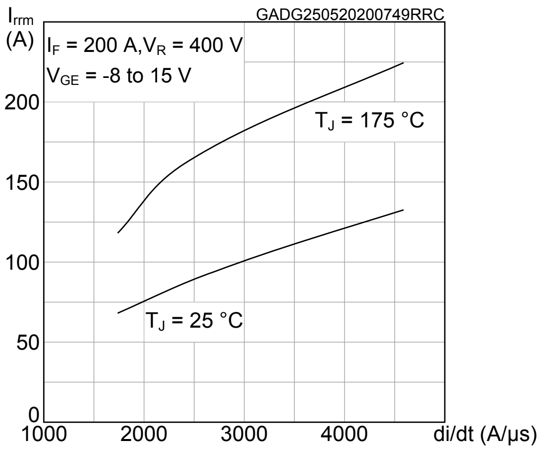


Figure 22. Reverse recovery time vs diode current slope

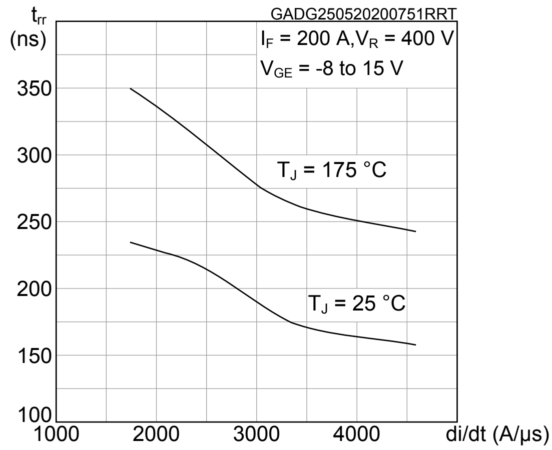


Figure 23. Reverse recovery charge vs diode current slope

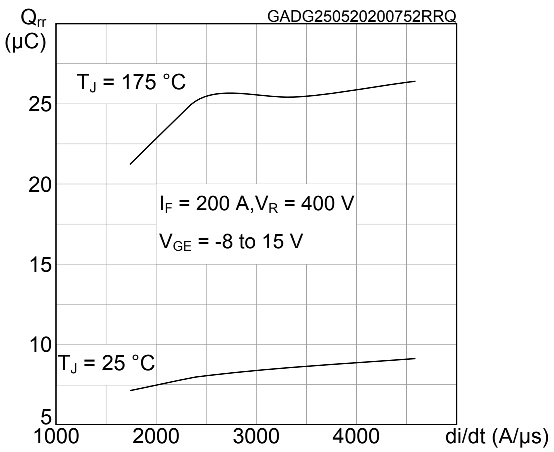


Figure 24. Reverse recovery energy vs diode current slope

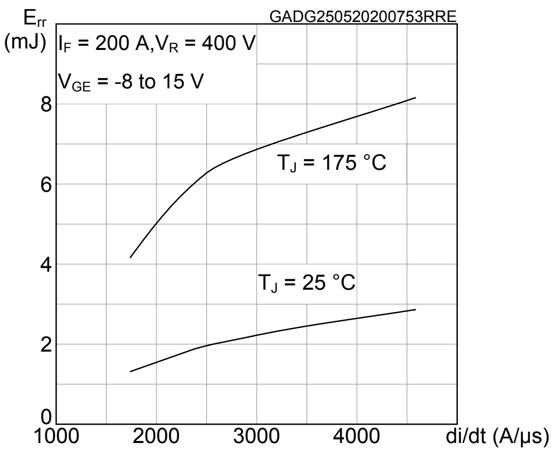
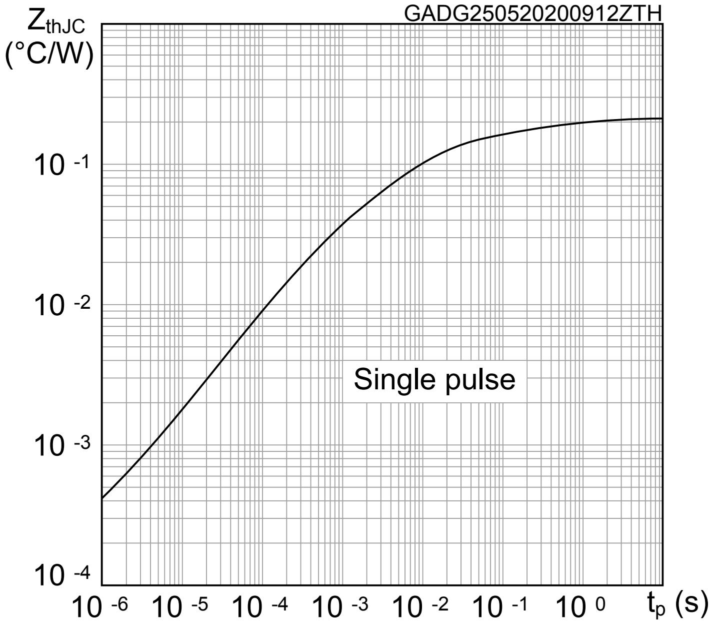


Figure 25. **Maximum transient thermal impedance**



3 Test circuits

Figure 26. Test circuit for inductive load switching

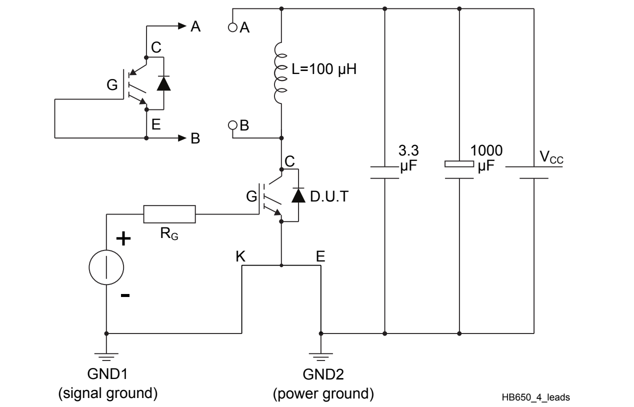


Figure 27. Gate charge test circuit

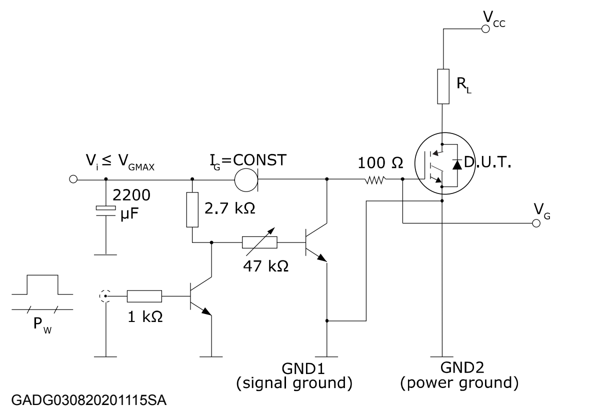


Figure 28. Switching waveform

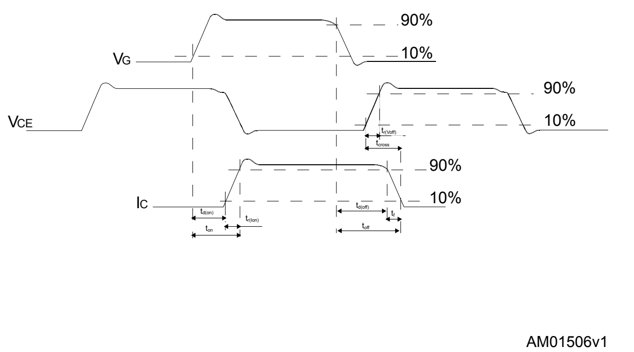
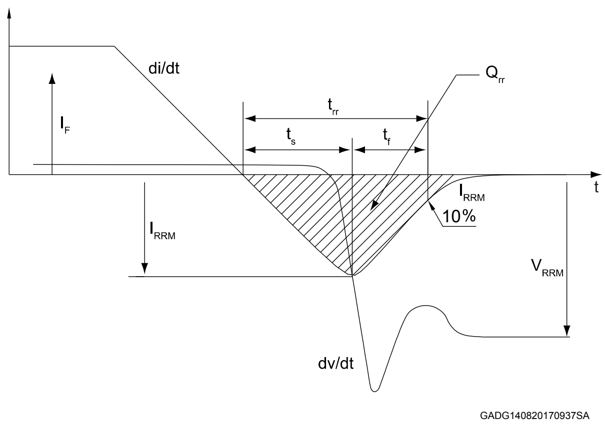


Figure 29. Diode reverse recovery waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 ACEPACK SMIT package information

Figure 30. ACEPACK SMIT package outline

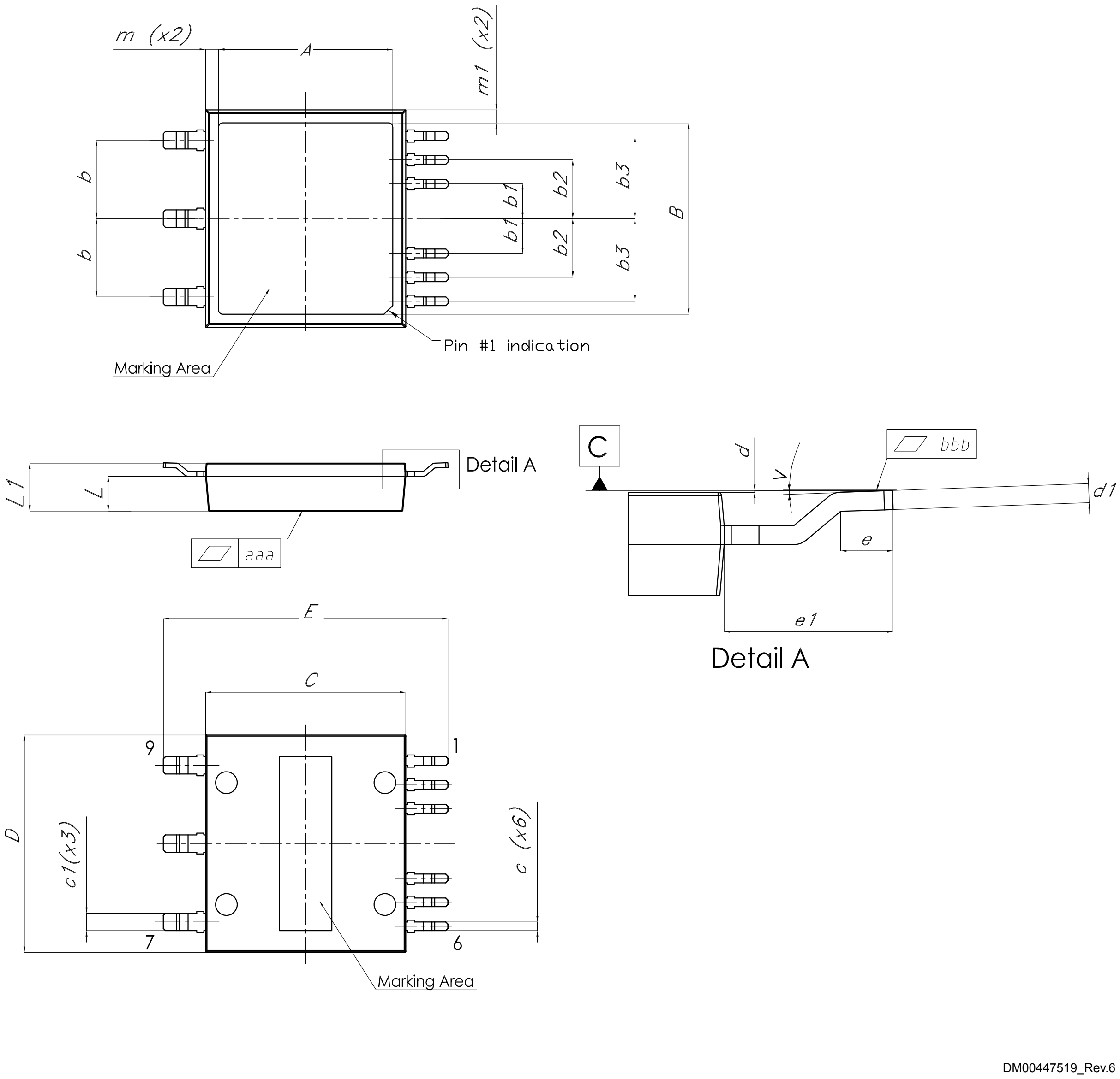
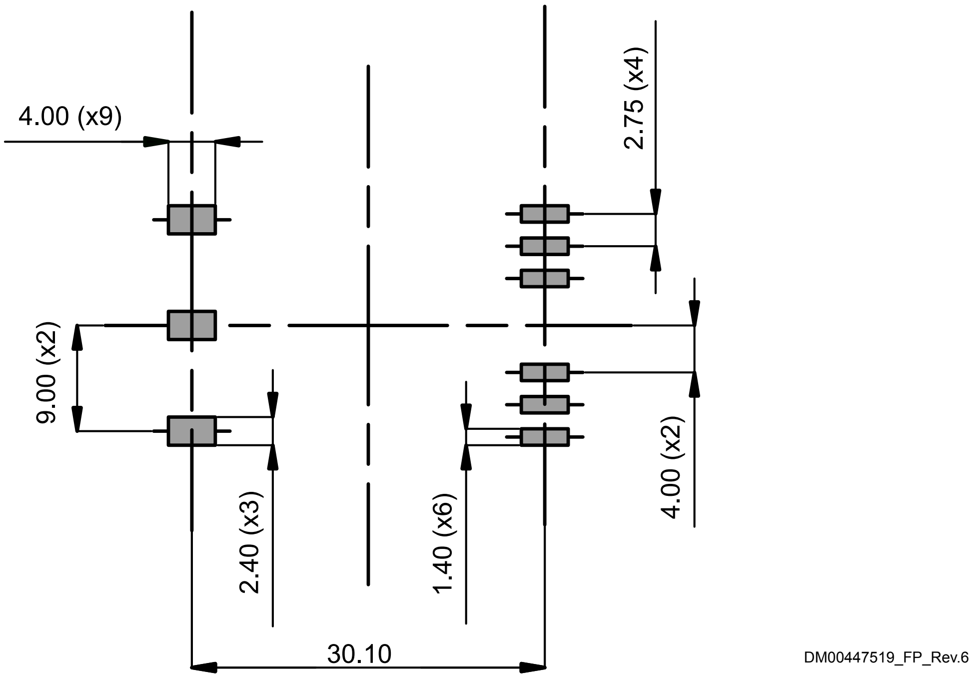


Table 7. ACEPACK SMIT package mechanical data

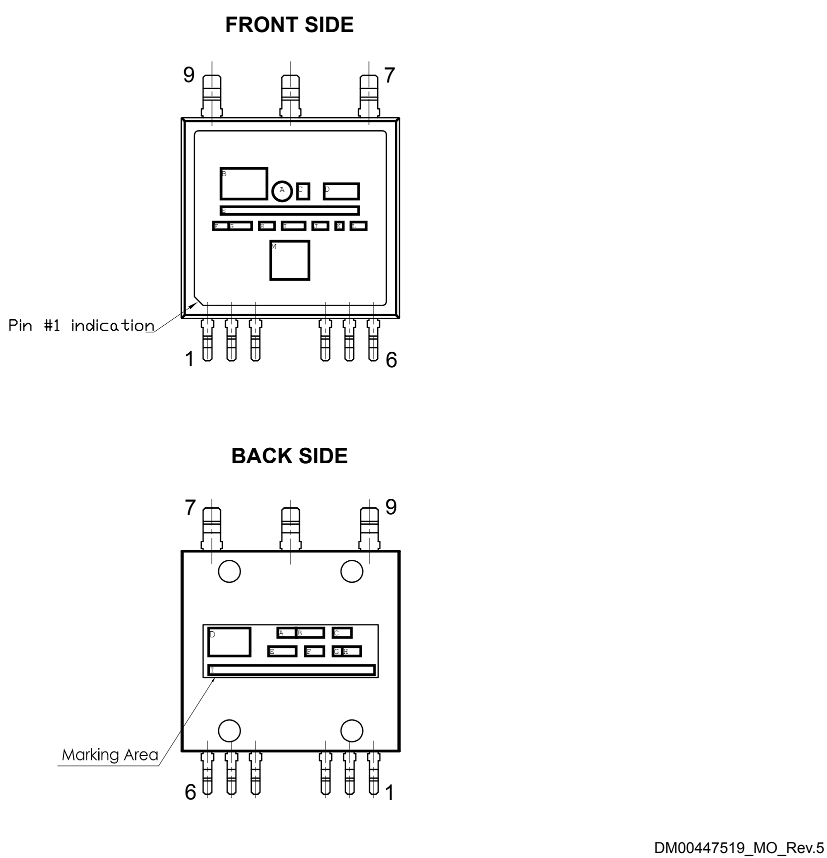
Dim.	mm		
	Min.	Typ.	Max.
A	19.50	20.00	20.50
B	21.50	22.00	22.50
C	22.80	23.00	23.20
D	24.80	25.00	25.20
E	32.20	32.70	33.20
b		9.00	
b1		4.00	
b2		6.75	
b3		9.50	
c	0.95	1.00	1.10
c1	1.95	2.00	2.10
d	0.00		0.15
d1	0.45	0.55	0.65
e	1.30	1.50	1.70
e1	4.65	4.85	5.05
L	3.95	4.00	4.05
L1	5.40	5.50	5.60
m	1.30	1.50	1.80
m1	1.30	1.50	1.80
V	0°	2°	4°
aaa	0.01		0.05
bbb	0.00		0.10

Figure 31. **ACEPACK SMIT recommended footprint**



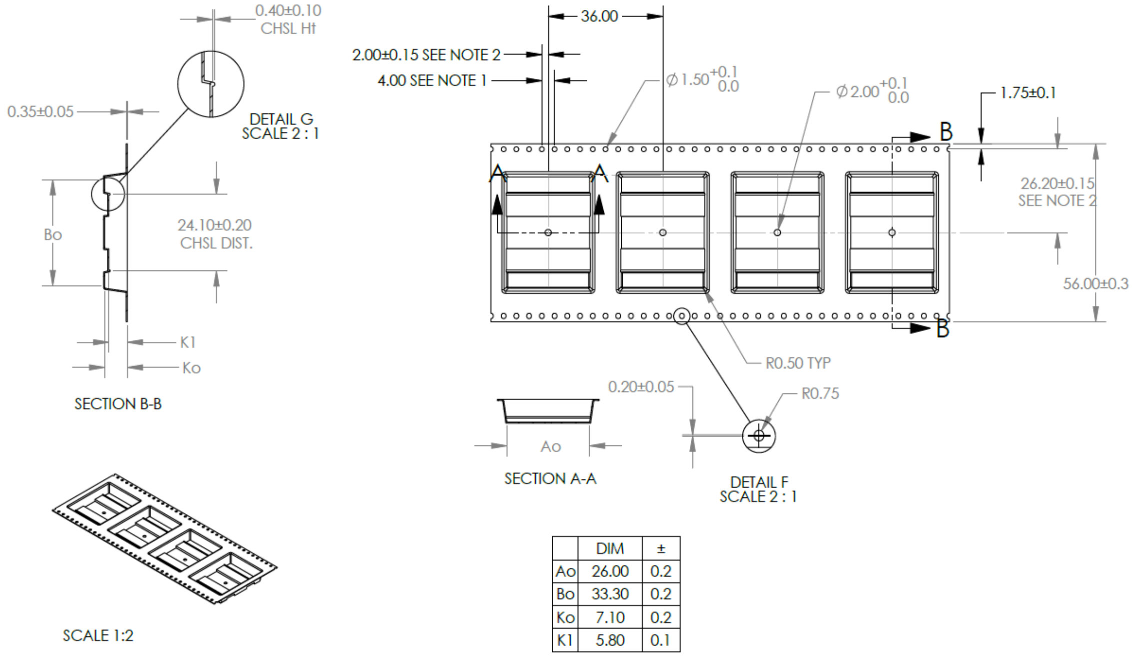
Note: Dimensions in mm.

Figure 32. **ACEPACK SMIT marking orientation vs pinout**



4.2 ACEPACK SMIT packing information

Figure 33. **ACEPACK SMIT tape outline**



	DIM	±
Ao	26.00	0.2
Bo	33.30	0.2
Ko	7.10	0.2
K1	5.80	0.1

NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.
3. Ao AND Bo ARE MEASURED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

DM00631393_Tape_Rev.1

Note: *Dimensions in mm.*

Revision history

Table 8. Document revision history

Date	Revision	Changes
24-Aug-2020	1	First release.
30-Oct-2020	2	Updated package silhouette in cover page. Updated *Absolute maximum ratings*, *Table 2. Thermal data*, *Table 4. Dynamic characteristics* and *Table 5. Switching characteristics (inductive load)*. Updated *Figure 16. Switching energy vs gate resistance* and *Section 3 Test circuits*. Minor text changes.
29-Nov-2021	3	Modified Table 3. Static characteristics and Figure 10. Diode V_F vs forward current. Updated Figure 31. ACEPACK SMIT recommended footprint. Minor text changes.

Contents