

# ARA240COM

## Ara240 Discrete Neural Processing Unit Data Sheet - Commercial

Rev. 3.0 — 3 July 2026

Product data sheet

## 1 Introduction

The Ara240 Discrete NPU (DNPU) delivers industry-leading performance. It offers low latency at low power levels. These capabilities make it suitable for edge applications such as smart retail, surveillance cameras, robots, drones, AR/VR headsets, and driver monitoring.

Ara240 DNPU is a second-generation AI accelerator, which increases performance by more than 5x compared to the first-generation Ara-1. It is ideal for running the latest Generative AI models including Vision-language Models (VLM), Vision-language-action (VLA) models as well as vision transformers and the traditional convolutional neural network (CNN) models for vision applications. It also adds new features such as secure mode of operation with secure boot.

## 2 General description

Ara240 Discrete NPU offers:

- Low power and low latency: The Ara240 Discrete NPU can run multiple Generative AI and traditional vision models at the edge with its proprietary architecture that is optimized for low-latency and power.
- Flexible programming model: AI and frameworks are evolving at a rapid pace. It is important that the underlying silicon architecture that runs the models is flexible enough to accommodate the evolution of AI workloads. The architecture is unique, programmable, and supports the latest AI frameworks, including transformers and Generative AI models.

## 3 Features and benefits

Table 1. Feature summary

| Subsystem             | Feature                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Processors            | <ul style="list-style-type: none"><li>• 8 Neural Network Processor (NNP) Cores</li><li>• 2 Vector Processing Units (VPUs)</li><li>• Management and Control Processor (MCP)<ul style="list-style-type: none"><li>– handles inference requests from the host</li></ul></li><li>• IO Control Processor (IOCP)<ul style="list-style-type: none"><li>– supports host IO interface (USB/PCIe)</li></ul></li><li>• Secure Boot Processor (SBP)</li></ul> |
| Host interfaces       | <ul style="list-style-type: none"><li>• PCIe<ul style="list-style-type: none"><li>– 4-lane Gen 4 Endpoint</li><li>– x1, x2, and x4 modes</li><li>– 16 GT/s per lane</li></ul></li><li>• USB<ul style="list-style-type: none"><li>– 1-lane Endpoint</li><li>– USB 3.2 Gen 1 (5 Gbps)</li><li>– USB 2.0 supported</li><li>– Built-in support for USB Type-C connector</li></ul></li></ul>                                                           |
| Peripheral interfaces | <ul style="list-style-type: none"><li>• GPIO</li><li>• JTAG</li><li>• I2C (Master mode only)</li></ul>                                                                                                                                                                                                                                                                                                                                            |



Table 1. Feature summary...continued

| Subsystem            | Feature                                                                                                                                                                                                                                                                                                                                                                                                |
|----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                      | <ul style="list-style-type: none"><li>• UART</li><li>• SPI</li></ul>                                                                                                                                                                                                                                                                                                                                   |
| Memory               | <ul style="list-style-type: none"><li>• L1 memory</li><li>• Shared on-chip memory</li><li>• External LPDDR4 Memory<ul style="list-style-type: none"><li>– 32-bit/64-bit<ul style="list-style-type: none"><li>– Upto 8 GB density in 32-bit mode</li><li>– Upto 16 GB density in 64-bit mode</li></ul></li><li>– Ara240 supports LPDDR4 with data rates up to 2133 MHz / 4266 MT/s.</li></ul></li></ul> |
| Security             | <ul style="list-style-type: none"><li>• Secure Boot</li><li>• Root-of-Trust Processor</li></ul>                                                                                                                                                                                                                                                                                                        |
| Power                | <ul style="list-style-type: none"><li>• Typical: 6-8W</li><li>• Idle: 2W</li></ul>                                                                                                                                                                                                                                                                                                                     |
| Operating conditions | <ul style="list-style-type: none"><li>• Core Voltage<ul style="list-style-type: none"><li>– 0.8V (Typical)</li></ul></li><li>• Operating Temperature (Junction)<ul style="list-style-type: none"><li>– 0°C to 85°C (Commercial grade)</li></ul></li></ul>                                                                                                                                              |
| Package type         | 17 mm x 17 mm EHS-FCBGA                                                                                                                                                                                                                                                                                                                                                                                |

4 Applications

Generative AI Applications

- Latent Diffusion Models
- Large Language Models
- Vision Language Models
- Vision Language Action Models
- Mixture of Experts (MOE)

Deep Learning Applications

- Vision Transformers
- Facial Detection/Recognition
- Object Localization/Detection/Tracking
- Activity Recognition
- Semantic/Instant Segmentation
- Pose Estimation
- Speech Recognition

Product Categories

- Industrial Automation
- Building & Energy
- In-Cabin & ADAS
- Autonomous Home

5 Ordering information

Table 2. Order part number

| Part Number                      | Features                            | Core frequency |
|----------------------------------|-------------------------------------|----------------|
| ARA-2120AA-CA0T-B <sup>[1]</sup> | Commercial Grade<br>Packaging: Bulk | 900 MHz        |
| ARA-2120AA-CA0T-T                | Commercial grade<br>Packaging: Tray | 900 MHz        |

[1] ARA-2120AA-XA0T-Y (Part Number) – For Commercial part, X = C. For the industrial part, X = I. For Bulk packaging, Y=B. For Tray packaging, Y=T

6 Block diagram

Figure 1 shows the Ara240 block diagram. The sub-blocks are explained in subsequent sections.

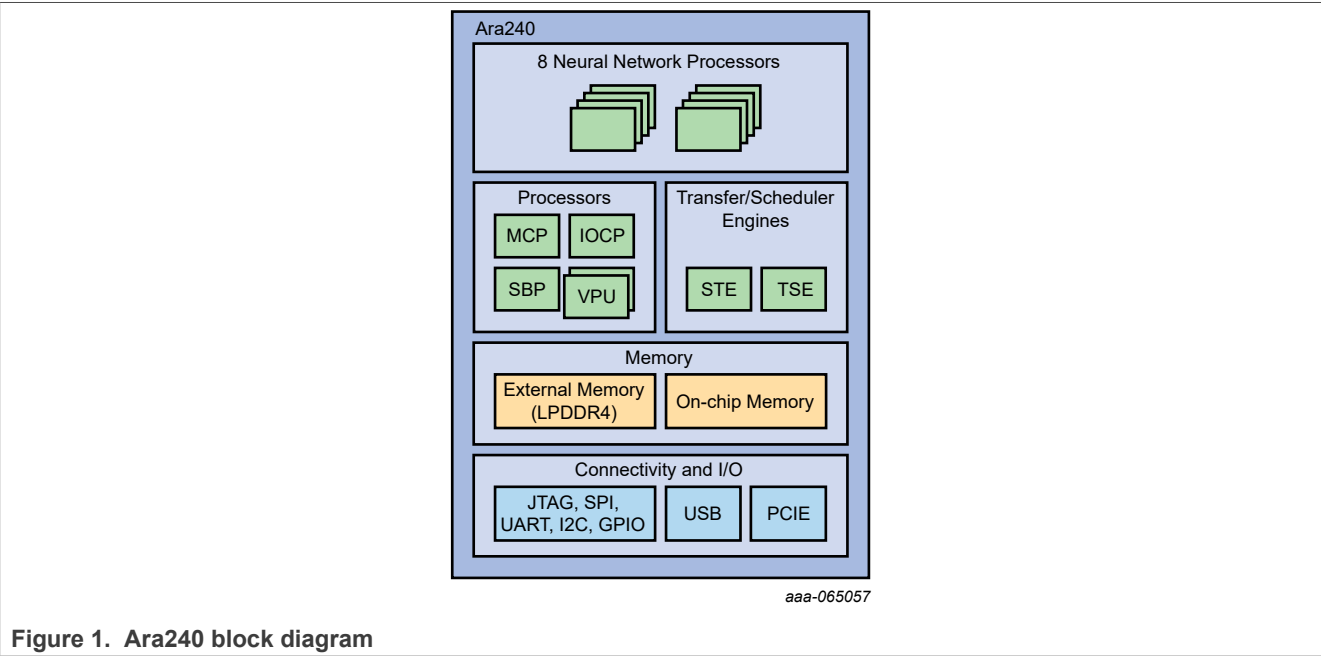


Figure 1. Ara240 block diagram

7 Pinning information

This section describes the device pin layout, ball map, and detailed pin functions for all interfaces.

7.1 Ball map



7.2 Pin description

Table 3. Ara240 Pin Description

| Ball number | Ara240 ball name | Type | Ara240 pin description                                     | Interface |
|-------------|------------------|------|------------------------------------------------------------|-----------|
| A1          | P_RXN0           | IN   | PCIE Lane 0 Differential RX input on the negative terminal | PCle      |
| A2          | VSS              | PWR  | Core Power Ground                                          | Core      |
| A3          | PCIE_REFCLK_N    | IN   | PCle Reference Clock Input Differential Pair (negative)    | PCle      |
| A4          | PCIE_REFCLK_P    | IN   | PCle Reference Clock Input Differential Pair (positive)    | PCle      |
| A5          | SPI_DQS_LB       | IN   | DNU                                                        | DNU       |
| A6          | SPI_DATA1        | I/O  | SPI Data 1                                                 | SPI       |
| A7          | SPI_CLK_N        | OUT  | DNU                                                        | DNU       |
| A8          | SPI_CLK_P        | OUT  | DNU                                                        | IDNU      |
| A9          | GPIO_04          | I/O  | General Purpose Input and Output-04                        | GPIO      |
| A10         | GPIO_13          | I/O  | General Purpose Input and Output-13                        | GPIO      |
| A11         | GPIO_21          | I/O  | General Purpose Input and Output-21                        | GPIO      |
| A12         | VDD_0P8          | PWR  | Fixed 0V8 Power Supply                                     | Core      |
| A13         | VSS              | PWR  | Core Power Ground                                          | Core      |
| A14         | VDD_0P8          | PWR  | Fixed 0V8 Power Supply                                     | Core      |

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Table 3. Ara240 Pin Description...continued

| Ball number | Ara240 ball name | Type | Ara240 pin description                                       | Interface |
|-------------|------------------|------|--------------------------------------------------------------|-----------|
| A15         | VSS              | PWR  | Core Power Ground                                            | Core      |
| A16         | VDD_0P8          | PWR  | Fixed 0V8 Power Supply                                       | Core      |
| A17         | VSS              | PWR  | Core Power Ground                                            | Core      |
| A18         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| A19         | VSS              | PWR  | Core Power Ground                                            | Core      |
| A20         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| A21         | VSS              | PWR  | Core Power Ground                                            | Core      |
| A22         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| A23         | VSS              | PWR  | Core Power Ground                                            | Core      |
| A24         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| A25         | VSS              | PWR  | Core Power Ground                                            | Core      |
| B1          | P_RXP0           | IN   | PCIe Lane 0 Differential RX input on the positive terminal.  | PCIe      |
| B2          | P_TXP0           | OUT  | PCIe Lane 0 Differential TX output on the positive terminal. | PCIe      |
| B3          | SPI_DQS          | I/O  | DNU                                                          | DNU       |
| B4          | SPI_DATA6        | I/O  | DNU                                                          | DNU       |
| B5          | SPI_RST0         | OUT  | DNU                                                          | DNU       |
| B6          | SPI_DATA2        | I/O  | SPI Data 2                                                   | SPI       |
| B7          | SPI_CEn          | OUT  | SPI Chip Select 0 (Active Low) Signal                        | SPI       |
| B8          | SPI_DATA0        | I/O  | SPI Data 0                                                   | SPI       |
| B9          | GPIO_01          | I/O  | General Purpose Input and Output-01                          | GPIO      |
| B10         | GPIO_11          | I/O  | General Purpose Input and Output-11                          | GPIO      |
| B11         | GPIO_22          | I/O  | General Purpose Input and Output-22                          | GPIO      |
| B12         | VSS              | PWR  | Core Power Ground                                            | Core      |
| B13         | VDD_0P8          | PWR  | Fixed 0V8 Power Supply                                       | Core      |
| B14         | VSS              | PWR  | Core Power Ground                                            | Core      |
| B15         | VDD_0P8          | PWR  | Fixed 0V8 Power Supply                                       | Core      |
| B16         | VSS              | PWR  | Core Power Ground                                            | Core      |
| B17         | VDD_0P8          | PWR  | Fixed 0V8 Power Supply                                       | Core      |
| B18         | VSS              | PWR  | Core Power Ground                                            | Core      |
| B19         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| B20         | VSS              | PWR  | Core Power Ground                                            | Core      |
| B21         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| B22         | VSS              | PWR  | Core Power Ground                                            | Core      |
| B23         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| B24         | VSS              | PWR  | Core Power Ground                                            | Core      |
| B25         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| C1          | VSS              | PWR  | Core Power Ground                                            | Core      |
| C2          | P_TXN0           | OUT  | PCIe Lane 0 Differential TX output on the negative terminal. | PCIe      |
| C3          | SPI_REn          | OUT  | DNU                                                          | DNU       |
| C4          | SPI_DATA7        | I/O  | DNU                                                          | DNU       |
| C5          | SPI_WEn          | OUT  | SPI Single Ended Clock Out Signal 1                          | SPI       |
| C6          | SPI_DATA5        | I/O  | DNU                                                          | DNU       |
| C7          | SPI_DATA3        | I/O  | SPI Data 3                                                   | SPI       |
| C8          | SPI_CLK          | OUT  | DNU                                                          | DNU       |
| C9          | GPIO_07          | I/O  | General Purpose Input and Output-07                          | GPIO      |
| C10         | GPIO_10          | I/O  | General Purpose Input and Output-10                          | GPIO      |
| C11         | GPIO_20          | I/O  | General Purpose Input and Output-20                          | GPIO      |
| C12         | VDD_0P8          | PWR  | Fixed 0V8 Power Supply                                       | Core      |
| C13         | VSS              | PWR  | Core Power Ground                                            | Core      |
| C14         | VDD_0P8          | PWR  | Fixed 0V8 Power Supply                                       | Core      |
| C15         | VSS              | PWR  | Core Power Ground                                            | Core      |

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Table 3. Ara240 Pin Description...continued

| Ball number | Ara240 ball name | Type | Ara240 pin description                                       | Interface |
|-------------|------------------|------|--------------------------------------------------------------|-----------|
| C16         | VDD_0P8          | PWR  | Fixed 0V8 Power Supply                                       | Core      |
| C17         | VSS              | PWR  | Core Power Ground                                            | Core      |
| C18         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| C19         | VSS              | PWR  | Core Power Ground                                            | Core      |
| C20         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| C21         | VSS              | PWR  | Core Power Ground                                            | Core      |
| C22         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| C23         | VSS              | PWR  | Core Power Ground                                            | Core      |
| C24         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| C25         | VSS              | PWR  | Core Power Ground                                            | Core      |
| D1          | P_RXN1           | IN   | PCIe Lane 1 Differential RX input on the negative terminal   | PCIe      |
| D2          | VSS              | PWR  | Core Power Ground                                            | Core      |
| D3          | STRAP0           | IN   | NNP-ID-0 Strap Input Signal                                  | Strap     |
| D4          | DDR_DISABLE      | IN   | DDR Interface Disable Signal (Active High)                   | Strap     |
| D5          | SCAN_EN          | IN   | Scan Mode Enable Signal (Active Low)                         | Strap     |
| D6          | XSPI_DATA4       | I/O  | DNU                                                          | DNU       |
| D7          | TESTCLK          | IN   | Test Mode Clock Input Signal                                 | System    |
| D8          | GPIO_09          | I/O  | General Purpose Input and Output-09                          | GPIO      |
| D9          | GPIO_03          | I/O  | General Purpose Input and Output-03                          | GPIO      |
| D10         | GPIO_05          | I/O  | General Purpose Input and Output-05                          | GPIO      |
| D11         | GPIO_17          | I/O  | General Purpose Input and Output-17                          | GPIO      |
| D12         | VSS              | PWR  | Core Power Ground                                            | Core      |
| D13         | VDD_0P8          | PWR  | Fixed 0V8 Power Supply                                       | Core      |
| D14         | VSS              | PWR  | Core Power Ground                                            | Core      |
| D15         | VDD_0P8          | PWR  | Fixed 0V8 Power Supply                                       | Core      |
| D16         | VSS              | PWR  | Core Power Ground                                            | Core      |
| D17         | VDD_0P8          | PWR  | Fixed 0V8 Power Supply                                       | Core      |
| D18         | VSS              | PWR  | Core Power Ground                                            | Core      |
| D19         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| D20         | VSS              | PWR  | Core Power Ground                                            | Core      |
| D21         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| D22         | VSS              | PWR  | Core Power Ground                                            | Core      |
| D23         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| D24         | VSS              | PWR  | Core Power Ground                                            | Core      |
| D25         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| E1          | P_RXP1           | IN   | PCIe Lane 1 Differential RX input on the positive terminal.  | PCIe      |
| E2          | P_TXP1           | OUT  | PCIe Lane 1 Differential TX output on the positive terminal. | PCIe      |
| E3          | STRAP1           | IN   | NNP-ID-1 Strap Input Signal                                  | Strap     |
| E4          | PCIE_DISABLE     | IN   | PCIE Interface Disable Signal (Active High)                  | Strap     |
| E5          | TME0             | IN   | Test Mode Enable 0                                           | Strap     |
| E6          | JTAG_SEL         | IN   | JTAG Interface Enable Signal (Active High)                   | Strap     |
| E7          | JTAG_TCK         | IN   | JTAG Test Clock Input                                        | JTAG      |
| E8          | GPIO_15          | I/O  | General Purpose Input and Output-15                          | GPIO      |
| E9          | GPIO_06          | I/O  | General Purpose Input and Output-06                          | GPIO      |
| E10         | GPIO_08          | I/O  | General Purpose Input and Output-08                          | GPIO      |
| E11         | GPIO_19          | I/O  | General Purpose Input and Output-19                          | GPIO      |
| E12         | VDD_0P8          | PWR  | Fixed 0V8 Power Supply                                       | Core      |
| E13         | VSS              | PWR  | Core Power Ground                                            | Core      |
| E14         | VDD_0P8          | PWR  | Fixed 0V8 Power Supply                                       | Core      |
| E15         | VSS              | PWR  | Core Power Ground                                            | Core      |
| E16         | VDD_0P8          | PWR  | Fixed 0V8 Power Supply                                       | Core      |

## Ara240 Discrete Neural Processing Unit Data Sheet - Commercial

Table 3. Ara240 Pin Description...continued

| Ball number | Ara240 ball name | Type | Ara240 pin description                                       | Interface |
|-------------|------------------|------|--------------------------------------------------------------|-----------|
| E17         | VSS              | PWR  | Core Power Ground                                            | Core      |
| E18         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| E19         | VSS              | PWR  | Core Power Ground                                            | Core      |
| E20         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| E21         | VSS              | PWR  | Core Power Ground                                            | Core      |
| E22         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| E23         | VSS              | PWR  | Core Power Ground                                            | Core      |
| E24         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| E25         | VSS              | PWR  | Core Power Ground                                            | Core      |
| F1          | VSS              | PWR  | Core Power Ground                                            | Core      |
| F2          | P_TXN1           | OUT  | PCIe Lane 1 Differential TX output on the negative terminal. | PCIe      |
| F3          | CLK_SEL          | IN   | Clock Selection Signal                                       | Strap     |
| F4          | STRAP3           | IN   | NNP-ID-3 Strap Input Signal                                  | Strap     |
| F5          | STRAP2           | IN   | NNP-ID-2 Strap Input Signal                                  | Strap     |
| F6          | STRAP4           | IN   | Strap Input Signal 4                                         | Strap     |
| F7          | JTAG_TDI         | IN   | JTAG Test Data In                                            | JTAG      |
| F8          | JTAG_TMS         | IN   | JTAG Test Mode Select                                        | JTAG      |
| F9          | GPIO_12          | I/O  | General Purpose Input and Output-12                          | GPIO      |
| F10         | GPIO_02          | I/O  | General Purpose Input and Output-02                          | GPIO      |
| F11         | GPIO_16          | I/O  | General Purpose Input and Output-16                          | GPIO      |
| F12         | VSS              | PWR  | Core Power Ground                                            | Core      |
| F13         | VDD_0P8          | PWR  | Fixed 0V8 Power Supply                                       | Core      |
| F14         | VSS              | PWR  | Core Power Ground                                            | Core      |
| F15         | VDD_0P8          | PWR  | Fixed 0V8 Power Supply                                       | Core      |
| F16         | VSS              | PWR  | Core Power Ground                                            | Core      |
| F17         | VDD_0P8          | PWR  | Fixed 0V8 Power Supply                                       | Core      |
| F18         | VSS              | PWR  | Core Power Ground                                            | Core      |
| F19         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| F20         | VSS              | PWR  | Core Power Ground                                            | Core      |
| F21         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| F22         | VSS              | PWR  | Core Power Ground                                            | Core      |
| F23         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| F24         | VSS              | PWR  | Core Power Ground                                            | Core      |
| F25         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| G1          | P_RXN2           | IN   | PCIe Lane 2 Differential RX input on the negative terminal   | PCIe      |
| G2          | VSS              | PWR  | Core Power Ground                                            | Core      |
| G3          | O_CLKOUT         | OUT  | System Clock Out                                             | System    |
| G4          | USB_DISABLE      | IN   | USB Interface Disable Signal (Active High)                   | Strap     |
| G5          | TME1             | IN   | Test Mode Enable 1                                           | Strap     |
| G6          | RESET_N          | IN   | Chip Reset (Active Low)                                      | System    |
| G7          | JTAG_TRST        | IN   | JTAG Test Reset                                              | JTAG      |
| G8          | JTAG_TDO         | OUT  | JTAG Test Data Out                                           | JTAG      |
| G9          | GPIO_18          | I/O  | General Purpose Input and Output-18                          | GPIO      |
| G10         | GPIO_00          | I/O  | General Purpose Input and Output-00                          | GPIO      |
| G11         | GPIO_14          | I/O  | General Purpose Input and Output-14                          | GPIO      |
| G12         | VDD_0P8          | PWR  | Fixed 0V8 Power Supply                                       | Core      |
| G13         | VSS              | PWR  | Core Power Ground                                            | Core      |
| G14         | VDD_0P8          | PWR  | Fixed 0V8 Power Supply                                       | Core      |
| G15         | VSS              | PWR  | Core Power Ground                                            | Core      |
| G16         | VDD_0P8          | PWR  | Fixed 0V8 Power Supply                                       | Core      |
| G17         | VSS              | PWR  | Core Power Ground                                            | Core      |

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Table 3. Ara240 Pin Description...continued

| Ball number | Ara240 ball name | Type | Ara240 pin description                                          | Interface |
|-------------|------------------|------|-----------------------------------------------------------------|-----------|
| G18         | VDD_CORE         | PWR  | Core Power Supply                                               | Core      |
| G19         | VSS              | PWR  | Core Power Ground                                               | Core      |
| G20         | VDD_CORE         | PWR  | Core Power Supply                                               | Core      |
| G21         | VSS              | PWR  | Core Power Ground                                               | Core      |
| G22         | VDD_CORE         | PWR  | Core Power Supply                                               | Core      |
| G23         | VSS              | PWR  | Core Power Ground                                               | Core      |
| G24         | VDD_CORE         | PWR  | Core Power Supply                                               | Core      |
| G25         | VSS              | PWR  | Core Power Ground                                               | Core      |
| H1          | P_RXP2           | IN   | PCIe Lane 2 Differential RX input on the positive terminal.     | PCIe      |
| H2          | P_TXP2           | OUT  | PCIe Lane 2 Differential TX output on the positive terminal.    | PCIe      |
| H3          | VCC12A_PCIE_RX   | PWR  | PCIe PHY RX 1.2V Analog Power Supply                            | PCIe      |
| H4          | VCC12A_PCIE_CMN  | PWR  | PCIe PHY CMN 1.2V Analog Power Supply                           | PCIe      |
| H5          | VCC12A_PCIE_RX   | PWR  | PCIe PHY RX 1.2V Analog Power Supply                            | PCIe      |
| H6          | VSS              | PWR  | Core Power Ground                                               | Core      |
| H7          | VCC12A_PCIE_TX   | PWR  | PCIe PHY TX 1.2V Analog Power Supply                            | PCIe      |
| H8          | VCC12A_PCIE_CMN  | PWR  | PCIe PHY CMN 1.2V Analog Power Supply                           | PCIe      |
| H9          | VCC12A_PCIE_TX   | PWR  | PCIe PHY TX 1.2V Analog Power Supply                            | PCIe      |
| H10         | VSS              | PWR  | Core Power Ground                                               | Core      |
| H11         | VQPS18_FUSE_CPC  | PWR  | CPC Fuse Burn Power Supply                                      | Fuse      |
| H12         | VSS              | PWR  | Core Power Ground                                               | Core      |
| H13         | VDD_0P8          | PWR  | Fixed 0V8 Power Supply                                          | Core      |
| H14         | VSS              | PWR  | Core Power Ground                                               | Core      |
| H15         | VDD_0P8          | PWR  | Fixed 0V8 Power Supply                                          | Core      |
| H16         | VSS              | PWR  | Core Power Ground                                               | Core      |
| H17         | VDD_0P8          | PWR  | Fixed 0V8 Power Supply                                          | Core      |
| H18         | VSS              | PWR  | Core Power Ground                                               | Core      |
| H19         | VDD_CORE         | PWR  | Core Power Supply                                               | Core      |
| H20         | VSS              | PWR  | Core Power Ground                                               | Core      |
| H21         | VDD_CORE         | PWR  | Core Power Supply                                               | Core      |
| H22         | VSS              | PWR  | Core Power Ground                                               | Core      |
| H23         | VDD_CORE         | PWR  | Core Power Supply                                               | Core      |
| H24         | VSS              | PWR  | Core Power Ground                                               | Core      |
| H25         | VDD_CORE         | PWR  | Core Power Supply                                               | Core      |
| J1          | VSS              | PWR  | Core Power Ground                                               | Core      |
| J2          | P_TXN2           | OUT  | PCIe Lane 2 Differential TX output on the negative terminal.    | PCIe      |
| J3          | XTAL_OUT         | OUT  | Crystal oscillator output (leave open or pull up when not used) | Clock     |
| J4          | VCC18A_PCIE      | PWR  | PCIe PHY 1.8V Analog Power Supply                               | PCIe      |
| J5          | VSS              | PWR  | Core Power Ground                                               | Core      |
| J6          | VDD33A_USBPHY    | PWR  | USB PHY 3.3V Analog Power Supply                                | USB       |
| J7          | GND18A_USB       | PWR  | USB PHY Analog Power Ground                                     | USB       |
| J8          | VDD08_PCIE       | PWR  | PCIe 0.8V Digital Power Supply                                  | PCIe      |
| J9          | VSS              | PWR  | Core Power Ground                                               | Core      |
| J10         | VDD08_PCIE       | PWR  | PCIe 0.8V Digital Power Supply                                  | PCIe      |
| J11         | VSS              | PWR  | Core Power Ground                                               | Core      |
| J12         | VDDIO            | PWR  | I/O Power Supply                                                | GPIO      |
| J13         | VSS              | PWR  | Core Power Ground                                               | Core      |
| J14         | VDDIO            | PWR  | I/O Power Supply                                                | GPIO      |
| J15         | VSS              | PWR  | Core Power Ground                                               | Core      |
| J16         | VDD_CORE         | PWR  | Core Power Supply                                               | Core      |
| J17         | VSS              | PWR  | Core Power Ground                                               | Core      |
| J18         | VDD_CORE         | PWR  | Core Power Supply                                               | Core      |



## Ara240 Discrete Neural Processing Unit Data Sheet - Commercial

Table 3. Ara240 Pin Description...continued

| Ball number | Ara240 ball name | Type | Ara240 pin description                                       | Interface |
|-------------|------------------|------|--------------------------------------------------------------|-----------|
| J19         | VSS              | PWR  | Core Power Ground                                            | Core      |
| J20         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| J21         | VSS              | PWR  | Core Power Ground                                            | Core      |
| J22         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| J23         | VSS              | PWR  | Core Power Ground                                            | Core      |
| J24         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| J25         | VSS              | PWR  | Core Power Ground                                            | Core      |
| K1          | P_RXN3           | IN   | PCIe Lane 3 Differential RX input on the negative terminal   | PCIe      |
| K2          | VSS              | PWR  | Core Power Ground                                            | Core      |
| K3          | XTAL_IN          | IN   | Crystal oscillator input                                     | Clock     |
| K4          | VSS              | PWR  | Core Power Ground                                            | Core      |
| K5          | VCC18A_PCIE      | PWR  | PCIe PHY 1.8V Analog Power Supply                            | PCIe      |
| K6          | VSS              | PWR  | Core Power Ground                                            | Core      |
| K7          | VCC08A_USB       | PWR  | USB PHY 0.8V Analog Power Supply                             | USB       |
| K8          | VSS              | PWR  | Core Power Ground                                            | Core      |
| K9          | VDD08_PCIE       | PWR  | PCIe 0.8V Digital Power Supply                               | PCIe      |
| K10         | VSS              | PWR  | Core Power Ground                                            | Core      |
| K11         | VDD08_PCIE       | PWR  | PCIe 0.8V Digital Power Supply                               | PCIe      |
| K12         | VSS              | PWR  | Core Power Ground                                            | Core      |
| K13         | VDDIO            | PWR  | I/O Power Supply                                             | GPIO      |
| K14         | VSSA_PVT_PCIE    | PWR  | PVT PCIe Analog Power Ground                                 | PVT       |
| K15         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| K16         | VSS              | PWR  | Core Power Ground                                            | Core      |
| K17         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| K18         | VSS              | PWR  | Core Power Ground                                            | Core      |
| K19         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| K20         | VSS              | PWR  | Core Power Ground                                            | Core      |
| K21         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| K22         | VSS              | PWR  | Core Power Ground                                            | Core      |
| K23         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| K24         | VSS              | PWR  | Core Power Ground                                            | Core      |
| K25         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| L1          | P_RXP3           | IN   | PCIe Lane 3 Differential RX input on the positive terminal.  | PCIe      |
| L2          | P_TXP3           | OUT  | PCIe Lane 3 Differential TX output on the positive terminal. | PCIe      |
| L3          | VSS              | PWR  | Core Power Ground                                            | Core      |
| L4          | CLK_IN           | IN   | Clock input signal from external Oscillator.                 | Clock     |
| L5          | GND08A_USB       | PWR  | USB PHY Analog Power Ground                                  | USB       |
| L6          | VDD08_USB        | PWR  | USB 0.8V Digital Power Supply                                | USB       |
| L7          | GND08A_USB       | PWR  | USB PHY Analog Power Ground                                  | USB       |
| L8          | VDD08_USB        | PWR  | USB 0.8V Digital Power Supply                                | USB       |
| L9          | VCC18A_USB       | PWR  | USB PHY 1.8V Analog Power Supply                             | USB       |
| L10         | VDD18A_PVT_DDR   | PWR  | PVT DDR Analog Power Supply                                  | PVT       |
| L11         | VSSA_PVT_DDR     | PWR  | PVT DDR Analog Power Ground                                  | PVT       |
| L12         | VDDIO            | PWR  | I/O Power Supply                                             | GPIO      |
| L13         | VSS              | PWR  | Core Power Ground                                            | Core      |
| L14         | VDD18A_PVT_PCIE  | PWR  | PVT PCIe Analog Power Supply                                 | PVT       |
| L15         | VSS              | PWR  | Core Power Ground                                            | Core      |
| L16         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| L17         | VSS              | PWR  | Core Power Ground                                            | Core      |
| L18         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| L19         | VSS              | PWR  | Core Power Ground                                            | Core      |

## Ara240 Discrete Neural Processing Unit Data Sheet - Commercial

Table 3. Ara240 Pin Description...continued

| Ball number | Ara240 ball name | Type | Ara240 pin description                                       | Interface |
|-------------|------------------|------|--------------------------------------------------------------|-----------|
| L20         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| L21         | VSS              | PWR  | Core Power Ground                                            | Core      |
| L22         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| L23         | VSS              | PWR  | Core Power Ground                                            | Core      |
| L24         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| L25         | VSS              | PWR  | Core Power Ground                                            | Core      |
| M1          | VSS              | PWR  | Core Power Ground                                            | Core      |
| M2          | P_TXN3           | OUT  | PCIe Lane 3 Differential TX output on the negative terminal. | PCIe      |
| M3          | PCIE_CLKREQ#     | I/OD | PCIe Clock Request (Active Low, Open Drain)                  | PCIe      |
| M4          | VSS              | PWR  | Core Power Ground                                            | Core      |
| M5          | VDD_DDR          | PWR  | DDR Core Power Supply                                        | DDR       |
| M6          | VDD18A_PLL3      | PWR  | PLL3 Analog Power Supply                                     | PLL3      |
| M7          | VDD18A_PLL2      | PWR  | PLL2 Analog Power Supply                                     | PLL2      |
| M8          | VDD18A_PLL1      | PWR  | PLL1 Analog Power Supply                                     | PLL1      |
| M9          | VDD18A_PLL0      | PWR  | PLL0 Analog Power Supply                                     | PLL0      |
| M10         | VSSA_XTAL        | PWR  | Crystal Analog Power Ground                                  | XTAL      |
| M11         | VDDA_SPI         | PWR  | DNU                                                          | DNU       |
| M12         | VSS              | PWR  | Core Power Ground                                            | Core      |
| M13         | VDD_DDR          | PWR  | DDR Core Power Supply                                        | DDR       |
| M14         | VSS              | PWR  | Core Power Ground                                            | Core      |
| M15         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| M16         | VSS              | PWR  | Core Power Ground                                            | Core      |
| M17         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| M18         | VSS              | PWR  | Core Power Ground                                            | Core      |
| M19         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| M20         | VSS              | PWR  | Core Power Ground                                            | Core      |
| M21         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| M22         | VSS              | PWR  | Core Power Ground                                            | Core      |
| M23         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| M24         | VSS              | PWR  | Core Power Ground                                            | Core      |
| M25         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| N1          | VSS              | PWR  | Core Power Ground                                            | Core      |
| N2          | VSS              | PWR  | Core Power Ground                                            | Core      |
| N3          | PCIE_PERST#      | IN   | PCIe Reset Signal (Active Low)                               | PCIe      |
| N4          | VQPS18_FUSE_DVC  | PWR  | DVC Fuse Burn Power Supply                                   | Fuse      |
| N5          | VSS              | PWR  | Core Power Ground                                            | Core      |
| N6          | VSSA_PLL3        | PWR  | PLL3 Analog Power Ground                                     | PLL3      |
| N7          | VSSA_PLL2        | PWR  | PLL2 Analog Power Ground                                     | PLL2      |
| N8          | VSSA_PLL1        | PWR  | PLL1 Analog Power Ground                                     | PLL1      |
| N9          | VSSA_PLL0        | PWR  | PLL0 Analog Power Ground                                     | PLL0      |
| N10         | VDD18A_XTAL      | PWR  | Crystal Analog Power Supply                                  | XTAL      |
| N11         | VSSA_SPI         | PWR  | DNU                                                          | DNU       |
| N12         | VDD_DDR          | PWR  | DDR Core Power Supply                                        | DDR       |
| N13         | VSS              | PWR  | Core Power Ground                                            | Core      |
| N14         | VDD_DDR          | PWR  | DDR Core Power Supply                                        | DDR       |
| N15         | VSS              | PWR  | Core Power Ground                                            | Core      |
| N16         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| N17         | VSS              | PWR  | Core Power Ground                                            | Core      |
| N18         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |
| N19         | VSS              | PWR  | Core Power Ground                                            | Core      |
| N20         | VDD_CORE         | PWR  | Core Power Supply                                            | Core      |

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Table 3. Ara240 Pin Description...continued

| Ball number | Ara240 ball name | Type | Ara240 pin description                                                                     | Interface |
|-------------|------------------|------|--------------------------------------------------------------------------------------------|-----------|
| N21         | VSS              | PWR  | Core Power Ground                                                                          | Core      |
| N22         | VDD_CORE         | PWR  | Core Power Supply                                                                          | Core      |
| N23         | VSS              | PWR  | Core Power Ground                                                                          | Core      |
| N24         | VDD_CORE         | PWR  | Core Power Supply                                                                          | Core      |
| N25         | VSS              | PWR  | Core Power Ground                                                                          | Core      |
| P1          | SS_TXP1          | OUT  | USB3.2 differential Super-Speed and Super-Speed-Plus output on the positive terminal TX1+  | USB       |
| P2          | SS_TXN1          | OUT  | USB3.2 differential Super-Speed and Super-Speed-Plus output on the negative terminal TX1-  | USB       |
| P3          | VSS              | PWR  | Core Power Ground                                                                          | Core      |
| P4          | U_DM             | I/O  | USB 2.0 and 1.1 High-speed/Full-speed/Low-Speed differential pad on the negative terminal. | USB       |
| P5          | VDD_DDR          | PWR  | DDR Core Power Supply                                                                      | DDR       |
| P6          | VSS              | PWR  | Core Power Ground                                                                          | Core      |
| P7          | VDD_DDR          | PWR  | DDR Core Power Supply                                                                      | DDR       |
| P8          | VSS              | PWR  | Core Power Ground                                                                          | Core      |
| P9          | VDD_DDR          | PWR  | DDR Core Power Supply                                                                      | DDR       |
| P10         | VSS              | PWR  | Core Power Ground                                                                          | Core      |
| P11         | VDD_DDR          | PWR  | DDR Core Power Supply                                                                      | DDR       |
| P12         | VSS              | PWR  | Core Power Ground                                                                          | Core      |
| P13         | VDD_DDR          | PWR  | DDR Core Power Supply                                                                      | DDR       |
| P14         | VSS              | PWR  | Core Power Ground                                                                          | Core      |
| P15         | VDD_CORE         | PWR  | Core Power Supply                                                                          | Core      |
| P16         | VSS              | PWR  | Core Power Ground                                                                          | Core      |
| P17         | VDD_CORE         | PWR  | Core Power Supply                                                                          | Core      |
| P18         | VSS              | PWR  | Core Power Ground                                                                          | Core      |
| P19         | VDD_CORE         | PWR  | Core Power Supply                                                                          | Core      |
| P20         | VSS              | PWR  | Core Power Ground                                                                          | Core      |
| P21         | VDD_CORE         | PWR  | Core Power Supply                                                                          | Core      |
| P22         | VSS              | PWR  | Core Power Ground                                                                          | Core      |
| P23         | VDD_CORE         | PWR  | Core Power Supply                                                                          | Core      |
| P24         | VSS              | PWR  | Core Power Ground                                                                          | Core      |
| P25         | VDD_CORE         | PWR  | Core Power Supply                                                                          | Core      |
| R1          | SS_TXN2          | OUT  | USB3.2 differential Super-Speed and Super-Speed-Plus output on the negative terminal TX2-  | USB       |
| R2          | SS_TXP2          | OUT  | USB3.2 differential Super-Speed and Super-Speed-Plus output on the positive terminal TX2+  | USB       |
| R3          | VSS              | PWR  | Core Power Ground                                                                          | Core      |
| R4          | U_DP             | I/O  | USB 2.0 and 1.1 High-speed/Full-speed/Low-Speed differential pad on the positive terminal. | USB       |
| R5          | VSS              | PWR  | Core Power Ground                                                                          | Core      |
| R6          | VDD_DDR          | PWR  | DDR Core Power Supply                                                                      | DDR       |
| R7          | VSS              | PWR  | Core Power Ground                                                                          | Core      |
| R8          | VDD_DDR          | PWR  | DDR Core Power Supply                                                                      | DDR       |
| R9          | DATA_RET         | IN   | DDR Data Retention Input Signal (Active High)                                              | DDR       |
| R10         | VDD_DDR          | PWR  | DDR Core Power Supply                                                                      | DDR       |
| R11         | VSS              | PWR  | Core Power Ground                                                                          | Core      |
| R12         | VDD_DDR          | PWR  | DDR Core Power Supply                                                                      | DDR       |
| R13         | VSS              | PWR  | Core Power Ground                                                                          | Core      |
| R14         | VDD_DDR          | PWR  | DDR Core Power Supply                                                                      | DDR       |
| R15         | VSS              | PWR  | Core Power Ground                                                                          | Core      |
| R16         | VDD_CORE         | PWR  | Core Power Supply                                                                          | Core      |
| R17         | VSS              | PWR  | Core Power Ground                                                                          | Core      |
| R18         | VDD_CORE         | PWR  | Core Power Supply                                                                          | Core      |

## Ara240 Discrete Neural Processing Unit Data Sheet - Commercial

Table 3. Ara240 Pin Description...continued

| Ball number | Ara240 ball name | Type | Ara240 pin description                                                                                                   | Interface |
|-------------|------------------|------|--------------------------------------------------------------------------------------------------------------------------|-----------|
| R19         | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| R20         | VDD_CORE         | PWR  | Core Power Supply                                                                                                        | Core      |
| R21         | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| R22         | VDD_CORE         | PWR  | Core Power Supply                                                                                                        | Core      |
| R23         | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| R24         | VDD_CORE         | PWR  | Core Power Supply                                                                                                        | Core      |
| R25         | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| T1          | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| T2          | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| T3          | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| T4          | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| T5          | VDDQX            | PWR  | DDR I/O Pre-driver Power Supply                                                                                          | DDR       |
| T6          | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| T7          | VDD_DDR          | PWR  | DDR Core Power Supply                                                                                                    | DDR       |
| T8          | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| T9          | VDD_DDR          | PWR  | DDR Core Power Supply                                                                                                    | DDR       |
| T10         | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| T11         | VDD_DDR          | PWR  | DDR Core Power Supply                                                                                                    | DDR       |
| T12         | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| T13         | VDD_DDR          | PWR  | DDR Core Power Supply                                                                                                    | DDR       |
| T14         | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| T15         | VDD_CORE         | PWR  | Core Power Supply                                                                                                        | Core      |
| T16         | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| T17         | VDD_CORE         | PWR  | Core Power Supply                                                                                                        | Core      |
| T18         | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| T19         | VDD_CORE         | PWR  | Core Power Supply                                                                                                        | Core      |
| T20         | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| T21         | VDD_CORE         | PWR  | Core Power Supply                                                                                                        | Core      |
| T22         | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| T23         | VDD_CORE         | PWR  | Core Power Supply                                                                                                        | Core      |
| T24         | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| T25         | VDD_CORE         | PWR  | Core Power Supply                                                                                                        | Core      |
| U1          | SS_RXP1          | IN   | USB3.2 differential Super-Speed and Super-Speed-Plus input on the Positive terminal RX1+                                 | USB       |
| U2          | SS_RXN1          | IN   | USB3.2 differential Super-Speed and Super-Speed-Plus input on the Negative terminal RX1-                                 | USB       |
| U3          | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| U4          | CC_1             | I/O  | Configuration Channel (CC1) used in the discovery, configuration and management of connections across a USB Type-C cable | USB       |
| U5          | VDDQX            | PWR  | DDR I/O Pre-driver Power Supply                                                                                          | DDR       |
| U6          | VDD_DDR          | PWR  | DDR Core Power Supply                                                                                                    | DDR       |
| U7          | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| U8          | VDD_DDR          | PWR  | DDR Core Power Supply                                                                                                    | DDR       |
| U9          | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| U10         | VDD_DDR          | PWR  | DDR Core Power Supply                                                                                                    | DDR       |
| U11         | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| U12         | VDD_DDR          | PWR  | DDR Core Power Supply                                                                                                    | DDR       |
| U13         | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| U14         | VDD_DDR          | PWR  | DDR Core Power Supply                                                                                                    | DDR       |
| U15         | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| U16         | VDD_CORE         | PWR  | Core Power Supply                                                                                                        | Core      |
| U17         | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |

## Ara240 Discrete Neural Processing Unit Data Sheet - Commercial

Table 3. Ara240 Pin Description...continued

| Ball number | Ara240 ball name | Type | Ara240 pin description                                                                                                   | Interface |
|-------------|------------------|------|--------------------------------------------------------------------------------------------------------------------------|-----------|
| U18         | VDD_CORE         | PWR  | Core Power Supply                                                                                                        | Core      |
| U19         | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| U20         | VDD_CORE         | PWR  | Core Power Supply                                                                                                        | Core      |
| U21         | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| U22         | VDD_CORE         | PWR  | Core Power Supply                                                                                                        | Core      |
| U23         | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| U24         | VDD_CORE         | PWR  | Core Power Supply                                                                                                        | Core      |
| U25         | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| V1          | SS_RXN2          | IN   | USB3.2 differential Super-Speed and Super-Speed-Plus input on the Negative terminal RX2-                                 | USB       |
| V2          | SS_RXP2          | IN   | USB3.2 differential Super-Speed and Super-Speed-Plus input on the Positive terminal RX2+                                 | USB       |
| V3          | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| V4          | CC_0             | I/O  | Configuration Channel (CC0) used in the discovery, configuration and management of connections across a USB Type-C cable | USB       |
| V5          | VDDQX            | PWR  | DDR I/O Pre-driver Power Supply                                                                                          | DDR       |
| V6          | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| V7          | VDD_DDR          | PWR  | DDR Core Power Supply                                                                                                    | DDR       |
| V8          | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| V9          | VDDPLL_MCB1      | PWR  | PLL MCB1 Power Supply                                                                                                    | DDR       |
| V10         | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| V11         | VDDPLL_TOP       | PWR  | PLL TOP Power Supply                                                                                                     | DDR       |
| V12         | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| V13         | VDD_DDR          | PWR  | DDR PHY Power Supply                                                                                                     | DDR       |
| V14         | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| V15         | VDD_CORE         | PWR  | Core Power Supply                                                                                                        | Core      |
| V16         | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| V17         | VDD_CORE         | PWR  | Core Power Supply                                                                                                        | Core      |
| V18         | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| V19         | VDD_CORE         | PWR  | Core Power Supply                                                                                                        | Core      |
| V20         | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| V21         | VDD_CORE         | PWR  | Core Power Supply                                                                                                        | Core      |
| V22         | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| V23         | VDD_CORE         | PWR  | Core Power Supply                                                                                                        | Core      |
| V24         | VSSA_PVT_VPC     | PWR  | VPC PVT Analog Power Ground                                                                                              | PVT       |
| V25         | VDD18A_PVT_VPC   | PWR  | VPC PVT Analog Power Supply                                                                                              | PVT       |
| W1          | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| W2          | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| W3          | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| W4          | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| W5          | VDDQX            | PWR  | DDR I/O Pre-driver Power Supply                                                                                          | DDR       |
| W6          | VDDQX            | PWR  | DDR I/O Pre-driver Power Supply                                                                                          | DDR       |
| W7          | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| W8          | VDD_DDR          | PWR  | DDR Core Power Supply                                                                                                    | DDR       |
| W9          | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| W10         | VDDQCK           | PWR  | DDR Clock I/O Power Supply                                                                                               | DDR       |
| W11         | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| W12         | VDDPLL_MCB2      | PWR  | PLL MCB2 Power Supply                                                                                                    | DDR       |
| W13         | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| W14         | VDD_DDR          | PWR  | DDR Core Power Supply                                                                                                    | DDR       |
| W15         | VSS              | PWR  | Core Power Ground                                                                                                        | Core      |
| W16         | VDD_CORE         | PWR  | Core Power Supply                                                                                                        | Core      |

## Ara240 Discrete Neural Processing Unit Data Sheet - Commercial

Table 3. Ara240 Pin Description...continued

| Ball number | Ara240 ball name   | Type | Ara240 pin description                                                                                 | Interface |
|-------------|--------------------|------|--------------------------------------------------------------------------------------------------------|-----------|
| W17         | VSS                | PWR  | Core Power Ground                                                                                      | Core      |
| W18         | VDD_CORE           | PWR  | Core Power Supply                                                                                      | Core      |
| W19         | VSS                | PWR  | Core Power Ground                                                                                      | Core      |
| W20         | VDD_CORE           | PWR  | Core Power Supply                                                                                      | Core      |
| W21         | VSS                | PWR  | Core Power Ground                                                                                      | Core      |
| W22         | VDD_CORE           | PWR  | Core Power Supply                                                                                      | Core      |
| W23         | VDDQ               | PWR  | DDR I/O Power Supply                                                                                   | DDR       |
| W24         | VSS                | PWR  | Core Power Ground                                                                                      | Core      |
| W25         | VDDQ               | PWR  | DDR I/O Power Supply                                                                                   | DDR       |
| Y1          | DDR_CA_7           | OUT  | DDR Command/Address Output Signal - 7                                                                  | DDR       |
| Y2          | DDR_DQ_19          | I/O  | Data Input/Output: Bi-direction data - 19                                                              | DDR       |
| Y3          | DDR_DQ_21          | I/O  | Data Input/Output: Bi-direction data - 21                                                              | DDR       |
| Y4          | DDR_DM_2           | OUT  | DDR Data mask output Signal - 2                                                                        | DDR       |
| Y5          | DDR_CA_9           | OUT  | DDR Command/Address Output Signal - 9                                                                  | DDR       |
| Y6          | DDR_CSN_7          | OUT  | Chip Select: CS is part of the command code. Each channel (A & B) has its own CS signal_7 (Active Low) | DDR       |
| Y7          | DDR_CSN_5          | OUT  | Chip Select: CS is part of the command code. Each channel (A & B) has its own CS signal_5 (Active Low) | DDR       |
| Y8          | DDR_CSN_1          | OUT  | Chip Select: CS is part of the command code. Each channel (A & B) has its own CS signal_1 (Active Low) | DDR       |
| Y9          | DDR_CSN_3          | OUT  | Chip Select: CS is part of the command code. Each channel (A & B) has its own CS signal_3 (Active Low) | DDR       |
| Y10         | DDR_CA_4           | OUT  | DDR Command/Address Output Signal - 4                                                                  | DDR       |
| Y11         | DDR_CA_1           | OUT  | DDR Command/Address Output Signal - 1                                                                  | DDR       |
| Y12         | DDR_CA_3           | OUT  | DDR Command/Address Output Signal - 3                                                                  | DDR       |
| Y13         | DDR_CKE_0          | OUT  | DDR Clock Enable - 0                                                                                   | DDR       |
| Y14         | DDR_CSN_6          | OUT  | Chip Select: CS is part of the command code. Each channel (A & B) has its own CS signal_6 (Active Low) | DDR       |
| Y15         | DDR_CA_10          | OUT  | DDR Command/Address Output Signal - 10                                                                 | DDR       |
| Y16         | DDR_PLL_TEST_OUT_P | OUT  | DDR Differential PLL Test Output Signal (Positive)                                                     | DDR       |
| Y17         | DDR_PLL_TEST_OUT_N | OUT  | DDR Differential PLL Test Output Signal (Negative)                                                     | DDR       |
| Y18         | VSS                | PWR  | Core Power Ground                                                                                      | Core      |
| Y19         | DDR_ATB0           | IN   | DDR Analog Test Bus 0                                                                                  | DDR       |
| Y20         | DDR_ATB1           | IN   | DDR Analog Test Bus 1                                                                                  | DDR       |
| Y21         | DDR_CAL            | A    | DDR PHY Calibration pin                                                                                | DDR       |
| Y22         | VDDQ               | PWR  | DDR I/O Power Supply                                                                                   | DDR       |
| Y23         | VSS                | PWR  | Core Power Ground                                                                                      | Core      |
| Y24         | VDDQ               | PWR  | DDR I/O Power Supply                                                                                   | DDR       |
| Y25         | DDR_DQ_56          | I/O  | Data Input/Output: Bi-direction data - 56                                                              | DDR       |
| AA1         | DDR_CA_11          | OUT  | DDR Command/Address Output Signal - 11                                                                 | DDR       |
| AA2         | DDR_DQ_20          | I/O  | Data Input/Output: Bi-direction data - 20                                                              | DDR       |
| AA3         | DDR_DQ_22          | I/O  | Data Input/Output: Bi-direction data - 22                                                              | DDR       |
| AA4         | DDR_DQ_23          | I/O  | Data Input/Output: Bi-direction data - 23                                                              | DDR       |
| AA5         | DDR_DQ_17          | I/O  | Data Input/Output: Bi-direction data - 17                                                              | DDR       |
| AA6         | DDR_CA_8           | OUT  | DDR Command/Address Output Signal - 8                                                                  | DDR       |
| AA7         | DDR_DQ_15          | I/O  | Data Input/Output: Bi-direction data - 15                                                              | DDR       |
| AA8         | DDR_DQ_13          | I/O  | Data Input/Output: Bi-direction data - 13                                                              | DDR       |
| AA9         | DDR_DQ_8           | I/O  | Data Input/Output: Bi-direction data - 8                                                               | DDR       |
| AA10        | DDR_DQ_11          | I/O  | Data Input/Output: Bi-direction data - 11                                                              | DDR       |
| AA11        | DDR_DQ_9           | I/O  | Data Input/Output: Bi-direction data - 9                                                               | DDR       |
| AA12        | DDR_CA_5           | OUT  | DDR Command/Address Output Signal - 5                                                                  | DDR       |
| AA13        | DDR_RSTN           | OUT  | DDR Reset active low output Signal. (Active Low)                                                       | DDR       |
| AA14        | DDR_CSN_0          | OUT  | Chip Select: CS is part of the command code. Each channel (A & B) has its own CS signal_0 (Active Low) | DDR       |

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Table 3. Ara240 Pin Description...continued

| Ball number | Ara240 ball name | Type | Ara240 pin description                                                                                 | Interface |
|-------------|------------------|------|--------------------------------------------------------------------------------------------------------|-----------|
| AA15        | DDR_DQ_45        | I/O  | Data Input/Output: Bi-direction data - 45                                                              | DDR       |
| AA16        | DDR_DQ_47        | I/O  | Data Input/Output: Bi-direction data - 47                                                              | DDR       |
| AA17        | DDR_DQ_46        | I/O  | Data Input/Output: Bi-direction data - 46                                                              | DDR       |
| AA18        | DDR_DQ_44        | I/O  | Data Input/Output: Bi-direction data - 44                                                              | DDR       |
| AA19        | DDR_DQ_43        | I/O  | Data Input/Output: Bi-direction data - 43                                                              | DDR       |
| AA20        | VSS              | PWR  | Core Power Ground                                                                                      | Core      |
| AA21        | DDR_DQ_58        | I/O  | Data Input/Output: Bi-direction data - 58                                                              | DDR       |
| AA22        | DDR_DM_7         | OUT  | DDR Data mask output Signal - 7                                                                        | DDR       |
| AA23        | DDR_DQ_63        | I/O  | Data Input/Output: Bi-direction data - 63                                                              | DDR       |
| AA24        | DDR_DQ_59        | I/O  | Data Input/Output: Bi-direction data - 59                                                              | DDR       |
| AA25        | DDR_DQ_57        | I/O  | Data Input/Output: Bi-direction data - 57                                                              | DDR       |
| AB1         | DDR_DQ_27        | I/O  | Data Input/Output: Bi-direction data - 27                                                              | DDR       |
| AB2         | DDR_DQ_16        | I/O  | Data Input/Output: Bi-direction data - 16                                                              | DDR       |
| AB3         | DDR_DQSN_2       | I/O  | Data Strobe Differential in/output clock -ve signals-2                                                 | DDR       |
| AB4         | DDR_DQSP_2       | I/O  | Data Strobe Differential in/output clock +ve signals - 2                                               | DDR       |
| AB5         | DDR_DQ_18        | I/O  | Data Input/Output: Bi-direction data - 18                                                              | DDR       |
| AB6         | DDR_CA_6         | OUT  | DDR Command/Address Output Signal - 6                                                                  | DDR       |
| AB7         | DDR_DQ_14        | I/O  | Data Input/Output: Bi-direction data - 14                                                              | DDR       |
| AB8         | DDR_DQ_12        | I/O  | Data Input/Output: Bi-direction data - 12                                                              | DDR       |
| AB9         | DDR_DQSN_1       | I/O  | Data Strobe Differential in/output clock -ve signals-1                                                 | DDR       |
| AB10        | DDR_DQSP_1       | I/O  | Data Strobe Differential in/output clock +ve signals - 1                                               | DDR       |
| AB11        | DDR_DM_1         | OUT  | DDR Data mask output Signal - 1                                                                        | DDR       |
| AB12        | DDR_CA_0         | OUT  | DDR Command/Address Output Signal - 0                                                                  | DDR       |
| AB13        | DDR_CKE_1        | OUT  | DDR Clock Enable - 1                                                                                   | DDR       |
| AB14        | DDR_CSN_2        | OUT  | Chip Select: CS is part of the command code. Each channel (A & B) has its own CS signal_2 (Active Low) | DDR       |
| AB15        | DDR_DQ_41        | I/O  | Data Input/Output: Bi-direction data - 41                                                              | DDR       |
| AB16        | DDR_DQ_42        | I/O  | Data Input/Output: Bi-direction data - 42                                                              | DDR       |
| AB17        | DDR_DQSP_5       | I/O  | Data Strobe Differential in/output clock +ve signals - 5                                               | DDR       |
| AB18        | DDR_DQSN_5       | I/O  | Data Strobe Differential in/output clock -ve signals-5                                                 | DDR       |
| AB19        | DDR_DM_5         | OUT  | DDR Data mask output Signal - 5                                                                        | DDR       |
| AB20        | DDR_DQ_40        | I/O  | Data Input/Output: Bi-direction data - 40                                                              | DDR       |
| AB21        | DDR_DQ_60        | I/O  | Data Input/Output: Bi-direction data - 60                                                              | DDR       |
| AB22        | DDR_DQ_61        | I/O  | Data Input/Output: Bi-direction data - 61                                                              | DDR       |
| AB23        | DDR_DQSN_7       | I/O  | Data Strobe Differential in/output clock -ve signals-7                                                 | DDR       |
| AB24        | DDR_DQSP_7       | I/O  | Data Strobe Differential in/output clock +ve signals - 7                                               | DDR       |
| AB25        | DDR_DQ_62        | I/O  | Data Input/Output: Bi-direction data - 62                                                              | DDR       |
| AC1         | DDR_DQ_28        | I/O  | Data Input/Output: Bi-direction data - 28                                                              | DDR       |
| AC2         | DDR_DQ_29        | I/O  | Data Input/Output: Bi-direction data - 29                                                              | DDR       |
| AC3         | DDR_DM_3         | OUT  | DDR Data mask output Signal - 3                                                                        | DDR       |
| AC4         | DDR_DQ_31        | I/O  | Data Input/Output: Bi-direction data - 31                                                              | DDR       |
| AC5         | DDR_DQ_25        | I/O  | Data Input/Output: Bi-direction data - 25                                                              | DDR       |
| AC6         | DDR_DQ_4         | I/O  | Data Input/Output: Bi-direction data - 4                                                               | DDR       |
| AC7         | DDR_DQ_5         | I/O  | Data Input/Output: Bi-direction data - 5                                                               | DDR       |
| AC8         | DDR_DQSP_0       | I/O  | Data Strobe Differential in/output clock +ve signals - 0                                               | DDR       |
| AC9         | DDR_DQ_3         | I/O  | Data Input/Output: Bi-direction data - 3                                                               | DDR       |
| AC10        | DDR_DQ_1         | I/O  | Data Input/Output: Bi-direction data - 1                                                               | DDR       |
| AC11        | DDR_DQ_10        | I/O  | Data Input/Output: Bi-direction data - 10                                                              | DDR       |
| AC12        | DDR_CKP_0        | OUT  | DDR Differential Clock Positive - 0                                                                    | DDR       |
| AC13        | DDR_CKN_1        | OUT  | DDR Differential Clock Negative - 1                                                                    | DDR       |
| AC14        | DDR_CA_2         | OUT  | DDR Command/Address Output Signal - 2                                                                  | DDR       |
| AC15        | DDR_DQ_36        | I/O  | Data Input/Output: Bi-direction data - 36                                                              | DDR       |

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Table 3. Ara240 Pin Description...continued

| Ball number | Ara240 ball name | Type | Ara240 pin description                                                                                 | Interface |
|-------------|------------------|------|--------------------------------------------------------------------------------------------------------|-----------|
| AC16        | DDR_DM_4         | OUT  | DDR Data mask output Signal - 4                                                                        | DDR       |
| AC17        | DDR_DQ_37        | I/O  | Data Input/Output: Bi-direction data - 37                                                              | DDR       |
| AC18        | DDR_DQ_38        | I/O  | Data Input/Output: Bi-direction data - 38                                                              | DDR       |
| AC19        | DDR_DQ_39        | I/O  | Data Input/Output: Bi-direction data - 39                                                              | DDR       |
| AC20        | DDR_DQ_49        | I/O  | Data Input/Output: Bi-direction data - 49                                                              | DDR       |
| AC21        | DDR_DQ_54        | I/O  | Data Input/Output: Bi-direction data - 54                                                              | DDR       |
| AC22        | DDR_DQ_55        | I/O  | Data Input/Output: Bi-direction data - 55                                                              | DDR       |
| AC23        | DDR_DM_6         | OUT  | DDR Data mask output Signal - 6                                                                        | DDR       |
| AC24        | DDR_DQ_53        | I/O  | Data Input/Output: Bi-direction data - 53                                                              | DDR       |
| AC25        | DDR_DQ_50        | I/O  | Data Input/Output: Bi-direction data - 50                                                              | DDR       |
| AD1         | DDR_DQ_24        | I/O  | Data Input/Output: Bi-direction data - 24                                                              | DDR       |
| AD2         | DDR_DQSP_3       | I/O  | Data Strobe Differential in/output clock +ve signals - 3                                               | DDR       |
| AD3         | DDR_DQSN_3       | I/O  | Data Strobe Differential in/output clock -ve signals-3                                                 | DDR       |
| AD4         | DDR_DQ_30        | I/O  | Data Input/Output: Bi-direction data - 30                                                              | DDR       |
| AD5         | DDR_DQ_26        | I/O  | Data Input/Output: Bi-direction data - 26                                                              | DDR       |
| AD6         | DDR_DQ_2         | I/O  | Data Input/Output: Bi-direction data - 2                                                               | DDR       |
| AD7         | DDR_DQ_6         | I/O  | Data Input/Output: Bi-direction data - 6                                                               | DDR       |
| AD8         | DDR_DQSN_0       | I/O  | Data Strobe Differential in/output clock -ve signals-0                                                 | DDR       |
| AD9         | DDR_DM_0         | OUT  | DDR Data mask output - 0                                                                               | DDR       |
| AD10        | DDR_DQ_7         | I/O  | Data Input/Output: Bi-direction data - 7                                                               | DDR       |
| AD11        | DDR_DQ_0         | I/O  | Data Input/Output: Bi-direction data - 0                                                               | DDR       |
| AD12        | DDR_CKN_0        | OUT  | DDR Differential Clock Negative - 0                                                                    | DDR       |
| AD13        | DDR_CKP_1        | OUT  | DDR Differential Clock Positive - 1                                                                    | DDR       |
| AD14        | DDR_CSN_4        | OUT  | Chip Select: CS is part of the command code. Each channel (A & B) has its own CS signal_4 (Active Low) | DDR       |
| AD15        | DDR_DQ_34        | I/O  | Data Input/Output: Bi-direction data - 34                                                              | DDR       |
| AD16        | DDR_DQ_35        | I/O  | Data Input/Output: Bi-direction data - 35                                                              | DDR       |
| AD17        | DDR_DQSP_4       | I/O  | Data Strobe Differential in/output clock +ve signals - 4                                               | DDR       |
| AD18        | DDR_DQSN_4       | I/O  | Data Strobe Differential in/output clock -ve signals-4                                                 | DDR       |
| AD19        | DDR_DQ_32        | I/O  | Data Input/Output: Bi-direction data - 32                                                              | DDR       |
| AD20        | DDR_DQ_33        | I/O  | Data Input/Output: Bi-direction data - 33                                                              | DDR       |
| AD21        | DDR_DQ_52        | I/O  | Data Input/Output: Bi-direction data - 52                                                              | DDR       |
| AD22        | DDR_DQ_51        | I/O  | Data Input/Output: Bi-direction data - 51                                                              | DDR       |
| AD23        | DDR_DQSN_6       | I/O  | Data Strobe Differential in/output clock -ve signals-6                                                 | DDR       |
| AD24        | DDR_DQSP_6       | I/O  | Data Strobe Differential in/output clock +ve signals - 6                                               | DDR       |
| AD25        | DDR_DQ_48        | I/O  | Data Input/Output: Bi-direction data - 48                                                              | DDR       |
| AE1         | VSS              | PWR  | Core Power Ground                                                                                      | Core      |
| AE2         | VDDQ             | PWR  | DDR I/O Power Supply                                                                                   | DDR       |
| AE3         | VSS              | PWR  | Core Power Ground                                                                                      | Core      |
| AE4         | VDDQ             | PWR  | DDR I/O Power Supply                                                                                   | DDR       |
| AE5         | VSS              | PWR  | Core Power Ground                                                                                      | Core      |
| AE6         | VDDQ             | PWR  | DDR I/O Power Supply                                                                                   | DDR       |
| AE7         | VSS              | PWR  | Core Power Ground                                                                                      | Core      |
| AE8         | VDDQ             | PWR  | DDR I/O Power Supply                                                                                   | DDR       |
| AE9         | VSS              | PWR  | Core Power Ground                                                                                      | Core      |
| AE10        | VDDQ             | PWR  | DDR I/O Power Supply                                                                                   | DDR       |
| AE11        | VSS              | PWR  | Core Power Ground                                                                                      | Core      |
| AE12        | VDDQ             | PWR  | DDR I/O Power Supply                                                                                   | DDR       |
| AE13        | VSS              | PWR  | Core Power Ground                                                                                      | Core      |
| AE14        | VDDQ             | PWR  | DDR I/O Power Supply                                                                                   | DDR       |
| AE15        | VSS              | PWR  | Core Power Ground                                                                                      | Core      |
| AE16        | VDDQ             | PWR  | DDR I/O Power Supply                                                                                   | DDR       |



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Table 3. Ara240 Pin Description...continued

| Ball number | Ara240 ball name | Type | Ara240 pin description | Interface |
|-------------|------------------|------|------------------------|-----------|
| AE17        | VSS              | PWR  | Core Power Ground      | Core      |
| AE18        | VDDQ             | PWR  | DDR I/O Power Supply   | DDR       |
| AE19        | VSS              | PWR  | Core Power Ground      | Core      |
| AE20        | VDDQ             | PWR  | DDR I/O Power Supply   | DDR       |
| AE21        | VSS              | PWR  | Core Power Ground      | Core      |
| AE22        | VDDQ             | PWR  | DDR I/O Power Supply   | DDR       |
| AE23        | VSS              | PWR  | Core Power Ground      | Core      |
| AE24        | VDDQ             | PWR  | DDR I/O Power Supply   | DDR       |
| AE25        | VSS              | PWR  | Core Power Ground      | Core      |

## 7.2.1 LPDDR4 interface signal description

Table 4. Ara240 LPDDR4 interface signal description

| Ball number | Ara240 DDR ball name | Type | Ara240 DDR interface signal description                                                                | Interface |
|-------------|----------------------|------|--------------------------------------------------------------------------------------------------------|-----------|
| Y19         | DDR_ATB0             | IN   | DDR Analog Test Bus 0                                                                                  | DDR       |
| Y20         | DDR_ATB1             | IN   | DDR Analog Test Bus 1                                                                                  | DDR       |
| AB12        | DDR_CA_0             | OUT  | DDR Command/Address Output Signal - 0                                                                  | DDR       |
| Y11         | DDR_CA_1             | OUT  | DDR Command/Address Output Signal - 1                                                                  | DDR       |
| AC14        | DDR_CA_2             | OUT  | DDR Command/Address Output Signal - 2                                                                  | DDR       |
| Y12         | DDR_CA_3             | OUT  | DDR Command/Address Output Signal - 3                                                                  | DDR       |
| Y10         | DDR_CA_4             | OUT  | DDR Command/Address Output Signal - 4                                                                  | DDR       |
| AA12        | DDR_CA_5             | OUT  | DDR Command/Address Output Signal - 5                                                                  | DDR       |
| AB6         | DDR_CA_6             | OUT  | DDR Command/Address Output Signal - 6                                                                  | DDR       |
| Y1          | DDR_CA_7             | OUT  | DDR Command/Address Output Signal - 7                                                                  | DDR       |
| AA6         | DDR_CA_8             | OUT  | DDR Command/Address Output Signal - 8                                                                  | DDR       |
| Y5          | DDR_CA_9             | OUT  | DDR Command/Address Output Signal - 9                                                                  | DDR       |
| Y15         | DDR_CA_10            | OUT  | DDR Command/Address Output Signal - 10                                                                 | DDR       |
| AA1         | DDR_CA_11            | OUT  | DDR Command/Address Output Signal - 11                                                                 | DDR       |
| Y21         | DDR_CAL              | A    | DDR PHY Calibration pin                                                                                | DDR       |
| Y13         | DDR_CKE_0            | OUT  | DDR Clock Enable - 0                                                                                   | DDR       |
| AB13        | DDR_CKE_1            | OUT  | DDR Clock Enable - 1                                                                                   | DDR       |
| AD12        | DDR_CKN_0            | OUT  | DDR Differential Clock Negative - 0                                                                    | DDR       |
| AC12        | DDR_CKP_0            | OUT  | DDR Differential Clock Positive - 0                                                                    | DDR       |
| AC13        | DDR_CKN_1            | OUT  | DDR Differential Clock Negative - 1                                                                    | DDR       |
| AD13        | DDR_CKP_1            | OUT  | DDR Differential Clock Positive - 1                                                                    | DDR       |
| AA14        | DDR_CSN_0            | OUT  | Chip Select: CS is part of the command code. Each channel (A & B) has its own CS signal_0 (Active Low) | DDR       |
| Y8          | DDR_CSN_1            | OUT  | Chip Select: CS is part of the command code. Each channel (A & B) has its own CS signal_1 (Active Low) | DDR       |
| AB14        | DDR_CSN_2            | OUT  | Chip Select: CS is part of the command code. Each channel (A & B) has its own CS signal_2 (Active Low) | DDR       |
| Y9          | DDR_CSN_3            | OUT  | Chip Select: CS is part of the command code. Each channel (A & B) has its own CS signal_3 (Active Low) | DDR       |
| AD14        | DDR_CSN_4            | OUT  | Chip Select: CS is part of the command code. Each channel (A & B) has its own CS signal_4 (Active Low) | DDR       |
| Y7          | DDR_CSN_5            | OUT  | Chip Select: CS is part of the command code. Each channel (A & B) has its own CS signal_5 (Active Low) | DDR       |
| Y14         | DDR_CSN_6            | OUT  | Chip Select: CS is part of the command code. Each channel (A & B) has its own CS signal_6 (Active Low) | DDR       |
| Y6          | DDR_CSN_7            | OUT  | Chip Select: CS is part of the command code. Each channel (A & B) has its own CS signal_7 (Active Low) | DDR       |
| AD9         | DDR_DM_0             | OUT  | DDR Data mask output Signal - 0                                                                        | DDR       |
| AB11        | DDR_DM_1             | OUT  | DDR Data mask output Signal - 1                                                                        | DDR       |
| Y4          | DDR_DM_2             | OUT  | DDR Data mask output Signal - 2                                                                        | DDR       |

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Table 4. Ara240 LPDDR4 interface signal description...continued

| Ball number | Ara240 DDR ball name | Type | Ara240 DDR interface signal description   | Interface |
|-------------|----------------------|------|-------------------------------------------|-----------|
| AC3         | DDR_DM_3             | OUT  | DDR Data mask output Signal - 3           | DDR       |
| AC16        | DDR_DM_4             | OUT  | DDR Data mask output Signal - 4           | DDR       |
| AB19        | DDR_DM_5             | OUT  | DDR Data mask output Signal - 5           | DDR       |
| AC23        | DDR_DM_6             | OUT  | DDR Data mask output Signal - 6           | DDR       |
| AA22        | DDR_DM_7             | OUT  | DDR Data mask output Signal - 7           | DDR       |
| AD11        | DDR_DQ_0             | I/O  | Data Input/Output: Bi-direction data - 0  | DDR       |
| AC10        | DDR_DQ_1             | I/O  | Data Input/Output: Bi-direction data - 1  | DDR       |
| AD6         | DDR_DQ_2             | I/O  | Data Input/Output: Bi-direction data - 2  | DDR       |
| AC9         | DDR_DQ_3             | I/O  | Data Input/Output: Bi-direction data - 3  | DDR       |
| AC6         | DDR_DQ_4             | I/O  | Data Input/Output: Bi-direction data - 4  | DDR       |
| AC7         | DDR_DQ_5             | I/O  | Data Input/Output: Bi-direction data - 5  | DDR       |
| AD7         | DDR_DQ_6             | I/O  | Data Input/Output: Bi-direction data - 6  | DDR       |
| AD10        | DDR_DQ_7             | I/O  | Data Input/Output: Bi-direction data - 7  | DDR       |
| AA9         | DDR_DQ_8             | I/O  | Data Input/Output: Bi-direction data - 8  | DDR       |
| AA11        | DDR_DQ_9             | I/O  | Data Input/Output: Bi-direction data - 9  | DDR       |
| AC11        | DDR_DQ_10            | I/O  | Data Input/Output: Bi-direction data - 10 | DDR       |
| AA10        | DDR_DQ_11            | I/O  | Data Input/Output: Bi-direction data - 11 | DDR       |
| AB8         | DDR_DQ_12            | I/O  | Data Input/Output: Bi-direction data - 12 | DDR       |
| AA8         | DDR_DQ_13            | I/O  | Data Input/Output: Bi-direction data - 13 | DDR       |
| AB7         | DDR_DQ_14            | I/O  | Data Input/Output: Bi-direction data - 14 | DDR       |
| AA7         | DDR_DQ_15            | I/O  | Data Input/Output: Bi-direction data - 15 | DDR       |
| AB2         | DDR_DQ_16            | I/O  | Data Input/Output: Bi-direction data - 16 | DDR       |
| AA5         | DDR_DQ_17            | I/O  | Data Input/Output: Bi-direction data - 17 | DDR       |
| AB5         | DDR_DQ_18            | I/O  | Data Input/Output: Bi-direction data - 18 | DDR       |
| Y2          | DDR_DQ_19            | I/O  | Data Input/Output: Bi-direction data - 19 | DDR       |
| AA2         | DDR_DQ_20            | I/O  | Data Input/Output: Bi-direction data - 20 | DDR       |
| Y3          | DDR_DQ_21            | I/O  | Data Input/Output: Bi-direction data - 21 | DDR       |
| AA3         | DDR_DQ_22            | I/O  | Data Input/Output: Bi-direction data - 22 | DDR       |
| AA4         | DDR_DQ_23            | I/O  | Data Input/Output: Bi-direction data - 23 | DDR       |
| AD1         | DDR_DQ_24            | I/O  | Data Input/Output: Bi-direction data - 24 | DDR       |
| AC5         | DDR_DQ_25            | I/O  | Data Input/Output: Bi-direction data - 25 | DDR       |
| AD5         | DDR_DQ_26            | I/O  | Data Input/Output: Bi-direction data - 26 | DDR       |
| AB1         | DDR_DQ_27            | I/O  | Data Input/Output: Bi-direction data - 27 | DDR       |
| AC1         | DDR_DQ_28            | I/O  | Data Input/Output: Bi-direction data - 28 | DDR       |
| AC2         | DDR_DQ_29            | I/O  | Data Input/Output: Bi-direction data - 29 | DDR       |
| AD4         | DDR_DQ_30            | I/O  | Data Input/Output: Bi-direction data - 30 | DDR       |
| AC4         | DDR_DQ_31            | I/O  | Data Input/Output: Bi-direction data - 31 | DDR       |
| AD19        | DDR_DQ_32            | I/O  | Data Input/Output: Bi-direction data - 32 | DDR       |
| AD20        | DDR_DQ_33            | I/O  | Data Input/Output: Bi-direction data - 33 | DDR       |
| AD15        | DDR_DQ_34            | I/O  | Data Input/Output: Bi-direction data - 34 | DDR       |
| AD16        | DDR_DQ_35            | I/O  | Data Input/Output: Bi-direction data - 35 | DDR       |
| AC15        | DDR_DQ_36            | I/O  | Data Input/Output: Bi-direction data - 36 | DDR       |
| AC17        | DDR_DQ_37            | I/O  | Data Input/Output: Bi-direction data - 37 | DDR       |
| AC18        | DDR_DQ_38            | I/O  | Data Input/Output: Bi-direction data - 38 | DDR       |
| AC19        | DDR_DQ_39            | I/O  | Data Input/Output: Bi-direction data - 39 | DDR       |
| AB20        | DDR_DQ_40            | I/O  | Data Input/Output: Bi-direction data - 40 | DDR       |
| AB15        | DDR_DQ_41            | I/O  | Data Input/Output: Bi-direction data - 41 | DDR       |
| AB16        | DDR_DQ_42            | I/O  | Data Input/Output: Bi-direction data - 42 | DDR       |
| AA19        | DDR_DQ_43            | I/O  | Data Input/Output: Bi-direction data - 43 | DDR       |
| AA18        | DDR_DQ_44            | I/O  | Data Input/Output: Bi-direction data - 44 | DDR       |
| AA15        | DDR_DQ_45            | I/O  | Data Input/Output: Bi-direction data - 45 | DDR       |

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Table 4. Ara240 LPDDR4 interface signal description...continued

| Ball number | Ara240 DDR ball name | Type | Ara240 DDR interface signal description                  | Interface |
|-------------|----------------------|------|----------------------------------------------------------|-----------|
| AA17        | DDR_DQ_46            | I/O  | Data Input/Output: Bi-direction data - 46                | DDR       |
| AA16        | DDR_DQ_47            | I/O  | Data Input/Output: Bi-direction data - 47                | DDR       |
| AD25        | DDR_DQ_48            | I/O  | Data Input/Output: Bi-direction data - 48                | DDR       |
| AC20        | DDR_DQ_49            | I/O  | Data Input/Output: Bi-direction data - 49                | DDR       |
| AC25        | DDR_DQ_50            | I/O  | Data Input/Output: Bi-direction data - 50                | DDR       |
| AD22        | DDR_DQ_51            | I/O  | Data Input/Output: Bi-direction data - 51                | DDR       |
| AD21        | DDR_DQ_52            | I/O  | Data Input/Output: Bi-direction data - 52                | DDR       |
| AC24        | DDR_DQ_53            | I/O  | Data Input/Output: Bi-direction data - 53                | DDR       |
| AC21        | DDR_DQ_54            | I/O  | Data Input/Output: Bi-direction data - 54                | DDR       |
| AC22        | DDR_DQ_55            | I/O  | Data Input/Output: Bi-direction data - 55                | DDR       |
| Y25         | DDR_DQ_56            | I/O  | Data Input/Output: Bi-direction data - 56                | DDR       |
| AA25        | DDR_DQ_57            | I/O  | Data Input/Output: Bi-direction data - 57                | DDR       |
| AA21        | DDR_DQ_58            | I/O  | Data Input/Output: Bi-direction data - 58                | DDR       |
| AA24        | DDR_DQ_59            | I/O  | Data Input/Output: Bi-direction data - 59                | DDR       |
| AB21        | DDR_DQ_60            | I/O  | Data Input/Output: Bi-direction data - 60                | DDR       |
| AB22        | DDR_DQ_61            | I/O  | Data Input/Output: Bi-direction data - 61                | DDR       |
| AB25        | DDR_DQ_62            | I/O  | Data Input/Output: Bi-direction data - 62                | DDR       |
| AA23        | DDR_DQ_63            | I/O  | Data Input/Output: Bi-direction data - 63                | DDR       |
| AD8         | DDR_DQSN_0           | I/O  | Data Strobe Differential in/output clock -ve signals-0   | DDR       |
| AC8         | DDR_DQSP_0           | I/O  | Data Strobe Differential in/output clock +ve signals - 0 | DDR       |
| AB9         | DDR_DQSN_1           | I/O  | Data Strobe Differential in/output clock -ve signals-1   | DDR       |
| AB10        | DDR_DQSP_1           | I/O  | Data Strobe Differential in/output clock +ve signals - 1 | DDR       |
| AB3         | DDR_DQSN_2           | I/O  | Data Strobe Differential in/output clock -ve signals-2   | DDR       |
| AB4         | DDR_DQSP_2           | I/O  | Data Strobe Differential in/output clock +ve signals - 2 | DDR       |
| AD3         | DDR_DQSN_3           | I/O  | Data Strobe Differential in/output clock -ve signals-3   | DDR       |
| AD2         | DDR_DQSP_3           | I/O  | Data Strobe Differential in/output clock +ve signals - 3 | DDR       |
| AD18        | DDR_DQSN_4           | I/O  | Data Strobe Differential in/output clock -ve signals-4   | DDR       |
| AD17        | DDR_DQSP_4           | I/O  | Data Strobe Differential in/output clock +ve signals - 4 | DDR       |
| AB18        | DDR_DQSN_5           | I/O  | Data Strobe Differential in/output clock -ve signals-5   | DDR       |
| AB17        | DDR_DQSP_5           | I/O  | Data Strobe Differential in/output clock +ve signals - 5 | DDR       |
| AD23        | DDR_DQSN_6           | I/O  | Data Strobe Differential in/output clock -ve signals-6   | DDR       |
| AD24        | DDR_DQSP_6           | I/O  | Data Strobe Differential in/output clock +ve signals - 6 | DDR       |
| AB23        | DDR_DQSN_7           | I/O  | Data Strobe Differential in/output clock -ve signals-7   | DDR       |
| AB24        | DDR_DQSP_7           | I/O  | Data Strobe Differential in/output clock +ve signals - 7 | DDR       |
| Y17         | DDR_PLL_TEST_OUT_N   | OUT  | DDR Differential PLL Test Output Signal (Negative)       | DDR       |
| Y16         | DDR_PLL_TEST_OUT_P   | OUT  | DDR Differential PLL Test Output Signal (Positive)       | DDR       |
| AA13        | DDR_RSTN             | OUT  | DDR Reset active low output Signal. (Active Low)         | DDR       |
| R9          | DATA_RET             | IN   | DDR Data Retention Signal (Active High)                  | DDR       |

## 7.2.2 PCIe interface signal description

Table 5. Ara240 PCIe interface signal description

| Ball number | Ball name | Type | PCIe interface signal description                           | Interface |
|-------------|-----------|------|-------------------------------------------------------------|-----------|
| A1          | P_RXN0    | IN   | PCIe Lane 0 Differential RX input on the negative terminal  | PCIe      |
| B1          | P_RXP0    | IN   | PCIe Lane 0 Differential RX input on the positive terminal  | PCIe      |
| C2          | P_TXN0    | OUT  | PCIe Lane 0 Differential TX output on the negative terminal | PCIe      |
| B2          | P_TXP0    | OUT  | PCIe Lane 0 Differential TX output on the positive terminal | PCIe      |
| D1          | P_RXN1    | IN   | PCIe Lane 1 Differential RX input on the negative terminal  | PCIe      |

Table 5. Ara240 PCIe interface signal description...continued

| Ball number | Ball name     | Type | PCIe interface signal description                           | Interface |
|-------------|---------------|------|-------------------------------------------------------------|-----------|
| E1          | P_RXP1        | IN   | PCIe Lane 1 Differential RX input on the positive terminal  | PCIe      |
| F2          | P_TXN1        | OUT  | PCIe Lane 1 Differential TX output on the negative terminal | PCIe      |
| E2          | P_TXP1        | OUT  | PCIe Lane 1 Differential TX output on the positive terminal | PCIe      |
| G1          | P_RXN2        | IN   | PCIe Lane 2 Differential RX input on the negative terminal  | PCIe      |
| H1          | P_RXP2        | IN   | PCIe Lane 2 Differential RX input on the positive terminal  | PCIe      |
| J2          | P_TXN2        | OUT  | PCIe Lane 2 Differential TX output on the negative terminal | PCIe      |
| H2          | P_TXP2        | OUT  | PCIe Lane 2 Differential TX output on the positive terminal | PCIe      |
| K1          | P_RXN3        | IN   | PCIe Lane 3 Differential RX input on the negative terminal  | PCIe      |
| L1          | P_RXP3        | IN   | PCIe Lane 3 Differential RX input on the positive terminal  | PCIe      |
| M2          | P_TXN3        | OUT  | PCIe Lane 3 Differential TX output on the negative terminal | PCIe      |
| L2          | P_TXP3        | OUT  | PCIe Lane 3 Differential TX output on the positive terminal | PCIe      |
| A3          | PCIE_REFCLK_N | IN   | PCIe Reference Clock Input Differential Pair (negative)     | PCIe      |
| A4          | PCIE_REFCLK_P | IN   | PCIe Reference Clock Input Differential Pair (positive)     | PCIe      |
| N3          | PCIE_PERST#   | IN   | PCIe Reset Signal (Active Low)                              | PCIe      |
| M3          | PCIE_CLKREQ#  | I/OD | PCIe Clock Request (Active Low Signal), Internal PU         | PCIe      |

### 7.2.3 USB interface signal description

Table 6. Ara240 USB interface signal description

| Ball number | Ara240 USB ball name | Type | Ara240 USB interface signal description                                                    | Interface |
|-------------|----------------------|------|--------------------------------------------------------------------------------------------|-----------|
| U2          | SS_RXN1              | IN   | USB3.2 differential Super-Speed and Super-Speed-Plus input on the positive terminal RX1-   | USB       |
| V1          | SS_RXN2              | IN   | USB3.2 differential Super-Speed and Super-Speed-Plus input on the positive terminal RX2-   | USB       |
| U1          | SS_RXP1              | IN   | USB3.2 differential Super-Speed and Super-Speed-Plus input on the positive terminal RX1+   | USB       |
| V2          | SS_RXP2              | IN   | USB3.2 differential Super-Speed and Super-Speed-Plus input on the positive terminal RX2+   | USB       |
| P2          | SS_TXN1              | OUT  | USB3.2 differential Super-Speed and Super-Speed-Plus output on the negative terminal TX1-  | USB       |
| R1          | SS_TXN2              | OUT  | USB3.2 differential Super-Speed and Super-Speed-Plus output on the negative terminal TX2-  | USB       |
| P1          | SS_TXP1              | OUT  | USB3.2 differential Super-Speed and Super-Speed-Plus output on the positive terminal TX1+  | USB       |
| R2          | SS_TXP2              | OUT  | USB3.2 differential Super-Speed and Super-Speed-Plus output on the positive terminal TX2+  | USB       |
| P4          | U_DM                 | I/O  | USB 2.0 and 1.1 High-speed/Full-speed/Low-Speed differential pad on the negative terminal. | USB       |
| R4          | U_DP                 | I/O  | USB 2.0 and 1.1 High-speed/Full-speed/Low-Speed differential pad on the positive terminal. | USB       |

Table 6. Ara240 USB interface signal description...continued

| Ball number | Ara240 USB ball name | Type | Ara240 USB interface signal description                                                                                   | Interface |
|-------------|----------------------|------|---------------------------------------------------------------------------------------------------------------------------|-----------|
| V4          | CC_0                 | I/O  | Configuration Channel (CC0) used in the discovery, configuration, and management of connections across a USB Type-C cable | USB       |
| U4          | CC_1                 | I/O  | Configuration Channel (CC1) used in the discovery, configuration, and management of connections across a USB Type-C cable | USB       |

## 7.2.4 SPI interface signal description

Table 7. Ara240 SPI interface signal description

| Ball number | Ara240 SPI ball name | Type | Ara240 SPI interface signal description | Interface |
|-------------|----------------------|------|-----------------------------------------|-----------|
| B7          | SPI_CEn              | I/O  | SPI Chip Select 0 (Active Low) Signal   | SPI       |
| B8          | SPI_DATA0            | I/O  | SPI Data 0                              | SPI       |
| A6          | SPI_DATA1            | I/O  | SPI Data 1                              | SPI       |
| B6          | SPI_DATA2            | I/O  | SPI Data 2                              | SPI       |
| C7          | SPI_DATA3            | I/O  | SPI Data 3                              | SPI       |
| C5          | SPI_WEn              | I/O  | SPI Single Ended Clock Out Signal 1     | SPI       |

## 7.2.5 GPIO signal description

Table 8. Ara240 GPIO signal description

| Ball number | Pad name | Internal pull-up/down | Default direction | Voltage domain | Functional mode            |                  |                |
|-------------|----------|-----------------------|-------------------|----------------|----------------------------|------------------|----------------|
|             |          |                       |                   |                | TME_0=0, TME_1=0 (Default) |                  |                |
|             |          |                       |                   |                | Default                    | Option           |                |
|             |          |                       |                   |                | GPIO                       | Special function | Direction      |
| G10         | GPIO_00  | PU                    | IN                | VDDIO          | GPIO_00                    | --               | Bi-directional |
| B9          | GPIO_01  | PU                    | IN                | VDDIO          | GPIO_01                    | --               | Bi-directional |
| F10         | GPIO_02  | PU                    | IN                | VDDIO          | GPIO_02                    | UART_RXD         | Input          |
| D9          | GPIO_03  | PU                    | IN                | VDDIO          | GPIO_03                    | UART_CTSn        | Input          |
| A9          | GPIO_04  | PU                    | IN                | VDDIO          | GPIO_04                    | UART_TXD         | Output         |
| D10         | GPIO_05  | PU                    | IN                | VDDIO          | GPIO_05                    | UART_RTSn        | Output         |
| E9          | GPIO_06  | PD                    | IN                | VDDIO          | GPIO_06                    | DDR_DAT_RET      | Input          |
| C9          | GPIO_07  | PU                    | IN                | VDDIO          | GPIO_07                    | I2C_SCL          | Bi-directional |
| E10         | GPIO_08  | PU                    | IN                | VDDIO          | GPIO_08                    | I2C_SDA          | Bi-directional |
| D8          | GPIO_09  | PU                    | IN                | VDDIO          | GPIO_09                    | PIB_TREF         | Output         |
| C10         | GPIO_10  | PU                    | IN                | VDDIO          | GPIO_10                    | TREF_DATA[0]     | Output         |
| B10         | GPIO_11  | PU                    | IN                | VDDIO          | GPIO_11                    | TREF_DATA[1]     | Output         |
| F9          | GPIO_12  | PU                    | IN                | VDDIO          | GPIO_12                    | TREF_DATA[2]     | Output         |
| A10         | GPIO_13  | PU                    | IN                | VDDIO          | GPIO_13                    | TREF_DATA[3]     | Output         |

Table 8. Ara240 GPIO signal description...continued

| Ball number | Pad name | Internal pull-up/down | Default direction | Voltage domain | Functional mode            |                  |           |
|-------------|----------|-----------------------|-------------------|----------------|----------------------------|------------------|-----------|
|             |          |                       |                   |                | TME_0=0, TME_1=0 (Default) |                  |           |
|             |          |                       |                   |                | Default                    | Option           |           |
|             |          |                       |                   |                | GPIO                       | Special function | Direction |
| G11         | GPIO_14  | PU                    | IN                | VDDIO          | GPIO_14                    | TREF_DATA[4]     | Output    |
| E8          | GPIO_15  | PU                    | IN                | VDDIO          | GPIO_15                    | TREF_DATA[5]     | Output    |
| F11         | GPIO_16  | PU                    | IN                | VDDIO          | GPIO_16                    | TREF_DATA[6]     | Output    |
| D11         | GPIO_17  | PU                    | IN                | VDDIO          | GPIO_17                    | TREF_DATA[7]     | Output    |
| G9          | GPIO_18  | PU                    | IN                | VDDIO          | GPIO_18                    | USB_PWR_PREST    | Output    |
| E11         | GPIO_19  | PU                    | IN                | VDDIO          | GPIO_19                    | USB_PHY_REFCLK   | Output    |
| C11         | GPIO_20  | PU                    | IN                | VDDIO          | GPIO_20                    | FRO_CLK          | Output    |
| A11         | GPIO_21  | PU                    | IN                | VDDIO          | GPIO_21                    | FRO_CLK_TEST     | Output    |
| B11         | GPIO_22  | PU                    | IN                | VDDIO          | GPIO_22                    | GPIO_INTR        | Input     |

**Note:**

- *TREF\** pins are processor trace outputs for debug
- *FRO\** pins are ring oscillator clock debug outputs
- *PU* = Internal Pad Pull Up Resistor
- *PD* = Internal Pad Pull Down Resistor
- Nominal Internal Pad Pull-up/Pull-down Resistor Value = 24KOhm
- No external Pull-up/Pull-down is needed for GPIOs

**7.2.6 JTAG interface signal description**

Table 9. Ara240 JTAG interface signal description

| Ball number | Ball name | Dir | Internal pull-up/pull-down | External pull-up/pull-down | JTAG interface signal description | Interface |
|-------------|-----------|-----|----------------------------|----------------------------|-----------------------------------|-----------|
| E7          | JTAG_TCK  | IN  | Pull-up                    | NC                         | JTAG Test Clock Input             | JTAG      |
| F7          | JTAG_TDI  | IN  | Pull-up                    | NC                         | JTAG Test Data In                 | JTAG      |
| G8          | JTAG_TDO  | OUT | Pull-up                    | NC                         | JTAG Test Data Out                | JTAG      |
| F8          | JTAG_TMS  | IN  | Pull-up                    | NC                         | JTAG Test Mode Select             | JTAG      |
| G7          | JTAG_TRST | IN  | Pull-down                  | NC                         | JTAG Test Reset                   | JTAG      |

**7.2.7 Strap selection signals**

Table 10. Ara240 strap selection signals

| Ball number | Ball name | Dir | Internal PU/PD | Voltage domain | Description | External pull-up/pull-down | Function         |
|-------------|-----------|-----|----------------|----------------|-------------|----------------------------|------------------|
| D3          | STRAP0    | IN  | PD             | VDDIO          | Strap 0     | NC                         | Normal Operation |
|             |           |     |                |                |             | Pull-up                    | Undefined        |
| E3          | STRAP1    | IN  | PD             | VDDIO          | Strap 1     | NC                         | Normal Operation |
|             |           |     |                |                |             | Pull-up                    | Undefined        |

Table 10. Ara240 strap selection signals...continued

| Ball number | Ball name    | Dir | Internal PU/PD | Voltage domain | Description        | External pull-up/pull-down | Function                   |
|-------------|--------------|-----|----------------|----------------|--------------------|----------------------------|----------------------------|
| F5          | STRAP2       | IN  | PD             | VDDIO          | Strap 2            | NC                         | Normal Operation           |
|             |              |     |                |                |                    | Pull-up                    | Undefined                  |
| F4          | STRAP3       | IN  | PD             | VDDIO          | Strap 3            | NC                         | Normal Operation           |
|             |              |     |                |                |                    | Pull-up                    | Undefined                  |
| F6          | STRAP4       | IN  | PD             | VDDIO          | Strap 4            | NC                         | Normal Operation           |
|             |              |     |                |                |                    | Pull-up                    | Undefined                  |
| E5          | TME0         | IN  | PD             | VDDIO          | Test Mode Enable 0 | NC                         | Normal Operation           |
|             |              |     |                |                |                    | Pull-up                    | Only for Tester            |
| G5          | TME1         | IN  | PD             | VDDIO          | Test Mode Enable 1 | NC                         | Normal Operation           |
|             |              |     |                |                |                    | Pull-up                    | Only for Tester            |
| D5          | SCAN_EN      | IN  | PU             | VDDIO          | DFT Scan Enable    | Pull-down                  | Normal Operation           |
|             |              |     |                |                |                    | NC                         | Only for Tester            |
| E4          | PCIE_DISABLE | IN  | PU             | VDDIO          | PCIE Disable       | NC                         | PCIE Disable               |
|             |              |     |                |                |                    | Pull-down                  | PCIE Enable                |
| G4          | USB_DISABLE  | IN  | PU             | VDDIO          | USB Disable        | NC                         | USB Disable                |
|             |              |     |                |                |                    | Pull-down                  | USB Enable                 |
| D4          | DDR_DISABLE  | IN  | PU             | VDDIO          | DDR Disable        | NC                         | DDR Disable                |
|             |              |     |                |                |                    | Pull-down                  | DDR Enable                 |
| F3          | CLK_SEL      | IN  | PD             | VDDIO          | Debug Clock Select | NC                         | Crystal clock              |
|             |              |     |                |                |                    | Pull-up                    | Oscillator Clock for debug |
| E6          | JTAG_SEL     | IN  | PD             | VDDIO          | JTAG Disable       | NC                         | JTAG Enable                |
|             |              |     |                |                |                    | Pull-up                    | JTAG Disable               |

**Note:**

- *PU = Internal Pad Pull Up Resistor*
- *PD = Internal Pad Pull Down Resistor*
- *Nominal Internal Pad Pull-up/Pull-down Resistor Value = 79 KOhm*
- *Recommended external Pull-up/Pull-down Resistor Value = 4.7 KOhm*
- *Normal Operation = Default user mode.*

**7.2.8 Ara240 system control signals**

Table 11. Ara240 system control signals

| Ball number | Ball name | Dir | PU/PD | Description                                                     | Interface |
|-------------|-----------|-----|-------|-----------------------------------------------------------------|-----------|
| K3          | XTAL_IN   | IN  |       | Crystal oscillator input <sup>[1]</sup>                         | Clock     |
| L4          | CLK_IN    | IN  |       | Clock input signal from an external oscillator.                 | Clock     |
| J3          | XTAL_OUT  | OUT |       | Crystal oscillator output (leave open or pull up when not used) | Clock     |
| G3          | O_CLKOUT  | OUT |       | System Clock Out                                                | System    |
| G6          | RESET_N   | IN  | PU    | Chip Reset (Active Low)                                         | System    |

Table 11. Ara240 system control signals...continued

| Ball number | Ball name | Dir | PU/PD | Description                  | Interface |
|-------------|-----------|-----|-------|------------------------------|-----------|
| D7          | TESTCLK   | IN  | PD    | Test Mode Clock Input Signal | System    |

[1] 25 MHz crystal is needed as reference clock.

8 Basic architecture

This section provides a device overview including processor architecture, supported features, and functional blocks within the processor, described in [Figure 1](#).

8.1 Processors

This section outlines the processing subsystems, including neural network processors, vector processing units, and control processors.

8.1.1 Neural Network Processor (NNP)

The NNP subsystem consists of eight homogenous processing cores. NNP cores are designed with a specialized instruction set architecture tailored for efficient execution of AI algorithms. This allows Ara240 to execute state-of-the-art high accuracy edge AI models within a very low-power envelope. Moreover, the instruction-set-based design of NNP makes it fully programmable so new AI algorithms can be easily and efficiently implemented on the cores. This contrasts with many competing solutions, which rely on fixed function compute accelerators, and as a result can only accelerate a set of predefined functions.

Examples of neural networks that can be mapped to NNP cores include GenAI models, such as Llama3 8B and Qwen 2.5VL 3B, convolutional neural networks, such as YOLOv8 and ResNet-50, EfficientNet Lite, Vision Transformers such as ViT and Efficient TAM and other workloads, such as LSTMs and RNNs. There is no restriction on the number of parameters. Networks with billions of parameters can be implemented with 3B to 8B LLMs and VLMs being a typical use case. There are also no restrictions on the operator types and number of layers.

8.1.2 Vector Processing Units (VPUs)

Ara240 implements a vector processing cluster consisting of two vector cores (RISC-V architecture with RV64IMACV extensions). Vector length of 512-bits is supported for INT8, INT16, INT32, FP16, and FP32 data formats. The vector cores complement Neural Network Processors and can be used to execute non-neural network tasks such as post-processing functions. The vector processors are not end user programmable and the set of functions executable on the vector cores are limited to the ones packaged as part of Ara SDK.

8.1.3 Management and IO Control Processors (MCP, IOCP)

Ara240 implements two control processors that perform the following functions:

- Communicate with the host processor to handle inference workloads and data movement (MCP).
- Orchestrate inference execution. Control processor receives inference requests from host, schedules inference execution & notifies host once the outputs are available (MCP).
- Error handling or any other management or control functions (MCP).
- xHCI protocol handling when connected to the host via USB interface (IOCP).



### 8.1.4 Secure Boot Processor (SBP)

Ara240 supports secure boot through the secure boot processor (SBP). On power up and after Ara240 hardware reset is de-asserted on Ara240, the SBP initializes the Ara240 chip by going through boot sequences and doing the following tasks:

- Performs tests of internal RAM and ROM.
- Performs basic Ara240 bring-up including programming the PLLs, enabling the host interface(s).
- Loads boot code from the external serial (SPI) flash.

Software continues the process with LPDDR4 configuration.

### 8.1.5 Transfer/scheduler engines

This section explains the hardware engines that manage task scheduling and high-speed data transfers across memory.

#### 8.1.5.1 Task Scheduler Engine (TSE)

The TSE is a hardware accelerated message passing mechanism that implements a set of queues and notification schemes. It is used by processor cores in Ara240 and the host runtime.

#### 8.1.5.2 Surface Traversal Engine (STE)

STE implements several channels and a full crossbar that allows for tensor transfers across various memory subsystems within Ara240 and external LPDDR4. A surface transfer descriptor that describes an input tensor and an output tensor, when presented to a channel, kick starts tensor transfer between two memory subsystems – say, between L1 memory and shared on-chip memory or shared on-chip memory and LPDDR4. All the channels operate concurrently and can fetch or prefetch the descriptors and executing tensor transfers without any CPU intervention.

## 8.2 Memory subsystem

The memory subsystem consists of L1 memory, shared on-chip memory, STE (Surface Traversal Engine) and corresponding configuration registers.

### 8.2.1 Data movement

The Ara240 memory subsystem is a statically allocated subsystem; the scheduling software manages data movement across the memory hierarchy in both directions – bringing data to and from the processor and generates an execution plan or a command stream which is then transferred to TSE.

### 8.2.2 Shared on-chip memory

Shared on-chip memory interfaces with the NNP subsystem through internal buses. Shared on-chip memory also interfaces with the LPDDR4 Memory controller through the LPDDR4 high-speed bus.

### 8.2.3 External memory

Ara240 supports LPDDR4 memory.

- Interface width: 32-bit/64-bit
  - Upto 8 GB of addressable memory space in 32-bit mode
  - Up to 16 GB addressable memory space in 64-bit mode

- LPDDR4 up to 4266 MT/s

### 8.2.3.1 Supported memory configurations

- Single 32-bit LPDDR4 ([Figure 3](#))
  - Maximum bandwidth: 17 GBps
  - Up to 8 GB density
- Single 64-bit LPDDR4 ([Figure 4](#))
  - Maximum bandwidth: 34 GBps
  - Up to 16 GB density
- Two 32-bit LPDDR4 memories ([Figure 5](#))
  - Maximum bandwidth: 34 GB/s
  - Up to 16 GB density

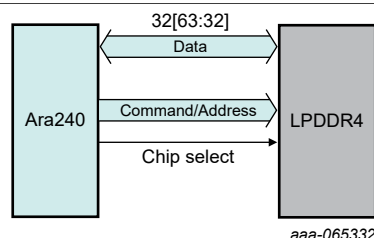


Figure 3. Ara240 with single 32-bit LPDDR4

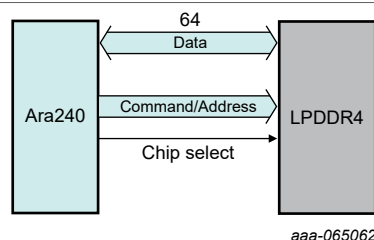


Figure 4. Ara240 with single 64-bit LPDDR4 device

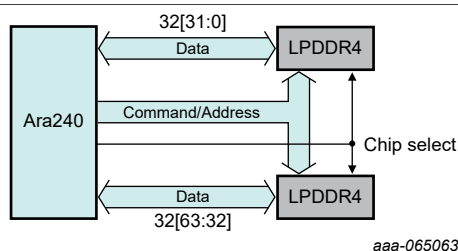


Figure 5. Ara240 with dual 32-bit LPDDR4 devices

## 8.3 Connectivity and I/O

This section describes the available peripheral interfaces and communication subsystems supported by the device.

### 8.3.1 GPIO

The GPIO controller has 23 GPIO pins that are programmed by registers to control very slow peripherals through serial protocols emulated by software.

### 8.3.2 SPI

The SPI (1.8 V) interface is used to connect Ara240 to an external SPI Flash device that stores the Ara240 boot image and firmware. Ara240 supports the following SPI Flash devices:

- Size: 1 MB to 32 MB (4 MB is typical)
- Interface: Single, Dual, Quad

### 8.3.3 Host interfaces

This section details the host communication interfaces, including PCIe and USB configurations.

#### 8.3.3.1 PCIe

The PCIe configuration for Ara240 is as follows:

- Number of Base Address Registers (BARs): 3
  - BAR0, BAR2 and BAR4
- Memory space: 1 MB
- Gen4 (16.0 GT/s) 4-lane Endpoint
- 64-bit address space
- 36-bit outbound

Ara240 implements 3 Base Address Registers (BARs) as shown below:

- BAR0: 16KB, PCIe controller configuration space
- BAR2: 1MB, Ara240 configuration register space
- BAR4: 1MB, Ara240 DRAM memory mapped to the host

BAR2 and BAR4 are resizable.

Ara240 PCIe also supports the following Low Power modes as defined by the PCIe specification:

- Active State Power Management (ASPM)
  - L0s, L1

PCIe Reset and Ara240 Reset should be connected in a specific configuration for proper operation. For more information, refer to [Section 11.1.6](#).

#### 8.3.3.2 USB

##### Basic Feature Lists

- Compatible with USB3.2 Gen 1.0 specifications
- Supports 4 BULK-IN & 4 BULK-OUT endpoints

### 8.4 Real-time Clock (RTC)

The RTC module must be loaded with a proper initialization value after Ara240 is booted from firmware. After that the module tracks the real-time (in seconds) until power off. The RTC clock is derived from the crystal oscillator (25 MHz) and needs to be initialized for every boot by Ara240 software. The RTC includes counters, which maintain the time in seconds. It also generates interrupts based on this time granularity.

One possible use of the RTC is to measure time duration of events within Ara240 irrespective of frequency such as inference time.

## 8.5 Interrupt control

The Ara240 interrupt controller (aka IPCU) aggregates interrupts from various sources within Ara240 and distributes them to all the masters present in Ara240 (CPs/NNPs/Host).

9 Limiting values

This section defines the absolute maximum ratings and stress limits for safe device operation.

9.1 Absolute maximum ratings

T<sub>j</sub> (Junction Temperature) = 125 °C

**Note:** The absolute maximum ratings reflect the stress levels that, if exceeded, will cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating conditions.

9.2 ESD Rating

Table 12. ESD Rating

|     |      |
|-----|------|
| HBM | 2KV  |
| CDM | 500V |

10 Thermal characteristics

This section provides thermal resistance parameters.

10.1 Thermal resistance

Table 13. Thermal resistance

| Theta-JA (°C/W) |       |       | Psi-JT (°C/W) | Theta-JC (°C/W) | Theta-JB (°C/W) |
|-----------------|-------|-------|---------------|-----------------|-----------------|
| 0 m/s           | 1 m/s | 2 m/s |               |                 |                 |
| 11.6            | 9.6   | 8.8   | 0.16          | 0.28            | 2.73            |

11 Electrical characteristics

This section specifies operating conditions, voltage rails, and power information.

11.1 Recommended operating conditions

**Note:** Operating conditions include design team-controlled parameters such as power supply voltage, power distribution impedances, and thermal conditions.

11.1.1 Operating conditions for voltage rails

**Note:** VDD\_0P8 should be tied to VDD\_CORE for optimal operation.

Table 14. Ara240 Voltage Rails

| Rail    | Voltage |         |       | Function                                                                                          |
|---------|---------|---------|-------|---------------------------------------------------------------------------------------------------|
|         | Min     | Typical | Max   |                                                                                                   |
| VDD_0P8 | 0.78V   | 0.80V   | 0.88V | Fixed voltage rail.<br>Feeds Chip Top, Boot processor, SRAM, LPDDR4, PCIe, USB, eFuse, PLLs, IOs. |

Table 14. Ara240 Voltage Rails...continued

| Rail     | Voltage |         |       | Function                                                                                                                           |
|----------|---------|---------|-------|------------------------------------------------------------------------------------------------------------------------------------|
|          | Min     | Typical | Max   |                                                                                                                                    |
| VDD_CORE |         |         |       | Core VDD. Characterized over a wide voltage range for power/perf trade off.<br>Feeds SRAM periphery, and logic of most partitions. |
| VDDQ     | 1.06V   | 1.1V    | 1.17V | LPDDR4 IO Rail                                                                                                                     |
| VDDQX    | 1.06V   | 1.1V    | 1.17V | LPDDR4 IO pre-driver power supply                                                                                                  |
| VDD_1P8  | 1.62V   | 1.8V    | 1.98V | USB, PCIe, GPIOs, PLLs, PVT monitors, eFuse, and so on.                                                                            |
| VDD_1P2  | 1.08V   | 1.2V    | 1.32V | PCIe IO Rail                                                                                                                       |
| VCC_3P3  | 2.97V   | 3.3V    | 3.63V | 3.3V USB Rail                                                                                                                      |

### 11.1.2 Thermal conditions

Table 15. Thermal operating conditions

| Symbol         | Description                                        | Min | Typ | Max | Unit |
|----------------|----------------------------------------------------|-----|-----|-----|------|
| T <sub>j</sub> | Junction temperature<br>—Commercial <sup>[1]</sup> | 0   | -   | 85  | °C   |
| T <sub>a</sub> | Ambient temperature<br>—Commercial                 | 0   | -   | -   | °C   |

[1] T<sub>j</sub> minimum temperature supported at startup where T<sub>j</sub> = T<sub>a</sub>.

### 11.1.3 Power measurement

This section shows the power measurement on the Ara240 chip with different workloads.

#### 11.1.3.1 Ara240 connected to host with PCIe interface, active, and idle

Table 16. Ara240 power measurement

| State of the chip                                                                                                                      | Workload                                             | T <sub>j</sub> (junction temperature) | Typical power (W) |
|----------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------|---------------------------------------|-------------------|
| Idle <ul style="list-style-type: none"> <li>NNP at 25 MHz</li> <li>LPDDR4 at 4266 MT/s</li> <li>System Clock at 25 MHz</li> </ul>      | None                                                 | 40 °C                                 | 2.16              |
| Active <ul style="list-style-type: none"> <li>NNP at 900 MHz</li> <li>LPDDR4 at 4266 MT/s</li> <li>System Clock at 1100 MHz</li> </ul> | YOLOv8n (nominal performance)                        | 40 °C                                 | 6.5               |
|                                                                                                                                        | YOLOv8n (maximum performance)                        |                                       | 7.88              |
|                                                                                                                                        | YOLOv8l (heavy workload running at max. performance) |                                       | 8.52              |

11.1.4 Power rails description

Table 17. Ara240 power rails description

| Ball number                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Ball name       | Description                           | Interface |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|---------------------------------------|-----------|
| A12, A14, A16, B13, B15, B17, C12, C14, C16, D13, D15, D17, E12, E14, E16, F13, F15, F17, G12, G14, G16, H13, H15, H17                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | VDD_0P8         | Fixed 0V8 Power Supply                | Core      |
| A18, A20, A22, A24, B19, B21, B23, B25, C18, C20, C22, C24, D19, D21, D23, D25, E18, E20, E22, E24, F19, F21, F23, F25, G18, G20, G22, G24, H19, H21, H23, H25, J16, J18, J20, J22, J24, K15, K17, K19, K21, K23, K25, L16, L18, L20, L22, L24, M15, M17, M19, M21, M23, M25, N16, N18, N20, N22, N24, P15, P17, P19, P21, P23, P25, R16, R18, R20, R22, R24, T15, T17, T19, T21, T23, T25, U16, U18, U20, U22, U24, V15, V17, V19, V21, V23, W16, W18, W20, W22                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | VDD_CORE        | Core Power Supply                     | Core      |
| A2, A13, A15, A17, A19, A21, A23, A25, B12, B14, B16, B18, B20, B22, B24, C1, C13, C15, C17, C19, C21, C23, C25, D2, D12, D14, D16, D18, D20, D22, D24, E13, E15, E17, E19, E21, E23, E25, F1, F12, F14, F16, F18, F20, F22, F24, G2, G13, G15, G17, G19, G21, G23, G25, H6, H10, H12, H14, H16, H18, H20, H22, H24, J1, J5, J9, J11, J13, J15, J17, J19, J21, J23, J25, K2, K4, K6, K8, K10, K12, K16, K18, K20, K22, K24, L3, L13, L15, L17, L19, L21, L23, L25, M1, M4, M12, M14, M16, M18, M20, M22, M24, N1, N2, N5, N13, N15, N17, N19, N21, N23, N25, P3, P6, P8, P10, P12, P14, P16, P18, P20, P22, P24, R3, R5, R7, R11, R13, R15, R17, R19, R21, R23, R25, T1, T2, T3, T4, T6, T8, T10, T12, T14, T16, T18, T20, T22, T24, U3, U7, U9, U11, U13, U15, U17, U19, U21, U23, U25, V3, V6, V8, V10, V12, V14, V16, V18, V20, V22, W1, W2, W3, W4, W7, W9, W11, W13, W15, W17, W19, W21, W24, Y18, Y23, AA20, AE1, AE3, AE5, AE7, AE9, AE11, AE13, AE15, AE17, AE19, AE21, AE23, AE25 | VSS             | Core Power Ground                     | Core      |
| M13, M5, N12, N14, P11, P13, P5, P7, P9, R10, R12, R14, R6, R8, T11, T13, T7, T9, U10, U12, U14, U6, U8, V13, V7, W14, W8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | VDD_DDR         | DDR Core Power Supply                 | DDR       |
| V9                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | VDDPLL_MCB1     | PLL MCB1 Power Supply                 | DDR       |
| W12                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VDDPLL_MCB2     | PLL MCB2 Power Supply                 | DDR       |
| V11                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VDDPLL_TOP      | PLL TOP Power Supply                  | DDR       |
| AE10, AE12, AE14, AE16, AE18, AE2, AE20, AE22, AE24, AE4, AE6, AE8, W23, W25, Y22, Y24                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | VDDQ            | DDR IO Power Supply                   | DDR       |
| W10                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VDDQCK          | DDR Clock IO Power Supply             | DDR       |
| T5, U5, V5, W5, W6                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | VDDQX           | DDR IO Pre-driver Power Supply        | DDR       |
| H11                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VQPS18_FUSE_CPC | CPC Fuse Burn Power Supply            | Fuse      |
| N4                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | VQPS18_FUSE_DVC | DVC Fuse Burn Power Supply            | Fuse      |
| J12, J14, K13, L12                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | VDDIO           | IO Power Supply                       | GPIO      |
| H4, H8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | VCC12A_PCIE_CMN | PCIe PHY CMN 1.2V Analog Power Supply | PCIe      |
| H3, H5                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | VCC12A_PCIE_RX  | PCIe PHY RX 1.2V Analog Power Supply  | PCIe      |
| H7, H9                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | VCC12A_PCIE_TX  | PCIe PHY TX 1.2V Analog Power Supply  | PCIe      |
| J4, K5                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | VCC18A_PCIE     | PCIe PHY 1.8V Analog Power Supply     | PCIe      |
| J8, J10, K9, K11                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | VDD08_PCIE      | PCIe 0.8V Digital Power Supply        | PCIe      |
| M9                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | VDD18A_PLL0     | PLL0 Analog Power Supply              | PLL0      |
| M8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | VDD18A_PLL1     | PLL1 Analog Power Supply              | PLL1      |
| M7                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | VDD18A_PLL2     | PLL2 Analog Power Supply              | PLL2      |
| M6                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | VDD18A_PLL3     | PLL3 Analog Power Supply              | PLL3      |
| N9                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | VSSA_PLL0       | PLL0 Analog Power Ground              | PLL0      |
| N8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | VSSA_PLL1       | PLL1 Analog Power Ground              | PLL1      |
| N7                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | VSSA_PLL2       | PLL2 Analog Power Ground              | PLL2      |
| N6                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | VSSA_PLL3       | PLL3 Analog Power Ground              | PLL3      |
| L10                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VDD18A_PVT_DDR  | PVT DDR Analog Power Supply           | PVT       |
| L14                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VDD18A_PVT_PCIE | PVT PCIe Analog Power Supply          | PVT       |
| V25                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VDD18A_PVT_VPC  | VPC PVT Analog Power Supply           | PVT       |
| V24                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VSSA_PVT_VPC    | VPC PVT Analog Power Ground           | PVT       |
| L11                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VSSA_PVT_DDR    | PVT DDR Analog Power Ground           | PVT       |
| K14                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VSSA_PVT_PCIE   | PVT PCIe Analog Power Ground          | PVT       |
| L5, L7                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | GND08A_USB      | USB PHY Analog Power Ground           | USB       |
| J7                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | GND18A_USB      | USB PHY Analog Power Ground           | USB       |
| K7                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | VCC08A_USB      | USB PHY 0.8V Analog Power Supply      | USB       |
| L9                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | VCC18A_USB      | USB PHY 1.8V Analog Power Supply      | USB       |
| L6, L8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | VDD08_USB       | USB 0.8V Digital Power Supply         | USB       |

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Table 17. Ara240 power rails description...continued

| Ball number | Ball name     | Description                      | Interface |
|-------------|---------------|----------------------------------|-----------|
| J6          | VDD33A_USBPHY | USB PHY 3.3V Analog Power Supply | USB       |
| N10         | VDD18A_XTAL   | Crystal Analog Power Supply      | XTAL      |
| M10         | VSSA_XTAL     | Crystal Analog Power Ground      | XTAL      |

## 11.1.5 Power tree

The recommended power tree configuration is as below:

Table 18. Ara240 power tree

| Input  | Regulator | Supply rail | Filter | Supply name          | Volt | Domain | Supply type                          | Ball name       |
|--------|-----------|-------------|--------|----------------------|------|--------|--------------------------------------|-----------------|
| 3.3/5V | BUCK-1    | 0.8         | --     | 0V8_Core             | 0.8  | Core   | Core Power Supply                    | VDD_CORE        |
|        |           |             | --     | 0V8_FIX              | 0.8  | Core   | Fixed 0V8 Power Supply               | VDD_0P8         |
|        |           |             | FB     | VDD_DDR08            | 0.8  | DDR    | DDR Core Power Supply                | VDD_DDR         |
|        |           |             | FB     | DDR_VDDPLL_MCB_TOP08 | 0.8  | DDR    | PLL MCB1 Power Supply                | VDDPLL_MCB1     |
|        |           |             |        |                      | 0.8  | DDR    | PLL MCB2 Power Supply                | VDDPLL_MCB2     |
|        |           |             |        |                      | 0.8  | DDR    | PLL TOP Power Supply                 | VDDPLL_TOP      |
|        |           |             | FB     | VDD08_PCIE           | 0.8  | PCIe   | PCIe 0.8V Digital Power Supply       | VDD08_PCIE      |
|        |           |             | FB     | VDD08_USBCORE        | 0.8  | USB    | USB PHY 0.8V Digital Power Supply    | VCC08A_USB      |
|        | BUCK-2    | 1.1         | FB     | VCC08A_USBPHY        | 0.8  | USB    | USB 0.8V Analog Power Supply         | VDD08_USB       |
|        |           |             | --     | DDR_VDDQ11           | 1.1  | DDR    | DDR IO Power Supply                  | VDDQ            |
|        |           |             | --     | DDR_VDDQCK11         | 1.1  | DDR    | DDR Clock IO Power Supply            | VDDQCK          |
|        |           |             | --     | DDR_VDDQX11          | 1.1  | DDR    | DDR IO Pre-driver Power Supply       | VDDQX           |
|        | BUCK/LDO  | 1.2         | FB     | VCC12A_PCIE_TXRX     | 1.2  | PCIe   | PCIe PHY RX 1.2V Analog Power Supply | VCC12A_PCIE_RX  |
|        |           |             |        |                      | 1.2  | PCIe   | PCIe PHY TX 1.2V Analog Power Supply | VCC12A_PCIE_TX  |
|        | BUCK-3    | 1.8         | --     | VCC18A_USBPHY        | 1.8  | USB    | USB PHY 1.8V Analog Power Supply     | VCC18A_USB      |
|        |           |             | --     | VCC18A_PCIE          | 1.8  | PCIe   | PCIe PHY 1.8V Analog Power Supply    | VCC18A_PCIE     |
|        |           |             | FB     | VDD18A_PVT           | 1.8  | PVT    | VPC PVT Analog Power Supply          | VDD18A_PVT_VPC  |
|        |           |             | FB     |                      | 1.8  | PVT    | PVT DDR Analog Power Supply          | VDD18A_PVT_DDR  |
|        |           |             | FB     |                      | 1.8  | PVT    | PVT PCIe Analog Power Supply         | VDD18A_PVT_PCIE |



Table 18. Ara240 power tree...continued

| Input | Regulator | Supply rail | Filter | Supply name   | Volt | Domain | Supply type                      | Ball name       |
|-------|-----------|-------------|--------|---------------|------|--------|----------------------------------|-----------------|
|       |           |             | FB     | VDD18A_PLL    | 1.8  | PLL0   | PLL0 Analog Power Supply         | VDD18A_PLL0     |
|       |           |             | FB     |               | 1.8  | PLL1   | PLL1 Analog Power Supply         | VDD18A_PLL1     |
|       |           |             | FB     |               | 1.8  | PLL2   | PLL2 Analog Power Supply         | VDD18A_PLL2     |
|       |           |             | FB     |               | 1.8  | PLL3   | PLL3 Analog Power Supply         | VDD18A_PLL3     |
|       |           |             | FB     |               | 1.8  | XTAL   | Crystal Analog Power Supply      | VDD18A_XTAL     |
|       |           |             | --     | FUSE_VQPS_18  | 1.8  | Fuse   | CPC Fuse Burn Power Supply       | VQPS18_FUSE_CPC |
|       |           |             |        |               | 1.8  | Fuse   | DVC Fuse Burn Power Supply       | VQPS18_FUSE_DVC |
|       |           |             | --     | VDDIO_18      | 1.8  | GPIO   | IO Power Supply                  | VDDIO           |
|       | BUCK/LDO  | 3.3         | --     | VCC33A_USBPHY | 3.3  | USB    | USB PHY 3.3V Analog Power Supply | VDD33A_USBPHY   |
|       |           |             |        |               |      |        |                                  |                 |

### 11.1.6 Power-on sequence and resets

For more information about the Ara240 power-on sequence requirement and reset architecture, refer to the *Ara240 Hardware Design Guide* (document [UG10411](#)).

### 11.1.7 Power islands

Each of the following interfaces have separate power islands and can be power gated:

1. PCIe
2. DDR
3. USB

## 12 Application information

This section presents example use cases for the device.

### 12.1 System solution example

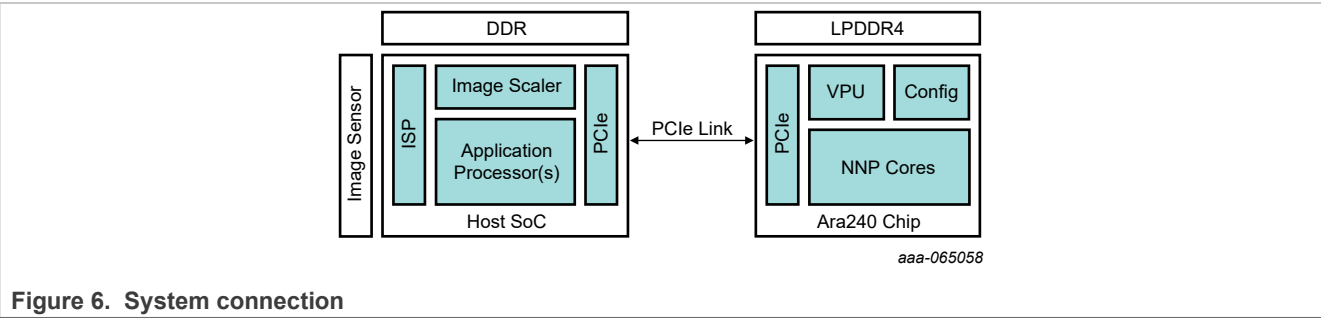


Figure 6. System connection

### 12.2 System overview

This section provides details on the system-level integration of Ara240 Discrete NPU.

#### 12.2.1 System modes

This section provides all the system connectivity modes supported by the Ara240. An external Host is required to boot, program, and control the Ara240.

##### 12.2.1.1 Edge appliance

In this mode, multiple Ara240 devices connect to the Host SoC over PCIe and/or USB (using a USB hub if needed).

**Note:** A PCIe switch may be needed to connect the host with multiple Ara240s if the host does not support PCIe bifurcation.

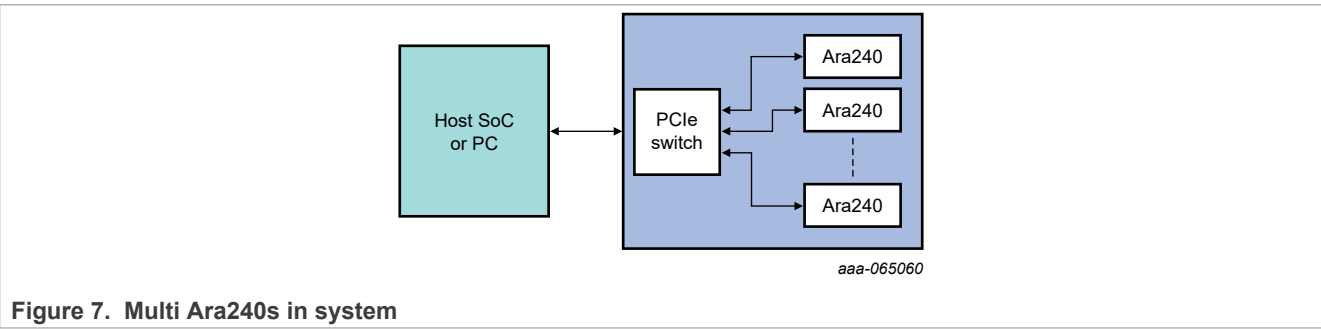
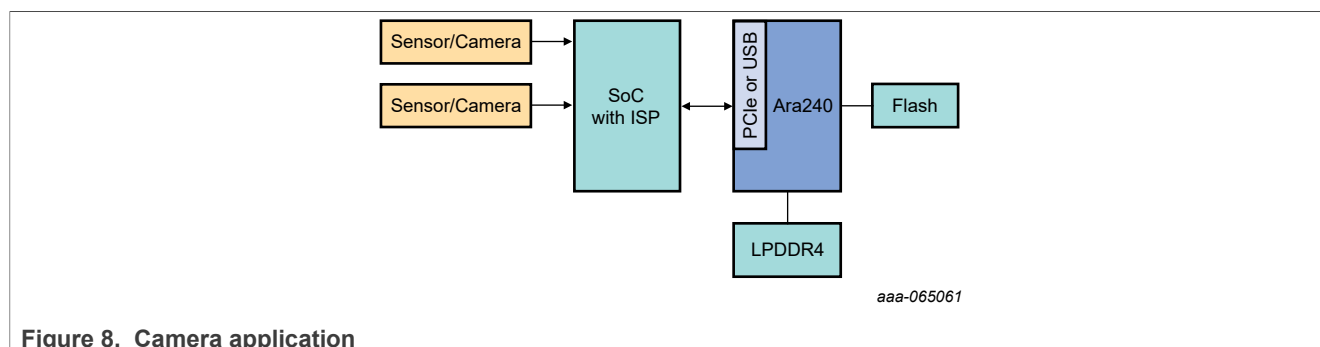


Figure 7. Multi Ara240s in system

#### 12.2.1.2 Embedded device or camera

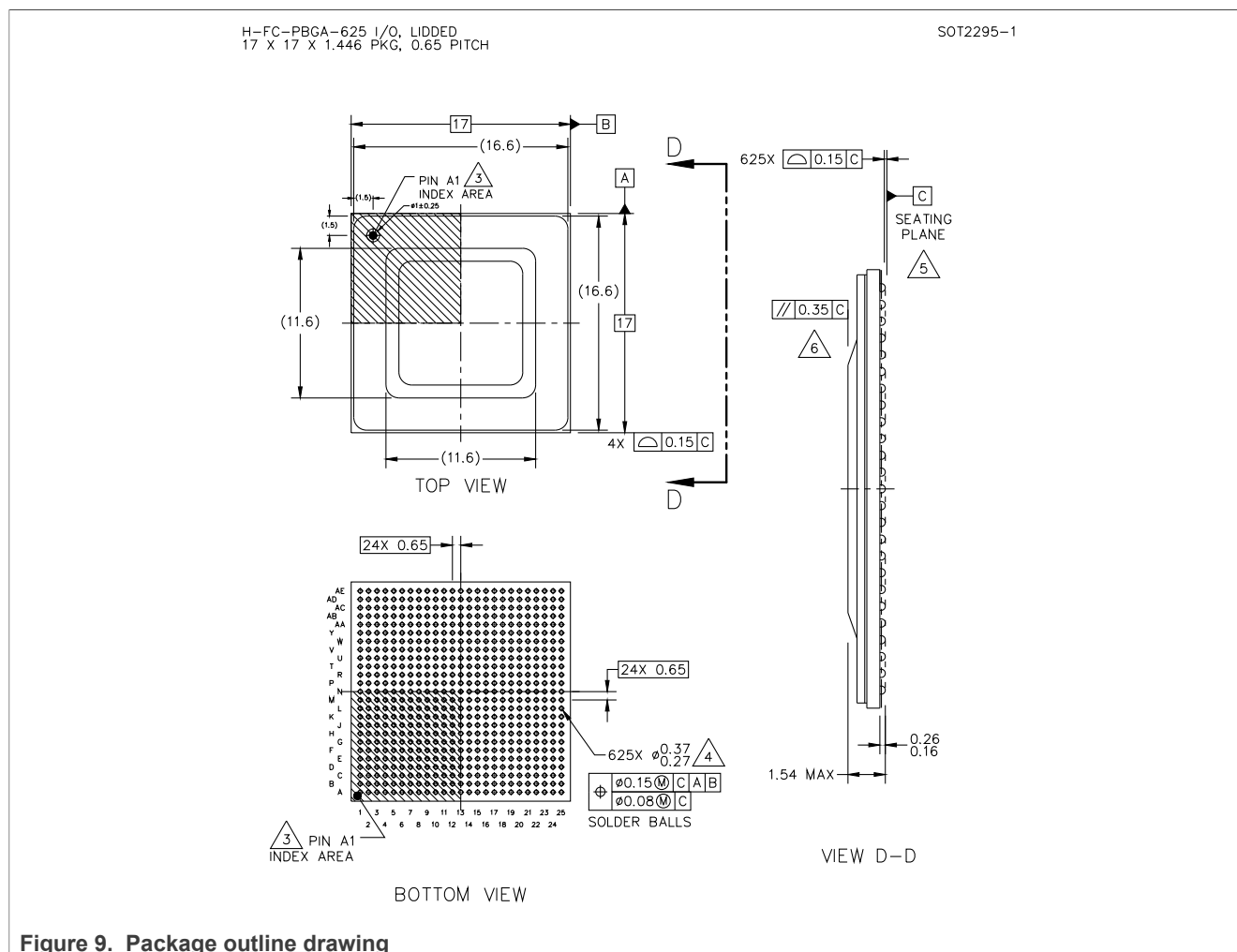


### Figure 8. Camera application

## 13 Package information

Ara240 is offered in a 17 mm x 17 mm EHS-FCBGA package with 0.65 mm pitch for pinout.

## 14 Package outline



**Figure 9. Package outline drawing**

## 15 Moisture Sensitivity Level (MSL)

The shipping process for Ara240 includes handling and dry packing of the product in accordance with the following standards:

- IPC/JEDEC J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface mount devices: Classifies devices that are sensitive to moisture-induced stress.
- IPC/JEDEC J-STD-033, Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount devices: Provides standardized methods for handling, packing, shipping, and use of moisture/reflow sensitive SMD packages to avoid damage and provide a minimum shelf life.

Ara240 is classified as Moisture Sensitivity Level (MSL) 3, defined as 168 hours out-of-bag floor life and  $\leq 30\text{ }^{\circ}\text{C}$  and 60 % relative humidity (RH).

## 16 Reflow profile

Reflow profile classification.

**Table 19. Reflow profile**

| Profile feature                                                                       | Pb free          |
|---------------------------------------------------------------------------------------|------------------|
| Preheat / Soak                                                                        | 150 °C           |
| Temperature min (T <sub>smin</sub> )                                                  | 200 °C           |
| Temperature max (T <sub>smax</sub> )                                                  | 60-120 sec       |
| Time (ts) from T <sub>smin</sub> to T <sub>smax</sub>                                 |                  |
| Ramp-up rate (TL to Tp)                                                               | 3 °C/second max. |
| Liquidous temperature (TL)                                                            | 217 °C           |
| Time (tL) maintained above TL                                                         | 60 ~ 150 seconds |
| Peak package body temperature (Tp)                                                    | 260 °C           |
| Time (tp) <sup>[1]</sup> within 5 °C of the specified classification temperature (Tc) | 30* seconds      |
| Ramp-down rate (Tp to TL)                                                             | 6 °C/second max  |
| Time 25 °C to peak temperature                                                        | 8 minutes max    |

[1] Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.

### Note:

1. All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (for example, live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (that is, dead-bug), Tp shall be within  $\pm 2\text{ }^{\circ}\text{C}$  of the live-bug Tp and still meet the Tc requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures, refer to JEP140 for recommended thermocouple use.
2. Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in [Table 19](#).  
For example, if Tc is 260 °C and time tp is 30 seconds, this means the following for the supplier and the user.  
For a user: The peak temperature must not exceed 260 °C. The time above 255 °C must not exceed 30 seconds.  
For a supplier: The peak temperature must be at least 260 °C. The time above 255 °C must be at least 30 seconds.
3. All components in the test load shall meet the classification profile requirements.

Figure 11 shows a sample reflow profile for a green package. To achieve optimum reflow, the profile values for your design may need to be adjusted.

Classification Profile

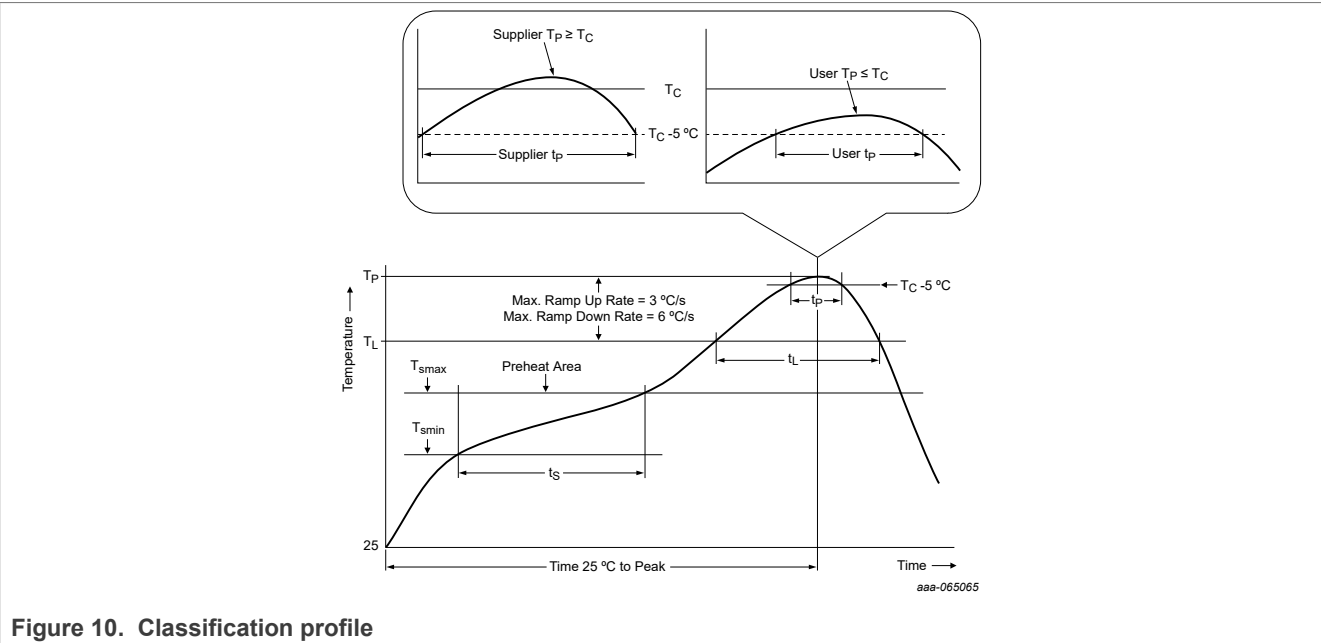


Figure 10. Classification profile

17 Packing information

This section describes packaging details (tray information).

17.1 Package tray information

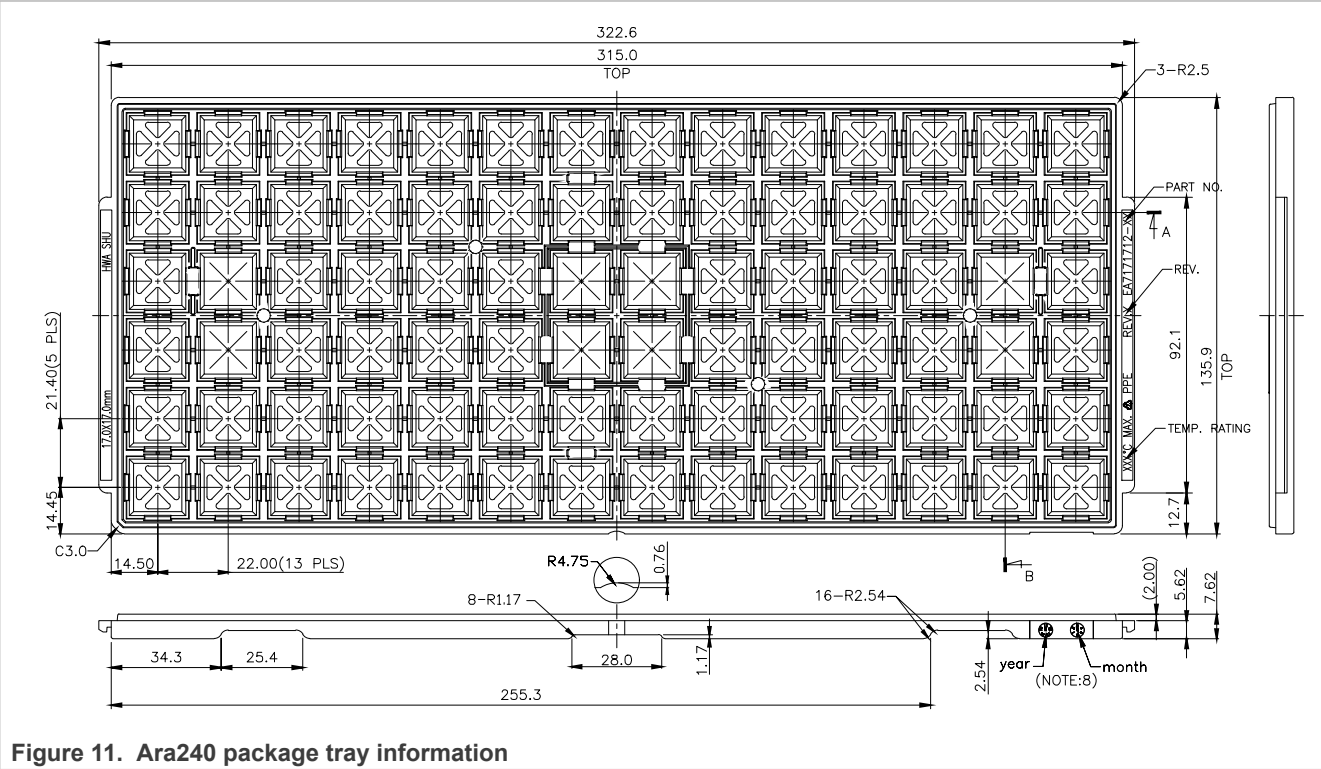


Figure 11. Ara240 package tray information

18 Abbreviations

Table 20. Abbreviations

| Abbreviation | Description                                                         |
|--------------|---------------------------------------------------------------------|
| DNPU         | Discrete Neural Processing Unit                                     |
| CP           | Control Processor                                                   |
| NNP          | Neural Network Processor                                            |
| VPU          | Vector Processing Unit                                              |
| TSE          | Task Scheduler Engine                                               |
| CAR          | Clock and Reset                                                     |
| STE          | Surface Traversal Engine to transfer data between memory subsystems |
| SBP          | Secure Boot Processor                                               |

19 Revision history

[Section 19](#) summarizes revisions to this document.

Table 21. Revision history

| Document ID     | Release date     | Description                                                             |
|-----------------|------------------|-------------------------------------------------------------------------|
| ARA240COM v.3.0 | 3 July 2026      | Updated <a href="#">Section 11.1.6 "Power-on sequence and resets"</a> . |
| ARA240COM v.2.0 | 2 April 2026     | Initial public release                                                  |
| ARA240COM v.1.0 | 20 February 2026 | Initial NDA release                                                     |

## Legal information

### Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition                                                                            |
|-----------------------------------|-------------------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <https://www.nxp.com>.

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