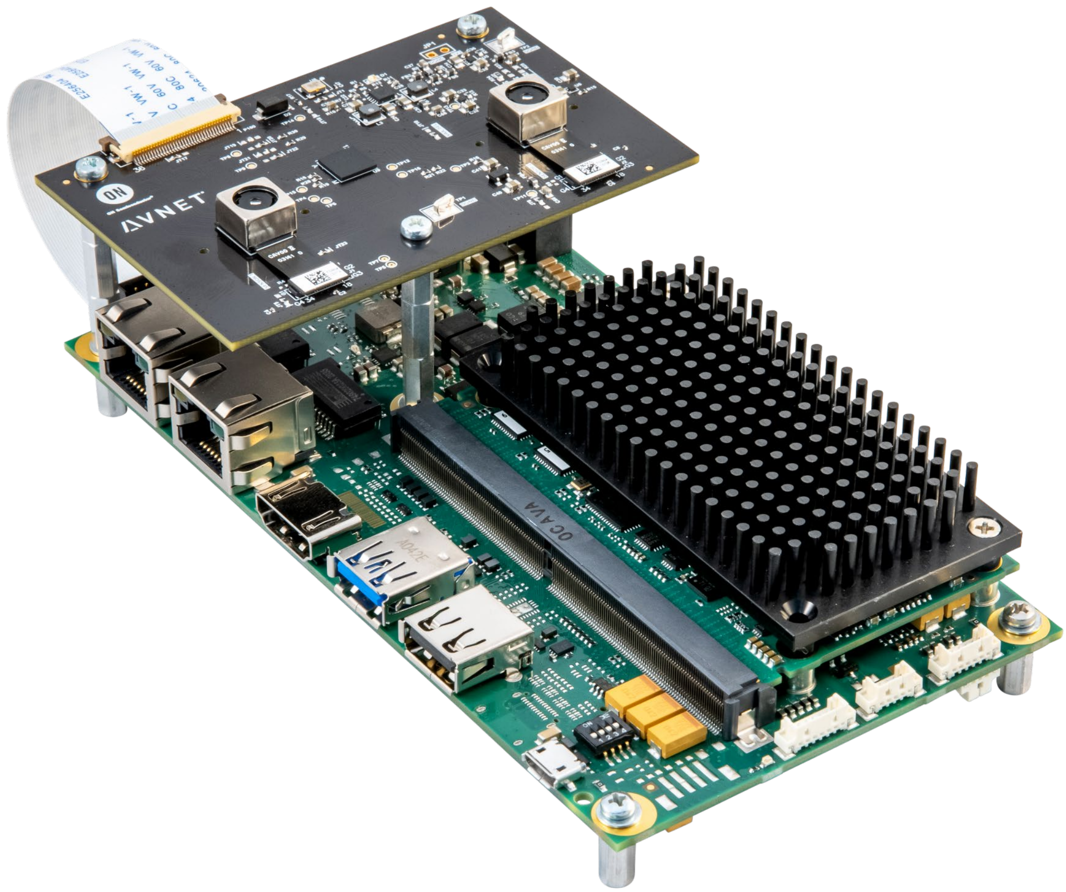


# i.MX 8M Plus Edge AI Kit

# Hardware User's Guide

**Version 1.5**



LIT# i.MX_8M_Plus_Edge_AI_Kit-HW-User-Guide-v1.5

# Contents

## Figures



AVNET®
Reach Further™

## Tables



# 1 Document Control

**Document Version:** 1.5

**Document Date:** 8 July 2022

# 2 Version History

| Version | Date | Comment |
|---|---|---|
| 1.0 | 09 Apr 2021 | Initial Release. |
| 1.1 | 11 Nov 2021 | Update to latest kit photos and add instructions on where to obtain additional hardware documentation and source code from Avnet Embedded site. |
| 1.2 | 03 Dec 2021 | Add terminology, kit contents, component user guides, and functional descriptions. |
| 1.3 | 26 May 2022 | Add dimensions for on semi camera adapter. Add details about GPU and NPU. Fix PDF name in properties. |
| 1.4 | 14 June 2022 | Add link to Hackster getting started project. Remove links to MSC support. Reorder Table 3 to reflect the order of the following sections that describe them. Add section for display. Change On Semiconductor to onsemi. |
| 1.5 | 8 July 2022 | Incorporate tables from MSC guides. Add section for I2S Audio, M.2, CAN, RS-232 and feature connectors. Add table of figures and table of tables. |

# 3 Introduction

The i.MX 8M Plus Edge AI Kit is a fully integrated Embedded Computing development platform based upon the SMARC specification targeted for broad use in many applications:

- Offer an NXP-based, Embedded Computing platform supported over Industrial (-40ºC to +85ºC) temperature grades for engineers to adopt in development, proof-of-concept, and production projects
- Combine ARM processing with neural network acceleration in a convenient and expandable hardware format
- Showcase a wide range of potential peripherals that are not available from other SMARC offerings
- Be a fully enabled development kit for machine learning developers targeting Edge AI applications
- Showcase hardware acceleration for machine learning bottlenecks found on traditional processing platforms
- Allow expansion to a variety of sensors and peripherals through the EP5 SMARC Carrier
- Target many applications for development, including:
    - Artificial Intelligence
    - Machine Learning
    - IoT/Cloud connectivity for add-on sensors
    - Industrial Embedded and Networked Computing
    - Point of Sale and Digital Signage in Retail
- When combining this development kit with the NXP eIQ Machine Learning Software Development Environment, many options for Inference Engines, Vision Libraries, and ML workflow can be used to quickly deploy applications needing the following types of model capabilities:
    - Classification
    - Object Detection
    - Face Recognition
    - Sequence Analysis

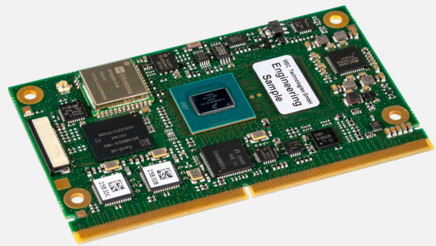
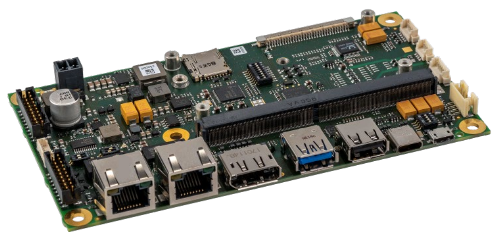
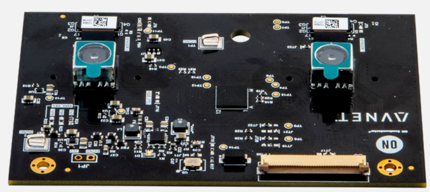
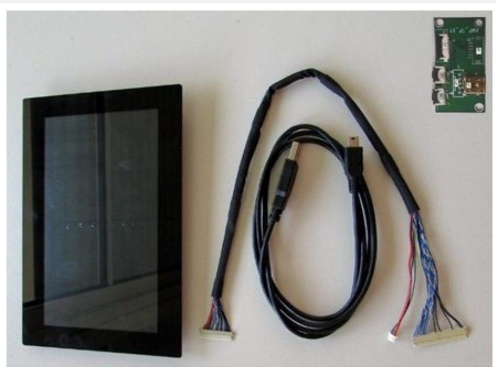
## 3.1 Terminology

| Term | Definition |
|---|---|
| IAS | Imager Access System - Imaging interface standard |
| ISP | Image Signal Processor – Processing engine used for image processing, in digital cameras or other devices. Typically provides Bayer pattern transformation, de-mosaicing, noise reduction, and image sharpening capabilities for raw CMOS image sensors. |
| NPU | Neural Processing Unit - Specialized circuit that implements all the necessary control and arithmetic logic necessary to execute machine learning algorithms, typically by operating on predictive models such as artificial neural networks (ANNs) or random forests (RFs). NPUs sometimes go by similar names such as a tensor processing unit (TPU), neural network processor (NNP) and intelligence processing unit (IPU) as well as vision processing unit (VPU) and graph processing unit (GPU). |
| SMARC | Smart Mobility ARChitecture - Small form factor computer SOM definition targeting applications that require low power, low costs, and high performance. SMARC SOM modules are used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, boot flash, power sequencing, CPU power supplies, GBE and a single channel LVDS display transmitter are concentrated on the Module. |
| SOM | System On Module - Board-level circuit that integrates a system function in a single module. It may integrate digital and analog functions on a single board. A typical application is in the area of embedded systems. |

## 3.2 Kit Contents

**Note:** In addition to the following items, you will need an 8GB - 64GB microSD card. For serial debugging you will need a D-SUB 9-pin female/female “null-modem” (Tx/Rx crossed) cable (not provided).

**Figure 1 - Kit Contents**

| Part name & accessories | Picture | More info |
| --- | --- | --- |
| Avnet i.MX 8M Plus SMARC SOM<br>• SMARC passive heatsink & mounting screws |  | NXP i.MX 8M Plus Overview<br>SMARC module standard<br><br>See section 5.1 |
| Avnet EP5 SMARC Carrier<br>• SMARC Cable kit:<br>o RS-232 breakout cable<br>o 2pin Würth WR-TBL connector Power connector |  | See section 5.2 |
| Dual  Camera Adapter<br>• Mounting hardware for Dual  Camera Adapter Midas FFC Cable |  | onsemi AR1335 IAS Module<br>onsemi AP1302 Image Signal Processor<br>Rapyrus Camera Module<br><br>See section 5.3 |
| 10.1 Inch Touch Display<br>• LVDS and backlight cable<br>• PCAP Touch Controller<br>• USB Cable |  | See section 5.4 |
| 12V Power Supply and adapter |  | Netzteil 12VDC/3.34A 3%<br>90-264VAC |

| Part name & accessories | Picture | More info |
|---|---|---|
| Cable Kit for SMARC 2.0 SimpleFlex Platform EP5<br>• Power Cable<br>• Feature Connector Cable 1 (USB)<br>• Feature Connector Cables 2<br>• Serial Connector Cable RS485 / RS232<br>• Serial Connector Cable CAN / RS485<br>• Audio Connector Cable<br>• Speaker Out Cables 1, 2 |  | Order No. 1152416<br><br>MSC CAB-SM2S-MB-EP5-KIT-001 |

**Table 1 - Kit Contents**

## 3.3 Reference Documents

[1] NXP i.MX 8M Plus Overview

[2] SMARC Specification

[3] Onsemi AR1335 IAS Module

[4] Onsemi AP1302 Image Signal Processor

[5] Rapyrus Camera Module

# 4 i.MX 8M Plus Edge AI Kit Architecture and Features

This section summarizes the features of the embedded computing platform, followed by functional descriptions of each circuit.

## 4.1 List of Features

The i.MX 8M Plus Edge AI Kit supports the following features:

**Hardware Features**

- Machine Learning Accelerator (2.25 TOPS)
- Image Sensor Processor 12MP@30fps
- Quad Core Arm Cortex-A53 ARM Applications Processor
- Arm Cortex-M7 Real-Time Processor
- GC7000UL 2D/3D Graphics Processor with OpenCL and Vulcan Support
- Hifi4 Audio DSP
- 4GB LPDDR4 Memory (inline ECC)
- 16GB eMMC 5.1 Flash Storage
- 64Kbit EEPROM for module information and user applications
- Two onsemi AR1335 IAS Camera Modules
- Onsemi AP1302 ISP

- Real-time clock: high accuracy RTC

**Communication Interfaces**

- Audio: $I^2S$ audio codec with 1W Mono amplifier
- Ethernet: 2x Gigabit Ethernet (IEEE 1588, 1x with TSN)
- USB:
  - 1x USB 3.0, 1x USB 2.0 Type A ports
  - Additional USB 2.0 interface available on MiniPCIe slot
  - Additional USB 3.0 port available on Feature Connector (cabled included)
- Video / Display:
  - Dual Channel LVDS 18-bit/24-bit (1920x1080p max.) or 2x Single Channel LVDS (1366x768p max.)
  - HDMI 2.0a up to 4K (3840x2160@30FPS)
- Camera: MIPI CSI-2 Camera interface with FFC connector (with GPIO and $I^2C$)
- CAN:
  - 1 CAN 2.0B bus on Molex Picoblade (1Mbps)
  - 1 CAN bus on Feature Connector
- UART:
  - 1x RS232 UART on Molex Picoblade (R232 cable included)
  - 2x UART without RTS/CTS support on Feature Connector
- SPI: 2x SPI buses on Feature Connector
- MicroSD Socket: 1x 1bit/4bit SD/SDIO/MMC Interface with power control

**General Specifications**

- SMARC 2.1 compliant
- 146mm x 80mm Form Factor
- -40C to +85C Industrial Temperature Rated
- 5 to 95% humidity rated
- Yocto Linux BSP available for download

## 4.2 i.MX 8M Plus Edge AI Kit Block Diagram

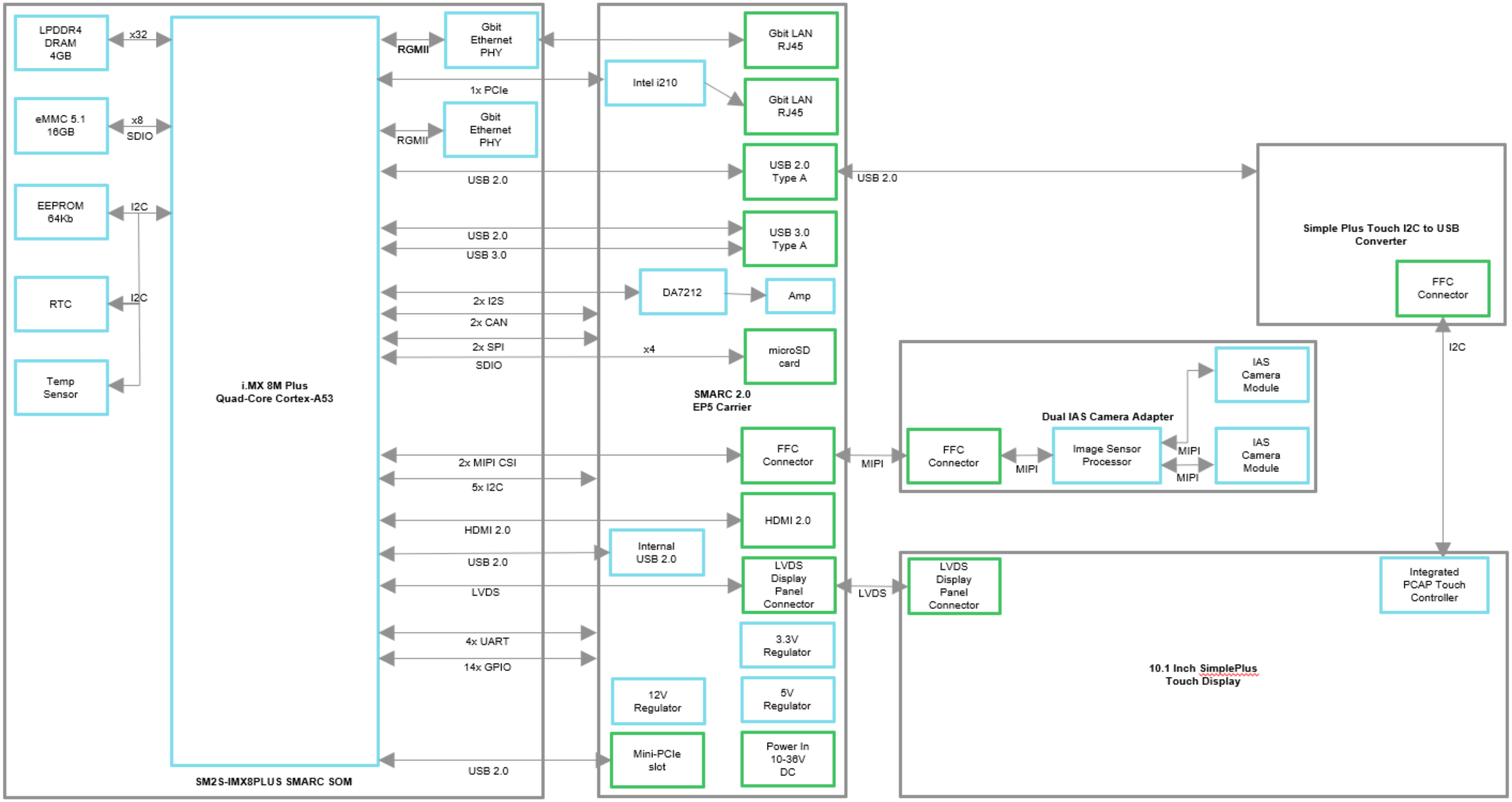



**Figure 2 - i.MX 8M Plus Edge AI Kit Block Diagram**

# 5 Functional Description
The following sections provide brief descriptions of each feature provided on the i.MX 8M Plus Edge AI Kit.

## 5.1 Processor
This section describes the processor architecture of the Avnet i.MX 8M Plus SMARC SOM.
Please see the *i.MX 8M Plus Applications Processor Reference Manual* from NXP for complete descriptions of the NXP processor components.

### 5.1.1 SoC Overview

| Description | i.MX8M Plus Quad-Core |
|---|---|
| Number of A53 Cores | 4 |
| A53 Core Speed | 1.6 GHz |
| NPU | ✓ |
| VPU | ✓ |
| ISP | ✓ |
| HiFi4 DSP | ✓ |
| Qualification | Industrial |
| Junction Temperature | -40°C to +105°C |

### 5.1.2 NPU (Machine Learning Accelerator)
The I.MX8M Plus SMARC SOM features a Neural Processing Unit (NPU) from VeriSilicon, also referred to as the Machine Learning Accelerator. It works in concert with the Cortex-M, Cortex-A, SRAM and flash to greatly accelerate machine learning. It delivers up to 2.3 TOPS.

### 5.1.3 Image Sensor Processor
The Edge AI Kit features two separate Image Sensor Processors: one is integrated in the I.MX8M Plus SOM, and the other is on SMARC Dual Camera Adapter.

#### *5.1.3.1 I.MX8M Plus Onboard ISP*
The I.MX8M Plus includes an onboard image sensor processor. This 375 Mpixel/s HDR ISP supports many configurations, such as 12MP@30fps, 4kp45, or 2x 1080p80.

#### *5.1.3.2 onsemi AP1302 ISP*
The SMARC Dual Camera Adapter features the AP1302 Image Signal Processor. This imaging co-processor is capable of processing dual cameras. It is the recommended ISP for use with onsemi camera modules.

### 5.1.4 Quad Core Arm Cortex-A53 ARM Applications Processor
The I.MX8M Plus has four Arm Cortex-A3 processors operating at 1.6GHz. It has the following features:

- Quad symmetric Cortex-A53 processors, including:
    - 32 KB L1 Instruction Cache
    - 32 KB L1 Data Cache

- Media Processing Engine (MPE) with NEON technology supporting the Advanced Single Instruction Multiple Data architecture:
    - Floating Point Unit (FPU) with support of the VFPv4-D16 architecture
    - Support of 64-bit Armv8-A architecture
    - 512 KB unified L2 cache

### 5.1.5 GPU

The i.MX8M Plus includes a Vivante GC7000UL 2D/3D Graphics Processor from VeriSilicon with OpenCL and Vulkan support.

- 1080p60 HEVC H.265, VP9, H.264, VP8 decode
- 1080p60 H.264, VP8 encode

### 5.1.6 Arm Cortex M7

The Arm Cortex-M7 (800MHz) is capable of real-time control and includes the following:

- 32 KB L1 Instruction Cache
- 32 KB L1 Data Cache
- 256 KB TCM

Available customer applications include:

- Low power standby mode
- IoT device control
- ML applications

### 5.1.7 Memory

#### *5.1.7.1 On-chip Memory*

The i.MX8M Plus's on-chip memory consists of the following:

- Boot ROM (256KB)
- On-Chip RAM - OCRAM (576KB)
- Audio Processor System RAM - OCRAM_A (256KB)
- On-Chip RAM for State Retention - OCRAM_S (36KB)

#### *5.1.7.2 External Memory*

The i.MX8M Plus SMARC SOM's external memory includes the following:

- 4GB LPDDR4 Memory

The i.MX8M Plus SMARC SOM uses one physical memory rank. The DDR Controller supports 32-bit LPDDR4-4000 with inline ECC.

| Memory Size | Memory Width | Memory Speed | Qualification | Operating Temperature |
|---|---|---|---|---|
| 4 GB | 1x 32-bit | 4000 MT/s | Industrial | -40°C to +95°C |

**Table 2 - SDRAM Features**

- 16GB eMMC 5.1 Flash Storage

| Memory Size | Max. Speed | Qualification | Operating Temperature |
|---|---|---|---|
| 16 GB | HS400 | Industrial | -40°C to +85°C |

Table 3 - eMMC 5.1 Flash Storage Features

## 5.2 Communication Interfaces

This section describes the communication interfaces provided by the Avnet EP5 SMARC Carrier in combination with the Avnet i.MX8M Plus SMARC SOM.

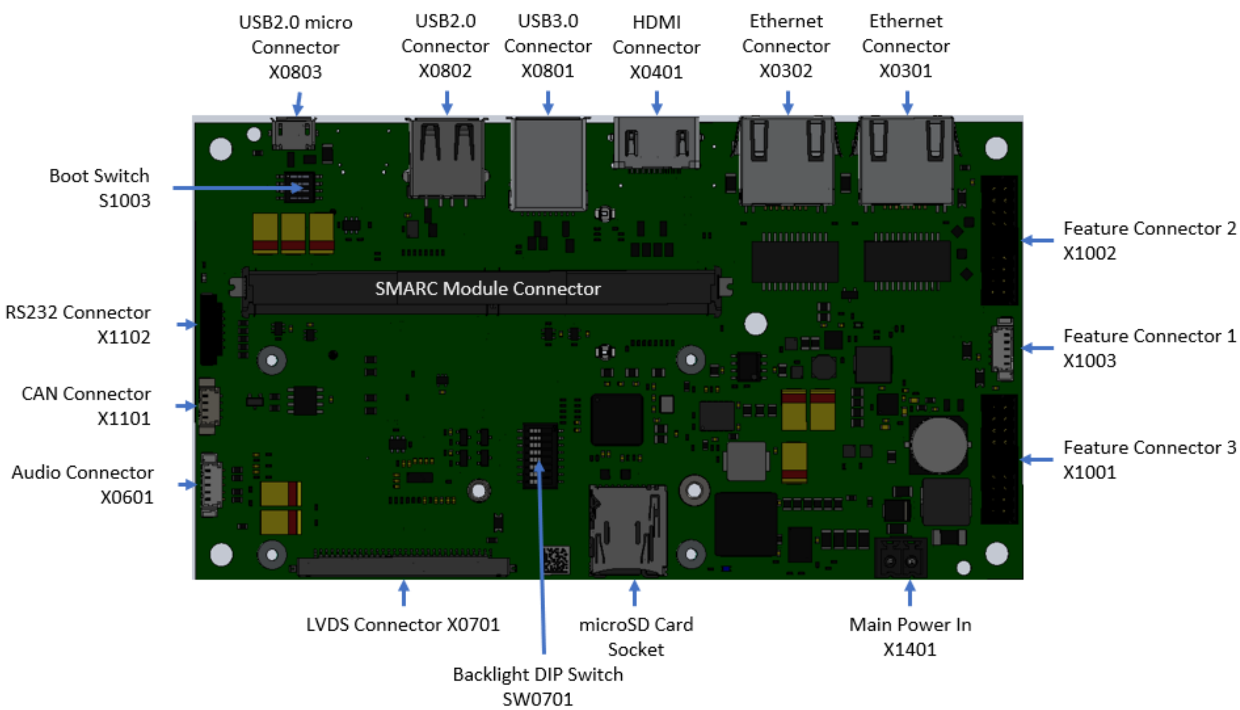



Figure 3 - SMARC Carrier Connector Map -Top

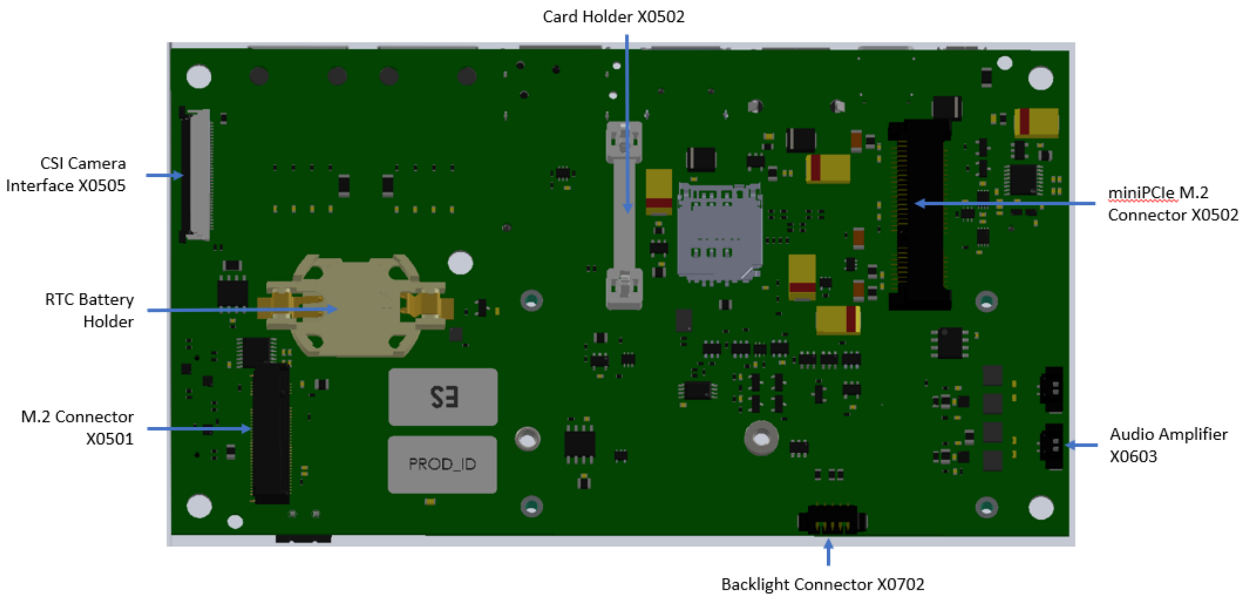



**Figure 4 - SMARC Carrier Connector Map - Bottom**

### 5.2.1 I²S Audio

The i.MX8M Plus SMARC SOM provides two I²S Links for connecting I²S codecs on the SMARC Carrier.

Some features:

- Programmable data interface modes such as I2S, LSB or MSB-justified
- Programmable word length (16, 20, 24 or 28bits)
- AC97 and TDM support
- Time Slot Mask Registers for reduced ARM platform overhead (for both Transmit and Receive)
- 128-word Transmit FIFO and 128-word Receive FIFO

#### *5.2.1.1 Audio Codec*

The Audio connector on the SMARC Carrier is a Molex Picoblade 53398-0571 with 5pins. The audio codec is Dialog DA7212 and uses I2S0. The kit includes a 5-pin Audio Connector cable.

| Signal | Pin Type | Signal Level | i.MX8M Plus Ball Number | i.MX8M Plus Ball Name | Power Tolerance | Description |
|---|---|---|---|---|---|---|
| I2S0_LRCK | O PP | 1.8V CMOS | AJ17 | SAI2_TXFS | 1.8V | Sample-synchronization signal |
| I2S0_CK | O PP | 1.8V CMOS | AH15 | SAI2_TXC | 1.8V | Serial data clock |
| I2S0_SDOUT | O PP | 1.8V CMOS | AH16 | SAI2_TXD0 | 1.8V | Serial TDM data output to the codec. |

| Signal | Pin Type | Signal Level | i.MX8M Plus Ball Number | i.MX8M Plus Ball Name | Power Tolerance | Description |
|---|---|---|---|---|---|---|
| I2S0_SDIN | I | 1.8V CMOS | AJ14 | SAI2_RXD0 | 1.8V | Serial TDM data inputs from the codec. |

Table 4 - I²S Signal Description (I2S0)

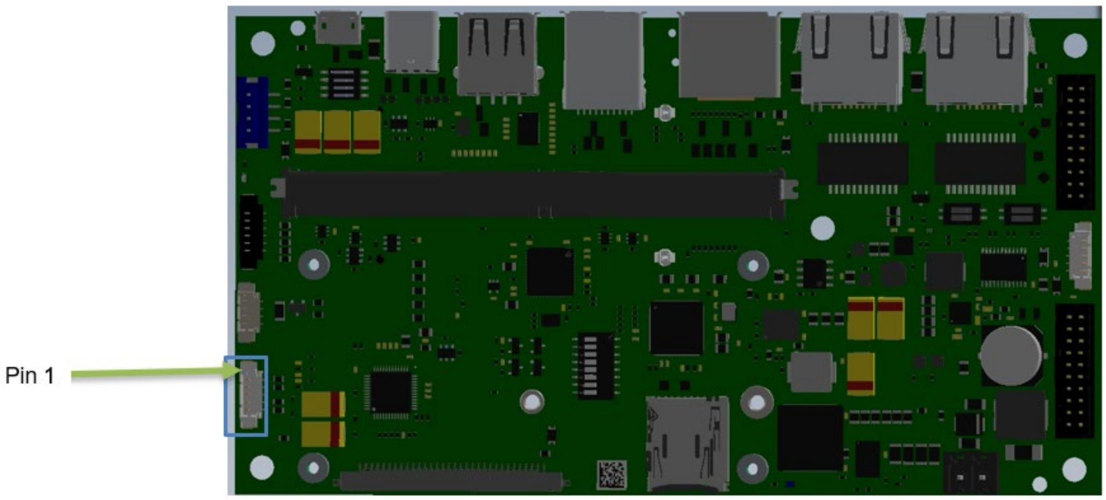



Figure 5 - EP5 Audio Connector X0601

| Signal | Pin Number | Signal Level | Description |
|---|---|---|---|
| MIC_IN_L | 1 | analog | Microphone In Left |
| MIC_IN_R | 2 | analog | Microphone In Right |
| GND | 3 | 0V | Ground, power return |
| LINE_OUT_L | 4 | analog | Line Out Left |
| LINE_OUT_R | 5 | analog | Line Out Right |

Table 5 - Audio Connector Description

#### *5.2.1.2 Audio Amplifier*

The internal amp is monaural and uses connector X0603. The Connector reference is Molex Picoblade 53398-0271 with 2pin. The kit includes a double-sided two-pin speaker-out cable.

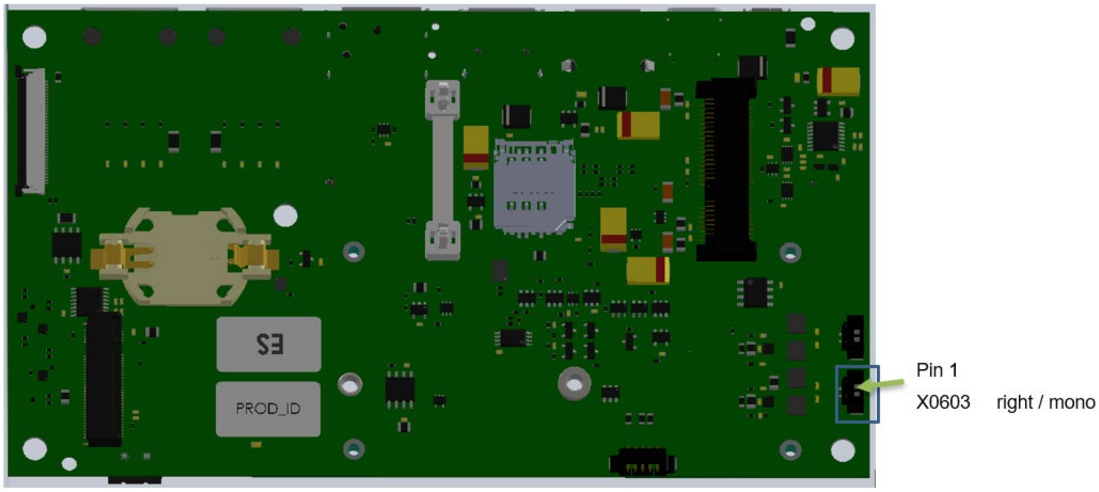



Figure 6 - EP5 Amplifier Connector X0603

### 5.2.2 Ethernet

The SMARC Carrier has two 10/100/1000 Base-T ethernet interfaces on standard RJ45 connectors.

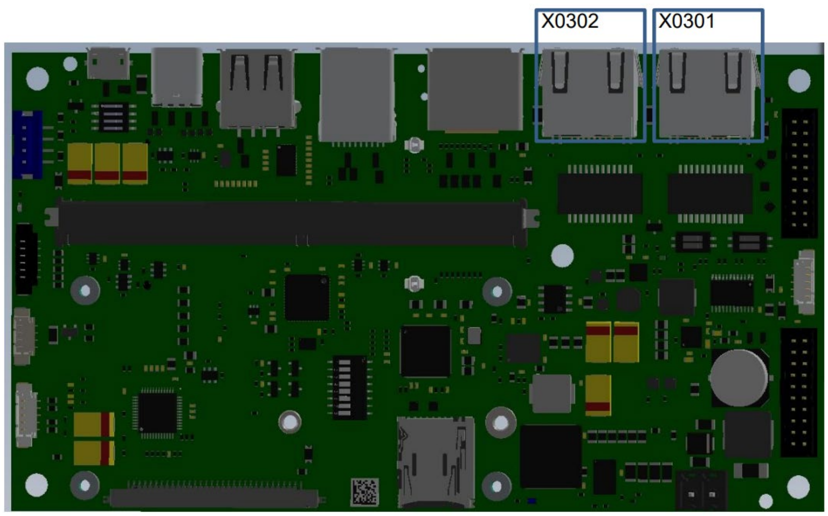



Figure 7 – Ethernet Ports

Both connectors have two LEDs (yellow=activity/green=Link). Their ethernet interface is generated by the i.MX8M Plus SMARC SOM. The SOM provides 10/100/1000 Mbit/s Ethernet with MDI differential pairs based on Texas Instruments™ DP83867 Ethernet Controller. They are capable of simultaneous operation.

- X0301/GbE1 - Gigabit Ethernet controller with support for TSN, EEE, Ethernet AVB and IEEE1588
- X0302/GbE2 - Gigabit Ethernet controller with support for EEE, Ethernet AVB and IEEE1588

### 5.2.3 M.2 / PCI Express

The i.MX8M Plus SOM supports PCIe Gen3 x1 lane. However, this is routed to the i210 GbE Controller on the SMARC Carrier.

Only USB2.0 is available from the MiniPCIe slot. The M.2 SATA slot on the SMARC Carrier is not functional as it's not supported by the i.MX8M PLUS SMARC SOM.

### 5.2.4 USB

The USB controller on the SMARC SOM can operate in super-speed, high-speed, full-speed and low-speed mode. An external USB Hub Texas Instruments™ TUSB8041 is connected to USB2 host controller of i.MX8M Plus SOM.

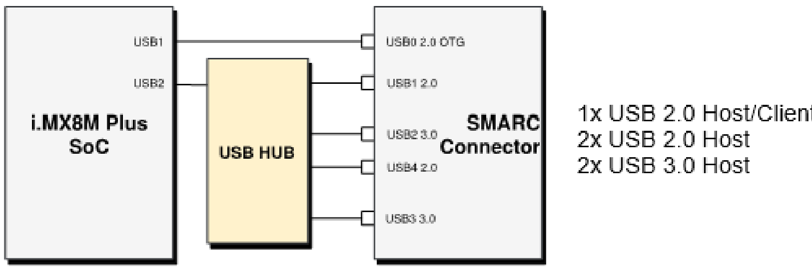



**Figure 8 - USB Port Block Diagram**

| Signal | Pin Type | Signal Level | Power Tolerance | PU/PD | Description |
|---|---|---|---|---|---|
| USB[0:4]+<br>USB[0:4]- | I/O | USB HS | 3.3V | | Differential USB 2.0 data pairs. |
| USB[2:3]_SSTX+<br>USB[2:3]_SSTX- | I/O | USB SS | 3.3V | | Transmit signal differential pairs for SuperSpeed. DC blocking capacitors 100nF placed on module. |
| USB[2:3]_SSRX+<br>USB[2:3]_SSRX- | I/O | USB SS | 3.3V | | Receive signal differential pairs for SuperSpeed. |
| USB[0:4]_EN_OC# | I/O OD | 3.3V CMOS | 3.3V | PU 10k 3.3V | Multi-function signal for enabling USB power and indicating an over-current event. [1] |
| USB0_OTG_ID | I | 3.3V CMOS | 3.3V | PU 10k 3.3V | USB host/client control select pin for the USB controller on the module. Tie to GND in case USB port is used as host only. |
| USB3_OTG_ID | I | 3.3V CMOS | 3.3V | PU 10k 3.3V | USB host/client control select pin for the USB controller on the module. Tie to GND in case USB port is used as host only. |
| USB0_VBUS_DET | I | 5V | 5V | | External VBUS detection pin. |
| USB3_VBUS_DET | I | 5V | 5V | | External VBUS detection pin. |

**Table 6 - USB Signal Description**

The SMARC Carrier connects USB3.0 Super-Speed lane and USB2.0 High-Speed lanes 0 to 5 as defined in the SMARC™ specification.

- USB3.0 lane2 and USB2.0 lane2 are routed to USB3.0 SuperSpeed connector X0801.

- USB2.0 lane0 is routed to MicroUSB OTG connector X0803
- USB2.0 lane1 is routed to USB2.0 Type A connector X0802
- USB2.0 lane4 is routed to the miniPCIe module.
- USB2.0 lane3 is routed to Feature Connector 1 X1003.

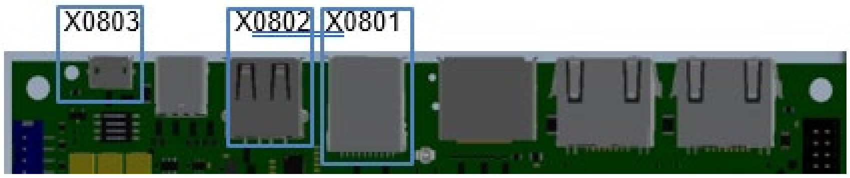



Figure 9 - USB Ports

The SMARC Carrier provides 1A current on X0801 (controlled by USB power switch). 0.5 A current is provided to X0802, X0803. Overcurrent situations are reported on the corresponding OC signal pins as defined in the SMARC™ specification.

### 5.2.5 LVDS Display Panel

The SMARC Carrier includes a 32-pin LVDS connector which can be configured either as dual channel or as two separate single channels. An on-module DSI bridge Texas Instruments™ SN65DSI84 converts the MIPI DSI data stream to single-link LVDS to provide an additional single channel port.

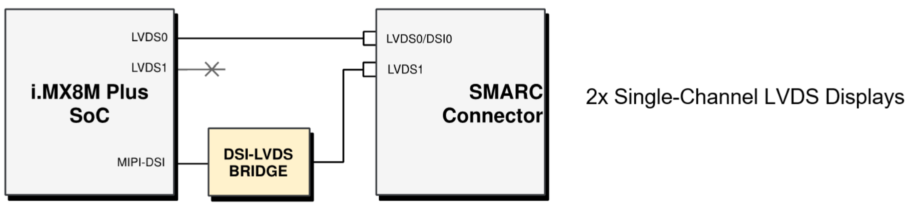



Figure 10 - Display Configurations Block Diagram

**Features:**

- Single-Link and Dual-Link with four data lanes per link
- Supports 18bpp and 24bpp
- Resolution up to 1366x768p@60Hz in single-channel configuration. Pixel clock up to 80 MHz.
- Resolution up to 1920x1080p@60Hz in dual-channel configuration. Pixel clock up to 160 MHz.
- Resolution up to 1920x1080p@60Hz in MIPI-DSI configuration. Pixel clock up to 250 MHz.

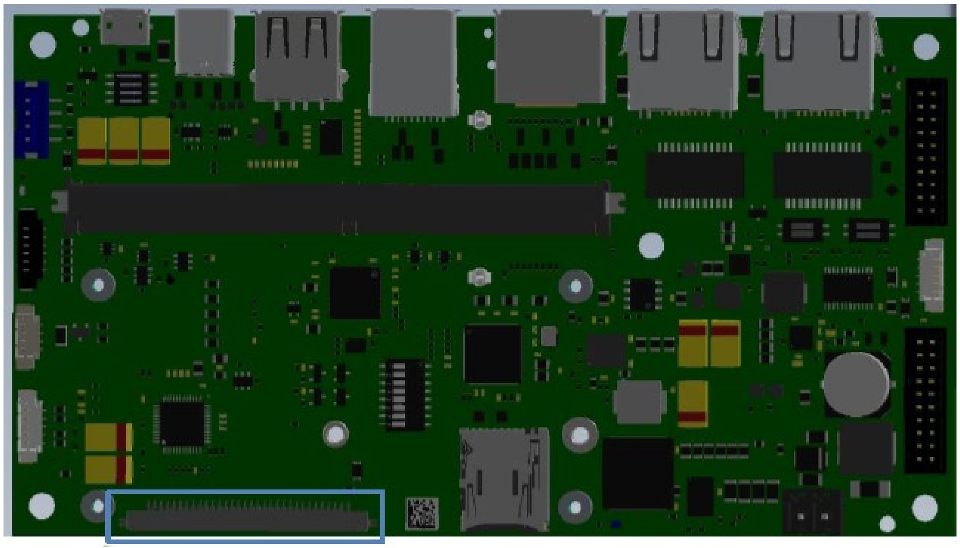


Figure 11 - LVDS Display Interface (X0701)

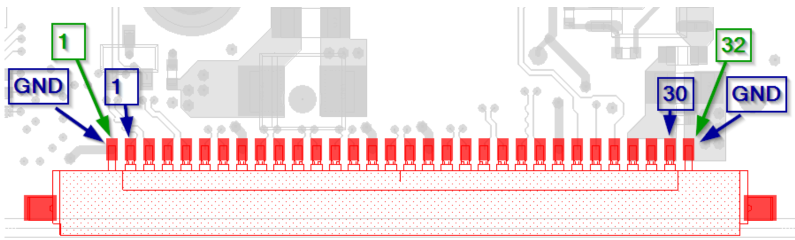



Figure 12 - LVDS / MIPI DSI connector pinout numbering

The SMARC Carrier routes both LVDS channels as defined in the SMARC™ specification to a standard JILI30 connector X0701. The display digital supply on this connector can be set to 3.3V or 5.0V (selectable via I2C). The power is switched on by the LCD0_VDD_EN (S133) signal, as defined in the SMARC™ specification.

| Signal | Alternate Signal | Pin Number* 1 - 32 | Pin Number 1 - 30 | Signal Level | Power Tolerance | Description |
|---|---|---|---|---|---|---|
| GND | GND | 1 * | n/a | 0V | | Ground, power return |
| LVDS_A0_N | DSI0_D0- | 2 | 1 | LVDS | 2.5V | |
| LVDS_A0_P | DSI0_D0+ | 3 | 2 | LVDS | 2.5V | |
| LVDS_A1_N | DSI0_D1- | 4 | 3 | LVDS | 2.5V | |
| LVDS_A1_P | DSI0_D1+ | 5 | 4 | LVDS | 2.5V | |
| LVDS_A2_N | DSI0_D2- | 6 | 5 | LVDS | 2.5V | |
| LVDS_A2_P | DSI0_D2+ | 7 | 6 | LVDS | 2.5V | |
| GND | GND | 8 | 7 | 0V | | Ground, power return |
| LVDS_A_CLK_N | DSI0_CLK- | 9 | 8 | LVDS | 2.5V | |
| LVDS_A_CLK_P | DSI0_CLK+ | 10 | 9 | LVDS | 2.5V | |
| LVDS_A3_N | DSI0_D3- | 11 | 10 | LVDS | 2.5V | |

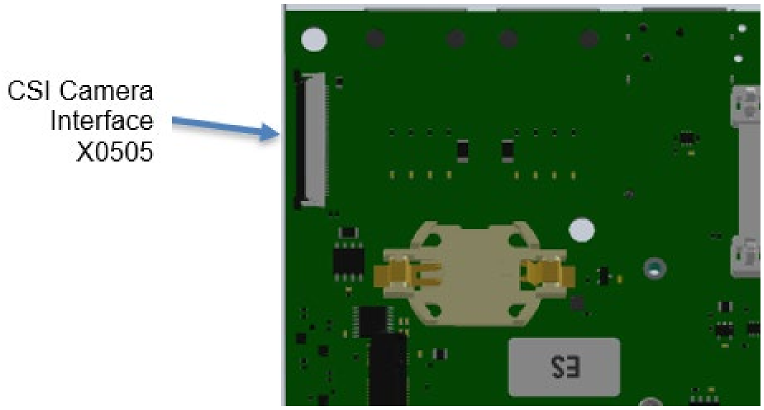
| Signal | Alternate Signal | Pin Number* 1 - 32 | Pin Number 1 - 30 | Signal Level | Power Tolerance | Description |
|---|---|---|---|---|---|---|
| LVDS_A3_P | DSI0_D3+ | 12 | 11 | LVDS | 2.5V | |
| LVDS_B0_N | DSI1_D0- | 13 | 12 | LVDS | 2.5V | |
| LVDS_B0_P | DSI1_D0+ | 14 | 13 | LVDS | 2.5V | |
| GND | GND | 15 | 14 | 0V | | Ground, power return |
| LVDS_B1_N | DSI1_D1- | 16 | 15 | LVDS | 2.5V | |
| LVDS_B1_P | DSI1_D1+ | 17 | 16 | LVDS | 2.5V | |
| GND | GND | 18 | 17 | 0V | | Ground, power return |
| LVDS_B2_N | DSI1_D2- | 19 | 18 | LVDS | 2.5V | |
| LVDS_B2_P | DSI1_D2+ | 20 | 19 | LVDS | 2.5V | |
| LVDS_B_CLK_N | DSI1_CLK- | 21 | 20 | LVDS | 2.5V | |
| LVDS_B_CLK_P | DSI1_CLK+ | 22 | 21 | LVDS | 2.5V | |
| LVDS_B3_N | DSI1_D3- | 23 | 22 | LVDS | 2.5V | |
| LVDS_B3_P | DSI1_D3+ | 24 | 23 | LVDS | 2.5V | |
| GND | GND | 25 | 24 | 0V | | Ground, power return |
| LVDS_I2C_DAT | NA | 26 | 25 | 3.3V CMOS | 3.3V | Connected to SMARC LVDS_EDID I2C interface. |
| LCD0_VDD_EN | NA | 27 | 26 | 3.3V CMOS | 3.3V | Output of SMARC SOM to switch on display power. |
| LVDS_I2C_CLK | NA | 28 | 27 | 3.3V CMOS | 3.3V | Connected to SMARC LVDS_EDID I2C interface. |
| Display Power | Display Power | 29 | 28 | Power | | Selectable 3.3V and 5.0V |
| Display Power | Display Power | 30 | 29 | Power | | Selectable 3.3V and 5.0V |
| Display Power | Display Power | 31 * | 30 | Power | | Selectable 3.3V and 5.0V |
| GND | GND | 32 * | n/a | 0V | | Ground, power return |

**Table 7 - LVDS / MIPI DSI Signal Description X0701**

### 5.2.6 Camera

#### *5.2.6.1 Camera Interface*

The Edge AI Kit includes a MIPI-CSI camera interface on the SMARC Carrier. The kit includes a flat flex connector (FFC) to attach the SMARC Camera Adapter to the Carrier.

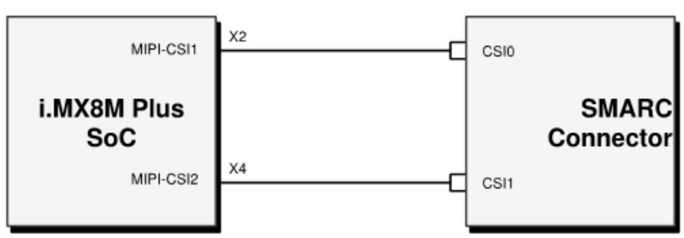



## Figure 13 - MIPI-CSI Camera Interface

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|---|---|
| 1 | VCC_3V3 | 2 | VCC_3V3 | 3 | CSI1_RX0_P | 4 | CSI1_RX0_N | 5 | GND |
| 6 | CSI1_RX1_P | 7 | CSI1_RX1_N | 8 | GND | 9 | CSI1_RX2_P | 10 | CSI1_RX2_N |
| 11 | GPIO3, CAM1_RST# | 12 | CSI1_RX3_P | 13 | CSI1_RX3_N | 14 | GND | 15 | CSI1_CK_P |
| 16 | CSI1_CK_N | 17 | GND | 18 | I2C_CAM1_CK | 19 | I2C_CAM1_DAT | 20 | GPIO1, CAM1_PWR# |
| 21 | CAM_MCK | 22 | GPIO0, CAM0_PWR# | 23 | I2C_CAM0_CK | 24 | I2C_CAM0_DAT | 25 | GND |
| 26 | CSI0_CK_P | 27 | CSI0_CK_N | 28 | GND | 29 | CSI0_RX0_P | 30 | CSI0_RX0_N |
| 31 | GPIO2, CAM0_RST# | 32 | CSI0_RX1_P | 33 | CSI0_RX1_N | 34 | GND | 35 | GPIO7, CAMFC_PWR |
| 36 | GPIO7, CAMFC_PWR | | | | | | | | |

## Table 8 – CSI Connector X0505

The SMARC SOM includes two instances of MIPI CSI interfaces: one on CSI0 (2 lane) and one on CSI1 (4 lane). Both support up to 277MHz pixel clock for both single camera and dual camera use.




## Figure 14 - MIPI-CSI Interface Block Diagram

| Signal | Pin Type | Signal Level | i.MX8M Plus Ball Number | i.MX8M Plus Ball Name | Power Tolerance | PU/PD | Description |
|---|---|---|---|---|---|---|---|
| CSI0_RX[0]-<br>CSI0_RX[0]+ | I | D-PHY | E18<br>D18 | MIPI_CSI1_D0_N<br>MIPI_CSI1_D0_P | 1.8V | | CSI differential data inputs |

| Signal | Pin Type | Signal Level | i.MX8M Plus Ball Number | i.MX8M Plus Ball Name | Power Tolerance | PU/PD | Description |
|---|---|---|---|---|---|---|---|
| CSI0_RX[1]-<br>CSI0_RX[1]+ | I | D-PHY | E20<br>D20 | MIPI_CSI1_D1_N<br>MIPI_CSI1_D1_P | 1.8V | | CSI differential data inputs |
| CSI1_RX[0]-<br>CSI1_RX[0]+ | I | D-PHY | B25<br>A25 | MIPI_CSI2_D0_N<br>MIPI_CSI2_D0_P | 1.8V | | CSI differential data inputs |
| CSI1_RX[1]-<br>CSI1_RX[1]+ | I | D-PHY | B24<br>A24 | MIPI_CSI2_D1_N<br>MIPI_CSI2_D1_P | 1.8V | | CSI differential data inputs |
| CSI1_RX[2]-<br>CSI1_RX[2]+ | I | D-PHY | B22<br>A22 | MIPI_CSI2_D2_N<br>MIPI_CSI2_D2_P | 1.8V | | CSI differential data inputs |
| CSI1_RX[3]-<br>CSI1_RX[3]+ | I | D-PHY | B21<br>A21 | MIPI_CSI2_D3_N<br>MIPI_CSI2_D3_P | 1.8V | | CSI differential data inputs |
| CSI0_CK-<br>CSI0_CK+ | I | D-PHY | E22<br>D22 | MIPI_CSI1_CLK_N<br>MIPI_CSI1_CLK_P | 1.8V | | CSI differential clock inputs |
| CSI1_CK+<br>CSI1_CK- | I | D-PHY | A23<br>B23 | MIPI_CSI2_CLK_N<br>MIPI_CSI2_CLK_P | 1.8V | | CSI differential clock inputs |
| CAM_MCK | O PP | 1.8V CMOS | L29 | CLKOUT2 | 1.8V | | Master clock for camera |
| I2C_CAM0_CK | O OD | 1.8V CMOS | AF8 | I2C4_SCL | 1.8V | PU 2.2k 1.8V | CAM0 DDC clock line (SoC I2C4_SCL) |
| I2C_CAM0_DAT | I/O OD | 1.8V CMOS | AD8 | I2C4_SDA | 1.8V | PU 2.2k 1.8V | CAM0 DDC data line (SoC I2C4_SDA) |
| I2C_CAM1_CK | O OD | 1.8V CMOS | AE18 | SPDIF_TX | 1.8V | PU 2.2k 1.8V | CAM1 DDC clock line (SoC I2C5_SCL) |
| I2C_CAM1_DAT | I/O OD | 1.8V CMOS | AD18 | SPDIF_RX | 1.8V | PU 2.2k 1.8V | CAM1 DDC data line (SoC I2C5_SDA) |
| CAM0_PWR# | I/O OD | 1.8V CMOS | D8 | GPIO1_IO11 | 1.8V | SOC PU 1.8V | CAM0 power enable, active low. |
| CAM1_PWR# | I/O OD | 1.8V CMOS | AH8 | SAI1_RXC | 1.8V | SOC PU 1.8V | CAM1 power enable, active low. |
| CAM0_RST# | I/O OD | 1.8V CMOS | AC10 | SAI1_RXD0 | 1.8V | SOC PU 1.8V | CAM0 reset, active low. |
| CAM1_RST# | I/O OD | 1.8V CMOS | AF10 | SAI1_RXD1 | 1.8V | SOC PU 1.8V | CAM1 reset, active low. |

**Table 9 - CSI Signal Description**

### *5.2.6.2 Dual Camera Adapter*

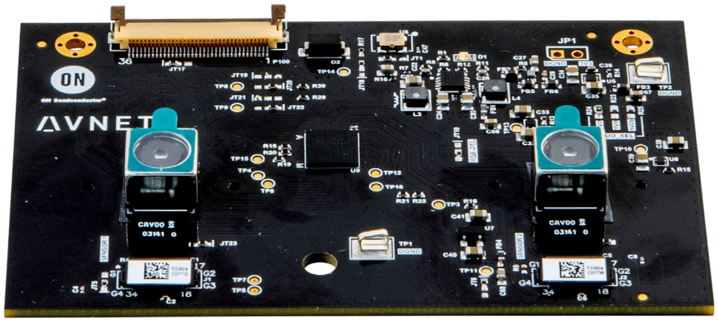


Figure 15 - SMARC Dual Camera Adapter

#### 5.2.6.3 onsemi AR1335 IAS Camera Modules

This section describes the camera modules and ISP found on the Avnet SMARC Dual Camera Adapter.

For more detailed information regarding the camera module and image sensor, please see the AR1335 IAS Module and AP1302 Image Signal Processor pages from onsemi.

Figure 16 - AR1335 IAS Camera Module

The Dual  Camera Adapter features two AR1335 IAS Camera modules, which are 1/3.2-inch CMOS active-pixel digital image sensors with a pixel array of 4208H x 3120V. The modules are manufactured by Rapyrus. The AR1335 digital image sensor features 1.1µm pixel technology that delivers superior low-light image quality through leading sensitivity, quantum efficiency and linear full well.

Features:

- 13MP CMOS sensor with advanced 1.1µm pixel BSI technology
- Rolling shutter
- Full resolution at 30fps
- Supported video modes: 4K 30fps, 1080P 60fps and 720P 120fps

### 5.2.7 HDMI

The HDMI 2.0a TX port on the SMARC Carrier supports one display.

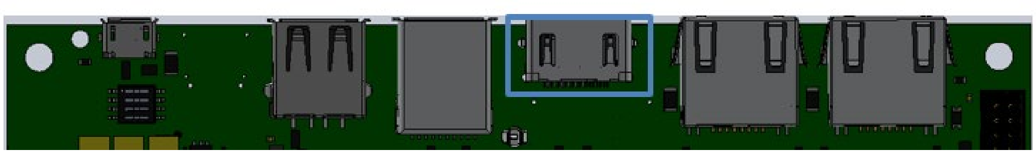


Figure 17 - HDMI Port (X0402)

It features:

- Resolutions of: 720 x 480p60, 1280 x 720p60, 1920 x 1080p60, 1920 x 1080p120, and 4K (3840x2160@30FPS)
- Pixel clock up to 297 MHz
- Audio support
- 32-channel audio output support
- 1 SPDIF audio eARC input support

### 5.2.8 CAN

The SMARC SOM offers two CAN 2.0B interfaces with flexible data-rate (FD) up to 8Mbps.

The CAN interface on the SMARC Carrier is routed to "CAN0" on the SMARC SOM. Speed is limited to 1Mbit/s.

CAN1 is provided by Feature Connector 2 on the SMARC Carrier.

Several features are supported (time-triggered protocols, data byte filtering and one-shot mode).

| Signal | Pin Type | Signal Level | i.MX8M Plus Ball Number | i.MX8M Plus Ball Name | Power Tolerance | Description |
|---|---|---|---|---|---|---|
| CAN0_TX | O | 1.8V CMOS | AD16 | SAI5_RXD1 | 1.8V | CAN Transmit output |
| CAN0_RX | I | 1.8V CMOS | AF16 | SAI5_RXD2 | 1.8V | CAN Receive input |
| CAN1_TX | O | 1.8V CMOS | AE14 | SAI5_RXD3 | 1.8V | CAN Transmit output |
| CAN1_RX | I | 1.8V CMOS | AF14 | SAI5_MCLK | 1.8V | CAN Receive input |

**Table 10 - CAN Signal Description**

The CAN connector is Molex Picoblade 53398-0471 with 4 pins.

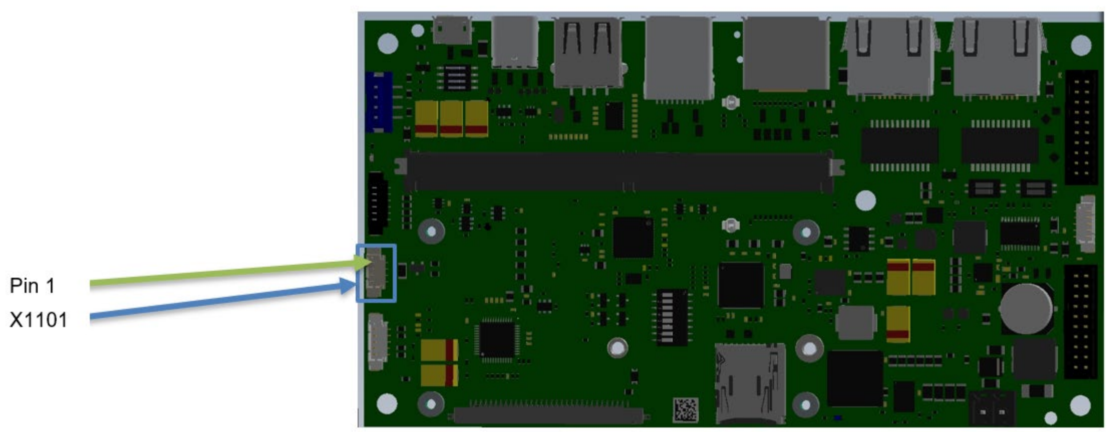



**Figure 18 - CAN connector (X1101)**

| Signal | Pin Number | Signal Level | Description |
|---|---|---|---|
| VCC_5V_ISO | 1 | Power | Isolated 5V voltage. Do not draw more than 50mA. |

| Signal | Pin Number | Signal Level | Description |
|---|---|---|---|
| CAN0_N | 2 | | CAN0 |
| CAN0_P | 3 | | CAN0 |
| GND_ISO | 4 | 0V | Isolated Ground, power return |

Table 11 - CAN connector Signal Description

### 5.2.9 RS232 (SER0)

The serial interface on the SMARC Carrier is routed to the “SER0” interface on the SOM and provides an RS232 interface.

The RS232 connector on the SMARC Carrier is Molex Picoblade 53398-0671 with 5 pins.

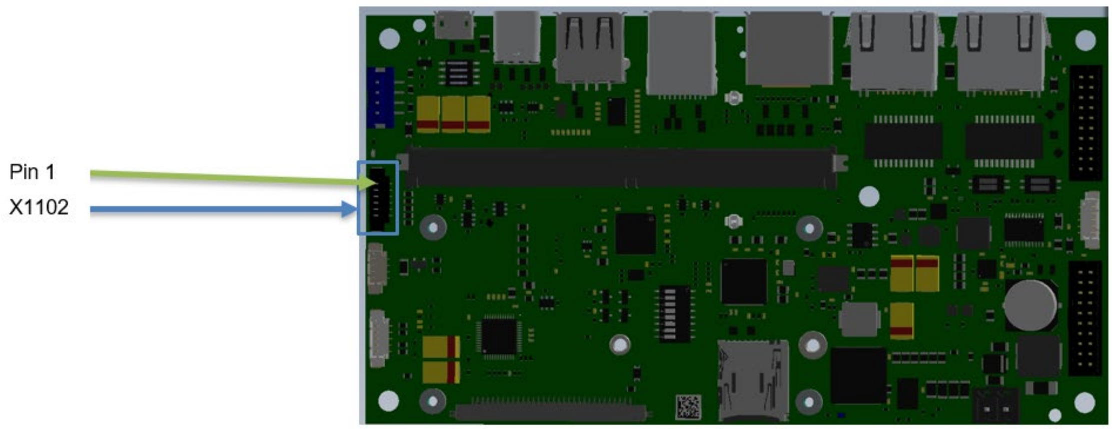



Figure 19 - RS232 connector (SER0)

| Signal | Pin Number | Signal Level | Description |
|---|---|---|---|
| VCC_5V | 1 | Power | Non-isolated 5V supply. Not fused. |
| RS232_RTS | 2 | | RS-232 RTS (SER0) |
| RS232_TX | 3 | | RS-232 TX (SER0) |
| RS232_CTS | 4 | | RS-232 CTS (SER0) |
| RS232_RX | 5 | | RS-232 RX (SER0) |
| GND | 6 | 0V | Non-isolated Ground, power return |

Table 12 - RS232 connector Signal Description X1102

#### *5.2.9.1 UART Interfaces*

In total, four UART interfaces are available from the SMARC SOM. SER1 and SER3 are available on Feature Connector 3 on the SMARC Carrier. The SOM’s UART interfaces support Serial RS-232NRZ mode and include the following features amongst others:

- High-speed TIA/EIA-232-F compatible, up to 5.0 Mbit/s
- 8 data bits for RS-232 characters
- 1 or 2 stop bits
- Programmable parity (even, odd, and no parity)
- Hardware flow control support for request to send (RTS_B) and clear to send (CTS_B) signals

- Edge-selectable RTS_B and edge-detect interrupts
- Status flags for various flow control and FIFO states
- Voting logic for improved noise immunity (16x oversampling)
- Transmitter FIFO empty interrupt suppression
- UART internal clocks enable/disable
- Auto baud rate detection (up to 115.2 Kbit/s)
- Receiver and transmitter enable/disable for power saving
- RX_DATA input and TX_DATA output can be inverted
- Maskable interrupts
- Two DMA Requests (TxFIFO DMA Request and RxFIFO DMA Request)
- Escape character sequence detection
- Software reset (SRST_B)
- Two independent, 32-entry FIFOs for transmit and receive

| Signal | Pin Type | Signal Level | i.MX8M Plus Ball Number | i.MX8M Plus Ball Name | Power Tolerance | PU/PD | Description |
|---|---|---|---|---|---|---|---|
| SER0_TX | O | 1.8V CMOS | AH4 | UART2_TXD | 1.8V | PU 10k 1.8V | UART transmit data[1] |
| SER0_RX | I | 1.8V CMOS | AF6 | UART2_RXD | 1.8V | PU 10k 1.8V | UART receive data[1] |
| SER0_RTS# | O | 1.8V CMOS | U26 | SD1_DATA4 | 1.8V | PU 10k 1.8V | UART handshake, ready to receive data |
| SER0_CTS# | I | 1.8V CMOS | AA29 | SD1_DATA5 | 1.8V | PU 10k 1.8V | UART handshake, ready to send data |

Table 13 - UART Signal Description (SER0)

### 5.2.10 Micro SD Card

The SMARC Carrier provides a Micro SD Card socket, which can be used as the primary boot device. The SDIO interface is using 3.3V signal level by default but can be negotiated between the SD card and the SMARC SOM to 1.8V for high-speed modes (i.e. HS-200 and HS-400).

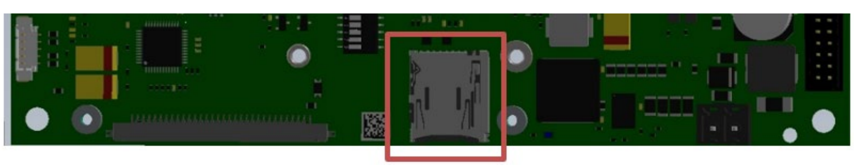


Figure 20 - SD Card socket

The SDIO interface on the SMARC connector supports:

- 1-bit / 4-bit for SD/SDIO mode (standard up to version 3.0)
- 1-bit / 4-bit for MMC mode (standard up to version 5.1)
- SD/SDIO 1.8 V or 3.3 V operation with auto detection
- Default Speed, High-Speed and UHS-I (SDR50, DDR50 and SDR104)



AVNET Reach Further™

| Signal | Pin Type | Signal Level | i.MX8M Plus Ball Number | i.MX8M Plus Ball Name | Power Tolerance | PU/PD | Description |
|---|---|---|---|---|---|---|---|
| SDIO_D0 | I/O | 3.3V / 1V8 CMOS | AC28 | SD2_DATA0 | 3.3V / 1.8V | PU 10k 3.3V / 1.8V | SDIO controller data |
| SDIO_D1 | I/O | 3.3V / 1V8 CMOS | AC29 | SD2_DATA1 | 3.3V / 1.8V | PU 10k 3.3V / 1.8V | SDIO controller data |
| SDIO_D2 | I/O | 3.3V / 1V8 CMOS | AA26 | SD2_DATA2 | 3.3V / 1.8V | PU 10k 3.3V / 1.8V | SDIO controller data |
| SDIO_D3 | I/O | 3.3V / 1V8 CMOS | AA25 | SD2_DATA3 | 3.3V / 1.8V | PU 10k 3.3V / 1.8V | SDIO controller data |
| SDIO_CMD | I/O | 3.3V / 1V8 CMOS | AB28 | SD2_CMD | 3.3V / 1.8V | PU 10k 3.3V / 1.8V | SDIO controller command |
| SDIO_CK | O | 3.3V / 1V8 CMOS | AB29 | SD2_CLK | 3.3V / 1.8V | PU 10k 3.3V / 1.8V | SDIO controller clock |
| SDIO_PWR_EN | O | 3.3V CMOS | AD28 | SD2_RESET_B | 3.3V | PU 10k 3.3V | SDIO controller power enable |
| SDIO_CD# | I | 3.3V / 1V8 CMOS | AD29 | SD2_CD_B | 3.3V / 1.8V | PU 10k 3.3V / 1.8V | SDIO controller card detect. |
| SDIO_WP | I | 3.3V / 1V8 CMOS | AC26 | SD2_WP | 3.3V / 1.8V | PU 10k 3.3V / 1.8V | SDIO controller write protect. |

**Table 14 - SDIO Signal Description**

Maximum bus speed for SDIO interface is set per default to High Speed Mode (HS) with a maximum frequency of 50MHz and 3.3V signal voltage. To achieve higher bus speed mode (SDR50 and SDR104) it is highly recommended to keep SD signal trace length less then 100mm. A load switch with quick output discharge should be used for SD-Card power supply

### 5.2.11 Feature Connectors

Feature connectors on the SMARC Carrier all allow access to lesser used signals including USB3, SPI, CAN and UART. The kit provides a cable for feature connector 1 (USB) and a cable for feature connectors 2 and 3.

For further information about USB signals, see section 5.2.4.

For further information about CAN signals, see section 5.2.8.

For further information about SPI signals, see section 5.2.12.

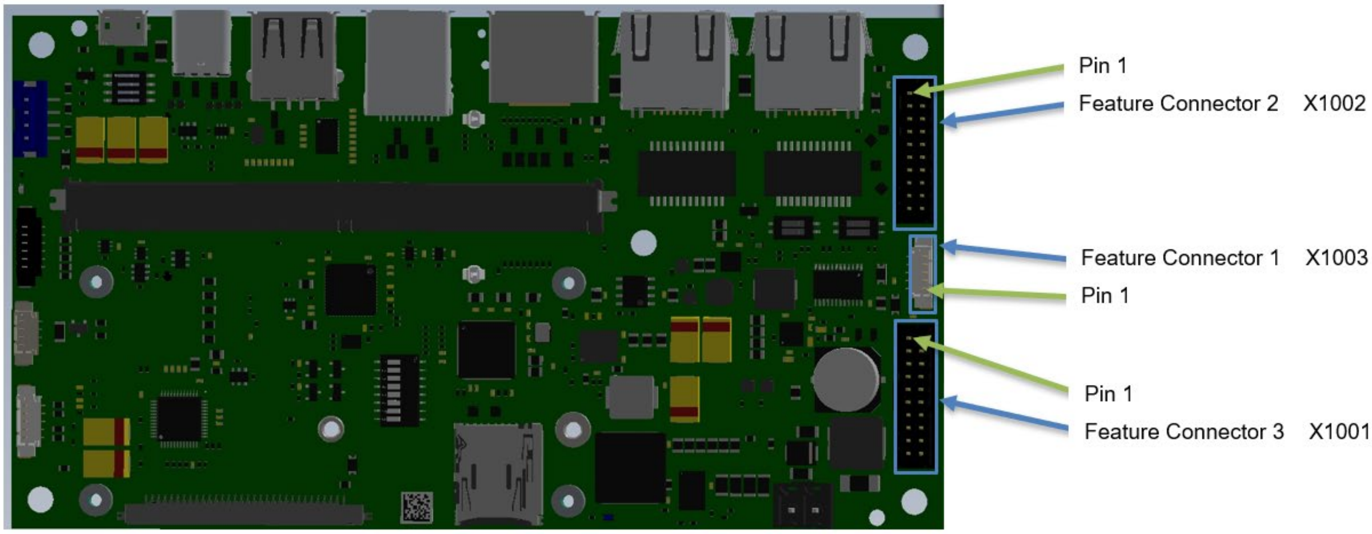
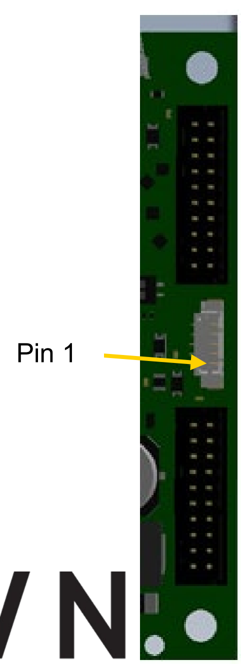



**Figure 21 - Feature Connectors**

USB3 is available on Feature Connector 1 (X1003).

Connector reference type: Molex Picoblade 53398-0571




| Signal | Pin Number | Signal Level | In/out | Description |
|---|---|---|---|---|
| VCC_5V | 1 | 5V | Power | 5V Supply, fused with 500mA (F1003) |
| USB3_OC | 2 | 3.3V | Bi-Dir | Power Enable & Over-Current control for USB3 |
| USB_P3+ | 3 | USB | Bi-Dir | USB 2.0 port #3 |
| USB_P3- | 4 | USB | Bi-Dir | USB 2.0 port #3 |
| GND | 5 | 0V | Power | Ground, Power return |

**Table 15 - Feature Connector 1 X1003**

SPI0, SPI1, and CAN1 are available on Feature Connector 2 (X1002).

Connector reference type: Molex Milli Grid 87832-5922

| Signal | Pin Number | Signal Level | IN/OUT | Description |
|---|---|---|---|---|
| VCC_1V8 | 1 | 1.8V | Power | 1.8V Supply, fused with 500mA (F1002) |
| VCC_5V | 2 | 5V | Power | 5V Supply, Shared with FC1 |
| SPI1_CS0# | 3 | 1.8V | Output | SPI Bus 1 Chip Select 0 |
| CAN1_N | 4 | 1.8V | Bi-Dir | CAN1 interface |
| SPI1_CS1# | 5 | 1.8V | Output | SPI Bus 1 Chip Select 1 |
| CAN1_P | 6 | 1.8V | Bi-Dir | CAN1 interface |
| SPI1_CLK | 7 | 1.8V | Output | SPI Bus 1 Clock |
| PWRBTN# | 8 | 1.8V | Input | Power Button ***(do not pull-up!)*** |
| SPI1_MISO | 9 | 1.8V | Input | SPI Bus 1 “Master In / Slave Out” |
| RSTBTN# | 10 | 1.8V | Input | Reset Button ***(do not pull-up!)*** |
| SPI1_MOSI | 11 | 1.8V | Output | SPI Bus 1 “Master Out / Slave In” |
| LID# | 12 | 1.8V | Input | Lid Button ***(do not pull-up!)*** |
| SPI0_CS0# | 13 | 1.8V | Output | SPI Bus 0 Chip Select 0 |
| SLEEP# | 14 | 1.8V | Input | Sleep Button ***(do not pull-up!)*** |
| SPI0_CS1# | 15 | 1.8V | Output | SPI Bus 0 Chip Select 1 |
| SPI0_CLK | 16 | 1.8V | Output | SPI Bus 0 Clock |
| SPI0_MISO | 17 | 1.8V | Input | SPI Bus 0 “Master In / Slave Out” |
| SPI0_MOSI | 18 | 1.8V | Output | SPI Bus 0 “Master Out / Slave In” |
| GND | 19 | 0V | Power | Ground, Power return |
| GND | 20 | 0V | Power | Ground, Power return |

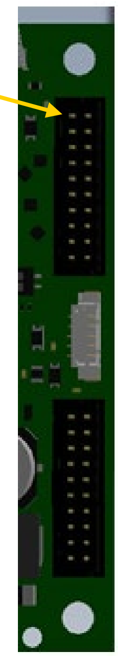
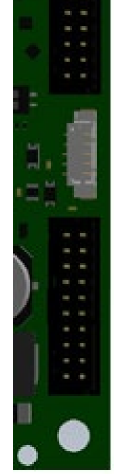



**Table 16 - Feature Connector 2 X1002**

RS232 (SER1 and SER3) is available on Feature Connector 3 (X1001).

| Signal | Pin Number | Signal Level | IN/OUT | Description |
|---|---|---|---|---|
| VCC_3V3 | 1 | 3.3V | Power | 3.3V Supply, fused with 500mA (F1001) |
| GPIO8 | 2 | 1.8V | Bi-Dir | Controlled by SMARC™ GPIO8 (P116) |
| GPIO9 | 4 | 1.8V | Bi-Dir | Controlled by SMARC™ GPIO9 (P117) |
| GPIO10 | 6 | 1.8V | Bi-Dir | Controlled by SMARC™ GPIO10 (P118) |
| GPIO11 | 8 | 1.8V | Bi-Dir | Controlled by SMARC™ GPIO11 (P119) |
| SER1_RX | 10 | RS-232 | Input | UART1 Rx (SER1) |

Pin 1



| Signal | Pin Number | Signal Level | IN/OUT | Description |
|---|---|---|---|---|
| GPIO4 | 11 | 3.3V | Bi-Dir | Controlled by SMARC™ GPIO4 (P112). |
| SER3_RX | 12 | RS-232 | Input | UART3 Rx (SER3) |
| GPIO5 | 13 | 3.3V | Bi-Dir | Controlled by SMARC™ GPIO5 (P113). |
| SER1_TX | 14 | RS-232 | Output | UART1 Tx (SER1) |
| GPIO6 | 15 | 3.3V | Bi-Dir | Controlled by SMARC™ GPIO6 (P114). |
| SER3_TX | 16 | RS-232 | Output | UART3 Tx (SER3) |
| GPIO7 | 17 | 1.8V | Bi-Dir | Controlled by SMARC™ GPIO7 (P115). |
| I2C_CLK | 18 | 3.3V | Output | Connected to “I2C_GP” Bus of SMARC (S48) |
| GND | 19 | 0V | Power | Ground, Power return |
| I2C_DAT | 20 | 3.3V | Bi-Dir | Connected to “I2C_GP” Bus of SMARC (S49) |

**Table 17 - Feature Connector 3 X1001**

SER1 and SER3 support the same features as SER0, but do not support hardware control flow.

| Signal | Pin Type | Signal Level | i.MX8M Plus Ball Number | i.MX8M Plus Ball Name | Power Tolerance | PU/PD | Description |
|---|---|---|---|---|---|---|---|
| SER1_TX | O | 1.8V CMOS | AJ3 | UART1_TXD | 1.8V | PU 10k 1.8V | UART transmit data |
| SER1_RX | I | 1.8V CMOS | AD6 | UART1_RXD | 1.8V | PU 10k 1.8V | UART receive data |
| SER2_TX | O | 1.8V CMOS | AJ4 | UART3_TXD | 1.8V | PU 10k 1.8V | UART transmit data |
| SER3_TX | O | 1.8V CMOS | AH5 | UART4_TXD | 1.8V | PU 10k 1.8V | UART transmit data |
| SER3_RX | I | 1.8V CMOS | AJ5 | UART4_RXD | 1.8V | PU 10k 1.8V | UART receive data |

**Table 18 - UART Signal Description (SER1 & SER3)**

### 5.2.12 SPI Bus

The SMARC SOM offers two Enhanced Configurable SPI (ECSPI) buses with two slave-select signals each. These are available on Feature Connector 2 (X1002) of the SMARC Carrier.

Key features of the ECSPI include:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Two Chip Select (CS) signals to support multiple peripherals
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 64-entry FIFO for both transmit and receive data

- Polarity and phase of the Chip Select (CS) and SPI Clock (SCLK) are configurable
- Direct Memory Access (DMA) support

| Signal | Pin Type | Signal Level | i.MX8M Plus Ball Number | i.MX8M Plus Ball Name | Power Tolerance | PU/PD | Description |
|---|---|---|---|---|---|---|---|
| SPI0_DIN | I | 1.8V CMOS | AD20 | ECSPI1_MISO | 1.8V | | Master Input slave output |
| SPI0_DO | O PP | 1.8V CMOS | AC20 | ECSPI1_MOSI | 1.8V | | Master output slave input |
| SPI0_CK | O PP | 1.8V CMOS | AF20 | ECSPI1_SCLK | 1.8V | | Clock output |
| SPI0_CS0# | O PP | 1.8V CMOS | AE20 | ECSPI1_SS0 | 1.8V | PU 10k 1.8V | Chip-select 0 |
| SPI0_CS1# | O PP | 1.8V CMOS | AA28 | SD1_DATA6 | 1.8V | PU 10k 1.8V | GPIO based Chip-select 1 (SoC GPIO2_IO08) |
| SPI1_DIN | I | 1.8V CMOS | AH20 | ECSPI2_MISO | 1.8V | | Master input slave output |
| SPI1_DO | O PP | 1.8V CMOS | AJ21 | ECSPI2_MOSI | 1.8V | | Master output slave input |
| SPI1_CK | O PP | 1.8V CMOS | AH21 | ECSPI2_SCLK | 1.8V | | Clock output |
| SPI1_CS0# | O PP | 1.8V CMOS | AJ22 | ECSPI2_SS0 | 1.8V | PU 10k 1.8V | Chip-select 0 |
| SPI1_CS1# | O PP | 1.8V CMOS | U25 | SD1_DATA7 | 1.8V | PU 10k 1.8V | GPIO based Chip-select 1 (SoC GPIO2_IO09) |

**Table 19 - SPI Signal Description**

### 5.2.13 I²C Bus

I2C_GP on the SMARC connector is also linked to an on-module EEPROM at address 0x50.

**NOTE: This EEPROM holds the Board Info structure that is required for proper booting. DO NOT delete or alter the first 0x80 bytes of the EEPROM.** Refer to section 8.1 for more details.

For further I²C bus signals see also Camera, LVDS and System Management interfaces.

The I²C bus driven by CPU core function has the following key features:

- Compatible with I2C bus standard
- Multimaster operation
- Software programmability for one of 64 different serial clock frequencies
- Software-selectable acknowledge bit

- Interrupt-driven, byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated Start signal generation
- Acknowledge bit generation/detection
- Bus-busy detection
- Data rates up to 100kbits/s in Standard mode and 400kbits/s in Fast mode

| Signal | Pin Type | Signal Level | i.MX8M Plus Ball Number | i.MX8M Plus Ball Name | Power Tolerance | PU/PD | Description |
|---|---|---|---|---|---|---|---|
| I2C_GP_CK | O OD | 1.8V CMOS | AC8 | I2C1_SCL | 1.8V | PU 2.2k 1.8V | General purpose I²C clock output |
| I2C_GP_DAT | I/O OD | 1.8V CMOS | AH7 | I2C1_SDA | 1.8V | PU 2.2k 1.8V | General purpose I²C data I/O |

Table 20 - I²C Signal Description

#### *5.2.13.1 I2C Bus Address Mapping*

| SoC Interface | Device | SMARC Interface | 7-bit Address |
|---|---|---|---|
| I2C6 | TPM | | 0x2E |
| | PMIC | | 0x30 |
| | Temp. Sensor | | 0x71 |
| | RTC | | 0x32 |
| | PCIe Clock Generator | | 0x6B |
| | IO Expander | | 0x20 |
| I2C2 | | I2C_PM | |
| I2C1 | EEPROM | I2C_GP | 0x50 |
| I2C3 | | I2C_LCD | |
| I2C4 | | I2C_CAM0 | |
| I2C5 | | I2C_CAM1 | |

Table 21 - I²C Interface Overview

### 5.2.14 Watchdog Timer

| Signal | Pin Type | Signal Level | i.MX8M Plus Ball Number | i.MX8M Plus Ball Name | Power Tolerance | Description |
|---|---|---|---|---|---|---|
| WDT_TIME_OUT# | O PP | 1.8V CMOS | B6 | GPIO1_IO02 | 1.8V | Watchdog timer output from the SoC. |

Table 22 - Watchdog Signal Description

### 5.2.15 System Management

| Signal | Pin Type | Signal Level | i.MX8M Plus Ball Number | i.MX8M Plus Ball Name | Power Tolerance | PU/PD | Description |
|---|---|---|---|---|---|---|---|
| VIN_PWR_BAD# | I OD | 1.8V | | | 5.0V | PU 200K Vin<br>PD 82K | Pulled low at carrier until external power supply is ready.<br>Do not connect any Pull-down or Pull-up resistors on carrier. |
| CARRIER_PWR_ON | O PP | 1.8V CMOS | | | 1.8V | | Carrier board circuits should not be powered up until module asserts this signal. |
| CARRIER_STBY# | O PP | 1.8V CMOS | | | 1.8V | | Module asserts this signal to indicate standby power state. |
| RESET_OUT# | O PP | 1.8V CMOS | AJ15 | SAI2_MCLK | 1.8V | PD 10k | General purpose reset for carrier board. (SoC GPIO4_IO27) |
| RESET_IN# | I OD | 1.8V CMOS | | | 1.8V | PU 1k 1.8V | Reset input from Carrier board. Carrier drives low to force a Module reset, floats the line otherwise. |
| POWER_BTN# | I | 1.8V CMOS | | | 1.8V | PU 100k 1.8V | Power button to bring system into a power state. Do not connect any Pull-down or Pull-up resistors on carrier. |
| SLEEP# | I OD | 1.8V CMOS | | | 1.8V | PU 10k 1.8V | Sleep indicator from Carrier board. |
| I2C_PM_CK | O OD | 1.8V CMOS | AH6 | I2C2_SCL | 1.8V | PU 2.2k 1.8V | Power management I²C clock output |
| I2C_PM_DAT | I/O OD | 1.8V CMOS | AE8 | I2C2_SDA | 1.8V | PU 2.2k 1.8V | Power management I²C data I/O |

**Table 23 - System Management Signal Description**

# 6 Touch Display

This section describes the specifications of the included 10.1” display.

The display features the following:

- 10.1 (16:9) inch active display area with WVGA (1280 by 800 pixel) resolution
- 16M colors (R, G, B 8 bit digital each)
- LCD Type: transmissive, normally black
- Pixel Pitch: 0.1695 x 0.1695 mm
- Brightness: 425cd/m²
- Display Interface: LVDS interface with JILI30 connector

- Backlight Interface
- PCAP touch screen with USB touch controller
- Multi-finger touch, no need for calibration

# 7 Power

## 7.1 Main Power In

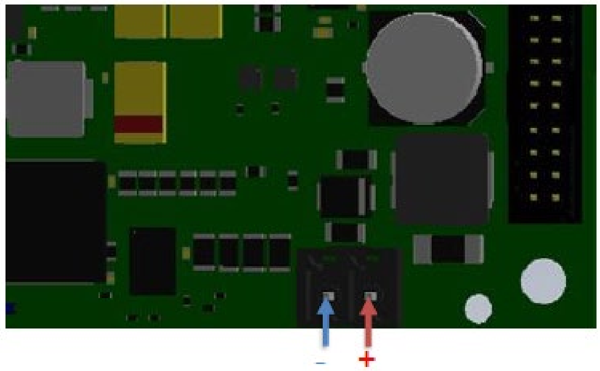



**Figure 22 - Main Power In via 2pin Würth connector (X1401)**

The included power supply is the Netzteil 12VDC/3.34A 3% 90-264VAC.

- Power supply via 2pin Würth WR-TBL connector Pitch 3.81mm
- Optional Preregulator for 12.6V-36V
- Input power range without Preregulator 12V +/-10%
- 3V RTC Backup Supply by Button Cell Battery 2032.

The power cable is provided in the kit, along with a 12V, 3.34A power supply and wall adapter.

## 7.2 i.MX8M Plus SMARC SOM Power Consumption

### 7.2.1 Electrical Specifications

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VDD_IN | Main power supply | 4.3 | 5 | 5.5 | V |
| VDD_RTC | Backup supply for timekeeping [1] | 1.1 | 3 | 3.3 | V |
| IDD_RTC | Current consumption for timekeeping | - | 100 | 360 | nA |
| RTC Accuracy | RTC timekeeping accuracy [2] | - | 14 | - | ppm |
| USB0_VBUS_DET | USB host port 0 power detection | 3.3 | 5 | 5.5 | V |
| USB3_VBUS_DET | USB host port 3 power detection | 3.3 | 5 | 5.5 | V |

**Table 24 - Module electrical specifications**

[1] May be source from a lithium cell or a super cap.
[2] At room temperature approx. 23°C.

### 7.2.2 Use Cases

- Uboot Idle: without ethernet, no display used, no USB devices. CPU running at 1200MHz

- Linux Idle: without ethernet, no display used, no USB devices. CPU running at 1200MHz

- Linux Heavy Load: CPU load 100% on each core, memory tester, HDMI, LVDS display and Ethernet traffic generated with iperf. CPU running at 1600MHz.

- Suspend to RAM: most efficient power saving mode, all unnecessary power supplies turned off, memory placed into self-refresh, wake on power button press.

### 7.2.3 Measurement Results

| Use Cases | | | | |
|---|---|---|---|---|
| **Uboot Idle** | **Linux idle** | **Linux Heavy Load** | **Suspend** | **Unit** |
| 2.60 | 1.98 | 5.30 | 0.44 | W |

**Table 25 - Peak Power Consumption**

## 7.3 i.MX8M Plus SMARC SOM Power-Up Behavior

The SOM will behave in the following ways:

- When coming from complete power off (5V unpowered), the module will boot if VIN_PWR_BAD# is de-asserted and 5V is present.

- When OS is shut down and 5V is still powered, a power button press is required to restart the module.

- On keeping the power button pressed for 8 seconds or longer, the module will shut down and restart as soon as the power button is pressed again.

### 7.3.1 Power-On Sequencing

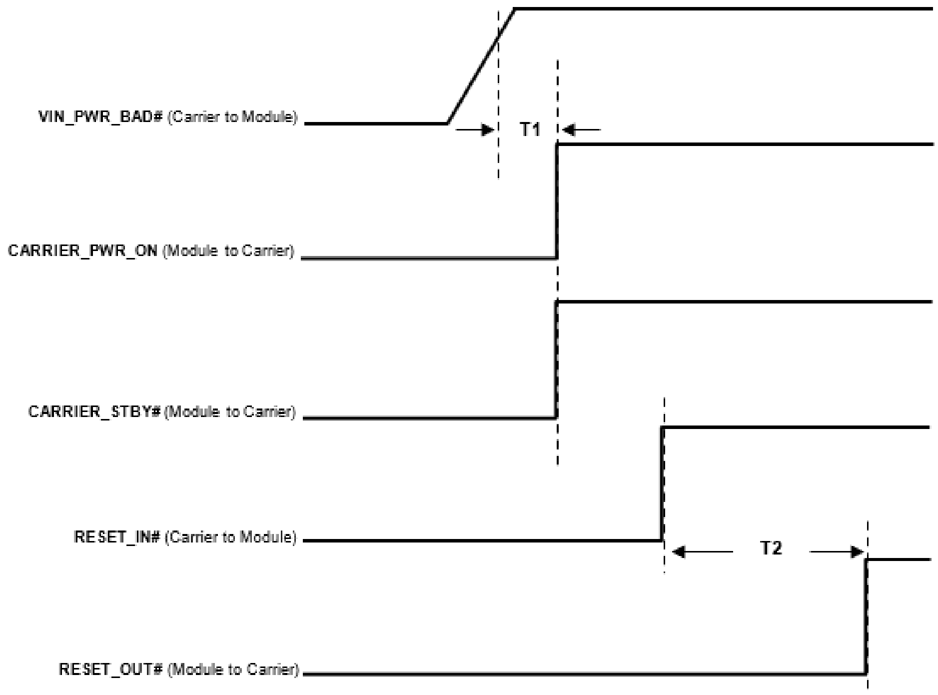



Figure 23 - Start-up sequence with asserted RESET_IN#

| Time Slot | Description | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| T1 | CARRIER_PWR_ON to VIN_PWR_BAD# timing | - | 24.1 | - | ms |
| T2 | RESET_OUT# [1] to RESET_IN# timing | - | 140 | - | ms |

Table 26 - Power-On timings with asserted RESET_IN#

[1] General purpose reset output. Connected to SoC GPIO.

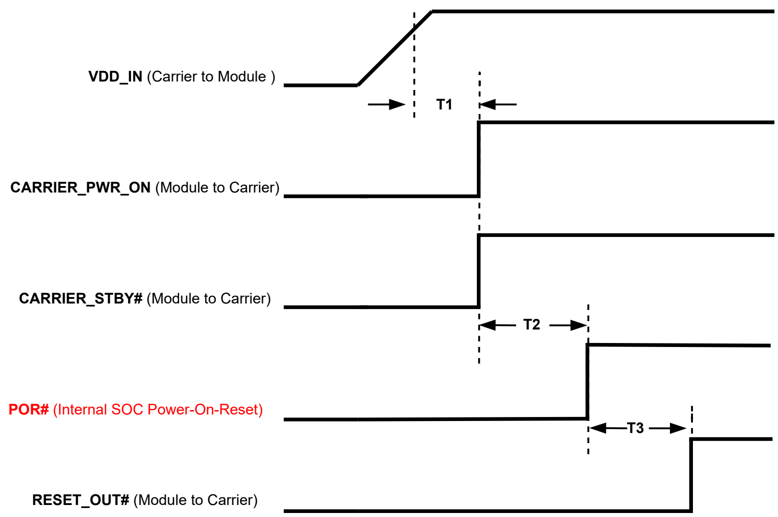



Figure 24 - Start-up sequence with de-asserted2 RESET_IN#

| Time Slot | Description | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| T1 | CARRIER_PWR_ON to VIN_PWR_BAD# timing | - | 24.1 | - | ms |
| T2 | POR#  to CARRIER_PWR_ON timing | - | 128 | 140 | ms |
| T3 | RESET_OUT# [1] to POR# timing | - | 136 | - | ms |

Table 27 - Power-On timings with de-asserted 2 RESET_IN#

[1] General purpose reset output. Connected to SoC GPIO.
[2] REST_IN# input kept floating.

### 7.3.2 Reset Behavior

Assertion of RESET_IN# signal resets SoC without a power cycle.

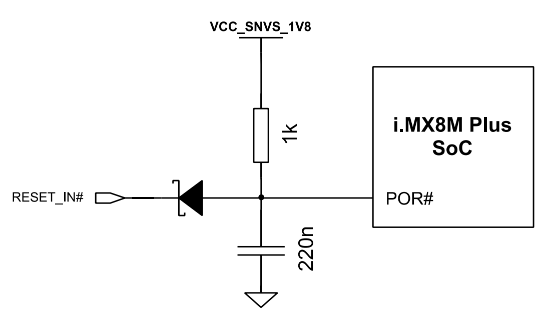



Figure 25 - Reset Circuit

# 8 Configuration and Debug

## 8.1 EEPROM

The 64Kb EEPROM on address 0x50 of the I2C_GP bus (at address 0x50) holds the board Information (boardinfo) structure, which is evaluated by U-Boot to determine the exact board variant and set necessary parameters.

**WARNING: Make sure to leave this EEPROM and the boardinfo content in place, and DO NOT block address 0x50 on the I2C_GP bus with other devices, otherwise the module will be unable to boot!**

The board information structure occupies the first 0x80 bytes. The remaining upper range starting at offset 0x80 is freely available for customer purposes. When making use of this option, make sure to keep the lower 0x80 bytes intact, otherwise the board will not be able to boot!

## 8.2 Boot Selection

The Edge AI Kit supports booting from SD Card, network boot (ethernet), from eMMC Flash, or via USB. The desired boot mode can be selected via a 4 pole Dipswitch located next to the microUSB port on the SMARC Carrier.

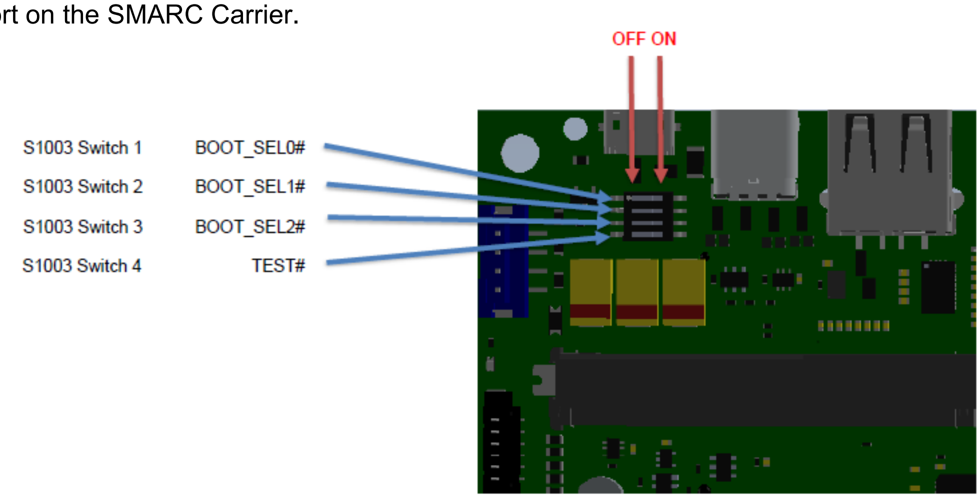



**Figure 26 - Boot Selection**

The following table describes the available boot options for the Edge AI Kit. See the i.MX 8M Plus Applications Processor Reference Manual from NXP for a complete description.

| Boot Source | BOOT_SEL2# | BOOT_SEL1# | BOOT_SEL0# |
|---|---|---|---|
| Carrier SD Card | ON (GND) | ON (GND) | OFF (Float) |
| Remote Device (ethernet boot) | OFF (Float) | ON (GND) | OFF (Float) |
| module eMMC Flash | OFF (Float) | OFF (Float) | ON (GND) |
| USB Mass Storage | OFF (Float) | OFF (Float) | OFF (Float) |

**Table 28 - Available Boot Options**

For DIP #4 (TEST#) -- Booting SPL (secondary program loader)/U-Boot:

If TEST# = HIGH (DIP Switch = OFF), the i.MX8M Plus Boot ROM code uses the module eMMC flash as primary and the Carrier SD card as secondary (fallback) boot media. The fall back media is always selected, when booting from primary media is not possible (empty, corrupted, etc.)

If TEST# = LOW (DIP Switch = ON), the i.MX8M Plus Boot ROM code uses the Carrier SD card as boot media regardless of whether the module eMMC flash contains a properly programmed system image or not.

## 8.3 Serial Debugging

The kit comes with an RS-232 cable that plugs directly into the RS232 connector on the SMARC Carrier (X1102).

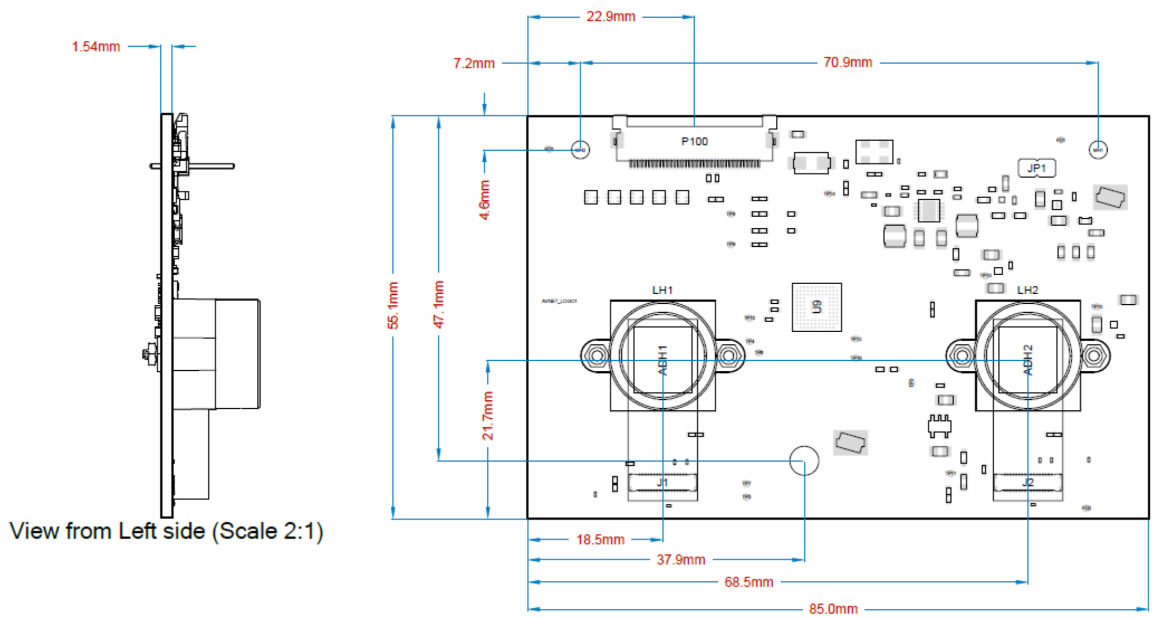
Additionally, you will need a D-SUB 9-pin "null-modem" (Tx/Rx crossed) female-female cable. You will also need an RS-232 to USB cable (if your PC doesn't have a native serial port).

# 9 Specifications and Ratings

## 9.1 Product Dimensions (in mm)

### 9.1.1 Product Dimensions for onsemi SMARC Camera Adapter

- Dimensions: 85 mm x 55.1 mm
- Board thickness: 1.54 mm




View from Left side (Scale 2:1)

View from Top side (Scale 2:1)

**Figure 27 - SMARC Camera Adapter Dimensions**

### 9.1.2 Product Dimensions for i.MX 8M Plus SMARC SOM

- SMARC Short Size formfactor: 82mm x 50mm
- Distance between mounting holes: 68mm

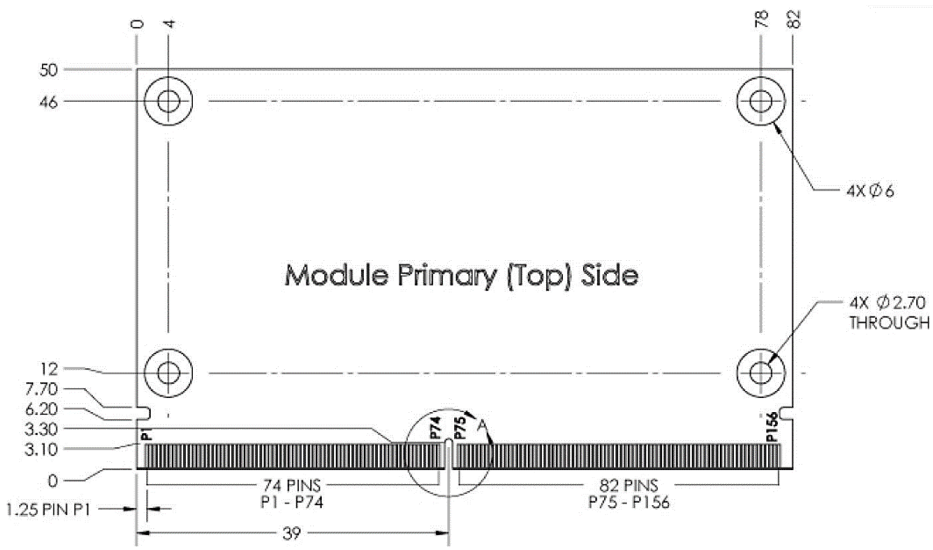



Figure 28 – SMARC SOM Dimensions

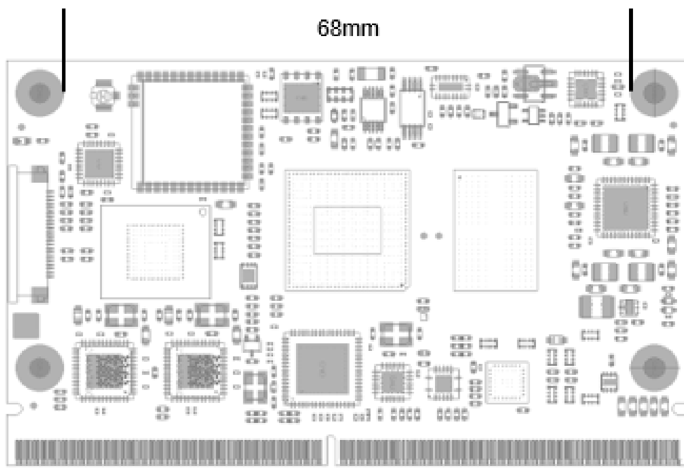



Figure 29 - Distance between mounting holes

### 9.1.3 Product Dimensions for the EP5 SMARC Carrier Board

- Dimensions: 146 mm x 80 mm
- Board thickness: 1.6 mm +/- 10%
- Drill hole positioning tolerance: +/- 0.1 mm in X and Y
- Drill hole diameter tolerance: +0.1 mm
- Max height of component on TOP side: RJ45 with 13.30 mm (+/- 0.15 mm, EMI shield fingers not included)
- Max height of component on BOTTOM side: Latch for miniPCIe card and M.2 SATA card with 11.90 mm (+/- 0.35 mm)

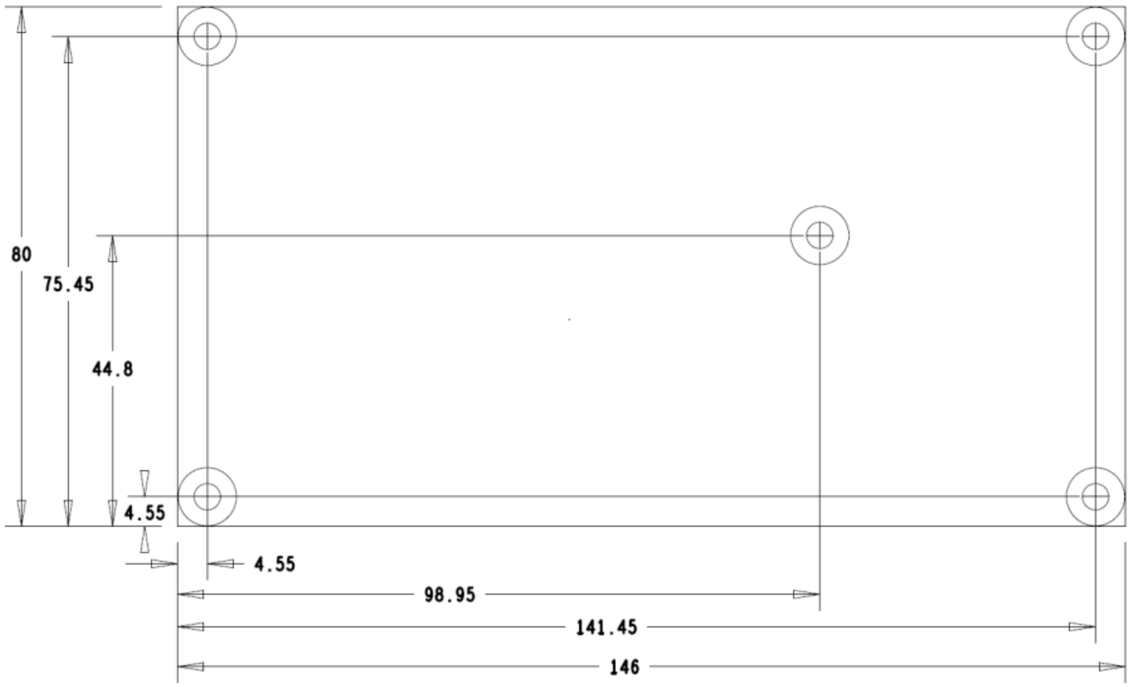



**Figure 30 - SMARC Carrier Board Dimensions**

## 9.2 Temperature and Humidity Ratings

Temperature Range:

- 0°C to +70°C operating commercial
- -40°C to +85°C operating extended
- -40°C to +85°C storage

Humidity:

- 5 to 95% (operating, non-condensing)
- 5 to 95% (storage, non-condensing)

## 9.3 Thermal Specification for i.MX8M Plus SMARC SOM

The cooling solution for a SMARC SOM is based on a heat spreader or heat-sink concept. The kit ships with the SMARC passive heatsink (SM2S-IMX8PLUS-01 HSI-001) that can be mounted on top of the SOM using the screws provided. It consists of a single-piece aluminum pin cooler and thermal pad for contact to the processor.

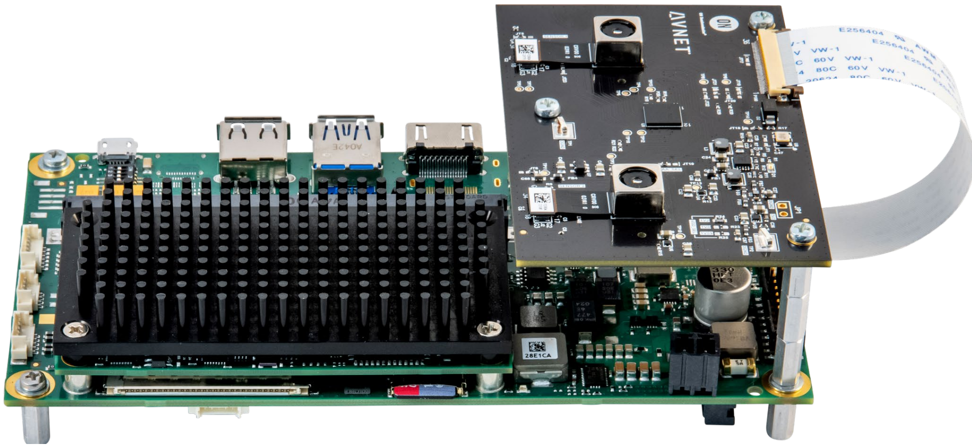


Figure 31 - Edge AI Kit with heatsink attached

The main goal for the thermal design of a system is that each device on the SOM is operated within its specified thermal limits. There may be system implementations where the heat spreader temperature could be higher. In such a case the cooling solution design should be validated such that the thermal specifications of all the components on the SOM are not violated across the system operating temperature range even under worst case conditions.

### 9.3.1 Mechanical Distortion of PCB

For thermal heat dissipation the heat sink needs to have a good mechanical contact to the CPU housing which means the heat sink should be mounted with some mechanical stress applied. The higher the force applied, the better the thermal resistance and consequently the better the thermal cooling. This pressure may result in a slight mechanical bending of the SMARC SOM PCB.

Production tolerance, material deviation and thermal expansion lead to a range of possible pressure range and bending. A negative pressure with an air gap between the heat spreader and the chip case needs to be avoided and likewise too much distortion.

The bending needs to be less than 1mm over 90mm. (1.11%) → 0.75mm

### 9.3.2 Thermal Definitions

The stabilized temperature measured on the heat spreader and the SMARC SOM PCB during runtime mostly depends on the computing power demand from the application and the cooling solution implemented in the system. It is the responsibility of the system designer to provide a cooling solution in addition to the heat spreader that fulfils the requirements of the application.

The temperature at the defined point on the PCB shall not exceed the temperature range in the following table.

| Tpcb_min | Tpcb_max |
|---|---|
| - 40 °C | + 85 °C |

Table 29 - Temperature Range

**Tpcb** This is the temperature on the surface of the module PCB at point P.

**Tpcb_max** + 85 °C The maximum temperature allowed for the surface of the module PCB at point P.

**Tpcb_min** - 40 °C This is defined as the minimum temperature allowed for the surface of the module PCB.

**P** The point on the module PCB where the PCB temperature must be measured.

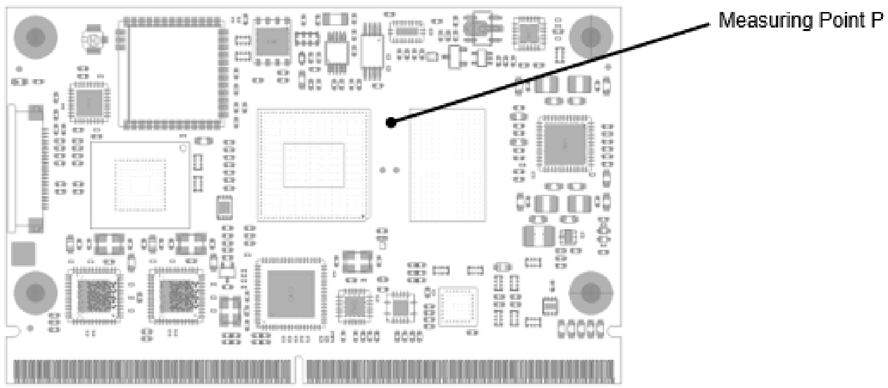



Figure 32 - Defined Temperature Point

# 10 Software

To download operating system images, visit http://avnet.me/imx8mplus-edgeai and select "Reference Designs" to download the out of box Yocto image.

To access the board support package (BSP) to build your own Yocto image for the Edge AI Kit, contact support.boards@avnet.com. In your email, please clearly state that you are working with the Edge AI Kit and would like that BSP.

NXP provides Machine Learning example code as part of its eIQ software. To download eIQ, and view NXP's reference material, visit nxp.com/eiq.

# 11 Getting Help and Support

If additional support is required, Avnet has many avenues to search depending on your needs.
For a project showing how to assemble the kit and get started project, please visit http://avnet.me/edgeai-kit-start.

You can find documentation, application examples, and other supporting documentation at our website at https://avnet.me/imx8mplus-edgeai.

Detailed questions regarding the i.MX 8M Plus Edge AI Kit hardware design, software application development, using NXP tools, training and other topics can be posted on the i.MX 8M Plus Edge AI Support Forums at http://avnet.me/imx8mplus-edgeai-forums. Avnet's technical support team monitors the forum during normal business hours in North America.

Those interested in customer-specific options on the i.MX 8M Plus Edge AI Kit or SMARC embedded computing platform can send inquiries to customize@avnet.com.