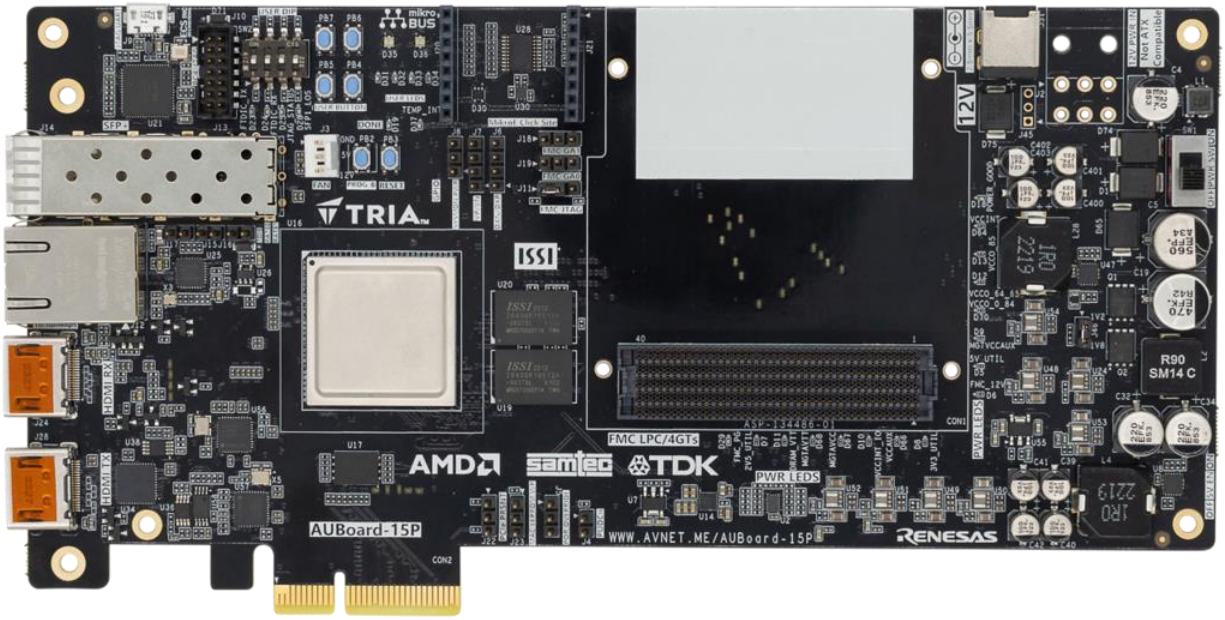
AUBOARD 15P



AUBoard-15P Development Kit
Hardware User Guide

Version 1.4

LIT# AUB-15P-DK-UG-V1P2

Contents

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1 Document Control

Document Version: 1.2

Document Date: 16 January 2025

2 Version History

Version	Date	Comment
1.0	08/29/2024	Initial Release
1.1	09/13/2024	Update DDR4 Info
1.2	01/16/2025	Production Photos
1.3	02/05/2025	Updated Website Links
1.4	06/10/2025	Updated AMD Branding and temp

3 Introduction

The AUBoard-15P Development Kit is an AMD Artix™ UltraScale+™ FPGA PCIe Gen4 x4 board targeted for broad use in many applications:

- Offer an AMD based Development Kit for engineers to adopt in development, proof-of-concept, and production projects.
- Combine programmable logic designs with a MicroBlaze soft microprocessor core in a convenient and expandable board.
- Allow expansion to a variety of sensors and peripherals through the Mikroe Click Board and FMC (FPGA Mezzanine Card) expansion connectors.
- Target many applications for development, including:
    - Embedded Vision
    - Embedded Processing
    - Industrial Networking
    - Wired Communications
    - Prototyping and Experimentation

3.1 Reference Documents

[1] **UltraScale Architecture and Product Datasheet: Overview DS890**

[2] **Artix UltraScale+ DC and AC Switching Characteristics DS931**

[3] **UltraScale+ Device Packaging and Pinout Product Specification UG575**

[4] **UltraScale Architecture PCB Design Guide UG583**

[5] **UltraScale Architecture SelectIO Resources UG571**

[6] **UltraScale Architecture Configuration User Guide (UG570)**

[7] **FFVB676 Package File**

[8] **AMD Vivado™ Design Suite**

[9] **AMD Vitis™ Unified Software Platform**

[10] **ISSI DDR4 SDRAM Product Page**

[11] **ISSI QSPI Flash Product Page**

[12] **Renesas FemtoClock™ NG Universal Frequency Translator**

[13] **Mikroe Click Boards Standards Specifications**

4 Architecture and Features

The AUBoard-15P Development Kit provides a hardware environment for developing designs targeting the AMD Artix™ UltraScale+™ XCAU15P-2FFVB676E FPGA. The AUBoard-15P Development Kit provides features common to many systems including DDR4 memory, a 4-lane PCI Express® interface, 10/100 Ethernet PHY, general purpose I/O, and UART interfaces. The details for the AUBoard-15P Development Kit features are described in Functional Description sections that follow.

4.1 List of Features

The AUBoard-15P Development Kit supports the following features:

- AMD Artix UltraScale+ FPGA **XCAU15P-2FFVB676E**
- Memory/Storage
  - ISSI 2 GB (512 x 32) DDR4 Memory
    - Part Number: **IS43QR16512A-083TBL**
  - ISSI 64 MB (64 x 8) Nor Flash Memory
    - Part Number: **IS25WP512M-JLLE**
- PCIe Gen4 4-lane (x4) Compatible Connectivity
- SFP+ Card Cage and Optical Module
  - TE Connectivity Optical Module
    - Part Number: **1888247-1**
  - TE Connectivity Cage
    - Part Number: **2007194-1**
- HDMI TX and RX Interfaces
- 10/100 Ethernet
  - Microchip 10/100 Base-T/TX Ethernet Transceiver
    - Part Number: **KSZ8091MNXIA**
- FMC (FPGA Mezzanine Card) Expansion Site
  - Mixed LPC (Low Pin Count) and Gigabit Transceivers
    - Samtec Connector Part Number: **ASP-134486-01**
- MikroE Click Expansion Site
    - Samtec Connector Part Number: **SSW-108-01-F-S**
- Clock Generation
  - Renesas FemtoClock™ NG Universal Frequency Translator
    - Part Number: **8T49N241-998NLGI**
- I2C Bus MAC ID EEPROM, Expander, and Temperature Sensor
  - I2C MAC ID / EEPROM Part Number: **AT24MAC402-XHM-B**
  - I2C Expander Part Number: **PCA9544APW,118**
  - I2C Temperature Sensor Part Number: **STTS22HTR**
- microUSB JTAG and USB-to-UART Debug Interface
- Voltage Regulators
  - Renesas Multi-topology and Buck Regulator / Converter
    - Part Number: **ISL8130IRZ**
    - Part Number: **ISL85014FRZ**
  - TDK Buck Regulator / Converter
    - Part Number: **FS1406-0600-AS**
    - Part Number: **FS1404-3300-AS**
- Power Sequencer
  - Renesas GreenPak™ Custom Power Sequencer
    - Part Number: **SLG7AV46723V**

4.2 Block Diagram

The following figure is a high-level block diagram of the AUBoard-15P Development Kit and the peripherals attached to the Artix UltraScale+ FPGA.

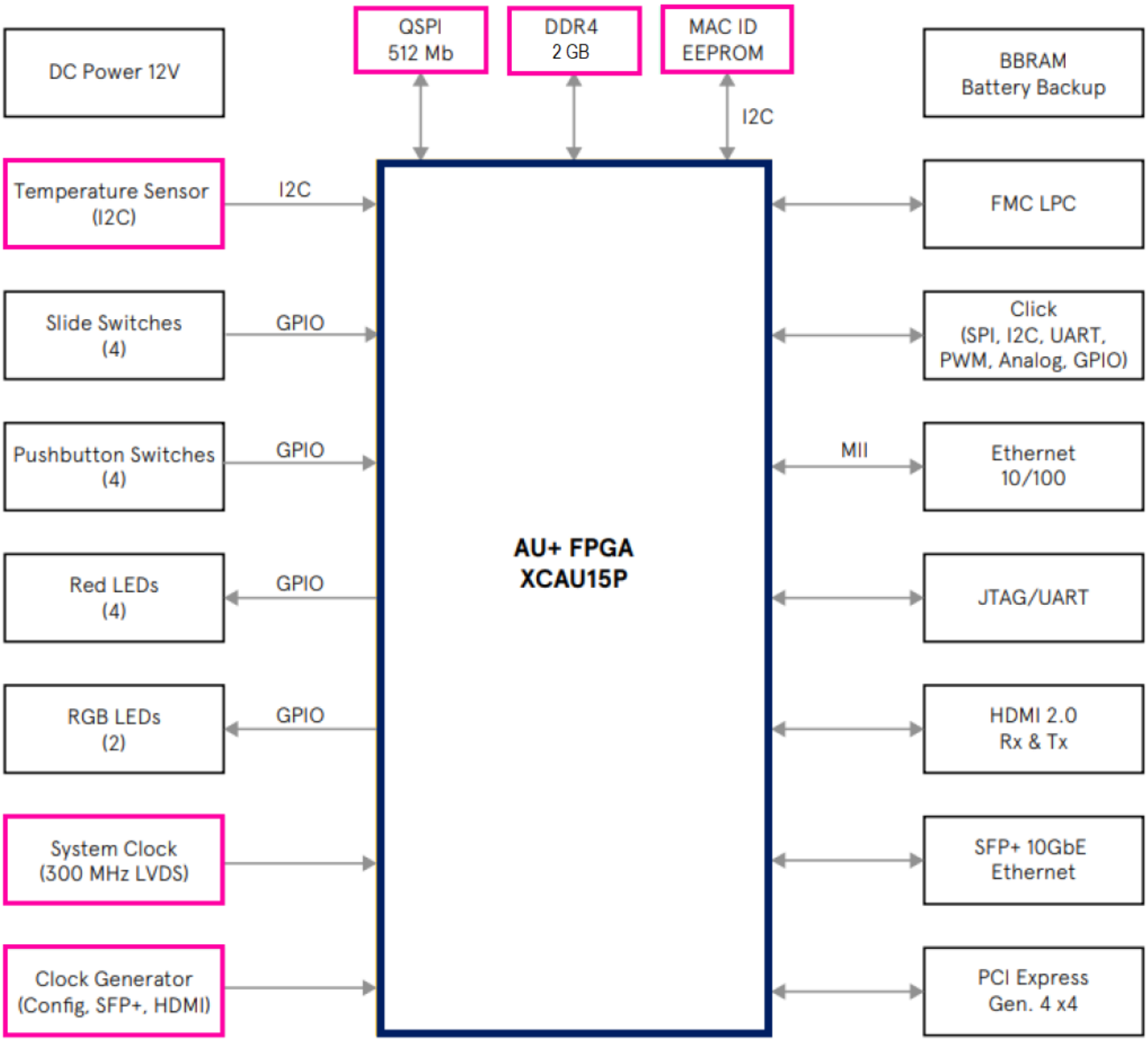

Figure 1 –Development Kit Block Diagram

5 Functional Description

The following sections provide brief descriptions of each feature provided on the AUBoard-15P Development Kit.

5.1 Artix UltraScale+ FPGA

AUBoard-15P Development Kit features an AMD Artix™ UltraScale+™ FPGA XCAU15P-2FFVB676E device (-2 Speed Grade, FFVB676 Package, -E Extended Temperature Grade).

The AU15P-FFVB676 features the following resources:

- 156 High Performance I/O (52 I/O x 3 banks)
- 72 High Density (24 I/O x 3 banks)
- 3 Clock Management Tiles (CMT) (1 MMCM, 2 PLLs)
- 1 System Monitor (SYSMON) interface
- 12 GTH transceivers
- 6 Transceiver PLLs
- 1 PCIE4C block

The following diagram lists the AUBoard-15P Development Kit device package diagram followed by a diagram of the XCAU15P device available banks.

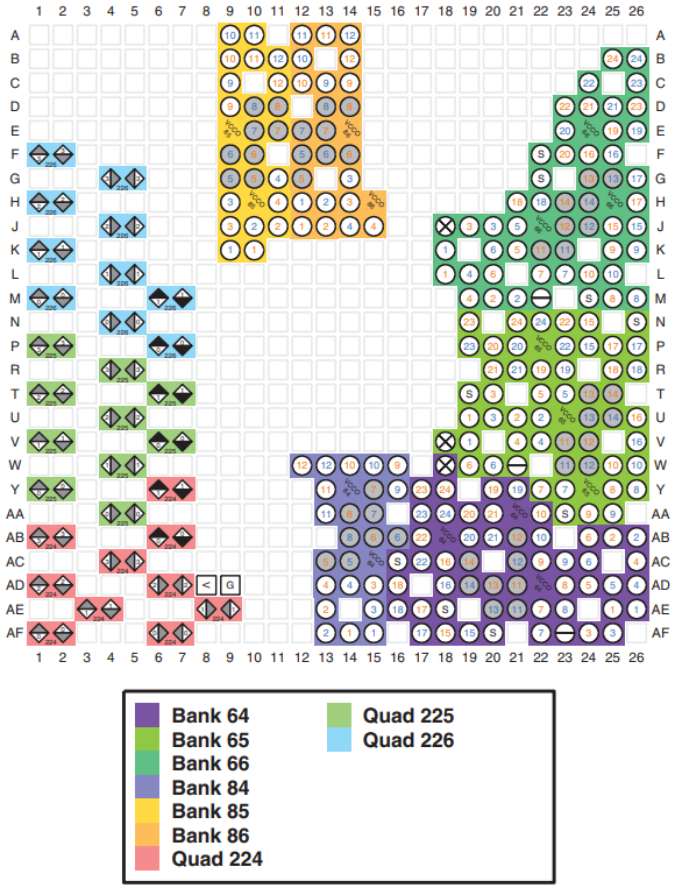

Figure 2 – FFVB676 Package Diagram

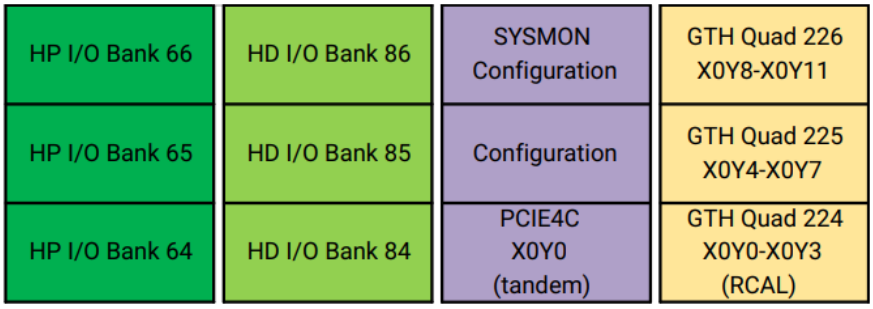

Figure 3 – XCAU15P Bank Diagram

5.1.1 FPGA Configuration

The FPGA is configured through Bank 0 which consists of QSPI, JTAG, System Monitor (SYSMON), and Encryption Key Backup Circuit interfaces.

The AUBoard-15P Development Kit supports two FPGA configuration modes:

- Master SPI flash memory using the onboard Quad SPI flash memory.
- JTAG using a standard-A to micro-B USB cable for connecting the host PC to the AUBoard-15P Development Kit configuration port or by J10 Platform Cable USB/Parallel Cable IV flat cable connector.

Each configuration interface corresponds to one or more configuration modes and bus widths as listed in Table 1. The default mode setting is **M[2:0] = 001**, which selects Master SPI flash memory at board power-on.

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master SPI Flash Memory	001	x1, x2, x4	Output
JTAG	Override	x1	Not Applicable

Table 1 – FPGA Configuration Modes

5.1.2 Configuration Support

The AUBoard-15P has headers and a push button on the board which provides support for configuration options of the XCAU15P FPGA. The headers are tied to pins on the FPGA that control the PUDC_B and POR_OVERRIDE settings of the FPGA. The push button is tied to a pin on the FPGA that controls the PROGRAM_B function of the FPGA.

The UltraScale+ FPGAs contain a pin called PUDC_B (Pull Up During Configuration). When PUDC_B is Low, internal pull-up resistors are enabled on each SelectIO pin. When PUDC_B is High, internal pull-up resistors are disabled on each SelectIO pin. The state of this pin effects the state of the I/O from power-on until configuration completes. Therefore, the I/Os will be 3-stated after power-on when PUDC is High.

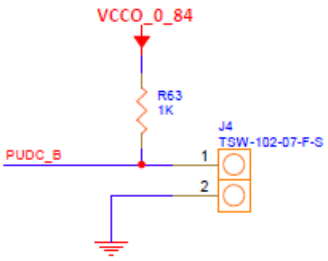

Figure 4 – PUDC_B Header

The UltraScale+ FPGAs contain a pin called POR_OVERRIDE (Power On Reset Override) that is used to override the power on reset delay. The Power On Reset Override select (POR_OVERRIDE) pin must be set High or Low to determine the power-on delay before configuration begins. The POR delay is shortened as specified in the data sheet (fast POR counter) with the POR_OVERRIDE pin tied high. When the POR_OVERRIDE pin is Low (e.g., connected to GND), the POR delay is longer (slow POR counter).

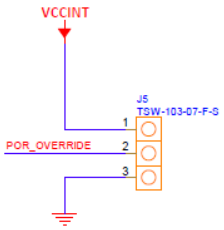

Figure 5 – POR_OVERRIDE Header

The UltraScale+ FPGAs contain a pin called PROGRAM_B that is used as an Active-Low reset to the configuration logic. When PROGRAM_B is pulsed Low, the FPGA configuration is cleared, and a new configuration sequence is initiated. Configuration reset is initiated upon the falling edge, and the configuration (i.e. programming) sequence begins upon the following rising edge. PROGRAM_B can externally be held Low during power-up to stall the power-on configuration sequence at the end of the initialization process. If PROGRAM_B is held Low, JTAG operations can be restricted. Dedicated pins remain disabled while PROGRAM_B is held Low.

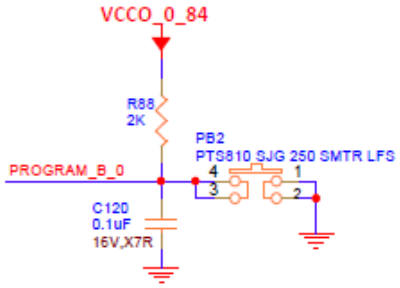

Figure 6 – PROGRAM_B Push Button

5.1.3 System Monitor

The Artix UltraScale+ architecture supports an on-chip system monitor. SYSMON monitors the physical environment via on-chip temperature and supply sensors with integrated analog-to-digital converters (ADC). An overview of the System Monitor primitive, SYSMON, is provided by AMD User Guide UG580 – UltraScale Architecture System Monitor.

On-board there is an option to select an internal or external reference voltage for the SYSMON interface via jumper J8. Shunting J8 from pin 1 to pin 2 selects the external shunt 1.25V voltage reference from STMicroelectronics with part number TS4061AICT-1.25. Shunting J8 from pin 3 to pin 1 selects the internal voltage reference.

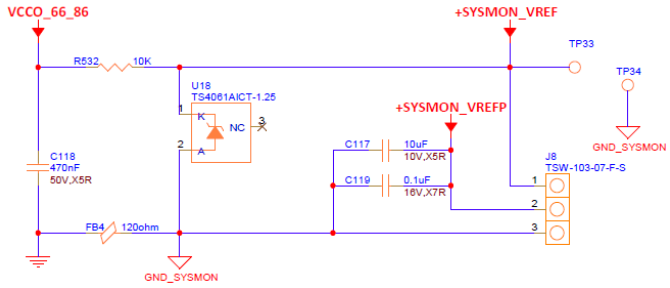

Figure 7 – SYSMON Voltage Reference Select

The AUBoard-15P Development Kit supports System Monitor functionality through SYSMON headers. The SYSMON_DX_P/N pins on FPGA U16 are provided on header J6 and the SYSMON_VP and SYSMON_VN pins on FPGA U16 are provided on header J7. See schematic for implementation of the SYSMON interfaces to headers J6 and J7.

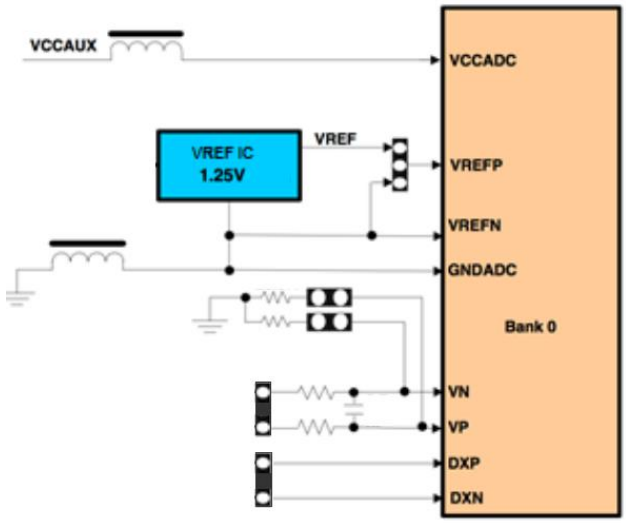

Figure 8 – SYSMON Interface Block Diagram

5.1.4 Battery Backup Circuit

The Artix UltraScale+ FPGA, U16, implements bitstream encryption key technology. The AUBoard-15P Development Kit provides the encryption key backup battery circuit. The rechargeable 1.5V lithium button-type battery, BAT1, is to be soldered to the board with the positive output connected to the Artix UltraScale+ FPGA, U16, VCCBATT pin Y9. BAT1 is charged from the **+VCCO_0_84** +1.8V rail through a series diode and a 4.7 kΩ current limit resistor.

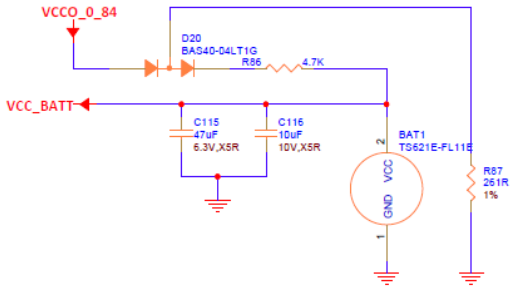

Figure 9 – Battery Backup Circuit

NOTE: The 1.5V lithium button-type battery, BAT1, is not installed and if this function is desired the proper battery must be procured and installed by the end user. The 1.5V lithium button-type battery is a Seiko Instruments TS621E-FL11E.

5.1.5 DDR4 Memory

The DDR4 memory implemented with devices at U19 and U20 is 2GB (512 x 32) DDR4 from manufacturer ISSI. It provides volatile synchronous dynamic random-access memory (SDRAM) for storing user code and data.

- Manufacturer: ISSI
- Part Number: IS43QR16512A-083TBL
- Configuration: 2GB (512Mb x 32)
- Supply Voltage: +1.2V
- Data Path Width: 32-bits
- Data Rate: Up to 2,400 Mb/s

The AUBoard-15P Development Kit FPGA memory interface performance is documented in the Artix UltraScale+ FPGAs Data Sheet: DC and AC Switching Characteristics (DS931).
The DDR4 interface is connected to the XCAU15P device HP banks 64 and 65.

The DDR4 0.60V VTT termination voltage (net **+DRAM_VREF)** is sourced from an **OnSemi NCP51402MNTXG.** Any additional interface connected to these banks that requires a reference voltage must use the VTT termination voltage as its reference. The connections between the DDR4 memories and the XCAU15P device banks 64 and 65 are listed in Table 2.

FPGA (U16) Pin	Schematic Net Name	I/O Standard	DDR4 Pin Number	DDR4 Pin Name	DDR4 REF DES
Y21	DDR4_ACT_N	SSTL12	L3	ACTn	U19, U20
AE22	DDR4_A0	SSTL12	P3	A0	U19, U20
AF22	DDR4_A1	SSTL12	P7	A1	U19, U20
AD23	DDR4_A2	SSTL12	R3	A2	U19, U20
AE23	DDR4_A3	SSTL12	N7	A3	U19, U20
AC22	DDR4_A4	SSTL12	N3	A4	U19, U20
AC23	DDR4_A5	SSTL12	P8	A5	U19, U20
AB21	DDR4_A6	SSTL12	P2	A6	U19, U20
AC21	DDR4_A7	SSTL12	R8	A7	U19, U20

AF20	DDR4_A8	SSTL12	R2	A8	U19, U20
AD20	DDR4_A9	SSTL12	R7	A9	U19, U20
AE20	DDR4_A10	SSTL12	M3	A10/AP	U19, U20
AC19	DDR4_A11	SSTL12	T2	A11	U19, U20
AD19	DDR4_A12	SSTL12	M7	A12/BCn	U19, U20
AF18	DDR4_A13	SSTL12	T8	A13	U19, U20
AF19	DDR4_ADR14/WE_N	SSTL12	L2	WEn/A14	U19, U20
AC18	DDR4_ADR15/CAS_N	SSTL12	M8	CASn/A15	U19, U20
AD18	DDR4_ADR16/RAS_N	SSTL12	L8	RASn/A16	U19, U20
AE17	DDR4_BA0	SSTL12	N2	BA0	U19, U20
AF17	DDR4_BA1	SSTL12	N8	BA1	U19, U20
AD16	DDR4_BG	SSTL12	M2	BG0	U19, U20
AA22	DDR4_CK_T	DIFF_SSTL12_DCI	K7	CK	U19, U20
AB22	DDR4_CK_C	DIFF_SSTL12_DCI	K8	CKn	U19, U20
AE18	DDR4_CKE	SSTL12	K2	CKE	U19, U20
AE16	DDR4_CS_N	SSTL12	L7	CSn	U19, U20
AE25	DDR4_DM_N0	POD12_DCI	E7	LDMn/LDBIn	U19
Y20	DDR4_DM_N1	POD12_DCI	E2	UDMn/UDBIn	U19
U19	DDR4_DM_N2	POD12_DCI	E7	LDMn/LDBIn	U20
Y22	DDR4_DM_N3	POD12_DCI	E2	UDMn/UDBIn	U20
AB25	DDR4_DQ0	POD12_DCI	G2	DQ0	U19
AB26	DDR4_DQ1	POD12_DCI	F7	DQ1	U19
AF24	DDR4_DQ2	POD12_DCI	H3	DQ2	U19
AF25	DDR4_DQ3	POD12_DCI	H7	DQ3	U19
AD24	DDR4_DQ4	POD12_DCI	H2	DQ4	U19
AD25	DDR4_DQ5	POD12_DCI	H8	DQ5	U19
AB24	DDR4_DQ6	POD12_DCI	J3	DQ6	U19
AC24	DDR4_DQ7	POD12_DCI	J7	DQ7	U19
AA19	DDR4_DQ8	POD12_DCI	A3	DQ8	U19
AB19	DDR4_DQ9	POD12_DCI	B8	DQ9	U19
AA20	DDR4_DQ10	POD12_DCI	C3	DQ10	U19
AB20	DDR4_DQ11	POD12_DCI	C7	DQ11	U19
Y17	DDR4_DQ12	POD12_DCI	C2	DQ12	U19
AA17	DDR4_DQ13	POD12_DCI	C8	DQ13	U19
Y18	DDR4_DQ14	POD12_DCI	D3	DQ14	U19
AA18	DDR4_DQ15	POD12_DCI	D7	DQ15	U19
U21	DDR4_DQ16	POD12_DCI	G2	DQ0	U20
U22	DDR4_DQ17	POD12_DCI	F7	DQ1	U20
T20	DDR4_DQ18	POD12_DCI	H3	DQ2	U20
U20	DDR4_DQ19	POD12_DCI	H7	DQ3	U20

T22	DDR4_DQ20	POD12_DCI	H2	DQ4	U20
T23	DDR4_DQ21	POD12_DCI	H8	DQ5	U20
W19	DDR4_DQ22	POD12_DCI	J3	DQ6	U20
W20	DDR4_DQ23	POD12_DCI	J7	DQ7	U20
Y25	DDR4_DQ24	POD12_DCI	A3	DQ8	U20
Y26	DDR4_DQ25	POD12_DCI	B8	DQ9	U20
AA24	DDR4_DQ26	POD12_DCI	C3	DQ10	U20
AA25	DDR4_DQ27	POD12_DCI	C7	DQ11	U20
V23	DDR4_DQ28	POD12_DCI	C2	DQ12	U20
W23	DDR4_DQ29	POD12_DCI	C8	DQ13	U20
V24	DDR4_DQ30	POD12_DCI	D3	DQ14	U20
W24	DDR4_DQ31	POD12_DCI	D7	DQ15	U20
AC26	DDR4_DQS_T0	DIFF_POD12_DCI	G3	DQSL	U19
AB17	DDR4_DQS_T1	DIFF_POD12_DCI	B7	DQSU	U19
V21	DDR4_DQS_T2	DIFF_POD12_DCI	G3	DQSL	U20
W25	DDR4_DQS_T3	DIFF_POD12_DCI	B7	DQSU	U20
AD26	DDR4_DQS_C0	DIFF_POD12_DCI	F3	DQSLn	U19
AC17	DDR4_DQS_C1	DIFF_POD12_DCI	A7	DQUn	U19
V22	DDR4_DQS_C2	DIFF_POD12_DCI	F3	DQSLn	U20
W26	DDR4_DQS_C3	DIFF_POD12_DCI	A7	DQUn	U20
AE26	DDR4_ODT	SSTL12	K3	ODT	U19, U20
AC16	DDR4_RESET_N	LVCMOS12	P1	RESETn	U19, U20

Table 2 – DDR4 Memory Connections to the FPGA

5.1.6 Quad SPI Flash Memory

The Quad SPI flash memory, U17, from manufacturer ISSI provides 64MB (64Mb x 8) of non-volatile storage that can be used for configuration and data storage.

- Manufacturer: ISSI
- Part Number: IS25WP512M-JLLE
- Configuration: 64MB (64Mb x 8)
- Supply Voltage: +1.8V
- Data Path Width: 4-bits
- Data Rate: Various depending on Single/Dual/Quad mode and CCLK rate

Four data lines and the XCAU15P CCLK pin are wire to the Quad SPI flash memory. The connections between the Quad SPI flash memory and the XCAU15P are listed in Table 3.

FPGA (U16) Pin	Schematic Net Name	I/O Standard	QSPI Pin Number	QSPI Pin Name
AD11	QSPI_D0	LVCMOS18	2	SI(IO0)
AC12	QSPI_D1	LVCMOS18	5	SO(IO1)
AC11	QSPI_D2	LVCMOS18	3	WPn(IO2)
AE11	QSPI_D3	LVCMOS18	7	HOLDn/RESETn(IO2)
Y11	QSPI_CLK	LVCMOS18	6	SCK
AA12	QSPI_CSn	LVCMOS18	1	CEn

Table 3 – Quad SPI Flash Memory Connections to the FPGA

The configuration section of the UltraScale Architecture Configuration User Guide (UG570) provides details on using the Quad SPI flash memory. Figure 10 shows the connections of the Quad SPI flash memory on the AUBoard-15P Development Kit.

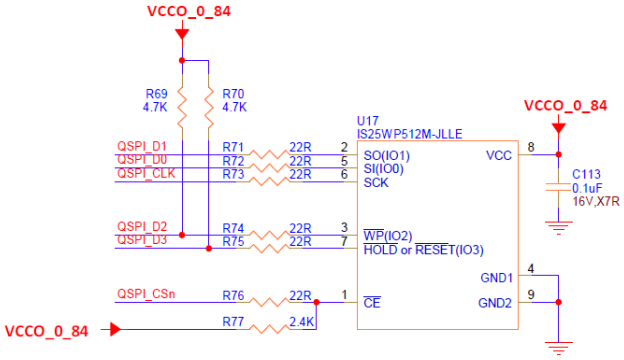

Figure 10 – 512Mb Quad SPI Flash Memory

5.1.7 USB JTAG Interface

JTAG configuration is provided through an onboard USB-to-JTAG configuration device (U21), in which a host computer accesses the AUBoard-15P Development Kit JTAG chain through a type-A (host side) to micro-B (AUBoard-15P Development Kit side J9) USB cable. A 2mm JTAG header (J10) is also provided in parallel for access by JTAG download cables. JTAG configuration is allowed at any time regardless of the FPGA mode pin settings. JTAG initiated configuration takes priority over the configuration method selected through the FPGA mode pins. The JTAG chain of the AUBoard-15P Development Kit is shown in Figure 11.

NOTE: A voltage translator, U23, between +3.3V and +VCCO_0_84 signaling exists but is not depicted in Figure 11. Also not shown in the Figure 11 is the parallel JTAG header J10.

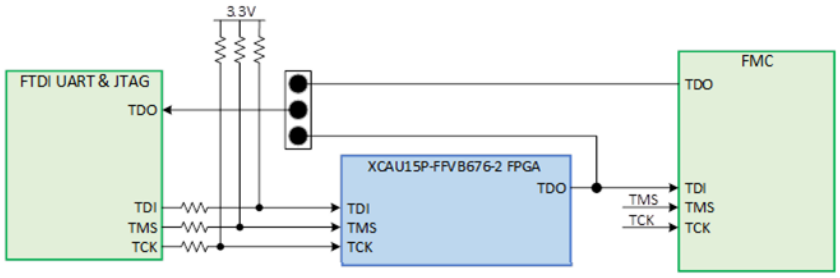

Figure 11 – JTAG Chain Block Diagram

When an FMC card is attached to the AUBoard-15P, it needs to manually be added to the JTAG chain through the 3-pin jumper J11 that is depicted in Figure 11. The header, J11, when shunted with Pin 1 to Pin 2 will have the FPGA only in the JTAG chain. The header, J11, when shunted with Pin 3 to Pin 2 will include both the FPGA and the FMC interface in the JTAG chain. When jumper J11 is set to both FPGA and FMC a FMC card must be attached and that FMC card must implement a TDI-to-TDO connection through a device or bypass jumper in order for the JTAG chain to be completed to the XCAU15P FPGA U16.

5.1.8 Clock Generation

There are five clock sources available for the XCAU15P FPGA logic on the AUBoard-15P board.

FPGA (U16) Pin	Schematic Net Name	I/O Standard	Clock Ref	Pin	Description
AD21	SYS_CLK_P	LVDS	X1	4	ECS 3.3V 300MHz Fixed Freq OSC
AE21	SYS_CLK_N	LVDS		5	
P6	HDMI_CLK_8T49N241_P	LVDS	U56	22	Programmable HDMI Reference Clock for GT
P7	HDMI_CLK_8T49N241_N	LVDS		23	
D11	HD_CLK_P	LVDS	U57	9	Programmable Reference Clock for FPGA – 300MHz
D10	HD_CLK_N	LVDS		8	
Y6	SFP_156.25M_P	LVDS	U57	22	156.25MHz Reference Clock for GT
Y7	SFP_156.25M_N	LVDS		23	
N21	CLK_150M	LVCMOS	U57	5	150MHz Reference Clock for FPGA_EMCCLK

Table 4 – Board Clock Sources

5.1.9 System Clock Source

The AUBoard-15P Development Kit has a 3.3V LVDS differential 300MHz oscillator (X1) wired to an FPGA GC clock input on bank 64. This 300MHz signal pair is named SYS_CLK_P and SYS_CLK_N, which are connected to FPGA U16 pins AD21 and AE21 respectively.

- Manufacturer: ECS
- Part Number: ECX-L33CN-300.000-TR
- Frequency: 300MHz
- PPM frequency tolerance: +/- 25ppm
- Differential Output

The system clock circuit is shown in Figure 12.

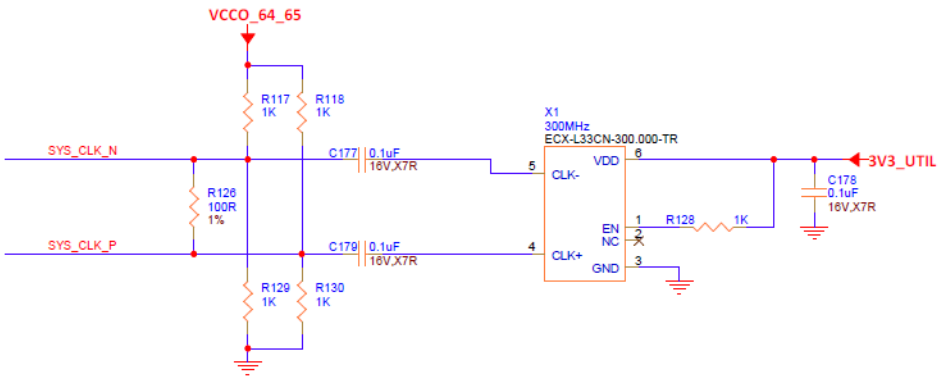

Figure 12 – System Clock Source

5.1.10 Programmable Clock Sources

The AUBoard-15P Development Kit has two programmable clock sources on board. The first programmable clock source is device U56, and the second programmable clock source is device U57.

The first programmable clock source, U56, is used to forward a jitter attenuated version of a differential clock generated by HDMI FPGA design from bank 65 and deliver it back to a GTH transceiver reference clock input on bank 226 for use with the HDMI FPGA design. The differential clock pair generated on bank 65 is called HDMI_REC_CLK_P and HDMI_REC_CLK_N, which are connected to FPGA U16 pins P25 and P26. The jitter attenuated differential clock pair forwarded to bank 226 is called HDMI_CLK_8T49N241_P and HDMI_CLK_8T49N241_N, which are connected to FPGA U16 pins P7 and P6.

The second programmable clock source, U57, is used to generate a GTH transceiver reference clock on bank 224, a general purpose programmable LVDS clock source on Bank 85, as well as the FPGA EMCCLK on bank 65 that is used as an external clock for configuration. The GTH differential clock pair generated for the GTH transceiver reference clock on bank 224 is called SFP_156.25M_P and SFP_156.25M_N, which are connected to FPGA U16 Y7 and Y6. The general purpose programmable differential clock source is called HD_CLK_P and HD_CLK_N and is connected to FPGA D11 and D10. The FPGA EMCCLK is a single ended signal called CLK_150M and it is connected to FPGA U16 pin N21.

On power-up, the GTH differential clock pair from device U57 will default to an output frequency of 156.25MHz, the general-purpose differential clock will default to an output of 300MHz, and the FPGA EMCCLK will default to an output frequency of 150MHz. User applications can change the output frequencies through an I2C interface. Power cycling the board will revert the user clocks to their default frequencies.

The clock generator I2C programming interface is connected to FPGA U16 via pin B9 (SCL_SCLK) and pin A9 (SDA_nCS). This I2C bus contains the clock generator U57 at I2C address 0x7C and a clock generator configuration EEPROM U58 at I2C address 0x50. Programming values for the configuration EEPROM are generated from the Timing Commander Tool from Renesas.

- Manufacturer: Renesas
- Part Number: 8T49N241-998NLGI
- Programmable clock generator
- Single-ended or Differential Outputs

The first programmable clock source circuit is shown in Figure 13.

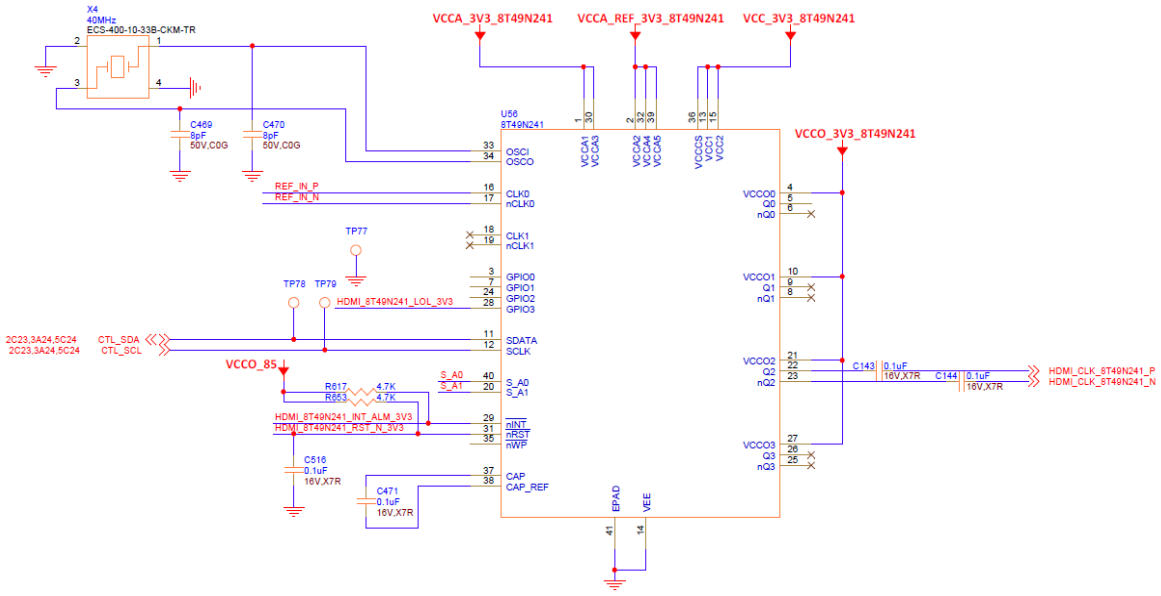

Figure 13 – First Programmable Clock Source

The second programmable clock source circuit is shown in Figure 14.

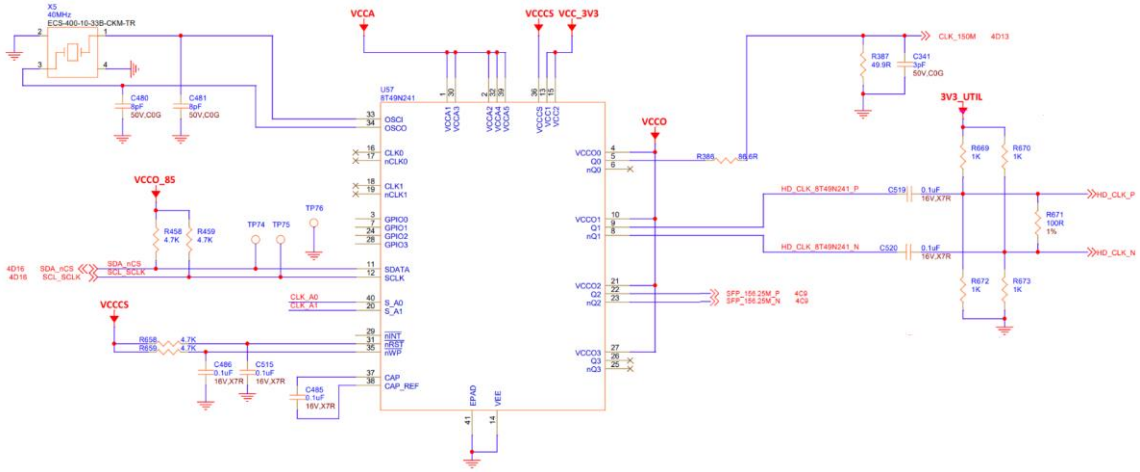

Figure 14 – Second Programmable Clock Source

5.1.11 GTH Transceiver Reference Clock Sources

The AUBoard-15P Development Kit has six clock sources available for the GTH transceiver reference clock inputs. The six clock sources are provided from varying interfaces such as the programmable clock sources, the PCIe Gen4 x4 card edge, the HDMI interface, and the FMC interface.

The six clock sources available for the XCAU15P GTH transceiver reference clocks input on the AUBoard-15P Development Kit is shown in Table 5.

FPGA (U16) Pin	Schematic Net Name	Bank Clock	Interface	Description
AB7	PCIE_CLKP	BANK 224	PCIe Card Edge	PCIe Card Edge 125MHz Fixed Freq
AB6	PCIE_CLKN	REFCLK0		
Y7	SFP_156.25M_P	BANK 224	Prog Clock Source	156.25MHz Reference Clock for GTH
Y6	SFP_156.25M_N	REFCLK1		
V7	MGTREFCLK0P	BANK 225	FMC Clock Source	Reference Clock for FMC GBTCLK0_M2C
V6	MGTREFCLK0N	REFCLK0		
T7	MGTREFCLK1P	BANK 225	FMC Clock Source	Reference Clock for FMC GBTCLK1_M2C
T6	MGTREFCLK1N	REFCLK1		
P7	HDMI_CLK_P	BANK 226	Prog Clock Source	Forwarded Jitter Attenuated HDMI Clock
P6	HDMI_CLK_N	REFCLK0		
M7	HDMI_RCLKOUT_P	BANK 226	HDMI RX Connector	HDMI Clock Received from HDMI RX Connector
M6	HDMI_RCLKOUT_N	REFCLK1		

Table 5 – GTH Transceiver Reference Clock Sources

5.1.12 GTH Transceiver Interface Mapping

The AUBoard-15P Development Kit provides access to twelve GTH transceivers:

- Four of the GTH transceivers are wired to the PCI Express x4 endpoint edge connector (CON2) fingers.
- Four of the GTH transceivers are wired to the FMC connector (CON1).
- Three of the GTH transceiver are wired to the HDMI interfaces (HDMI RX: J24, HDMI TX: J28).
- One GTH transceiver is wired to the SFP+ Module connector (J13).

The GTH transceivers in Artix UltraScale+ FPGAs are grouped into four channels described as Quads. The reference clock for a Quad can be sourced from the Quad above or Quad below the GTH Quad of interest. There are three GTH transceiver Quads on the AUBoard-15P Development Kit with connectivity as shown here:

- Quad 224
  - Contains four GTH transceivers for PCIe lanes 0-3
  - MGTREFCLK0 PCIe edge connector clock
  - MGTREFCLK1 Programmable clock source 2

- Quad 225
  - Contains four GTH transceivers for FMC lanes 0-3
  - MGTREFCLK0 FMC connector GBTCLK0
  - MGTREFCLK1 FMC connector GBTCLK1

- Quad 226
  - Contains four GTH transceivers for FMC lanes 0-3
    - GTH0-GTH2 HDMI RX/TX Interface
    - GTH3 SFP+
  - MGTREFCLK0 Programmable clock source 1
  - MGTREFCLK1 HDMI RX connector clock source

Table 6 lists the GTH transceivers interface connections to the FPGA (U16).

Transceiver Bank	Pin Number	Pin Name	Schematic Net Name	Connected Pin	Connected Device
BANK 224	AF2	MGTHRXP0_224	PCIE_RX0_P	CON2.B14	PCIe Edge Connector (CON2)
	AF1	MGTHRXN0_224	PCIE_RX0_N	CON2.B15	
	AF7	MGTHTXP0_224	PCIE_TX0_P	CON2.A16	
	AF6	MGTHTXN0_224	PCIE_TX0_N	CON2.A17	
	AE4	MGTHRXP1_224	PCIE_RX1_P	CON2.B19	
	AE3	MGTHRXN1_224	PCIE_RX1_N	CON2.B20	
	AE9	MGTHTXP1_224	PCIE_TX1_P	CON2.A21	
	AE8	MGTHTXN1_224	PCIE_TX1_N	CON2.A22	
	AD2	MGTHRXP2_224	PCIE_RX2_P	CON2.B23	
	AD1	MGTHRXN2_224	PCIE_RX2_N	CON2.B24	
	AD7	MGTHTXP2_224	PCIE_TX2_P	CON2.A25	
	AD6	MGTHTXN2_224	PCIE_TX2_N	CON2.A26	
	AB2	MGTHRXP3_224	PCIE_RX3_P	CON2.B27	
	AB1	MGTHRXN3_224	PCIE_RX3_N	CON2.B28	
	AC5	MGTHTXP3_224	PCIE_TX3_P	CON2.A29	
	AC4	MGTHTXN3_224	PCIE_TX3_N	CON2.A30	
BANK 225	Y2	MGTHRXP0_225	GTH_225_RX0_P	CON1.C6	FMC Connector (CON1)
	Y1	MGTHRXN0_225	GTH_225_RX0_N	CON1.C7	
	AA5	MGTHTXP0_225	GTH_225_TX0_P	CON1.C2	
	AA4	MGTHTXN0_225	GTH_225_TX0_N	CON1.C3	
	V2	MGTHRXP1_225	GTH_225_RX1_P	CON1.A2	
	V1	MGTHRXN1_225	GTH_225_RX1_N	CON1.A3	
	W5	MGTHTXP1_225	GTH_225_TX1_P	CON1.A22	
	W4	MGTHTXN1_225	GTH_225_TX1_N	CON1.A23	
	T2	MGTHRXP2_225	GTH_225_RX2_P	CON1.A6	
	T1	MGTHRXN2_225	GTH_225_RX2_N	CON1.A7	
	U5	MGTHTXP2_225	GTH_225_TX2_P	CON1.A26	
	U4	MGTHTXN2_225	GTH_225_TX2_N	CON1.A27	
	P2	MGTHRXP3_225	GTH_225_RX3_P	CON1.A10	
	P1	MGTHRXN3_225	GTH_225_RX3_N	CON1.A11	
	R5	MGTHTXP3_225	GTH_225_TX3_P	CON1.A30	
	R4	MGTHTXN3_225	GTH_225_TX3_N	CON1.A31	
BANK 226	M2	MGTHRXP0_226	HDMI_RX0_P	J24.7	HDMI RX (J24) HDMI TX (J28)
	M1	MGTHRXN0_226	HDMI_RX0_N	J24.9	
	N5	MGTHTXP0_226	HDMI_TX0_P	J28.7	
	N4	MGTHTXN0_226	HDMI_TX0_N	J28.9	
	K2	MGTHRXP1_226	HDMI_RX1_P	J24.4	

	K1	MGTHRXN1_226	HDMI_RX1_N	J24.6	
	L5	MGTHTXP1_226	HDMI_TX1_P	J28.4	
	L4	MGTHTXN1_226	HDMI_TX1_N	J28.6	
	H2	MGTHRXP2_226	HDMI_RX2_P	J24.1	
	H1	MGTHRXN2_226	HDMI_RX2_N	J24.3	
	J5	MGTHTXP2_226	HDMI_TX2_P	J28.1	
	J4	MGTHTXN2_226	HDMI_TX2_N	J28.3	
	F2	MGTHRXP3_226	SFP1_RDP	J13.13	SFP+ Connector (J13)
	F1	MGTHRXN3_226	SFP1_RDN	J13.12	
	G5	MGTHTXP3_226	SFP1_TDP	J13.18	
	G4	MGTHTXN3_226	SFP1_TDN	J13.19	

Table 6 – GTH Transceiver Interface Connections

5.1.13 PCI Express Edge Connector

The AUBoard-15P Development Kit contains a 4-lane PCI Express edge connector which can perform data transfers at rates up to 16.0 GT/s for Gen4 applications. Figure 15 shows the 4-lane PCI Express edge connector schematic.

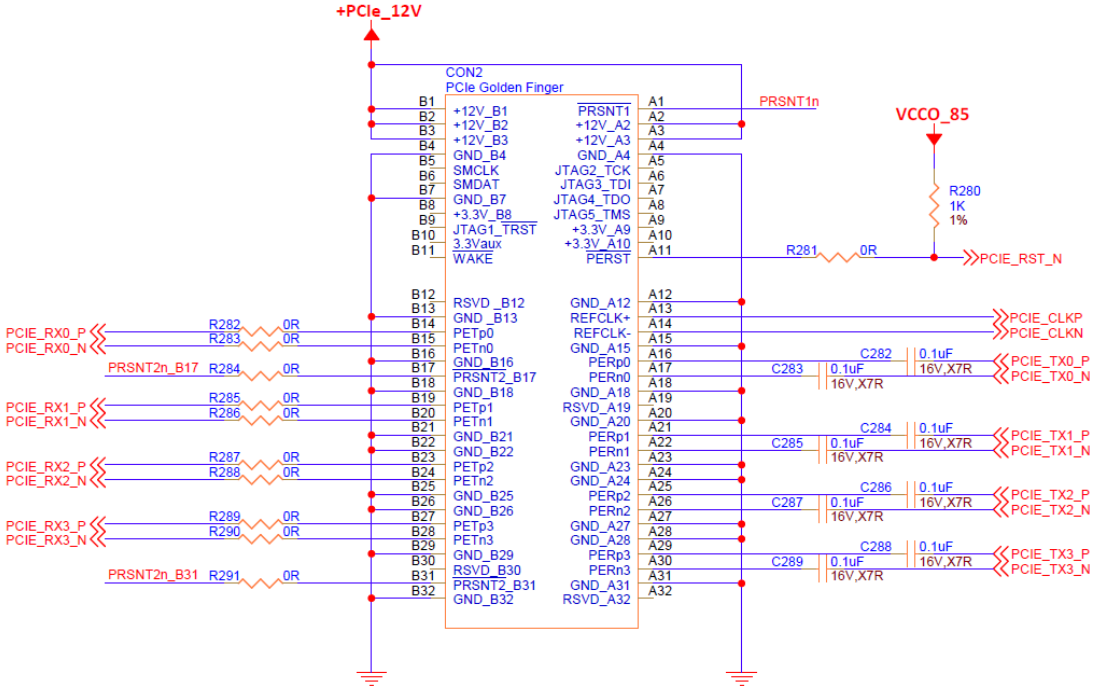

Figure 15 – PCI Express Clock Source

The Artix UltraScale+ FPGA GTH transceivers are used for the multi-gigabit per second serial interfaces. The XCAU15P-2FFVB676C FPGA (-2 speed grade) included with the AUBoard-15P Development Kit supports up to Gen4 x4. Table 7 lists the PCI Express connections to the FPGA, U16.

FPGA (U16) Pin	Schematic Net Name	PCIe Pin	PCIe Pin Name
E11	PCIE_RST_N	A11	PERSTn
AB7	PCIE_CLKP	A13	REFCLK+
AB6	PCIE_CLKN	A14	REFCLK-
AF7	PCIE_TX0_P	A16	PERp0
AF6	PCIE_TX0_N	A17	PERn0
AE9	PCIE_TX1_P	A21	PERp1
AE8	PCIE_TX1_N	A22	PERn1
AD7	PCIE_TX2_P	A25	PERp2
AD6	PCIE_TX2_N	A26	PERn2
AC5	PCIE_TX3_P	A29	PERp3
AC4	PCIE_TX3_N	A30	PERn3
AF2	PCIE_RX0_P	B14	PETp0
AF1	PCIE_RX0_N	B15	PETn0
AE4	PCIE_RX1_P	B19	PETp1
AE3	PCIE_RX1_N	B20	PETn1
AD2	PCIE_RX2_P	B23	PETp2
AD1	PCIE_RX2_N	B24	PETn2
AB2	PCIE_RX3_P	B27	PETp3
AB1	PCIE_RX3_N	B28	PETn3

Table 7 – FPGA U16 to PCI Express Connector

The PCIe clock is input from the edge connector. It is AC coupled to the FPGA through the MGTREFCLK0 pins of Quad 224. PCIE_CLKP is connected to FPGA U16 pin AB7, and the _N net is connected to pin AB6. The PCI Express clock circuit is shown in Figure 16.

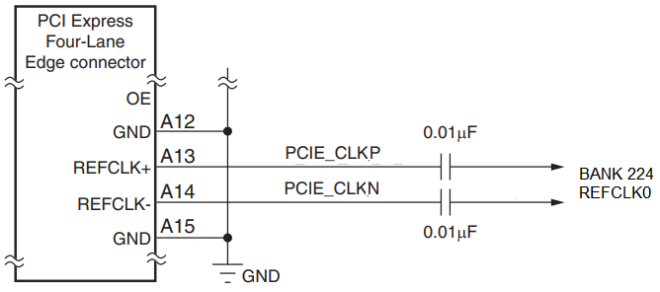

Figure 16 – PCI Express Connector Circuitry

PCIe lane width/size is selected using jumper J22 (Figure 17). The default lane size selection is 4-lane (J22 pins 2 and 3) shunted.

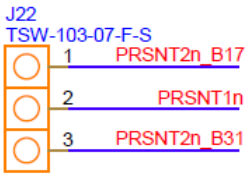

Figure 17 – PCI Express Lane Width Jumper J22

5.1.14 SFP+ Connector

The AUBoard-15P Development Kit contains a small form-factor pluggable (SFP+) connector (J13) and cage assembly (J14) that accepts SFP or SFP+ modules. Figure 18 shows the SFP+ module connector circuitry.

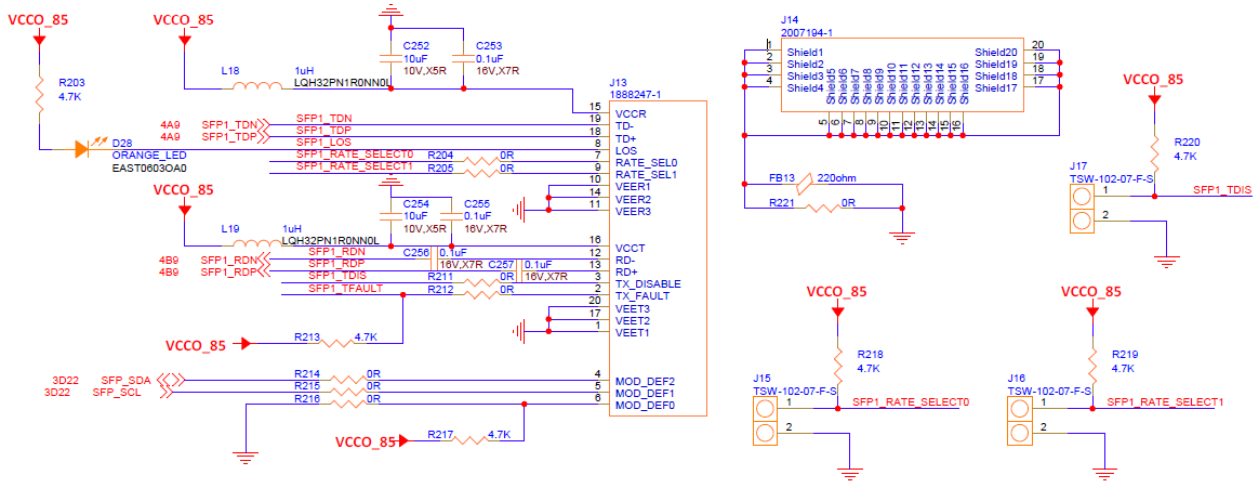

Figure 18 – SFP+ Module Connector Circuitry

Table 8 lists the SFP+ module receive and transmit connections to the FPGA, U16.

FPGA (U16) Pin	Schematic Net Name	SFP+ Pin	SFP+ Pin Name
F2	SFP1_RDP	J13.13	RD+
F1	SFP1_RDN	J13.12	RD-
G5	SFP1_TDP	J13.18	TD+
G4	SFP1_TDN	J13.19	TD-
N22	SFP1_TDIS	J13.3	TX_DISABLE
V26	SFP1_LOS	J13.8	LOS

Table 8 – FPGA U16 to SFP+ Module Connections

Table 9 lists the SFP+ module control and status connections.

SFP Control and Status Signal	Board Connection
SFP1_TFAULT	FPGA Pin V26 High = Fault Low = Normal Operation
SFP1_TDIS	Jumper J17 and FPGA Pin N22 Off = SFP Disable On = SFP Enabled
SFP1_RATE_SELECT0	Jumper J15 Pins 1-2 = Full Receiver Bandwidth Pins 2-3 = Reduced Receiver Bandwidth
SFP1_RATE_SELECT1	Jumper J16 Pins 1-2 = Full Receiver Bandwidth Pins 2-3 = Reduced Receiver Bandwidth
SFP1_LOS	Active-Low LED D28 and FPGA Pin E10 High = Loss of Receiver Signal Low = Normal Operation

Table 9 –SFP+ Module Control and Status

5.1.15 FMC Connector

The AUBoard-15P Development Kit contains an FMC (FPGA Mezzanine Card) HPC (high pin count) connector (CON1) that is populated with FPGA GPIO as an LPC (low pin count) FMC along with 4 lanes of GTs (Gigabit Transceivers).

The Samtec connector system is rated for signal speeds up to 9 GHz (Gb/s) based on a -3 dB insertion loss point within a two-level signal environment.

- Manufacturer: Samtec
- Connector Series: SEAF – 1.27mm (0.050 in) pitch.
- Part Number: ASP-134486-01
- Positions: 400
- Number of Rows: 10
- Connector Mating Series: SEAM – 1.27mm (0.050 in) pitch.

The 400-pin HPC connector implemented to FMC specifications provides connectivity for up to:

- 160 single-ended or 80 differential user-defined signals
- 10 GT transceivers
- 2 GT transceiver clocks
- 4 differential clocks
- 159 ground and 15 power connections

The AUBoard-15P Development Kit implements a hybrid solution of LPC GPIO interface and 4 lanes of GTs. The connections between the FPGA, U16, and the FMC connector (CON1) contains a subset of the full HPC connector with the following connectivity:

- 34 differential user defined pairs
  - 34 LA pairs (LA00-LA33)
- 2 differential clocks
- 4 GT transceivers
- 2 GT transceiver clocks
- 159 ground and 15 power connections

Table 10 shows the connections to the between the FMC connector, CON1, and the FPGA, U16.

FMC Pin (CON1)	FMC Pin Name	Schematic Net Name	FPGA Pin (U16)
A2	DP1_M2C_P	GTH_225_RX1_P	V2
A3	DP1_M2C_N	GTH_225_RX1_N	V1
A6	DP2_M2C_P	GTH_225_RX2_P	T2
A7	DP2_M2C_N	GTH_225_RX2_N	T1
A10	DP3_M2C_P	GTH_225_RX3_P	P2
A11	DP3_M2C_N	GTH_225_RX3_N	P1
A22	DP1_C2M_P	GTH_225_TX1_P	W5
A23	DP1_C2M_N	GTH_225_TX1_N	W4
A26	DP2_C2M_P	GTH_225_TX2_P	U5
A27	DP2_C2M_N	GTH_225_TX2_N	U4
A30	DP3_C2M_P	GTH_225_TX3_P	R5
A31	DP3_C2M_N	GTH_225_TX3_N	R4
B20	GBTCLK1_M2C_P	MGTREFCLK1P	T7
B21	GBTCLK1_M2C_N	MGTREFCLK1N	T6
C2	DP0_C2M_P	GTH_225_TX0_P	AA5
C3	DP0_C2M_N	GTH_225_TX0_N	AA4
C6	DP0_M22_P	GTH_225_RX0_P	Y2
C7	DP0_M2C_N	GTH_225_RX0_N	Y1
C10	LA06_P	HP_DP_23_P	D26
C11	LA06_N	HP_DP_23_N	C26
C14	LA10_P	HP_DP_19_P	E25
C15	LA10_N	HP_DP_19_N	E26
C18	LA14_P	HP_DP_06_P	L20
C19	LA14_N	HP_DP_06_N	K20
C22	LA18_GC_P	HP_DP_13_GC_P	G24
C23	LA18_GC_N	HP_DP_13_GC_N	G25
C26	LA27_P	HD_DP_04_P	J15
C27	LA27_N	HD_DP_04_N	J14
C30	SCL	FMC_SCL (I2C_SCL_3V3)	D9

C31	SDA	FMC_SDA (I2C_SDA_3V3)	C9
C34	GA0	JUMPER J19	-
C35	12P0V_1	+FMC_12V	-
C37	12P0V_2	+FMC_12V	-
C39	3P3V_1	+3V3_UTIL	-
D1	PG_C2M	PG_C2M	LED D29
D4	GBTCLK0_M2C_P	MGTREFCLK0P	V7
D5	GBTCLK0_M2C_N	MGTREFCLK0N	V6
D8	LA01_P_CC	HP_DP_12_GC_P	J23
D9	LA01_N_CC	HP_DP_12_GC_N	J24
D11	LA05_P	HP_DP_04_P	M19
D12	LA05_N	HP_DP_04_N	L19
D14	LA09_P	HP_DP_18_P	H21
D15	LA09_N	HP_DP_18_N	H22
D17	LA13_P	HP_DP_11_GC_P	K22
D18	LA13_N	HP_DP_11_GC_N	K23
D20	LA17_P_CC	HP_DP_15_P	J25
D21	LA17_N_CC	HP_DP_15_N	J26
D23	LA23_P	HP_DP_24_P	B25
D24	LA23_N	HP_DP_24_N	B26
D26	LA26_P	HP_DP_07_P	L22
D27	LA26_N	HP_DP_07_N	L23
D29	TCK	FTDI_TCK (TCK_1V8)	AE12
D30	TDI	FPGA_TDO (TDO_1V8)	Y10
D31	TDO	FMC_TDO (FTDI_TDO)	-
D32	3P3VAUX	+3V3_UTIL	-
D33	TMS	FTDI_TMS (TMS_1V8)	AB10
D34	TRST_L	TRST_L	F9
D35	GA1	JUMPER J18	-
D36	3P3V_2	+3V3_UTIL	-
D38	3P3V_3	+3V3_UTIL	-
D40	3P3V_4	+3V3_UTIL	-
E39	VADJ_1	+VCCO_66_86	-
F1	PG_M2C	+3V3_UTIL	-
F40	VADJ_2	+VCCO_66_86	-
G2	CLK1_M2C_P	HD_DP_06_GC_P	F14
G3	CLK1_M2C_N	HD_DP_06_GC_N	F13
G6	LA00_P_CC	HP_DP_16_P	F24
G7	LA00_N_CC	HP_DP_16_N	F25
G9	LA03_P	HP_DP_02_P	M20

G10	LA03_N	HP_DP_02_N	M21
G12	LA08_P	HD_DP_03_P	H14
G13	LA08_N	HD_DP_03_N	G14
G15	LA12_P	HP_DP_01_P	J18
G16	LA12_N	HP_DP_01_N	L18
G18	LA16_P	HP_DP_10_P	L24
G19	LA16_N	HP_DP_10_N	L25
G21	LA20_P	HP_DP_21_P	D24
G22	LA20_N	HP_DP_21_N	D25
G24	LA22_P	HD_DP_12_P	B14
G25	LA22_N	HD_DP_12_N	A14
G27	LA25_P	HD_DP_02_P	J13
G28	LA25_N	HD_DP_02_N	H13
G30	LA29_P	HD_DP_08_GC_P	D14
G31	LA29_N	HD_DP_08_GC_N	D13
G33	LA31_P	HD_DP_10_P	C12
G34	LA31_N	HD_DP_10_N	B12
G36	LA33_P	HP_DP_08_P	M25
G37	LA33_N	HP_DP_08_N	M26
G39	VADJ_3	+VCCO_66_86	-
H2	PRSNT_M2C_L	PRSNT_M2C_L	PRSNT_M2C_L
H4	CLK0_M2C_P	HD_DP_05_GC_P	G12
H5	CLK0_M2C_N	HD_DP_05_GC_N	F12
H7	LA02_P	HP_DP_17_P	H26
H8	LA02_N	HP_DP_17_N	G26
H10	LA04_P	HP_DP_03_P	J19
H11	LA04_N	HP_DP_03_N	J20
H13	LA07_P	HD_DP_01_P	J12
H14	LA07_N	HD_DP_01_N	H12
H16	LA11_P	HD_DP_07_CC_P	E13
H17	LA11_N	HD_DP_07_CC_N	E12
H19	LA15_P	HP_DP_05_P	K21
H20	LA15_N	HP_DP_05_N	J21
H22	LA19_P	HP_DP_20_P	F23
H23	LA19_N	HP_DP_20_N	E23
H25	LA21_P	HP_DP_22_P	D23
H26	LA21_N	HP_DP_22_N	C24
H28	LA24_P	HP_DP_14_CC_P	H23
H29	LA24_N	HP_DP_14_CC_N	H24
H31	LA28_P	HP_DP_09_P	K25

H32	LA28_N	HP_DP_09_N	K26
H34	LA30_P	HD_DP_09_P	C14
H35	LA30_N	HD_DP_09_N	C13
H37	LA32_P	HD_DP_11_P	A13
H38	LA32_N	HD_DP_11_N	A12
H40	VADJ_4	+VCCO_66_86	-

Table 10 – FMC Connections CON1 to FPGA U16

5.1.16 USB-to-UART Bridge

The AUBoard-15P Development Kit contains a USB-to-UART bridge device (U21) which allows a connection to a host computer with a USB port. This USB-to-UART bridge device is shared with the device that also provides the USB-to-JTAG interface functionality.

NOTE: Device U21 is not powered by the USB 5V provided by the host PC USB cable. It is powered by the onboard +3V3+UTIL power rail.

AMD UART IP is expected to be implemented in the FPGA logic. The FPGA supports the USB-to-UART bridge using two signal pins: Transmit (TX) and Receive (RX).

Note: The VCP (Virtual COM Port) device drivers must be installed on the host PC prior to establishing communications with the AUBoard-15P Development Kit.

Table 11 shows the USB signal definitions at J9.

USB Conn Pins (J9)	Receptacle Pin Name	Schematic Net Name	Description	Device U21 Pin Number	Device U21 Pin Name
1	USB5V0	+USB_5V	+5V from Host System	-	-
3	D_P	USBDP	Bi-Dir Diff Serial Data (P-side)	8	USBDP
2	D_N	USBDM	Bi-Dir Diff Serial Data (N-side)	7	USBDM
4	GND	GND	Signal Ground	Many	-

Table 11 – microUSB Connector Pin Assignments

Table 12 shows the USB connections between the FPGA and the UART.

FPGA Pins (U16)	Function	Direction	Schematic Net Name	U21 Pin	U21 Function
AF15	Transmit	Data Output	UART_TX / FTDI_RX	39	Data Input
AF14	Receive	Data Input	UART_RX / FTDI_TX	38	Data Output

Table 12 – FPGA to UART Connections

5.1.17 10/100 Mb/s Ethernet PHY

The AUBoard-15P uses a Microchip PHY device (KSZ8091) at U25 for Ethernet communications at 10 Mb/s and 100 Mb/s. The PHY connection to the user-provided ethernet cable is through a Bel Fuse L829-1X1T-91 RJ-45 connector (J12) with built-in magnetics.

- Manufacturer: Microchip
- Part Number: KSZ8091MNXIA-TR
- 10/100 Mb/s Ethernet PHY

- Manufacturer: Bel Fuse
- Part Number: L829-1X1T-91
- 10/100 Mb/s RJ-45 Connector

On power-up, or on reset, the PHY is configured to operate in MII mode with PHY address 0b00001 using the settings shown in Table 13. These settings can be overwritten by commands passed over the MDIO interface.

U25 Pin Name / No	Setting	Configuration	
RXD1/PHYAD2 (15)	GND	PHYAD[2] = 0	PHY ADDRESS = 0x01
RXD2/PHYAD1 (14)	GND	PHYAD[1] = 0	
RXD2/PHYAD0 (12)	VCCO_0_84	PHYAD[0] = 1	
COL/CONFIG0 (28)	GND	CONFIG[2] = 0	DEFAULT – UNUSED
CRS/CONFIG1 (29)	GND	CONFIG[1] = 0	
RXDV/CONFIG2 (18)	GND	CONFIG[0] = 0	
RXD0/DUPLEX (16)	GND	DUPLEX = 0	FULL-DUPLEX
RXC/B-CAST_OFF (19)	GND	BROADCAST = 0	DEFAULT – BCAST ON
RXER/ISO (20)	GND	ISOLATE = 0	ISOLATE – DISABLED
TXC/PME_EN (22)	GND	WAKE ON LAN = 0	WAKE - DISABLED
RINTRP/PME_N2/ NAND_TREE_N (21)	VCCO_0_84	NAND TREE = 1	NAND TREE - DISABLED
LED0/PME_N1/ NWAYEN (30)	VCCO_0_84	AUTO-NEG-ENB = 1	AUTO-NEG - ENABLED

Table 13 – Ethernet PHY U25 Configuration Pin Settings

The Ethernet connections from the XCAU15P at U16 to the KSZ8091 device at U25 are listed in Table 14 Ethernet PHY Connections to FPGA U16.

FPGA Pin (U16)	Schematic Net Name	KSZ8091 (U25) Pin Name / No
AC13	ENET_MDIO	MDIO (11)
AB15	ENET_MDC	MDC (12)
AA14	ENET_TX_CLK	TXC/PME_EN (22)
AB14	ENET_TXEN	TXEN (23)
AE13	ENET_TXER	TXER (31)
W13	ENET_TD0	TXD0 (24)
W12	ENET_TD1	TXD1 (25)
AA13	ENET_TD2	TXD2 (26)
Y13	ENET_TD3	TXD3 (27)
Y15	ENET_RX_CLK	RXC/B-CAST_OFF (19)
AA15	ENET_RX_DV	RXDV/CONFIG2 (18)
AB16	ENET_RX_ER	RXER/ISO (20)
W15	ENET_RD0	RXD0/DUPLEX (16)
W14	ENET_RD1	RXD1/PHYAD2 (15)
Y16	ENET_RD2	RXD2/PHYAD1 (14)
W16	ENET_RD3	RXD3/PHYAD0 (13)
AD13	ENET_CRS	CRS/CONFIG1 (29)
AD14	ENET_COL	COL/CONFIG0 (28)
AC14	ENET_RSTn	RSTn (32)

Table 14 – Ethernet PHY Connections to U16

5.1.18 Ethernet PHY Clock Source

A 25MHz, 50ppm CMOS oscillator at X3 is the clock source for the KSZ8091 PHY at U25. Figure 19 shows the clock source.

- Manufacturer: ECS
- Part Number: ECS-2016MV-250-BN-TR
- 25MHz XO CMOS Oscillator

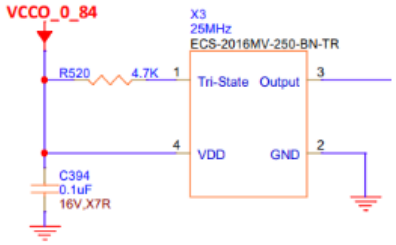

Figure 19 – Ethernet PHY Clock Source

5.1.19 Ethernet PHY LED

There is a single LED driver, LED0, from the Ethernet PHY that connects to the RJ45 Ethernet Jack (J12). The Microchip KSZ8091 data sheet contains details concerning the potential functions mapped to the LED0 pin. By default, the register/bits associated with this pin, 0x1F / 5:4 defaults to 0b00. For LED0, this maps a LINK/ACTIVITY function to this pin. There are two LED ports on the RJ45 Ethernet Jack (J12) and LED0 is mapped to both LED ports.

5.1.20 HDMI RX and TX Interfaces

The AUBoard-15P Development Kit provides HDMI video input and video output using 6-Gbps TMDS to HDMI Level Shifter Re-timer devices. The HDMI video input and video output is provided on Molex 2086581061 HDMI connectors (J24 and J28). The HDMI video solutions support Ultra HD 4Kx2K/60-Hz with 8-bits per color high-resolution video as well as HDTV 1920x1080/60-Hz with 16-bits color depth.

Figure 20 shows the HDMI Interface Block Diagram. For additional circuitry detail please reference the AUBoard-15P HDMI RX Interface, HDMI TX Interface, and HDMI MISC Interface pages in the schematic.

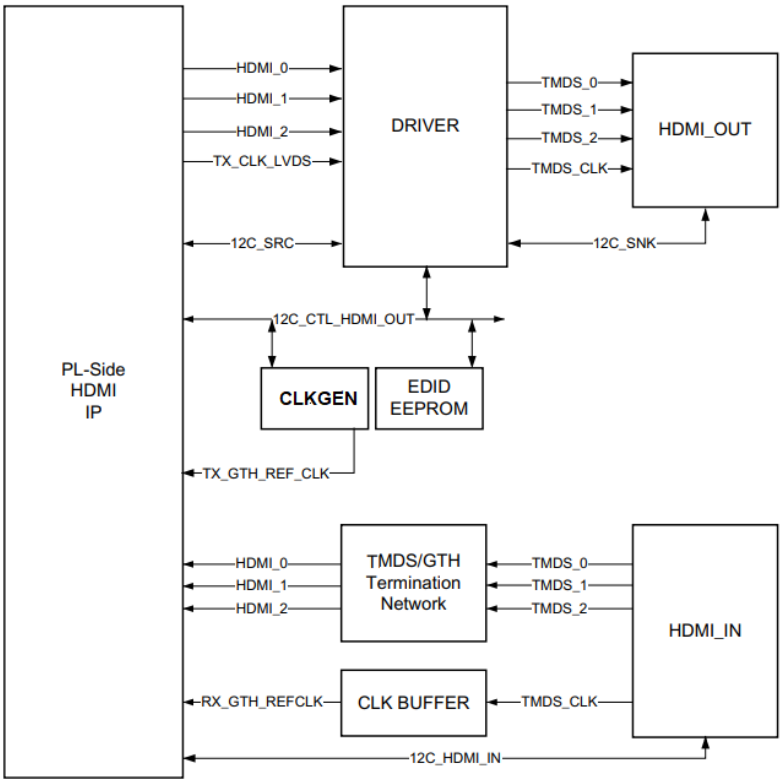

Figure 20 – HDMI Interface Block Diagram

The XCAU15P U16 to HDMI circuit connections are listed in Table 15.

FPGA Pin (U16)	Schematic Net Name	Connected Component Pin No / Pin Name
N5	HDMI_TX0_P	U34 / 8 / IN_D0p
N4	HDMI_TX0_N	U34 / 9 / IN_D0n
L5	HDMI_TX1_P	U34 / 5 / IN_D1p
L4	HDMI_TX1_N	U34 / 6 / IN_D1n
J5	HDMI_TX2_P	U34 / 2 / IN_D2p
J4	HDMI_TX2_N	U34 / 3 / IN_D2n
T25	HDMI_TX_CLK_P	U34 / 11 / IN_CLKp
U25	HDMI_TX_CLK_N	U34 / 12 / IN_CLKn
R25	HDMI_TX_SRC_SCL	U34 / 46 / SCL_SRC
R26	HDMI_TX_SRC_SDA	U34 / 47 / SDA_SRC
Y23	HDMI_TX_EN	U34 / 42 / OE
AA23	HDMI_TX_CEC	U35 / 24 / CEC_A
W21	HDMI_TX_HPD	U35 / 3 / HPD_A
M24	HDMI_8T49N241_INT_ALM	U56 / 29 / INTn
G22	HDMI_8T49N241_RST_N	U56 / 31 / RSTn
F22	HDMI_8T49N241_LOL	U56 / 28 / GPIO3
P25	HDMI_REC_CLK_P	U56 / 16 / CLK0p
P26	HDMI_REC_CLK_N	U56 / 17 / CLK0n
M7	HDMI_CLK_8T49N241_P	U56 / 22 / Q2p
M6	HDMI_CLK_8T49N241_N	U56 / 23 / Q2n
M2	HDMI_RX0_P	U31 / 29 / OUT_D0p
M1	HDMI_RX0_N	U31 / 28 / OUT_D0n
K2	HDMI_RX1_P	U31 / 32 / OUT_D1p
K1	HDMI_RX1_N	U31 / 31 / OUT_D1n
H2	HDMI_RX2_P	U31 / 35 / OUT_D2p
H1	HDMI_RX2_N	U31 / 34 / OUT_D2n
M7	HDMI_RCLKOUT_P	U31 / 26 / OUT_CLKp
M6	HDMI_RCLKOUT_N	U31 / 25 / OUT_CLKp
T24	HDMI_RX_HPD	U31 / 33 / HPD_SNK
U24	HDMI_RX_PWR_DET	Q22
N26	HDMI_RX_SNK_SCL	U31 / 38 / SCL_SNK
T19	HDMI_RX_SNK_SDA	U31 / 39 / SDA_SNK
R23	HDMI_CTL_SCL	U31 / U34 / U37 / U56
R22	HDMI_CTL_SDA	U31 / U34 / U37 / U56

Table 15 – HDMI Connections to FPGA U16

5.1.21 HDMI Clock Recovery

The AUBoard-15P Development Kit includes a Renesas 8T49N241 jitter attenuator U56. The 8T49N241 has one fractional feedback phase-locked loop (PLL) that can be used as a jitter attenuator and frequency translator.

- Manufacturer: Renesas
- Part Number: 8T49N241-998NLGI
- Programmable clock generator
- Single-ended or Differential Outputs

The FPGA can output the RX recovered clock to a differential I/O pair on I/O bank 65 (HDMI_REC_CLOCK_P, pin P25 and HDMI_REC_CLOCK_N, pin P26) for jitter attenuation. The jitter attenuated clock (HDMI_CLK_8T49N241_P (U56 pin 22), HDMI_CLK_8T49N241_N (U56 pin 23) is then routed as a series capacitor coupled reference clock to GTH Quad 226 inputs MGTREFCLK0P (U16 pin P7) and MGTREFCLK0N (U16 pin P6).

The 8T49N241 is used to generate the reference clock for the HDMI transmitter subsystem. When the HDMI transmitter is used in standalone mode, the 8T49N241 operates in free-running mode and uses an external oscillator as the reference. When the HDMI transmitter is used in pass-through mode, the 8T49N241 generates a jitter attenuated reference clock to drive the HDMI transmitter subsystem with a phase-aligned version of the HDMI Rx subsystem HMDI Rx TMDS clock, so that they are phase aligned. The 8T49N241 is controlled by an I2C interface connected to the FPGA. Enabling the jitter attenuation feature requires additional user programming through the FPGA connected HDMI_CTL I2C bus. The jitter attenuated clock circuit is show in Figure 21.

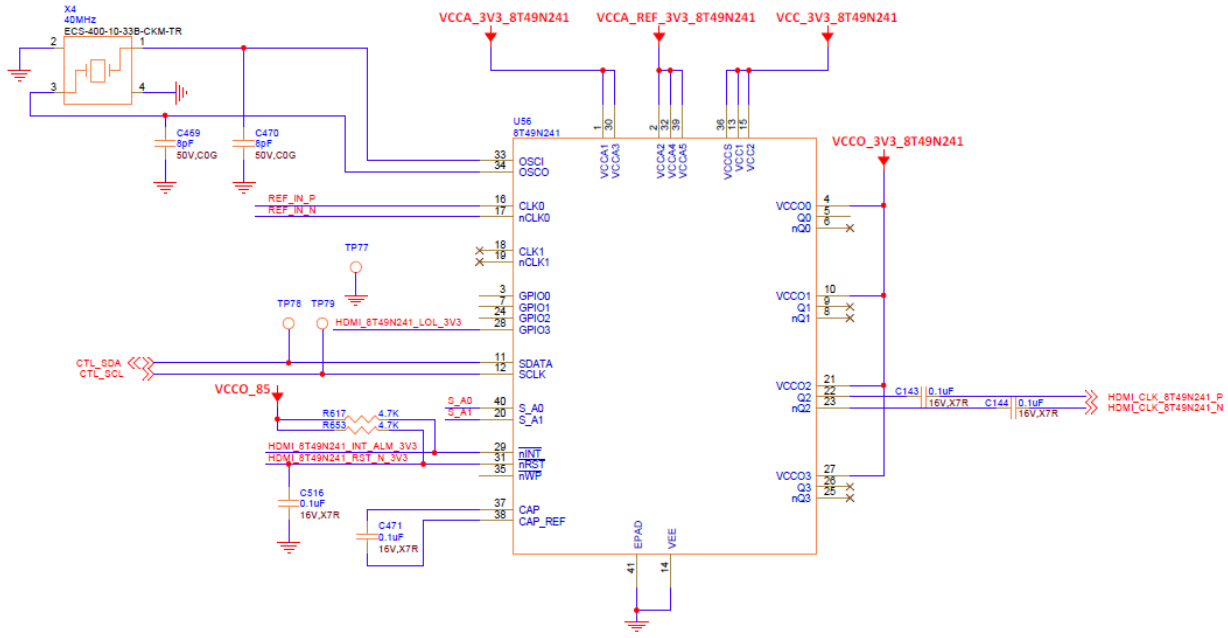

Figure 21 – HDMI Interface Clock Recovery

The Renesas 8T49N241 pin 31 reset net HDMI_8T49N241_RST_N must be driven HIGH to enable the device. 8T49N241 pin 31 reset net HDMI_8T49N241_RST_N is connected to the FPGA U16 bank 65 pin G22.

5.1.22 Click Interface

The AUBoard-15P Development Kit contains a single MikroE compatible Click site. This Click site allows inexpensive Click Board expansion through the MikroE Click ecosystem. The Click site is implemented through Samtec SSW-108-01-F-S connectors.

Visit **https://avnet.me/click** for a listing of some of the available Click boards.

Figure 22 is the implementation of the MikroE Click site interface. The analog pin, AN, has support provided by a Microchip MCP3201T-CI/SN A/D converter. The I2C interface on the MikroE Click site is accessed via an NXP PCA9544APW,118 which is a 4CH I2C bus multiplexer.

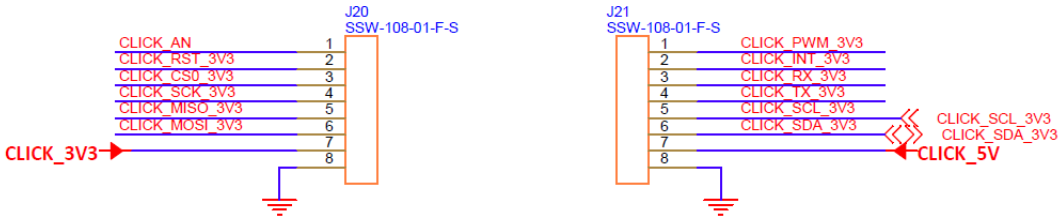

Figure 22 – MikroE Click Site Implementation

Table 16 shows the pinout of the MikroE Click Expansion Header and the differences from the MikroE Click specification.

FPGA Pin (U16)	Schematic Net Name	Click Interface (J20 / J21) Pin Name / No
H9	CLICK_CS1	U27 / SPI IF
U27 / SPI IF	CLICK_AN	AN / J20-1
K10	CLICK_RST	RST / J20-2
H11	CLICK_CS0	CS0 / J20-3
G11	CLICK_SCK	SCK / J20-4
G10	CLICK_MISO	MISO / J20-5
G9	CLICK_MOSI	MOSI / J20-6
J9	CLICK_PWM	PWM / J21-1
K9	CLICK_INT	INT / J21-2
J10	CLICK_RX	RX / J21-3
J11	CLICK_TX	TX / J21-4
U28 / D9	CLICK_SCL	SCL / J21-5
U28 / C9	CLICK_SDA	SDA / J21-6

Table 16 – MikroE Click Site Connections to FPGA U16

5.1.23 I2C Bus Switch

The AUBoard-15P Development Kit provides access to many I2C peripherals through an NXP PCA9544APW,118 which is a 4CH I2C bus multiplexer, U28. The PCA9544APW,188 is set to address **0x70**. The I2C bus that is the master to this multiplexer maps to FPGA U16 via pins D9 (I2C_SCL) and pins C9 (I2C_SDA).

Table 17 shows the list of I2C peripherals attached to the 4Ch I2C bus multiplexer.

U28 Mux Port (ADDR 0x70)	I2C Bus Device	Target Device Address
0	SFP Connector J13	0xTBD
1	Click Interface J20/J21	0xTBD
2	FMC Interface CON1	0xTBD
3	Temp Sensor Interface U30	0x30

Table 17 – I2C Bus Multiplexer Connections

5.1.24 I2C MAC ID EEPROM

The AUBoard-15P Development Kit contains a Microchip AT24MAC402 I2C based MAC ID EEPROM. This EEPROM provide a unique MAC address for the Ethernet solution on the AUBoard-15P Development Kit. It also provides the user with 2Kbit of EEPROM storage accessed at up to 1MHz.

The I2C bus that is the master to this EEPROM maps to FPGA U16 via pins D9 (I2C_SCL) and pins C9 (I2C_SDA). The I2C address of the MAC ID EEPROM is set to **0x58**.

There is an onboard header, J23, which can be used to enable/disable the WRITE PROTECT feature on the EEPROM. Shunting pin 1 to pin 2 will disable WRITE PROTECT. Shunting pin 3 to pin 2 will enable WRITE PROTECT.

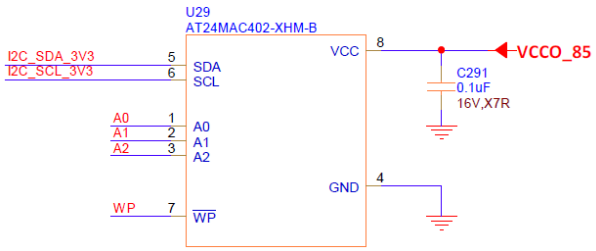

Figure 23 – MAC ID EEPROM

5.1.25 I2C Temperature Sensor

The AUBoard-15P Development Kit contains a STMicroelectronics STTS22HTR I2C based digital temperature sensor, U30. This low power, high accuracy temperature sensor provides temperature measurement across the entire operating temperature range via a 16-bit temperature data output.

The I2C bus that is the master to this temperature sensor maps to FPGA U16 via pins D9 (I2C_SCL) and pins C9 (I2C_SDA). The I2C address of the temperature sensor is set to **0x3C**.

The temperature sensor has two registers where temperature limits, high and low, can be set. If these limits are programmed and the set thresholds are exceeded the temperature sensor can inform the user via the ALERT/INT active-low output which will lead to LED D37 illuminating on the AUBoard-15P Development Kit.

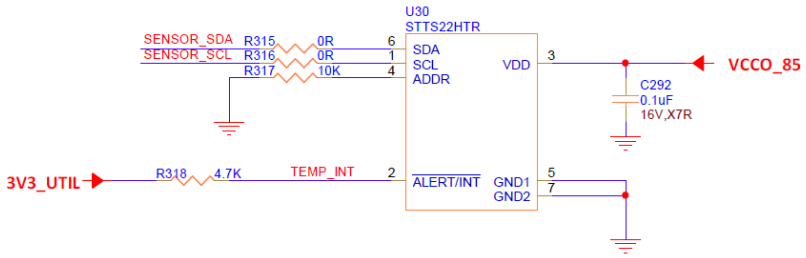

Figure 24 – I2C Temperature Sensor

5.1.26 Board LEDs

The AUBoard-15P Development Kit contains several board LEDs to convey power and status information to the end user. Table 18 lists these various LEDs.

LED	Schematic Net Name	LED Color	Description
D18	POWER_GOOD	GREEN	Power Sequencing Complete
D19	DONE_0	BLUE	FPGA Configuration Complete
D23	UART_RX	ORANGE	FPGA UART RX Activity
D24	UART TX	ORANGE	FPGA UART TX Activity
D25	PWREN_N	ORANGE	USB-UART Enable
D28	SFP1_LOS	ORANGE	SFP Loss of Sync
D29	PG_C2M	ORANGE	FMC Power Good Carrier to Mezzanine
D37	TEMP_INT	ORANGE	Temperature Sensor Alert

Table 18 – Board LEDs

5.1.27 User LEDs

The AUBoard-15P Development Kit provides several User LEDs so an application can display program status visually.

The board provides four fixed color active-high RED User LEDs:

- LED1 - D31: RED User LED attached FPGA U16 pin A10
- LED2 - D32: RED User LED attached FPGA U16 pin B10
- LED3 - D33: RED User LED attached FPGA U16 pin B11
- LED4 - D34: RED User LED attached FPGA U16 pin C11

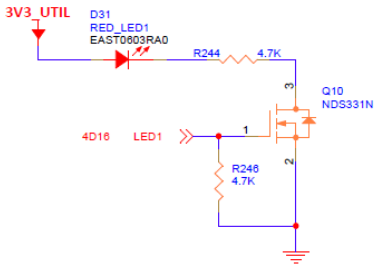

Figure 25 – RED User LED

The board also provides two programmable color active-high RGB User LEDs:

- LED_RGB_R1 – D35 RED attached to FPGA U16 pin AE15
- LED_RGB_G1 – D35 GREEN attached to FPGA U16 pin AD15
- LED_RGB_B1 – D35 BLUE attached to FPGA U16 pin AF13

- LED_RGB_R2 – D36 RED attached to FPGA U16 pin U26
- LED_RGB_G2 – D37 GREEN attached to FPGA U16 pin P24
- LED_RGB_B2 – D38 BLUE attached to FPGA U16 pin N24

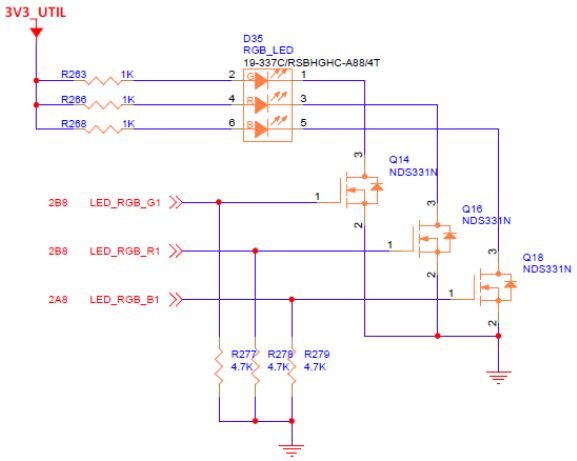

Figure 26 – RGB User LED

5.1.28 User Dip Switch

The AUBoard-15P Development Kit contains a User Switch so an application can be controlled with a physical switch.

The board provides a single User Switch that contains four switches:

- GPIO_SW1 - SW2 pins 1-8: FPGA U16 pin P19
- GPIO_SW2 - SW2 pins 2-7: FPGA U16 pin N19
- GPIO_SW3 - SW2 pins 3-6: FPGA U16 pin P23
- GPIO_SW4 - SW2 pins 4-5: FPGA U16 pin N23

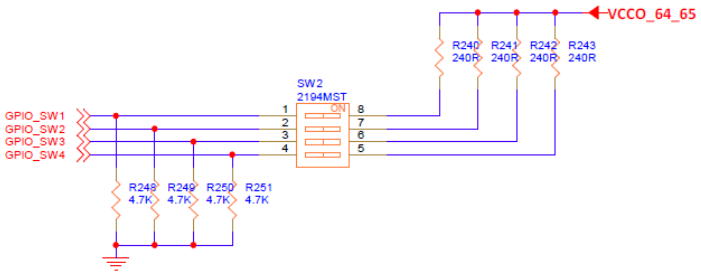

Figure 27 – User Dip Switch

5.1.29 User Push Buttons

The AUBoard-15P Development Kit contains User Push Buttons so an application can be controlled with a physical button.

The board provides four User Push Buttons:

- GPIO_PB1 – PB4: FPGA U16 pin R21
- GPIO_PB2 – PB5: FPGA U16 pin R20
- GPIO_PB3 – PB6: FPGA U16 pin P21
- GPIO_PB4 – PB7: FPGA U16 pin P20

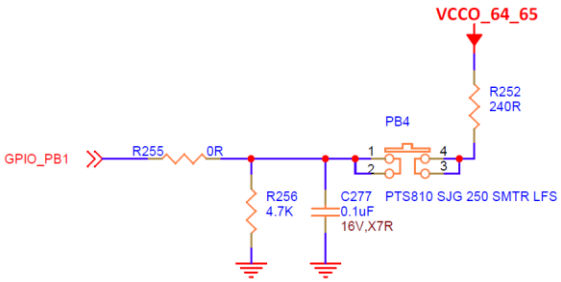

Figure 28 – User Push Buttons

5.1.30 Reset Push Button

The AUBoard-15P Development Kit provides a push button that can be used specifically as a reset to the programmable logic. It is isolated from the other User Push Buttons near the PROGRAM_B push button on the AUBoard-15P Development Kit. This push button is an active-low signal attached to FPGA U16 pin V19.

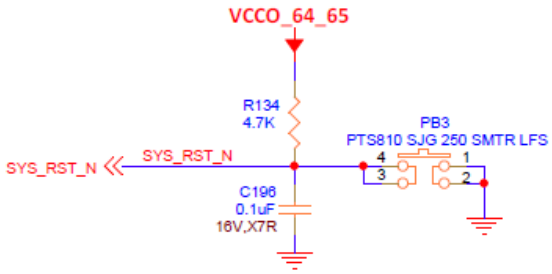

Figure 29 – Reset Push Button

5.1.31 Power Inputs and On/Off Slide Switch

The AUBoard-15P Development Kit power switch is SW1. Sliding the switch actuator from the off to the on position applies 12V power from one of three sources: a 6-pin mini-fit connector J2 (not populated), a 2.5mm DC barrel jack J51, and the PCIe card edge. A green LED D18 illuminates when the AUBoard-15P board power is on and fully sequenced.

A 12V/5A supply is provided with the AUBoard-15P that plugs into the 2.5mm DC barrel jack.

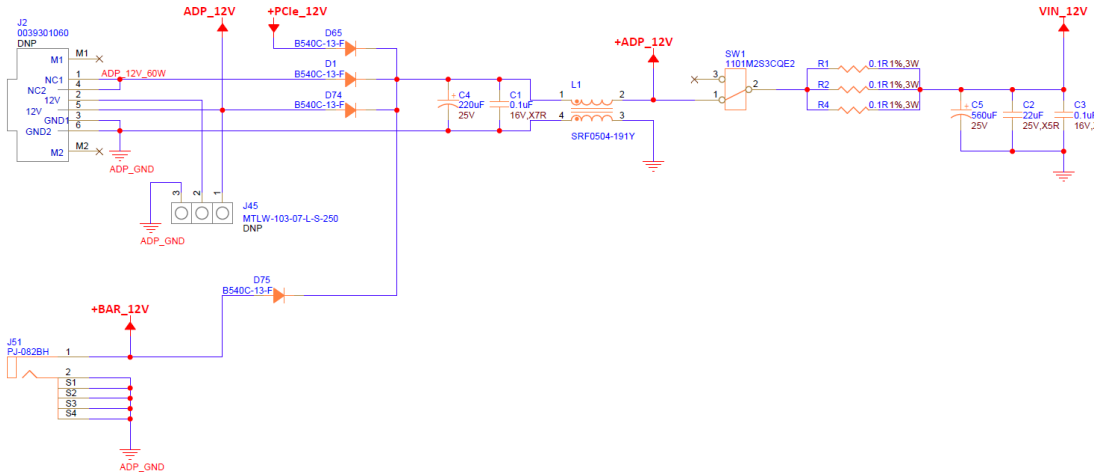

Figure 30 – Power Inputs and On/Off Slide Switch

CAUTION! Do NOT plug a PC ATX power supply or PCIe power supply 6-pin connector into the AUBoard-15P Development Kit power connector J2. These 6-pin connectors have different pinouts than J2. Connecting one of these 6-pin connectors into J2 can damage the AUBoard-15P Development Kit and will void the board warranty.

5.1.32 Voltage Rails

There are 13 regulators and a load switch that reside on the AUBoard-15P Development Kit that provides 0.85V, 0.9V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5V, and 12V power rails. These voltages are used to power the peripheral devices as well as the Artix UltraScale+ device.

There are seven bank voltages required by the FPGA and are supplied by 4 regulators.

- Bank 0 (+VCCO_0_84) +1.8V up to 6A shared
- Bank 64 (+VCCO_64_65) +1.2V up to 6A shared
- Bank 65 (+VCCO_64_65) +1.2V up to 6A shared
- Bank 66 (+VCCO_66_86) +1.2V or +1.8V up to 6A shared
- Bank 84 (+VCCO_0_84) +1.8V up to 6A shared
- Bank 85 (+VCCO_85) +3.3V up to 4A
- Bank 86 (+VCCO_66_86) +1.2V or +1.8V up to 6A shared

There are three voltages required by the FPGA to power the gigabit transceivers that each implemented with their own regulator.

- +MGTAVCC +0.9V up to 6A
- +MGTAVTT +1.2V up to 6A
- +MGTVCCAUX +1.5V up to 1A

There are three voltages required by the FPGA to power the core functions of the XCAU15P device.

- +VCCINT +0.85V up to 14A
- +VCCINT_IO / +VCCBRAM +0.85V up to 6A
- +VCCAUX / +VCCAUX_IO +1.8V up to 6A

There are several regulators and a load switch that the AUBoard-15P Development Kit uses as utility regulators to support the development of the overall power solution.

- +5V_UTIL +5.0V up to 20A
- +3V3_UTIL +3.3V up to 14A
- +2V5_UTIL +2.5V up to 1A
- +FMC_12V +12.0V up to 1A (load switch)

The following figure shows the AUBoard-15P Development Kit power solution block diagram.

Note: This diagram is intended to show the power solutions required for the AUBoard-15P Development Kit and may not be the final sequenced solution. Please reference the available schematic for the final sequenced implementation.

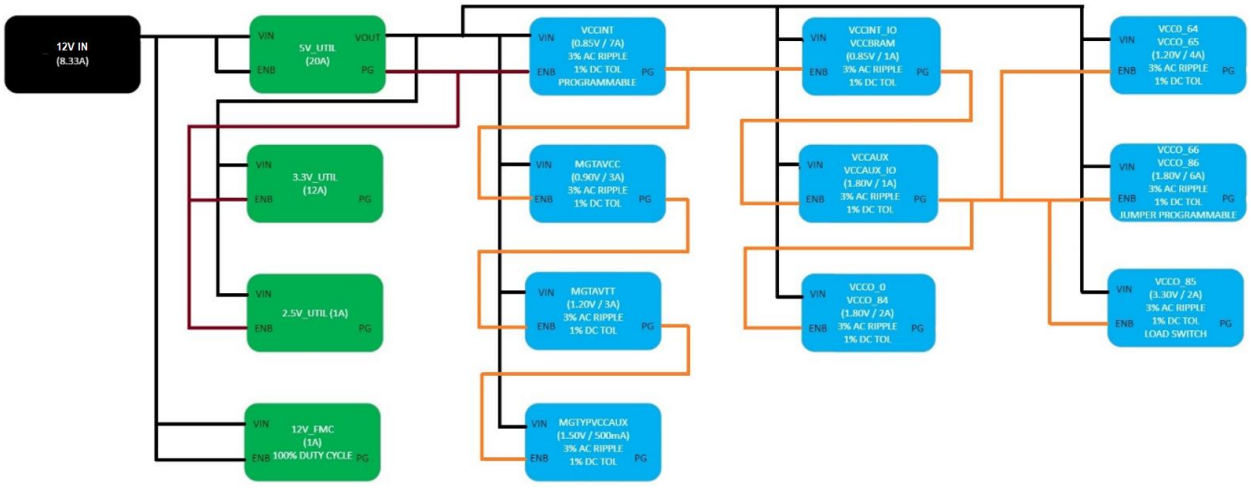

Figure 31 – Power Solution Block Diagram

Here are the required power rails and sequence for the XCAU15P device:

POWER RAIL NET NAME	VOLTAGE	AC RIPPLE	DC TOLERANCE	POWER SEQUENCE
+VCCINT`	+0.72V/+0.85V	3%	1%	1
+VCCINT_IO	+0.85V	3%	1%	2
+VCCBRAM	+0.85V	3%	1%	2
+VCCAUX	+1.80V	3%	1%	3
+VCCAUX_IO	+1.80V	3%	1%	3
+VCCO_0	+1.80V	3%	1%	4
+VCCO_64	+1.20V	3%	1%	5
+VCCO_65	+1.20V	3%	1%	5
+VCCO_66	+1.20V/+1.80V	3%	1%	6
+VCCO_84	+1.80V	3%	1%	4
+VCCO_85	+3.3V	3%	1%	7
+VCCO_86	+1.20V/+1.80V	3%	1%	6
+MGTAVCC	+0.90V	3%	1%	8
+MGTAVTT	+1.20V	3%	1%	9
+MGTVCCAUX	+1.80V	3%	1%	10
+VCCADC	+1.80V	3%	1%	NONE
+VREFP	+1.25V	3%	1%	NONE

Figure 32 – FPGA Power Solution Requirements

The Artix UltraScale+ devices are available in -2 and -1 speed grades and with a -1L voltage grade offering different levels of performance. The -2 device has the highest performance and power consumption while the -1L device would offer the lowest performance and power consumption. The AUBoard-15P standard product is populated with a -2 device. Alternative speed grades may be available as a design customization subject to opportunity review.

5.1.33 Power Sequencing

The AUBoard-15P Development Kit power architecture follows the POWER SUPPLY SEQUENCING GUIDELINES provided in the ARTIX ULTRASCALE+ FPGA DATA SHEET: DC and AC SWITCHING CHARACTERISTICS document (DS931)**.** The following is a quick list of the recommended power-on / power-off sequencing:

Power-ON Sequence:

VCCINT -> VCCINT/IO and VCCBRAM -> VCCAUX and VCCAUX_IO, and then the bank VCCOs

VCCADC and VREFP no power-up sequencing requirement

VCCINT -> MGTAVCC -> MGTAVTT or MGTAVCC -> VCCINT -> MGTAVTT

MGTVCCAUX no power-up sequencing requirement

Power-OFF Sequence:

The reverse of the Power-ON Sequence.

To meet the power sequencing guidelines for the Artix UltraScale+ device a power sequencer was developed using a Renesas GreenPak device. This device can sequence up to 9 regulators using combinations of EN (enable) pins and PG (power good) pins and logic gates.

The Renesas GreenPak is a custom programmed device developed by TRIA and available from the Renesas factory. The Renesas part number is SLG7AV46723. A datasheet for this device is available. Contact your local FAE if you would like more information about the SLG7AV46723.

The following figure is a timing diagram of the SLG7AV46723. The SOM_PWR_ENB_IN signal represents the CTRL pin on the device and is used to start the power sequence on power up or reverse the power sequence on power down.

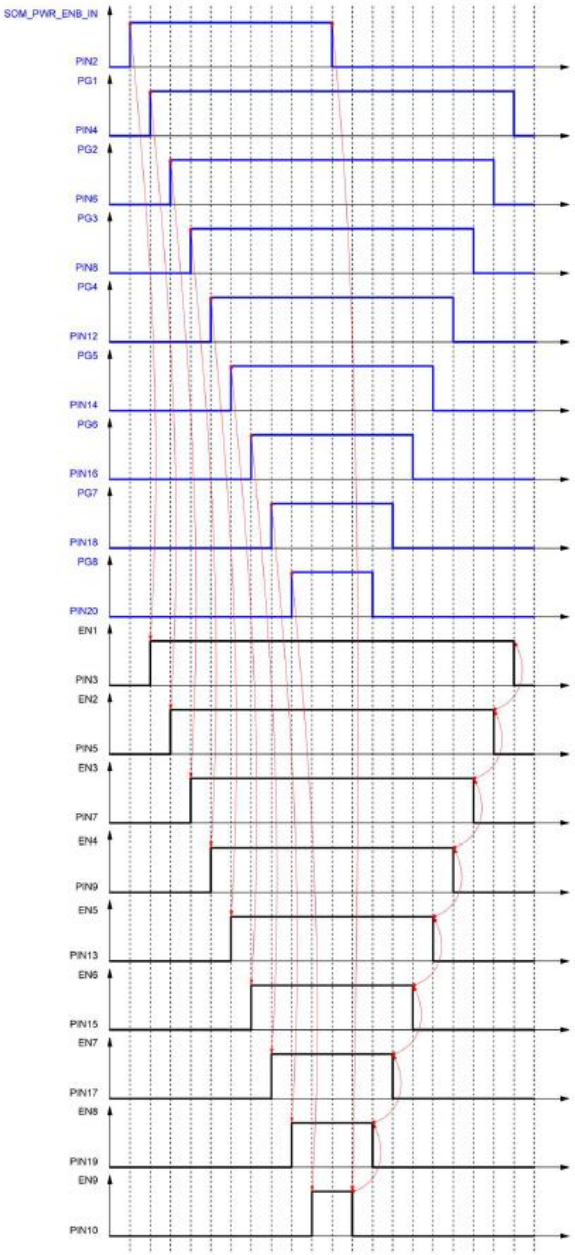

Figure 33 – Power Sequencer Timing Diagram

The following figure shows how the AUBoard-15P implements the SLG7AV46723.

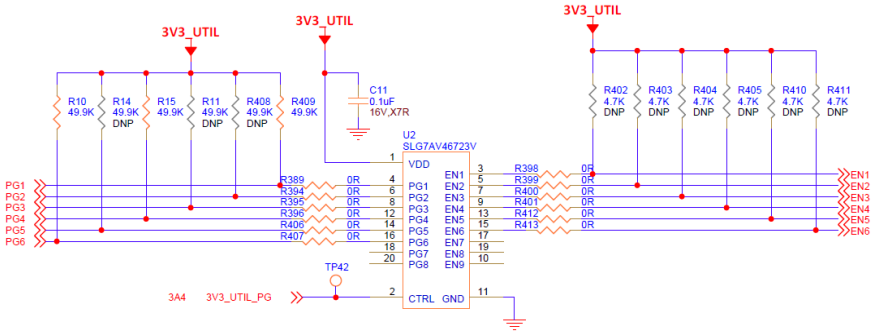

Figure 34 – Power Sequencer Schematic

5.1.34 Thermal Management

Depending on the end-user application, the performance of the Artix UltraScale+ may require a thermal solution to help maintain performance across temperature. The AUBoard-15P has been tested with an example thermal solution of a 24.5mm Heatsink attached via a BGA Clip with T710 thermal interface material (TIM).

The example thermal solution is from Aavid Thermalloy (Boyd)with orderable part number EA-270-H245-T710. If the example Heatsink solution is sufficient for end user application, please review the installation instructions necessary to secure the heatsink assembly to the Artix UltraScale+ BGA.

The clip solution provides for a ruggedly secure thermal solution versus thermal tape only if the end application warrants it. If customer end solution warrants active thermal management, a fan can be powered connecting it to a three-position connector, J3, on the AUBoard-15P Development Kit. This 3-pin keyed connector is .100” pitch and has a 5V conductor as pin 2 on the connector and a 12V conductor on pin 3 of the connector.

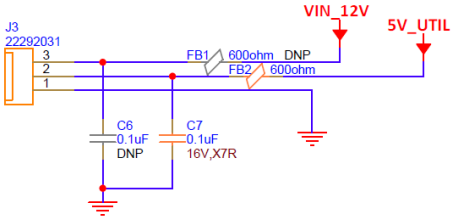

Figure 35 – Fan Header

For safety reasons, the ferrite filter bead FB1 is not populated on the platform preventing 12V from shorting to 5V at the connector. If a 12V fan is to be utilized, the end user should populate the appropriate components to source 12V to the fan header.

Under most circumstances on a passive heatsink may be required to provide adequate relief across temperature, but it cannot be guaranteed to support all environmental conditions due to lack of knowledge regarding end-user’s thermal environment and the possible enclosure of the AUBoard-15P Development Kit. For aggressive applications it is recommended that an accurate worst-case

power analysis be performed to avoid the pitfalls of over designing or under designing your product's power and thermal management system.

NOTE: End users should design a custom thermal solution that is more conducive to the requirements of their system including alternative mounting techniques for the assembly which could enhance the thermal reliability of the system.

5.1.35 Recommended Operating Conditions

This section contains the recommended operating conditions for AUBoard-15P Development Kit. Values listed are those available at the time of publication. Users may want to consult the latest device manufacturer's specifications if their application approaches any of the limits.

Parameter	Min	Max	Units	Notes
Operating Temperature	0	35	C	See errata

Table 19 – Recommended Temperature Range

Parameter	Min	Max	Units	Notes
Input Voltage	11.4	12.6	V	12V Needed for FMC Connector

Table 20 – Recommended Input Voltage

5.1.36 Mechanical

The AUBoard-15P Development Kit is designed to be a full-size PCI Express Add-In Card form factor. The board measures 216mm x 106.65mm (approximately 8.50" x 4.20").

Several factors can affect the maximum vertical dimension of the board including boards attached to expansion ports such as the MikroE Click site or the FMC connector or a thermal solution attached to the FPGA BGA. A STEP model / DXF file of the PCB and its components can be made available to end users that may require it.

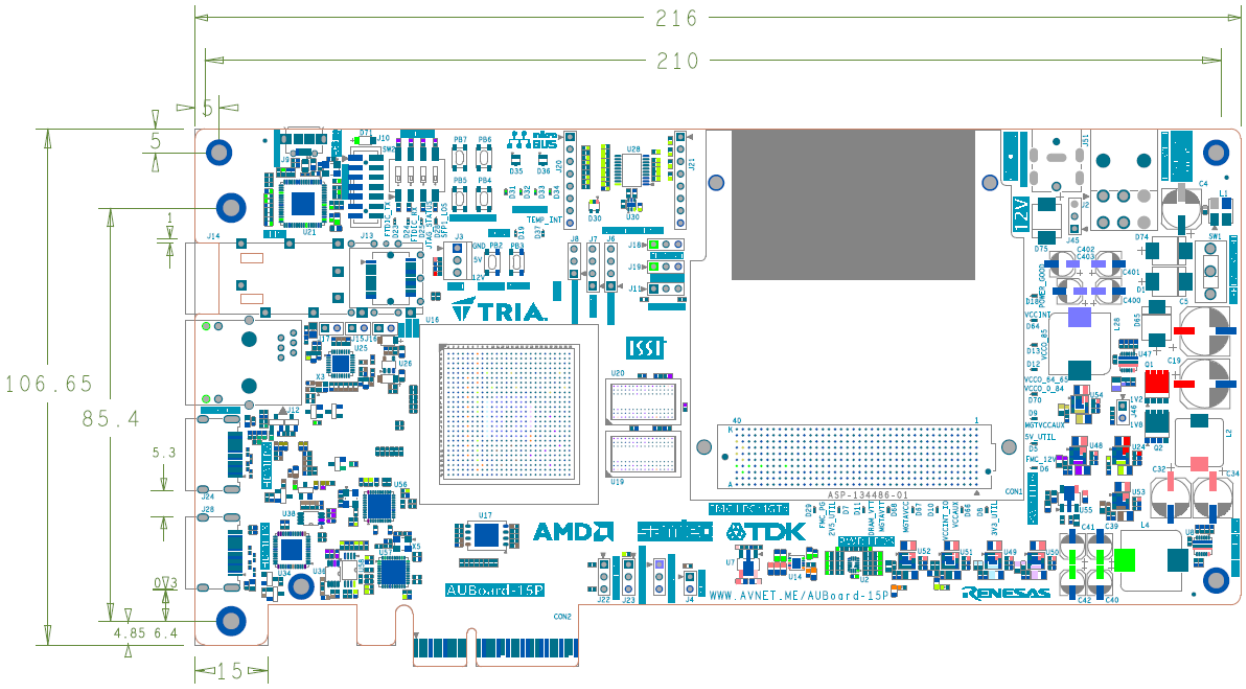

Figure 36 – Mechanical Dimensions

6 Getting Help and Support

If additional support is required, TRIA Technologies has many avenues to search depending on your needs.

For general question regarding AUBoard-15P Development Kit, please visit our website at **http://avnet.me/auboard-15p**. Here you can find any available documentation, technical specifications, videos and tutorials, reference designs and other support.

Detailed questions regarding AUBoard-15P Development Kit hardware design, software application development, using AMD tools, training and other topics can be posted on the AUBoard-15P Development Kit Support Forum at **http://avnet.me/auboard-15p-forum**. Avnet's technical support team monitors the forum during normal business hours in North America.

Those interested in customer-specific options on AUBoard-15P Development Kit can send inquiries to **customize@avnet.com**.