ERRATA

August 1, 2025

Products Affected:

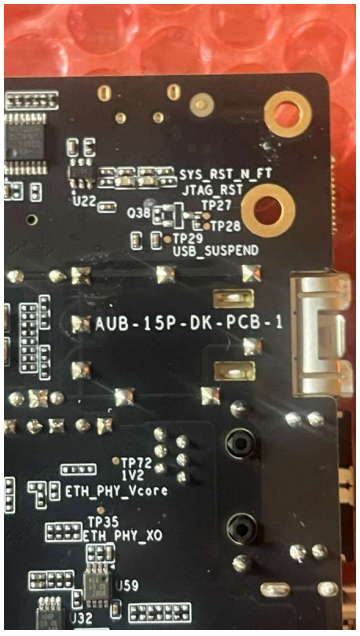
AUBoard-15P Development Kit – Revision 1

Introduction:

Thank you for your interest in the Tria AUBoard-15P Development Kit. Although Tria has made every effort to ensure the highest possible quality, these kits and associated software are subject to the limitations described in this errata notification. Be aware that any of the optional workarounds requiring physical modifications to the board are done at the user's own risk, and Tria is not liable for poorly performed rework.

Identifying Affected Boards:

The AUBoard-15P Development Kits affected by these errata can be identified by the PCB Revision listed in silkscreen on the back of the PCB. The PCB Revision of the AUBoard-15P is listed in silkscreen and can be found on the bottom side of the board near the top right edge by the SFP connector. The current production revision is "AUB-15P-DK-PCB-1". Boards that are at this production revision are affected.



Board Bottom Side View

Errata:

Bank 65 VRP pin W21 not connected to 240-ohm resistor to GND to support DCI on DDR4

Applications Affected – Designs implementing DDR4 with HDMI will see a build error in Vivado when creating the design.

Description – Bank 65 VRP pin W21 was inadvertently connected to HDMI TX HPD signal. The VRP pin in this bank should have been connected to a 240-ohm resistor to GND to support DCI for the DDR4 signals that exist on this bank.

Workaround – To overcome the build error in Vivado it is necessary to implement an XDC constraint for DCI Cascading and limit the performance of the DDR4 interface. Examples of the DCI Cascading XDC constraint and DDR4 performance limitation is implemented in the Board Definition File (BDF) that exists on Avnet's GITHUB and/or the XilinxBoardStore GITHUB.

github.com/Avnet/bdf

github.com/Xilinx/XilinxBoardStore/tree/2024.1/boards/Avnet

Performance Limitation – The DDR4 interface is designed to function at the Artix UltraScale+ -2 Speed Grade performance maximum of 2400Mb/s. Designs using DDR4 without HDMI can operate at the 2400Mb/s performance limit. The implementation of DCI Cascading results in a derating of the DDR4 performance to 2133Mb/s which is the Artix UltraScale+ -1 Speed Grade performance limit.

Can not simultaneously use the PC4 connector J10 with MicroUSB connector J9

Applications Affected – None

Description – PC4 connector J10 is populated on boards. The PC4 connector was intended as a fallback solution for programming/configuring the AUBoard-15P Development Kit and it was not intended to be populated in production. The design shares the JTAG signals and simultaneous use of the connectors mentioned would lead to contention on the JTAG interface. The design needs to have a selectable buffer that selects one or the other connector as the JTAG interface.

Workaround – It is recommended that the user utilize the MicroUSB connector J9 as it offers support for both JTAG and the debug UART port.

JTAG reliability at higher temperatures

Applications Affected – Designs which desire programming/configuration through JTAG at higher design temperatures.

Description – During temperature thermal testing of the AUBoard-15P there were JTAG reliability issues uncovered when attempting to utilize JTAG to program/configure the platform.

Workaround – It is recommended that the user program the QSPI with the required configuration for designs that are needed to operate above 35C. This erratum affects the JTAG interface and should not affect the debug UART port.

Revision 1 of the AUBoard will only support operating temperatures near ambient and documentation for this board revision will be updated to support this limitation.

HD_CLK User Clock Differential Pair not pre-programmed at the factory

Applications Affected – Designs which desire to utilize the HD_CLK User Clock differential pair.

Description – It was determined that the incorrect configuration was programmed to the clock configuration eeprom, U58 at the factory. This eeprom configuration programs the clock generator device, U57, on power-up. There are three clocks configured on U57 at power-up and the eeprom configuration only included two of the three clocks.

Workaround – Tria is developing an application note and a reference design that will show users how to generate appropriate configuration files for the clock generator device and provide instruction on how to program that configuration file into the clock configuration eeprom, U58. The reference design will set the HD_CLK User Clock differential pair to 300MHz. The user can use the application note as an example of how they can change the frequency of this reference clock to better suit their design requirements if 300MHz is not what is desired.

The application note and reference design will be posted to the Reference Design tab of the AUBoard-15P Development Kits product page: http://avnet.me/AUBoard-15P

Incorrect Value on PCIe AC Coupling Capacitors

Applications Affected – Designs which desire to utilize the PCIe at Gen 3 or higher performance.

Description – It has been determined that the incorrect AC coupling capacitor value has been populated on the data lanes of the PCIe interface. 100nF AC coupling was populated on the boards when a value such as 220nF is more in line with PCIe specifications when supporting PCIe Gen 3 or Gen 4 data rates.

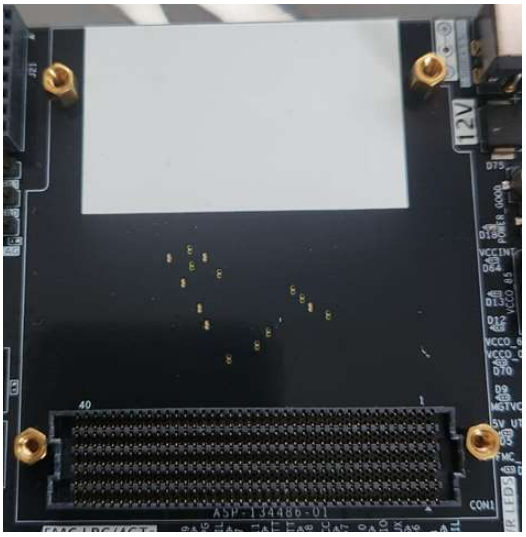
During our testing, the 100nF coupling didn’t not show an overall effect during operation.

Workaround – While we have not seen erroneous behaviour with the capacitors populated on the board, it does not mean that the 100nF solution will work in all cases as it is not possible to validate all mating platforms. The only available option here would be to replace the data lane 100nF capacitors with suitable 220nF capacitors.

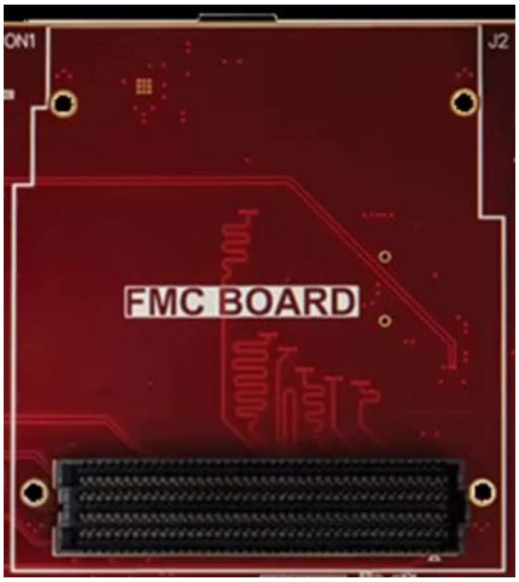
Incorrect Silkscreen / Mounting Holes for FMC Add-on Cards

Applications Affected – Designs desiring to physically mount FMC add-on card to the AUBoard-15P.

Description – It has been determined that the silkscreen and the top mounting holes for the FMC add-on card location were accidently inverted. The images below show the AUBoard-15P and a comparison to a platform with the appropriate silkscreen and top mounting holes.



AUBoard-15 FMC Add-On Location



Appropriate FMC Add-On Location

Workaround – The AUBoard-15P top mounting hole alignment is skewed. A potential solution for mounting may be to make use of smaller hardware components to provide flexibility to mount with. Aside from this, the misalignment and silkscreens with be corrected in Revision 2 of the AUBoard-15P.

New Errata:

If new errata are discovered it will be posted to the AUBoard-15P Development Kit product page, under the Technical Documents tab: http://avnet.me/AUBoard-15P

Additional Support:

For additional support, please review the discussions and post your questions in the AUBoard-15P Development Kit Forum located here: http://avnet.me/AUBoard-15P-forum

Alternatively, you can also reach out to your local Avnet Field Application Engineer (FAE) for support.

Revision History:

Date	Version	Revision
18-Dec-24	1.0	Initial Release
19-May-25	1.1	PCIe Capacitor Value
05-June-25	1.2	JTAG Reliability Statement Update
01-August-25	1.3	FMC Add-On Silkscreen and Mounting Holes