Delivering Active Power Management with Fewer Components

Integrated PMBus DC-DC Regulators Simplify PoL Configuration and Control

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Requirements to optimize efficiency and to address the complex power requirements of CPUs, ASICs and other sophisticated ICs are making active power management a critical design requirement in applications such as datacenter servers, embedded telecoms systems and networking equipment. At the same time, engineers tasked with designing power schemes are expected to keep board space to a minimum while reducing the time between initial concept and final product.

To address the challenges of active management, engineers are increasingly considering digital power schemes built around the PMBus specification, which offers a standardized platform for monitoring and controlling power management devices. And to address the real estate issue they are looking to implement these schemes with the lowest possible number of components. Highly integrated digital power converters with built-in PMBus support provide a way for designers to meet both sets of challenges.

DC/DC Conversion Design Challenges

The typical distributed power architecture employed in servers and network infrastructure equipment comprises the AC-DC front end responsible for generating a DC voltage of typically 48 V in a datacom system (figure 1) and in some computer servers. This is fed into a DC-DC converter that supplies the 12 V or 5 V intermediate bus architecture (IBA) and the intermediate voltage is then distributed to multiple point-of-load (POL) converters on the board to provide the power rails for the ICs. Historically, the choice of 12V for the intermediate bus has been considered high enough to allow the power supply to satisfy the demands of the ICs on board, while incurring the lowest possible conversion and distribution losses.

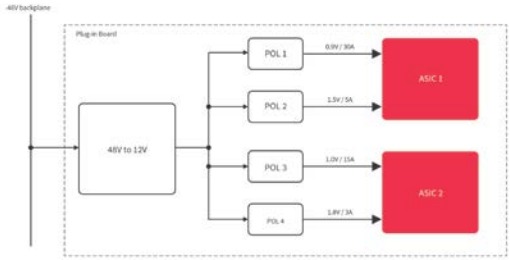

Figure 1. The intermediate bus architecture minimizes conversion losses, and is evolving to allow dynamic optimization of bus voltages

Now, however, a need for more flexible power distribution is emerging. The traditional IBA with fixed bus voltages is known to lose efficiency when the load on the converters is reduced at time of low compute demand or data traffic. At the other end of the scale the peak power consumption of server boards is increasing, driven by insatiable end-user demand for better and faster services. Moore's Law scaling now allows designers to pack multiple high-performance processors within the confines of a standard-size server board. Experts are suggesting that peak power could exceed 5 kW per blade in the near future. Bearing in mind that today's network and datacenter operators are already concerned about power consumption as a major component of their overall operating costs, power supplies need to be able to adapt dynamically to ensure optimum efficiency at all load levels.

The power requirements of the major functional ICs of a typical board are also becoming more complex, partly driven by the push for greater computing performance. Today's multi-core processors, fabricated at advanced process nodes such as 20 nm or beyond, are capable of drawing significantly more than 100 A at core voltages of 1.0 V or lower, while also requiring I/O voltages such as 3.3 V or 2.5 V. Moreover, board designers are also incorporating other devices such as complex ASICs or FPGAs to further accelerate performance within the constraints on board real estate imposed by fixed rack dimensions. These devices add further complexity to the demands placed on the power architecture.

Digital Power

Digital power technology, which is capable of supporting techniques such as dynamic adjustment of intermediate bus and IC supply voltages, phase spreading, control over fault-protection settings, and telemetry, is now being deployed to meet the demands placed on next-generation power distribution. Moreover, the digital power design flow addresses engineers' demands for an approach that is more flexible and faster than traditional analog power supply design.

The ability to adjust parameters in firmware in order to optimize performance is a major strength of digital power technology. This optimization can be done throughout the design stages, as well as in real-time while the power supply is active, without needing to interrupt operation.

The Power Management Bus (PMBus) provides a unified and standardized means of monitoring the status of digital power converters and adjusting parameters in real-time. The PMBus specification defines a set of instructions that are conceived to allow communication with power management devices and designed to run on top of the SMBus (System Management Bus) data packet protocol. SMBus itself is based around the established I^2C physical layer protocol.

PMBus defines a total of 200 instructions for controlling various aspects of the power supply, and enables interoperability between devices from different manufacturers. The instructions are concerned with issues such as converter configuration, turn-on/turn-off and margin testing, fault management, sequencing, status interrogation, telemetry and commanding output voltages. The instruction set is diverse and covers a wide variety of power conversion requirements, such as offline conversion or point-of-load conversion. Hence a given controller may support only a subset of the total number of instructions.

As demand grows for intelligent power management, PMBus is becoming increasingly adopted. The instructions allow much greater flexibility in the power supply, for example by allowing dynamic bus voltage adjustment (DBV) to optimize the intermediate bus voltage to ensure minimum losses at maximum or minimum load. The latest PMBus specification (version 1.3) introduces Adaptive Voltage Scaling (AVS), which supports the processor's ability to slow down its clock frequency and reduce the supply voltage autonomously and thereby minimize its own power consumption at times when the workload is light. This can deliver significant power savings, taking advantage of the quadratic relationship between voltage and power consumption in CMOS circuitry. At higher loads, AVS increases the operating voltage to permit faster switching of CMOS transistors. AVS also allows compensation for process and temperature variations in the processor.

In addition to the introduction of the 50 MHz AVSBus supporting adaptive voltage scaling, PMBus version 1.3 offers a number of further improvements such as a faster PMBus speed that allows increased data throughput, enhanced tracking of output voltages to inform warning thresholds, Fast Zone read/write for high-speed communication with high-priority devices, and a revised data format that allows higher precision over a wider range.

Faster Digital Power Design

As well as the energy efficiency advantages that can be realized by taking advantage of the adaptability of digital power, developing and validating a digital power supply design is also faster compared to the traditional analog approach. The basic design can be accomplished quickly with the aid of software

debuggers embedded in a development tool such as PowIRCenter to address and configure the controller internal registers via the PMBus connections. Whereas debugging an analog design can be a time-consuming process that obliges the engineer first to ascertain the reason the power supply may be shutting down, the GUI-based digital approach allows fault status to be easily read and changes made on the fly to adjust the design, optimize fault-protection settings and make any necessary revisions to system fault behavior (figure 2).

Optimization and characterization are similarly fast and efficient, making it possible to finalize the validated power system design within about one week compared with the typical timeline of about six weeks for a conventional analog design.

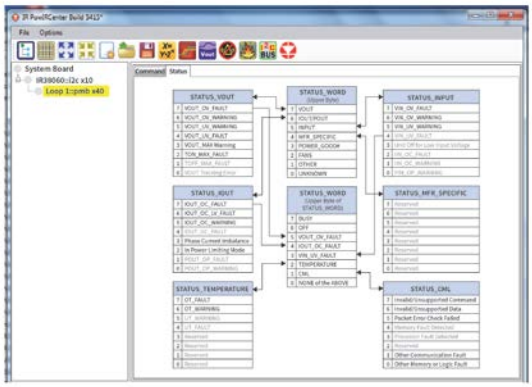

Figure 2. Digital controller settings can be adjusted quickly using a graphical tool

The faster project cycles and simplified design approach enabled by digital power delivers greater advantages as system complexity increases. For example, powering a large FPGA that requires many supply rails at different voltages and power ratings, and even with different tolerances, presents complex challenges for which few tools are available to help accelerate a conventional analog design flow. With digital controllers and configuration tools, the task can be approached confidently and completed within a significantly shorter timeframe. The flexibility of the digital controller also makes it possible to apply system updates in the field, whereas a conventional power system would require substantial hardware modification involving equipment recall and down time.

Integrated PMBus-Compatible Converters

Infineon has now gone one step further with its fully integrated SupIRBuck™ family of synchronous buck regulators for digital POL applications.

As shown in Figure 3, these regulators combine the PMBus controller with built-in high-performance control and sync FETs in the same package, saving around 70% of board real-estate over a comparable discrete circuit comprising a separate controller IC and output stage.

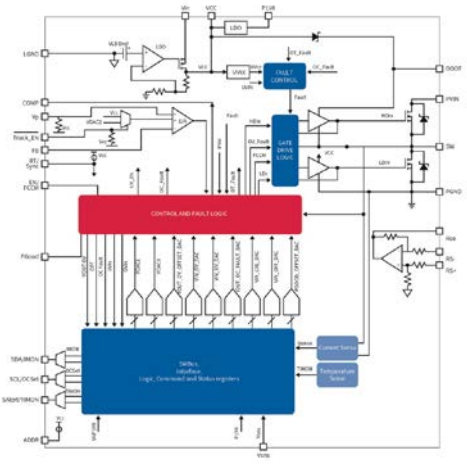

Figure 3: Block diagram of Infineon IR38060/IR38063 synchronous buck regulator with PMBus interface

Infineon's IR38060, IR38062, IR38063 and IR38064 integrated buck regulators with PMBus interface are able to supply up to 6 A, 15A, 25A or 35 A respectively, taking advantage of synchronous rectification for optimum efficiency and are housed in thermally-enhanced 5 mm x 6 mm (IR38060) or 5 mm x 7 mm (IR38062/3/4) PQFN packages. A family of PMBus-compatible multiphase controllers is also available, allowing designers to quickly implement space-efficient, scalable and digital power management schemes for complex ICs requiring even higher currents as illustrated in Figure 4.

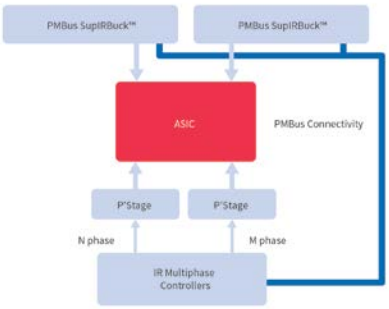

Figure 4. Integrated PMBus-compatible POL converters minimize the board space needed to supply multiple power rails

All parameters of the controller are set via firmware that is stored in non-volatile memory, giving the engineer control over areas such as number of phases, switching frequency, frequency response, dynamic voltage change, and fault and protection features including over-current and over-voltage protection.

Telemetry data is made available via the PMBus, including output voltage, high-accuracy output current data for individual phases, and total current, power stage temperature, controller temperature, input voltage, and input current. This data is useful both during debug and during normal operation. Because the PMBus supports two-way system communication, these control parameters can be modified in the deployed system.

Conclusion

Digital power holds the key to achieving the level of in-system adaptability essential for meeting the energy efficiency demands of tomorrow's data communication and networking industries. It is also the way power supply designers will be able to deliver new designs within tight turnaround times and cost constraints.

The PMBus specification provides a versatile instruction set for exercising the features and taking advantage of the adaptability of new digital controllers. The latest generation of integrated PMBus-compatible converters that combine the control IC and high-performance power stage in the same package deliver ease of use and flexibility in an extremely space-efficient solution.

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