Xilinx® Kintex™-7 325T/410T Mini-Module Plus User Guide

Rev 1.3 01/07/2015

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1 Introduction

The purpose of this manual is to describe the functionality and contents of the Avnet Kintex-7 Mini Module Plus from Avnet Electronics Marketing. This document includes instructions for operating the board, descriptions of the hardware features, and explanations of the test code programmed into the on-board programmable memory. For reference design documentation and example projects, see the Avnet Design Resource Center (DRC).

Design Resource Center

Mini-Module Plus Development Kit Supporting the Kintex-7 FPGA Family

Xilinx Kintex-7 FPGA Mini-Module Plus

Mini-Module Plus Baseboard 2

Analog Devices Power Module

GE Energy Power Module

Maxim Power Module

STMicroelectronics Power Module

Texas Instruments Power Module

Texas Instruments SIMPLE SWITCHER® Power Module

1.1 Description

The Kintex-7 Mini Module Plus Development Kit provides a complete hardware environment for designers to accelerate their time to market. The kit delivers a stable platform to develop and test designs targeted to the high-performance and low-power Xilinx Kintex-7 325T FPGA. The installed Kintex-7 325T device offers a prototyping environment to effectively demonstrate the enhanced benefits of mid-range cost Xilinx FPGA solutions. Reference designs are included with the kit to exercise standard peripherals on the evaluation board for a quick start to device familiarization.

The Kintex-7 Mini Module Plus kit contains the following three separately ordered pieces:

- AES-MMP-7K325T-G Xilinx Kintex-7 Mini-Module Plus
  - Populated with an XC7K325T-1FFG676 FPGA
  - Shunts installed at:
    - J2: 1-2
    - J4: 1-2
    - P2: 1-2
    - P3: 1-2
  - Switches set to:
    - Sw1: 1-OFF, 2-ON, 3-OFF
    - Sw2: All OFF

        - Sw3: All ON
        - Sw4: All ON
    - CAT5 Ethernet Cable (10-100-1000 capable)
    - USB3 Cable
    - Welcome Letter
    - Getting Started Guide

- AES-MMP-BB2-G Avnet Mini-Module Plus baseboard 2
    - Shunts installed at:
        - JP2: 2-3
        - JP4: 1-2
    - Switches set to:
        - Sw1: All ON
        - Sw2: All ON
        - Sw6: 1-OFF, 2-ON, 3-OFF, 4-ON, 5-OFF, 6-ON 7-OFF, 8-ON
        - Sw11: All OFF
        - Sw13: UP,K (**Not installed on Rev C Baseboards**)
        - Sw14: UP K (**Not installed on Rev C Baseboards**)
        - Sw15 = DN K
    -
    - Type A – micro B USB Cable For JTAG I/O
    - Type A – micro B USB Cable For Console I/O
    - 6-pin 12VDC Power Supply

- AES-POM-XXXX-G One Customer Selected Power Module
    - Analog Devices
    - GE Energy
    - Maxim
    - STMicroelectronics
    - Texas Instruments
    - Texas Instruments SIMPLE SWITCHER®

1.2 Kintex-7 Mini Module Plus Board Features

Xilinx FPGA Devices Supported

- Xilinx Kintex-7 XC7K160T-1FFG676 FPGA
- Xilinx Kintex-7 XC7K325T-1FFG676 FPGA (Only option currently available)
- Xilinx Kintex-7 XC7K410T-1FFG676 FPGA

I/O Connectors

- One Mini Module Plus Interface with JX1 / JX2 signal / power connectors, and JX3 power sense.
- One 20 pin XADC Analog Header
- One 10/100/1000 RJ-45 Ethernet Connector
- One USB3 Micro B Connector
- One USB3 JTAG fly-wire Header

GTX Transceivers Accessed Through JX1/JX2

- One PCI Express interface 4 lanes @ 5.0 Gbps (PCI Express 2.0)

- Four single lane General-Purpose MGT.

Memory

- 256MB of DDR3 memory (64M x 32) at 1600 Mbps
- 64 MB of Flash memory in Master BPI configuration with a 50 MHz user CCLK.
- 8KB of I2C EEPROM
- 128KB of I2C EEPROM dedicated to EZ-USB FX3 SuperSpeed USB Controller

Communication

- EZ-USB FX3 SuperSpeed USB Controller
- 10/100/1000 PHY Interface
- RS232 Port accessed through JX1/JX2
- JTAG Port accessed through JX1/JX2

Clocks

- 200MHz LVDS Clock Source
- Programmable LVDS Clock Source (MGT reference clock input)
- EMC LVCMOS 50MHz Clock Source
- Dedicated 50MHz and 25MHz Clock Sources
- Two MGT reference clock inputs available through JX1/JX2
- Four Differential clock inputs available through JX1/JX2
- Dedicated PHY receive and 125MHz clocks

User I/O

- 118 Differential IO available through JX1/JX2

Power

- Regulated 3.3, 2.5, 1.8, 1.5, 1.2, 1.0 V supply voltages must be supplied through JX1/JX2
- Regulated 5.0, 1.8, 1.25 V analog supply voltages are generated on board

Configuration

- JTAG Port accessed through JX1/JX2

1.3 Supported Baseboard Board Features available through JX1/JX2

Xilinx FPGA Mini-Modules Supported

- Xilinx Kintex-7 AES-MMP-7K325T-G
- Xilinx Virtex-5 AES-MMP-V5FXT30-G
- Xilinx Virtex-5 AES-MMP-V5FXT70-G

I/O Connectors

- One Mini Module Plus Slot (JX1, JX2, JX3)
- One FMC LPC Slot (2.5V or 3.3V VADJ)
- DisplayPort Output
- Two PMOD Headers

GTX Transceiver Connectors

- One PCI Express add-in card interface
  - 4 lanes @ 5.0 Gbps with Kintex-7 Mini-Module (PCI Express 2.0)
  - 4 lanes @ 2.5 Gbps with Virtex-5 Mini-Module (PCI Express)
- One Small-Form Pluggable (SFP) cage

- One transceiver supplied on an FMC connectors for use by an expansion module
- One transmitter via Display Port Connector
- One General-Purpose MGT via SMA Connectors

Memory

- Micro SD Card Interface

Communication

- USB-RS232 Port

Clocks

- Programmable LVDS Clock Source (MGT reference clock input)
- Programmable LVCMOS Clock Source

User I/O

- 5 User LEDs
- 8-position DIP Switch
- 4 User Push Button Switches

Power

- Power is supplied from a customer selected Power Module plug-in.
- Regulated 5.0, 3.3, 2.5, 1.8, 1.5, 1.2, 1.0 V output supply voltages derived from 12.0 V supply input from either a ATX 4-pin Molex connector or a separate 6-pin Molex connector.
- Power Module is supplied from the PCI Express slot or an external 12 V supply
- Power Configuration is switchable for V5, K7, and FMC power requirements.
- Point of Load Power Sense Feedback for all supply rails

Power Connectors

- One x4 PCI Express slot
- One 4 pin Molex external 12 V supply connector
- One 6 pin Molex external 12 V supply connector
- One 10 pin Samtec HPF power connector
- One 8 pin Samtec HPF power connector
- One 10 pin Samtec CLP sense feedback connector

Configuration

- Digilent JTAG-SMT1 Module
- PC4 JTAG Header

1.4 Power Module Features available through JX1/JX2/JX3

Power

- Power is supplied from a customer selected Power Module plug-in, designed to meet a common specification
- Generates all required voltage rails to power the FPGA module, FMC slot and baseboard circuits.
- Regulated 5.0, 3.3, 2.5, 1.8, 1.5/1.35, 1.2, 1.0 V output supply voltages derived from 12.0 V supply input from Base Board.
- SSTL2 Termination Regulators
- Point of Load Regulators for all supply rails
- Point of Load Power Sense Feedback provided for all supply rails
- Supply regulation sufficient to meet V5 and K7 requirements
- Power on/off sequencing to meet K7 requirements

Power Connectors

- One 10 pin Samtec HPF power connector
- One 8 pin Samtec HPF power connector
- One 10 pin Samtec CLP sense feedback connector
- **Power Connectors**

Available Power Modules

- Analog Devices
- GE Energy
- Maxim
- STMicroelectronics
- Texas Instruments
- Texas Instruments SIMPLE SWITCHER®

1.5 Test Files

The configuration PROM on both Kintex-7 and Virtex-5 Mini-Modules come programmed with a factory test example design. Additional test files that can be used to verify the functionality of the peripherals on the board can be found on the Avnet Electronics Marketing Design Resource Center (DRC) web site: **www.em.avnet.com/drc**. The test designs available are listed below.

- Factory Test
- Ethernet Test

The test files for each Mini-Module are located on the Mini-Module web pages respectively. Below are the links to each Mini-Module's web page on the DRC:

Design Resource Center

Mini-Module Plus Development Kit Supporting the Kintex-7 FPGA Family

Xilinx Kintex-7 FPGA Mini-Module Plus

Xilinx Virtex-5 FXT Mini-Module Plus

1.6 Reference Designs

Reference designs that demonstrate some of the potential applications of the Mini-Module Plus Baseboard 2 can be downloaded from the Avnet Design Resource Center (**www.em.avnet.com/drc**). The reference designs include all of the source code and project files necessary to implement the designs. See the PDF document included with each reference design for a complete description of the design and detailed instructions for running a demonstration on the development board. Check the DRC periodically for updates and new designs.

Design Resource Center

Mini-Module Plus Development Kit Supporting the Kintex-7 FPGA Family

Xilinx Kintex-7 FPGA Mini-Module Plus

Xilinx Virtex-5 FXT Mini-Module Plus

1.7 Product Pictures

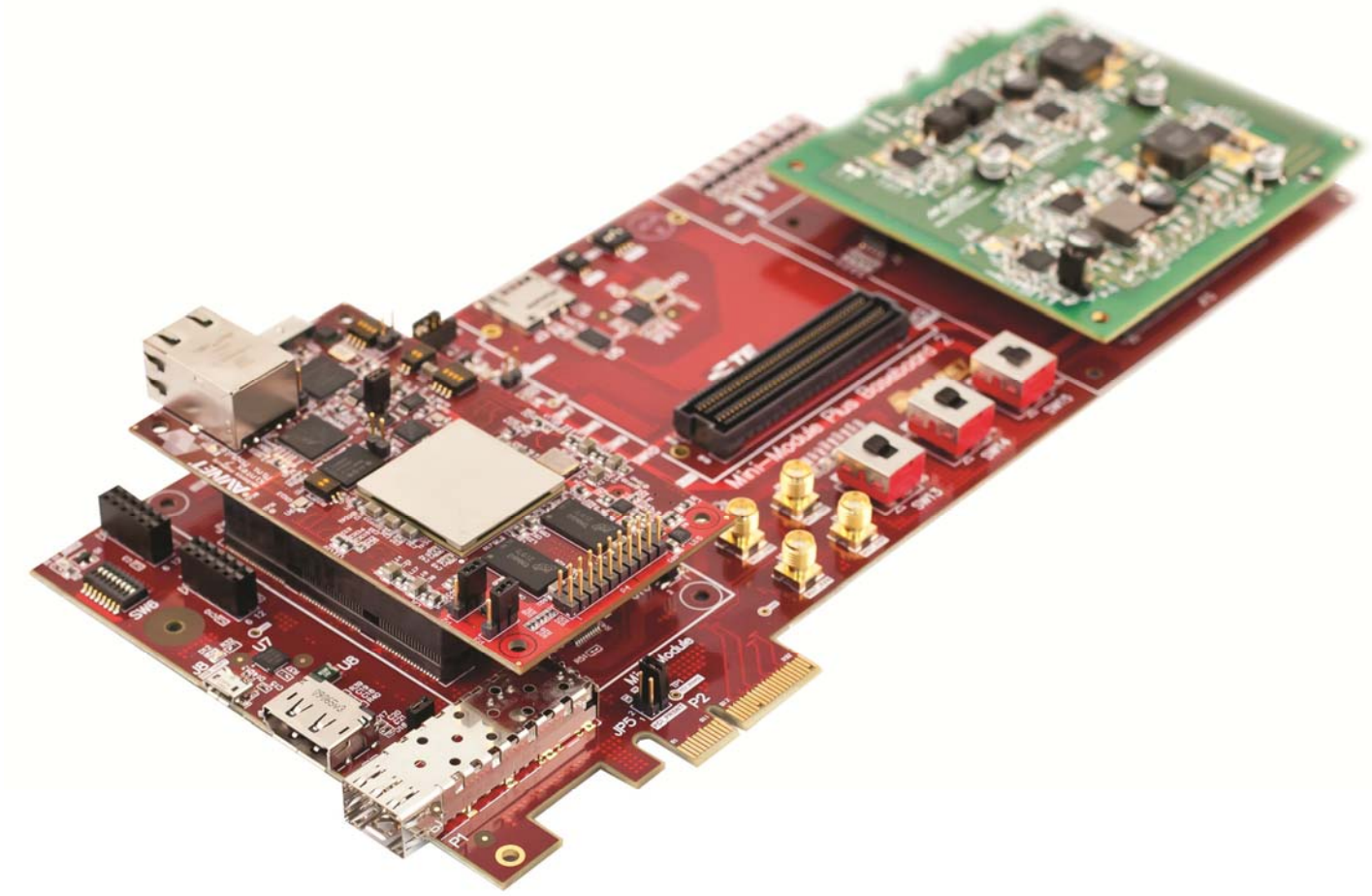


Figure 1 – Assembled Kintex-7 Mini Module Plus Kit (without power supply or cables)

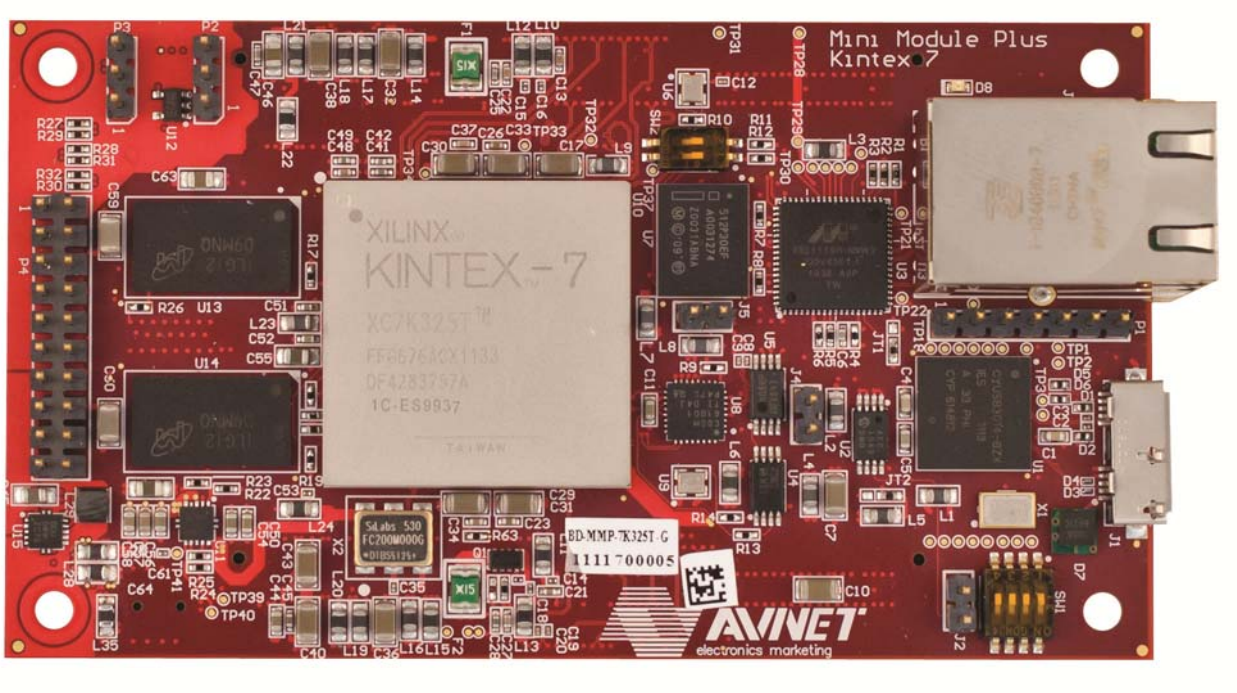


Figure 2 – AES-MMP-7K325T-G Xilinx Kintex-7 Mini-Module Plus (top view)

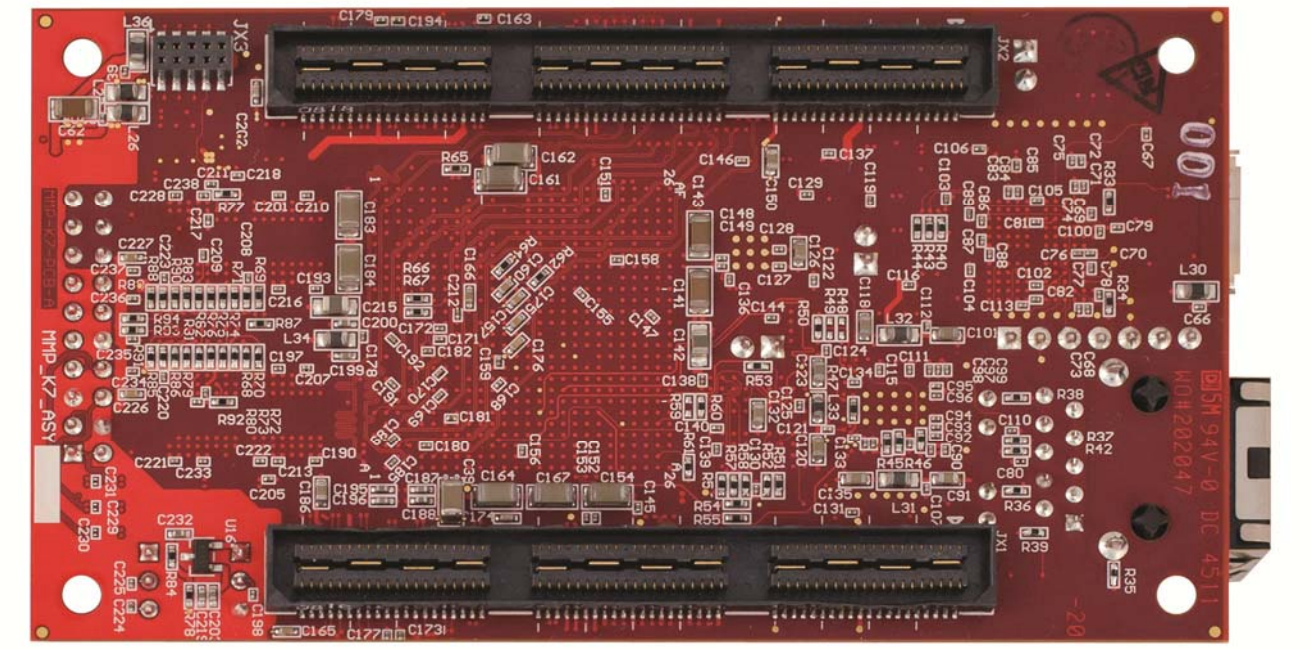


Figure 3 – AES-MMP-7K325T-G Xilinx Kintex-7 Mini-Module Plus (bottom view)

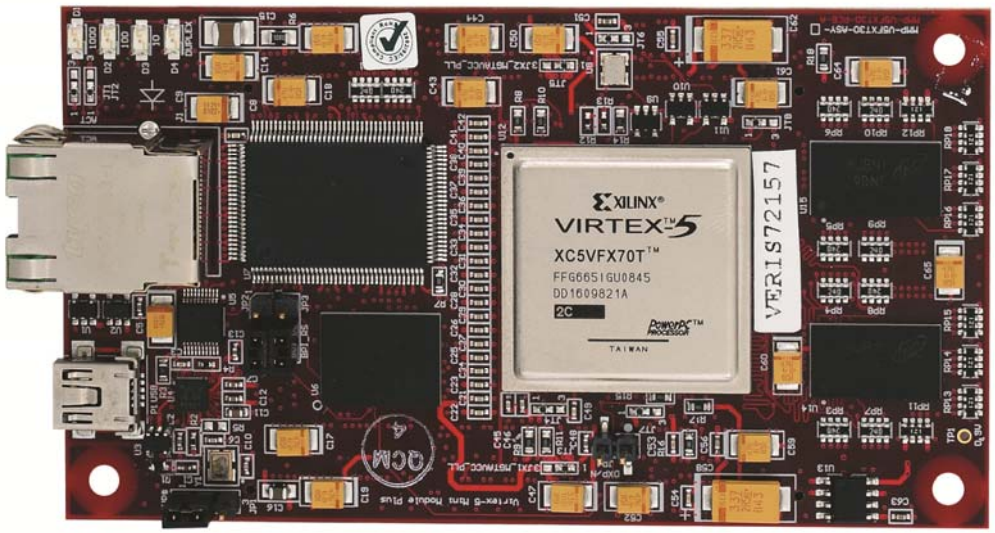


Figure 4 – AES-MMP-V5FXT70-G Xilinx Virtex-5 FXT Mini-Module Plus

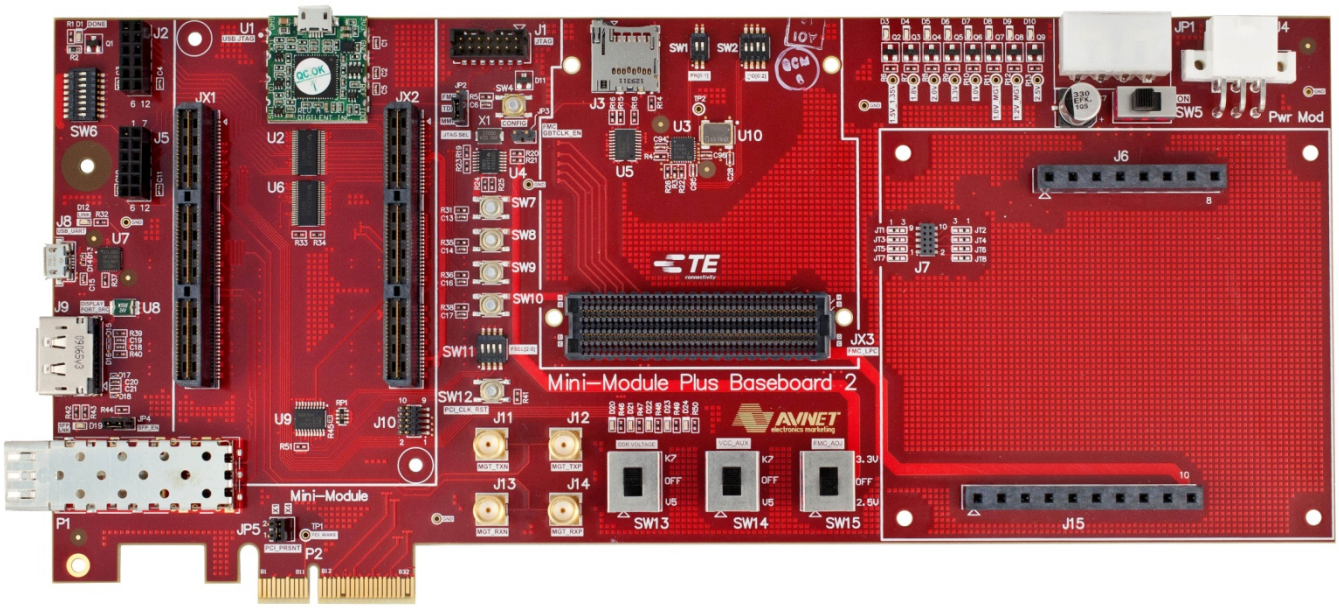


Figure 5 – AES-MMP-BB2-G Avnet Mini-Module Plus baseboard 2 (top view)

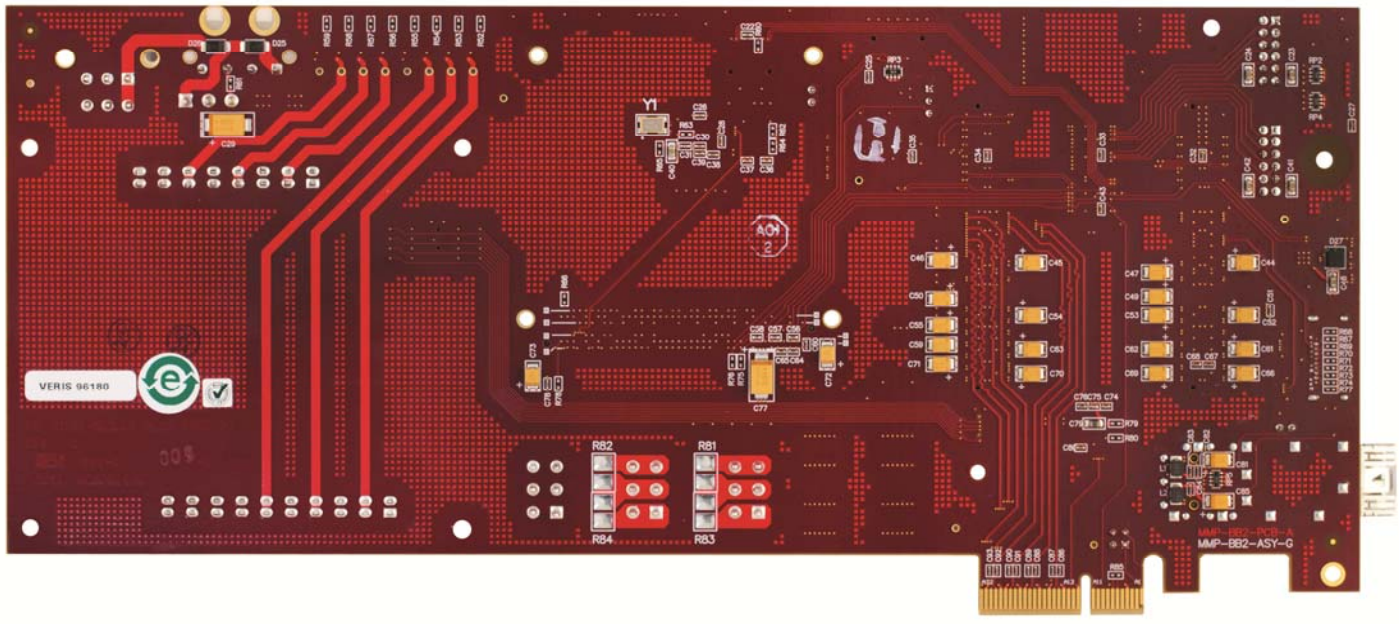


Figure 6 – AES-MMP-BB2-G Avnet Mini-Module Plus baseboard 2 (bottom view)

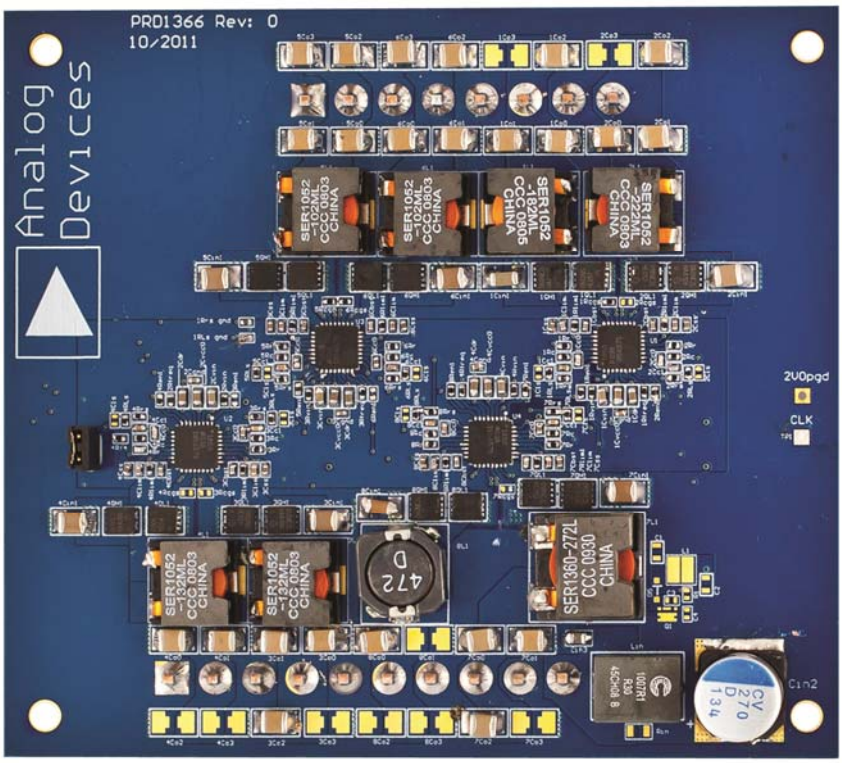


Figure 7 – AES-POM-ANA1-G Analog Devices Power Module

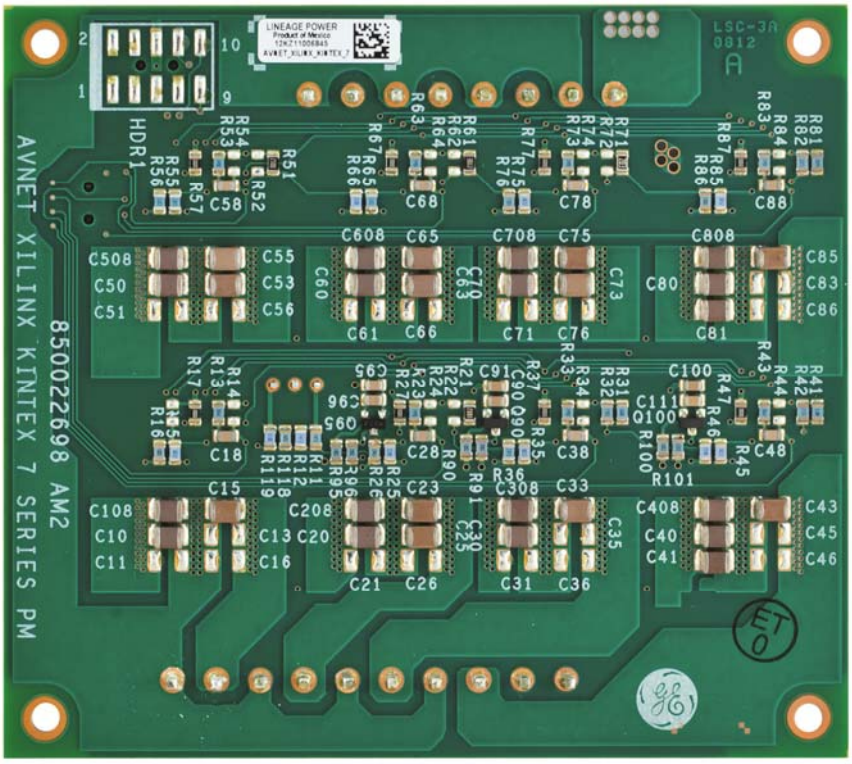


Figure 8 – AES-POM-LTM1-G GE Energy Power Module

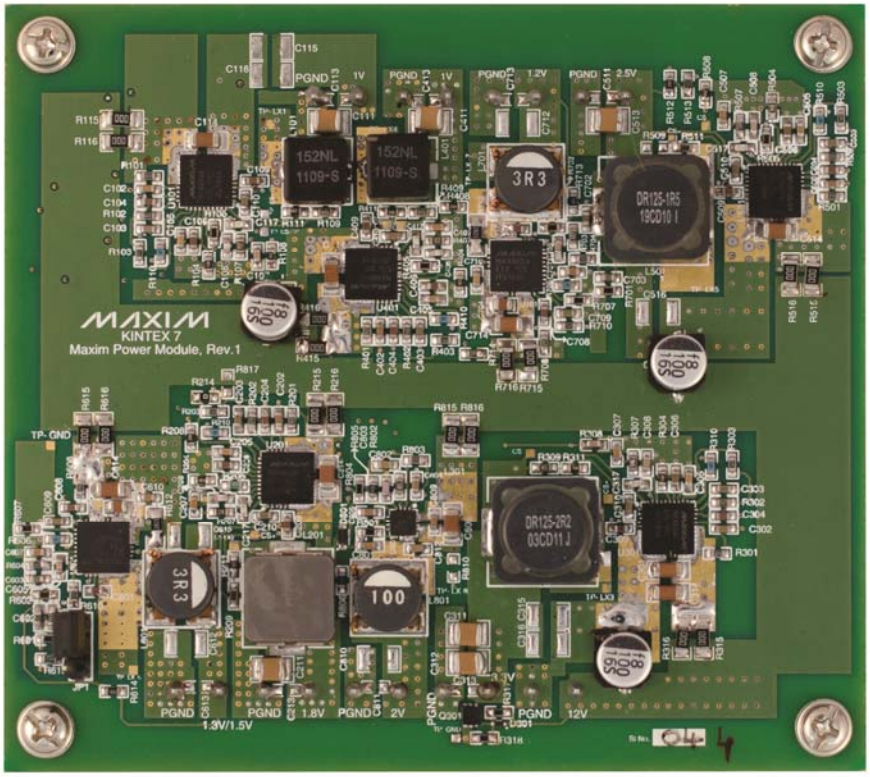


Figure 9 – AES-POM-MXM1-G Maxim Power Module

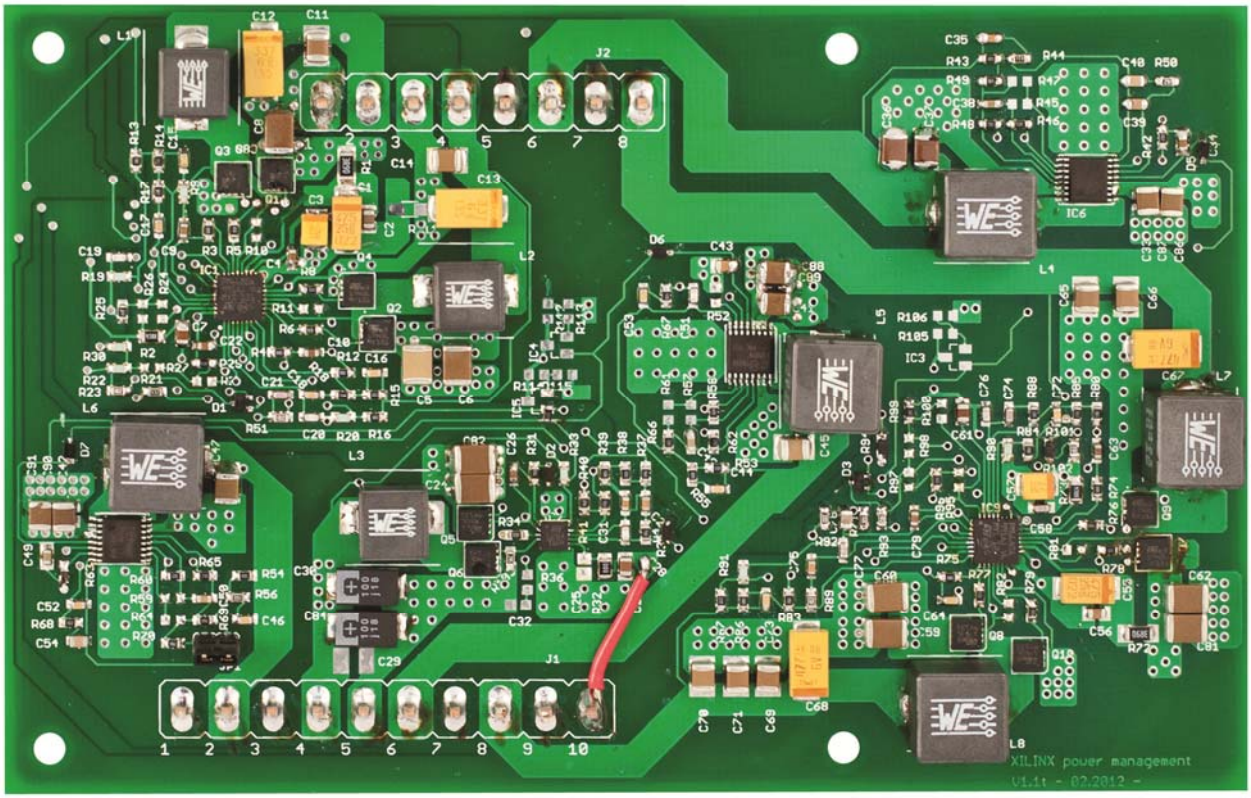


Figure 10 – AES-POM-SGS1-G STMicroelectronics Power Module

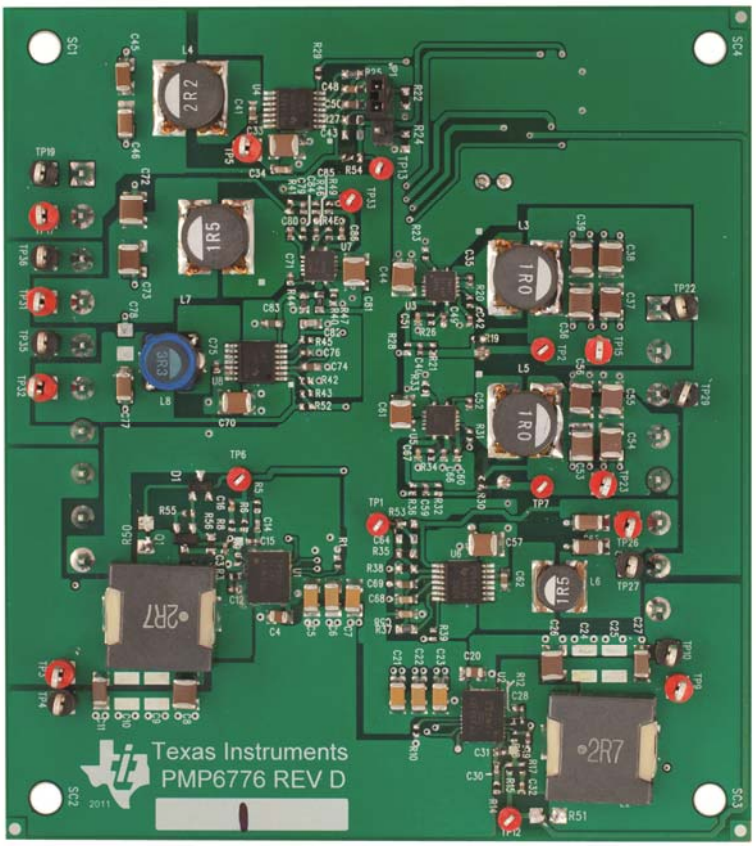


Figure 11 – AES-POM-TIS1-G Texas Instruments Power Module

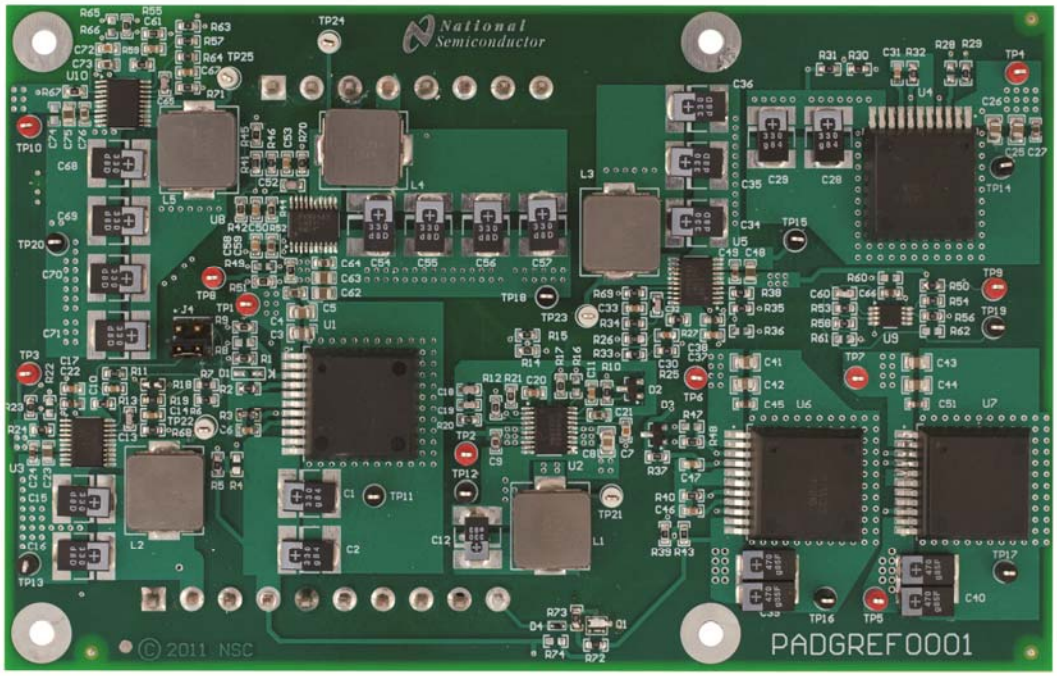


Figure 12 – AES-POM-TISN-G Texas Instruments Simple Switcher Power Module

1.8 Ordering Information

The following table lists the Avnet Mini-Module Plus Baseboard 2 part number and available Mini-Module hardware options.
Internet link at **http://www.em.avnet.com/drc**

	Part Number	Hardware
Baseboard	AES-MMP-BB2-G	Avnet Mini-Module Plus baseboard 2
Mini-Module Hardware Options	AES-MMP-7K325T-G	Xilinx Kintex-7 FXT Mini-Module Plus populated with XC7K325T-1FFG676 FPGA
	AES-MMP-7K410T-G	Xilinx Kintex-7 FXT Mini-Module Plus populated with XC7K410T-1FFG676 FPGA
	AES-MMP-V5FXT70-G	Xilinx Virtex-5 FXT Mini-Module Plus populated with XC5VFX70T-2FF665 FPGA
	AES-MMP-V5FXT30-G	Xilinx Virtex-5 FXT Mini-Module Plus populated with XC5VFX30T-2FF665 FPGA
Power Module Hardware Options	AES-POM-ANA1-G	Analog Devices Power Module
	AES-POM-LTM1-G	GE Energy Power Module
	AES-POM-MXM1-G	Maxim Power Module
	AES-POM-SGS1-G	STMicroelectronics Power Module
	AES-POM-TIS1-G	Texas Instruments Power Module
	AES-POM-TISN-G	Texas instruments Simple Switcher Power Module

Table 1 - Ordering Information

2 Functional Description

The figure below shows the layout of an assembled Kintex-7 Mini Module Plus Kit. The Kintex-7 Mini Module Plus Kit consists of three components, the Kintex-7 Mini Module Plus (#1), Mini Module Plus Baseboard 2 (background), and the Power Module (#3) as shown in the following figure. Modular power supply design allows users to use different manufacturer's power solution on the Mini Module Plus Baseboard 2. For more information on the various Power Modules, please refer to the link **Avnet Power Modules.** The FMC slot (#2) on the Mini Module Plus Baseboard 2 (background) allows customizing user applications using various FMC modules offered by Avnet, Xilinx, and other third party partners.

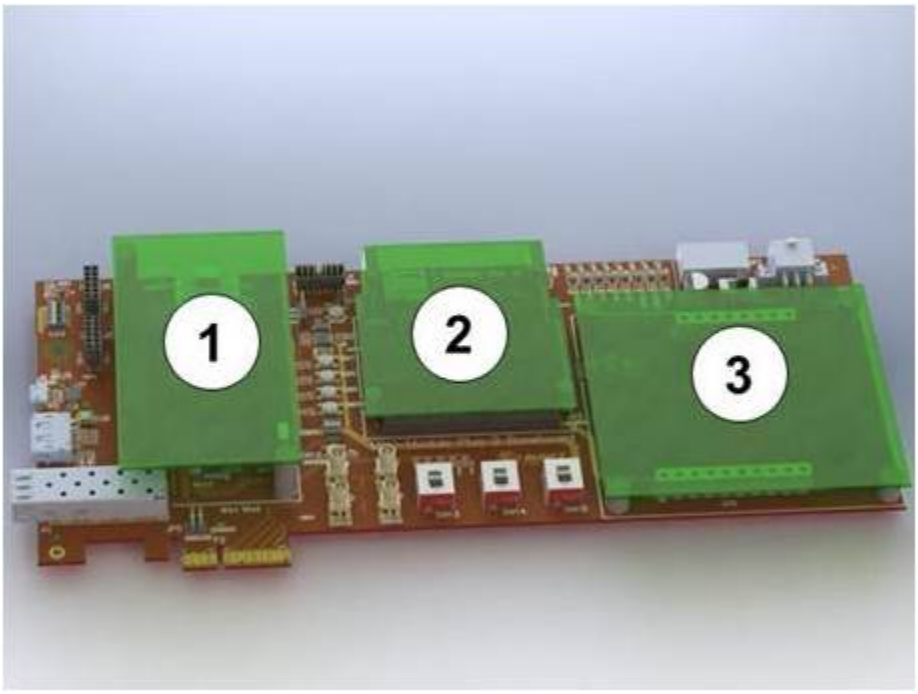


Figure 13 – Assembled Kintex-7 Mini Module Plus Kit Locations.

The Kintex-7 Mini-Module Plus (#1) and the Mini-Module Plus Baseboard 2 (background) combine to make up a powerful FPGA based system with significant capability. The Power Module (#3) supplies power to both. To facilitate describing the entire system, first the Kintex-7 Mini Module Plus (#1) is discussed followed by the Mini Module Plus Baseboard 2.

2.1 Kintex-7 Mini-Module Plus Functional Description

The Kintex-7 MMP is designed to utilize either the XC7K160T, the XC7K325T, or the XC7K410T in the FFG676 package. The –1 speed grade of these two devices will meet the requirements of the MMP design. The following table shows the features of the XC7K160T/XC7K325T/ XC7K410T devices. Note that at present, only the XC7K325T configuration is available.

Device	XC7K160T-1FFG676	XC7K325T-1FFG676	XC7K410T-1FFG676
Slices	**25,350**	**50.950**	**63,550**
Logic Cells	**162,240**	**326,080**	**406,720**
Maximum Distributed RAM (Kbits)	**1,938**	**4,000**	**5,663**
Block RAM (36Kbits)	**325**	**445**	**795**
Mixed Mode Clock Managers (MMCM)	**8**	**10**	**10**
Maximum Single-Ended I/O	**400**	**400**	**400**
Maximum Differential Pairs	**192**	**240**	**240**
DSP48E1 Slices	**600**	**840**	**1540**
PCIe Blocks	**1**	**1**	**1**
Analog Front End (XADC)	**1**	**1**	**1**
GTX Transceivers	**8**	**8**	**8**
Configuration Memory (Mbits)	**51.1**	**87.3**	**121.1**
Maximum DDR3 Data Rate	**1600 Mbps**	**1600 Mbps**	**1600 Mbps**

Table 2 - Kintex-7 Features

Note 1: To achieve maximum DDR3 data rate of 1600 Mbps using a Kintex-7 –1 speed grade part, the Kintex-7 **VCCAUX_IO** rail must be **2.0V** (VCCAUX_IO of 1.8V will support maximum DDR3 data rate of 1066 Mbps). Please refer to the power section of this document for more information.

Kintex-7 Mini-Module Plus Functional Description

A high-level block diagram of the Kintex-7 Mini Module Plus is shown below followed by a brief description of each sub-section.

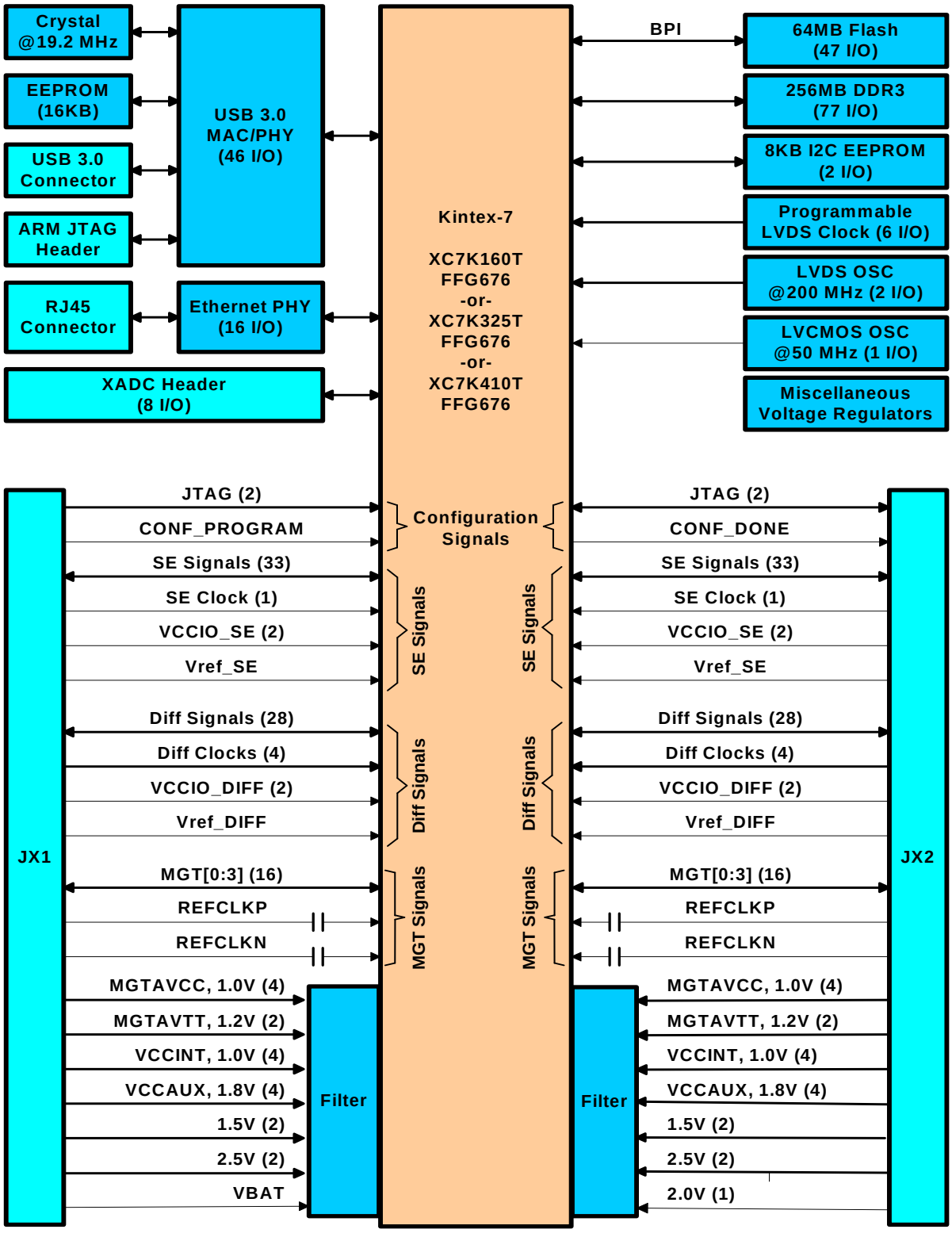


Figure 14 – Kintex-7 Mini Module Plus Block Diagram.

2.1.1 Kintex-7 Bank Pin Assignments

The Kintex-7 MMP uses the XC7K160T, the XC7K325T or the XC7K410T device, which has 8 I/O banks along with 2 GTX banks. The following figure shows the Kintex-7 bank pin assignments on the Kintex-7 Mini Module Plus.

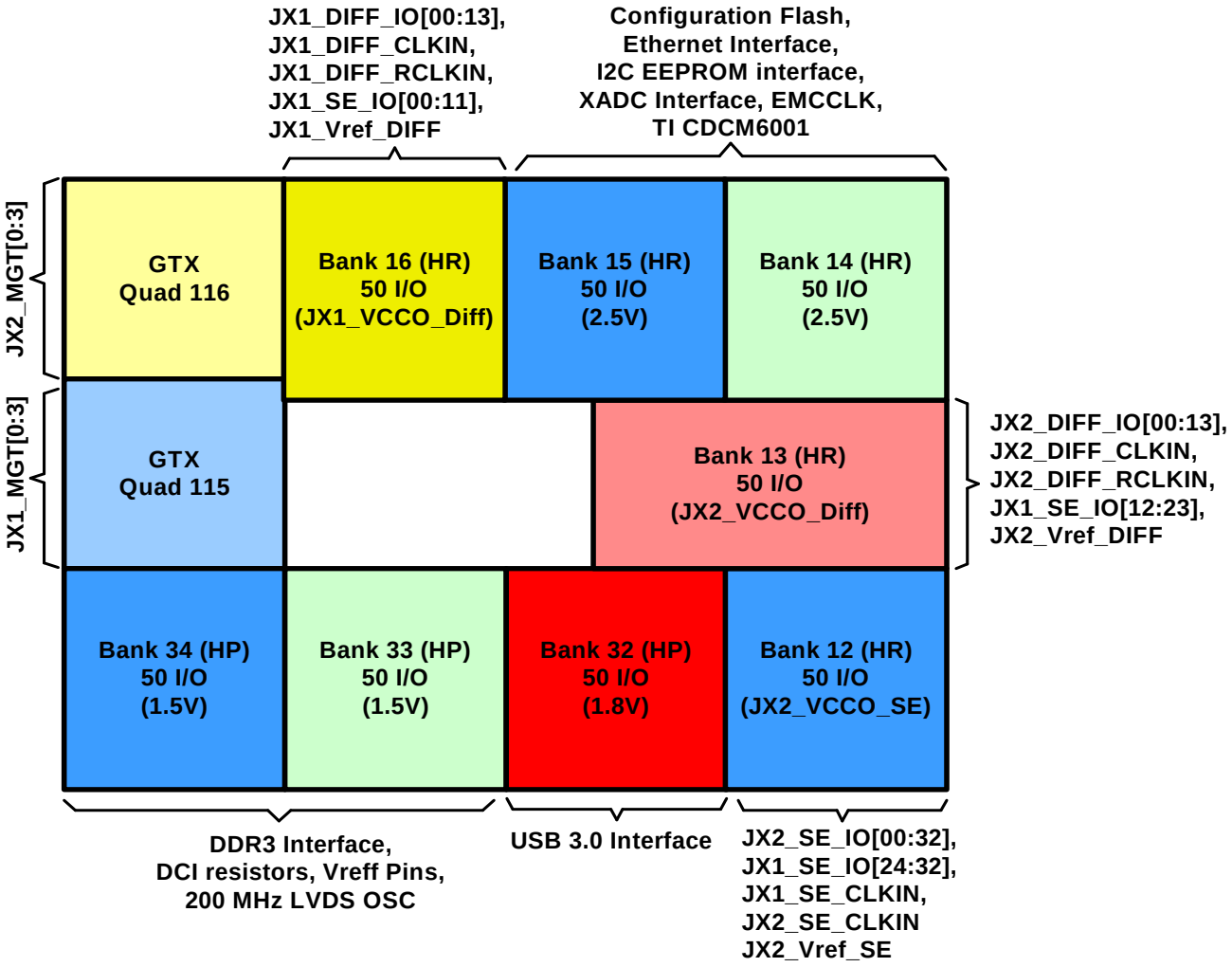


Figure 15 – Kintex-7 Bank Pin Assignments.

Note: Although defined as Single-Ended, all JX1_SE_IO and JX2_SE_IO pins are routed as differential where possible starting with JX1_SE_IO[00:01] pair. This will give the MMP users more flexibility when designing their MMP baseboards. These differential pairs are derived to match the quasi- differential pairing originating from the Virtex-5 FXT Mini-Module Plus.

The bank assignments shown in the above figure are based on the rules shown in the following table.

Kintex-7 Bank	Usage
GTX Quad 116	The four GTX ports in this bank are connected to the MMP JX2 connector and is used on the MMP baseboard for PCIe interface (this is required in order to comply with the PCIe Core Generator design). Please refer to the GTX pin assignment section for more information.
GTX Quad 115	The four GTX ports in this bank is connected to the MMP JX1 connector and is used on the MMP baseboard for FMC LPC slot, SFP module, SMA

	connectors, and the DisplayPort. Please refer to the GTX pin assignment section for more information.
Bank 34 and 34	These two high-performance banks with a maximum VCCO of 1.8V is used for the DDR3 interface in order to comply with the 7-Series MIG design. The 200 MHz LVDS system clock input will also reside in bank 33. Please refer to the DDR3 pinout table for more information.
Bank 32	This high-performance bank with a maximum VCCO of 1.8V is used for the USB 3.0 interface.
Bank 14 and 15	The FPGA BPI configuration interface resides in these two banks. The BPI configuration Flash requires 48 out of maximum 100 I/O pins available in these two banks (please refer to the Flash interface section of this document for specific pin assignments). The remaining of the I/O pins in these banks is used for the Ethernet, I2C EEPROM, XADC, and the TI CDCM6001 interfaces as well as the configuration clock signal EMCCLK. Bank 14 – Flash interface (35 signals), I2C EEPROM interface (2 signals), EMCCLK Bank 15 – Flash interface (12 signals), Ethernet (16 signals), XADC (8 signals), TI CDCM6001 (6 signals)
Bank 12, 13, 16	These are the remaining banks in Kintex-7 device and is used to interface to the JX1/JX2 connectors. Bank 16 is primarily dedicated to the JX1 differential signals, bank 13 is primarily dedicated to the JX2 differential signals, and bank 12 is dedicated to the JX2 single-ended signals. Since there are only three banks available for the JX1/JX2 interface, the JX1 single-ended signals are spread over banks 12, 13, and 16. Banks 12, 13, and 16 each have 22 differential pairs, 4 single-ended pins and 2 Vref pins. Banks 16 is populated starting with the JX1 differential pairs (JX1_DIFF_IO[00:13], JX1_DIFF_CLKIN, and JX1_DIFF_RCLKIN) followed by JX1_SE_IO[00:11] routed as 6 differential pairs. Banks 13 is populated starting with the JX2 differential pairs (JX2_DIFF_IO[00:13], JX2_DIFF_CLKIN, and JX2_DIFF_RCLKIN) followed by JX1_SE_IO[12:23] routed as 6 differential pairs. The bank 16 VCCO is connected to the JX1_VCCO_Diff rail, bank 13 VCCO is connected to the JX2_VCCO_Diff rail, and bank 12 VCCO is connected to the JX2_VCCO_SE rail. The JX1_VCCO_SE rail of the MMP JX1 connector will not be used on the Kintex-7 MMP. Please refer to the above Kintex-7 Bank Pin Assignment figure for detail information on JX1/JX2 pin mapping.

Table 3 - Kintex-7 Bank Usage

2.1.2 DDR3 SDRAM Interface

The Kintex-7 Mini Module Plus provides 256MB of DDR3 memory (64M x 32) as shown in the following figure. The **Micron MT41J64M16JT-125** (1.5V DDR3, 1600 Mbps) is used to implement the DDR3 SDRAM interface.

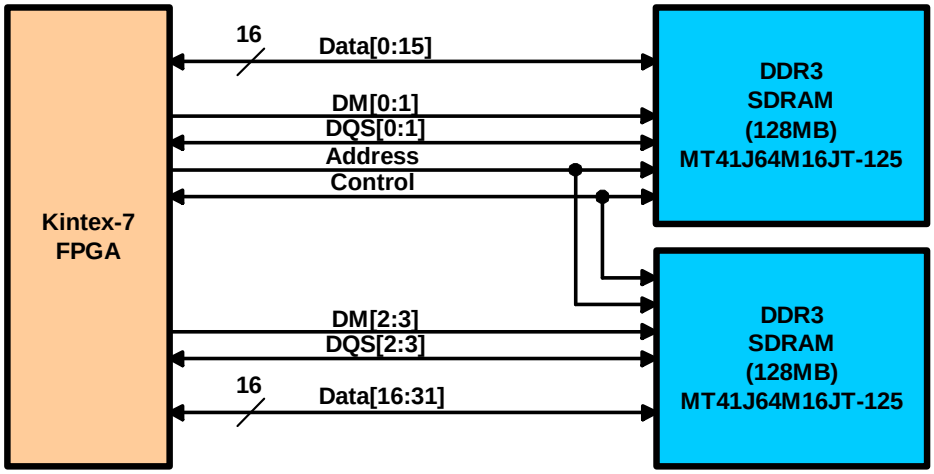


Figure 16 – Kintex-7 MMP DDR3 Memory Interface.

The following table shows the DDR3 interface pinout for the Kintex-7 Mini Module Plus, based on **MIG 7 Series 1.1** version. The XC7K160T / XC7K325T / XC7K410T -FFG676 banks 33 and 34 are used to implement the DDR3 interface. **It should be noted that the VRN/VRP pins for banks 33 and 34 must be used for DCI resistors**.

DDR3 Signal	U10 FPGA Pin	U13 DDR3A Pin	U14 DDR3 B Pin	Other Pins
DDR3_A0	AA8	N3	N3	
DDR3_A1	AF7	P7	P7	
DDR3_A2	AE7	P3	P3	
DDR3_A3	W8	N2	N2	
DDR3_A4	V9	P8	P8	
DDR3_A5	Y10	P2	P2	
DDR3_A6	Y11	R8	R8	
DDR3_A7	Y7	R2	R2	
DDR3_A8	Y8	T8	T8	
DDR3_A9	V7	R3	R3	
DDR3_A10	V8	L7	L7	
DDR3_A11	W11	R7	R7	
DDR3_A12	V11	N7	N7	
DDR3_BA0	AD8	M2	M2	
DDR3_BA1	AC8	N8	N8	
DDR3_BA2	AA7	M3	M3	
DDR3_CAS_N	AC7	K3	K3	
DDR3_RAS_N	AB7	J3	J3	
DDR3_WE_N	AA9	L3	L3	
DDR3_CKE0	AD9	K9	K9	
DDR3_CS_N0	AB9	L2	L2	

DDR3_ODT0	AB11	K1	K1	
DDR3_CK_P0	W10	J7	J7	
DDR3_CK_N0	W9	K7	K7	
DDR3_DM3	AD4		D3	
DDR3_DM2	AA4		E7	
DDR3_DM1	Y3	D3		
DDR3_DM0	U6	E7		
DDR3_DQS_N3	AF4		C7	
DDR3_DQS3	AF5		B7	
DDR3_DQS_N2	AB5		F3	
DDR3_DQS2	AA5		G3	
DDR3_DQS_N1	AC1	C7		
DDR3_DQS1	AB1	B7		
DDR3_DQS_N0	W5	F3		
DDR3_DQS0	W6	G3		
DDR3_DQ31	AF2		A3	
DDR3_DQ30	AF3		B8	
DDR3_DQ29	AE5		A2	
DDR3_DQ28	AE6		A7	
DDR3_DQ27	AE2		C2	
DDR3_DQ26	AE3		C8	
DDR3_DQ25	AE1		C3	
DDR3_DQ24	AD1		D7	
DDR3_DQ23	AD6		H7	
DDR3_DQ22	Y5		G2	
DDR3_DQ21	Y6		H8	
DDR3_DQ20	AC6		H3	
DDR3_DQ19	AB6		F8	
DDR3_DQ18	AC3		F2	
DDR3_DQ17	AC4		F7	
DDR3_DQ16	AB4		E3	
DDR3_DQ15	AA3	A3		
DDR3_DQ14	AC2	B8		
DDR3_DQ13	AB2	A2		
DDR3_DQ12	Y1	A7		
DDR3_DQ11	W1	C2		
DDR3_DQ10	V1	C8		
DDR3_DQ9	V2	C3		
DDR3_DQ8	Y2	D7		
DDR3_DQ7	V4	H7		
DDR3_DQ6	V6	G2		
DDR3_DQ5	U7	H8		
DDR3_DQ4	W3	H3		
DDR3_DQ3	V3	F8		
DDR3_DQ2	U1	F2		
DDR3_DQ1	U2	F7		
DDR3_DQ0	U5	E3		
DDR3_RESETn	AC9	T2	T2	
SYSCLK_P (200 MHz LVDS Clock Source)	AA10			U2.4

SYSCLK_N (200 MHz LVDS Clock Source)	**AB10**			**U2p5**
VRN DCI resistor (bank 33 and 34)	**U9, U4**			
VRP DCI resistor (bank 33 and 34)	**V12, T7**			
Vref (bank 33 and 34)(VTTref)	**W8, W4, AE11, AD3**	**M8, H1**	**M8, H1**	**U11.6**

Table 4 - DDR3 Pinout for the Kintex-7 Mini Module Plus

A “T” termination scheme was used for the split addressing. All routing guidelines used to route the DDR3 memory were based on Micron TN-46-14 and Xilinx UG388. These guidelines encompass the following rules:

DDR3 Trace Impedance is 40 Ohms.
On Die Termination (ODT) is used for data lines.
Digitally Controlled Impedance (DCI) may be used for Address / Control Lines.
Address and control lines use balanced T-routing
Address and command trace spacing is 10 mil min for short runs, 4 mils clearance for parallel runs less than 500 mils.
Data trace spacing is 10 mil min for short runs, 4 mils clearance for parallel runs less than 500 mils
Clock is terminated at the split if length is >1" from split to DDR.
Clock pairs should be equivalent within +/- 20 mil.
Clock should exceed DQS by 1000 mil.
Clock to Address / Control should be matched within +/-400 mil.
Longest to Shortest trace length is <= 800 mil.
Max trace length should be <= 2".
DQ and DQS traces should be matched +/-50 mil, within byte lane.
Follow all other guidelines in Micron TN-46-14 and Xilinx UG388.

Table 5 - DDR3 Routing Rules for the Kintex-7 Mini Module Plus

2.1.3 Parallel Flash Interface

The Kintex-7Mini Module Plus provides **64 Mbytes** of Flash (x16 configuration) using the **Numonyx/Micron PC28F512P30EF** Flash device. The Flash device is used to store the FPGA configuration data as well as user code/data for embedded applications. The **PC28F512P30EF** Flash device can support synchronous read at up to 52 MHz.

The BPI connection between the Flash device and the Kintex-7 FPGA can run in synchronous mode (Master BPI Configuration Mode), which will allow the fastest FPGA configuration. The Kintex-7 XC7K325T has 88.2Mb of configuration memory. Using the Master BPI Synchronous configuration mode and a user CCLK of 50 MHz, the XC7K325T device can be configured in 110ms to meet the FPGA configuration time for PCIe applications (the Kintex-7 XC7K160T with 45.1Mb of configuration memory can be configured in 56ms). The BPI Flash interface signals span over Kintex-7 banks 0, 14, and 15 with most of the signals residing in bank 14 (CCLK and INIT_B signals are dedicated pins and reside in bank 0). Please refer to the Kintex-7 Configuration User Guide (UG470) for more information on BPI Flash connections to the FPGA.

Please note that the 50MHz CCLK (Configuration Clock) is derived from the EMCCLK (External Memory Clock) provided. In order to use this faster configuration clock the following bitgen switches must be enabled:

'#-g StartUpClk:JTAGCLK
'-g StartUpClk:CCLK
'-g ExtMasterCclk_en:div-1
'-g BPI_sync_mode:Type2

Table 6 - Parallel Flash Fast Configuration Bitgen Settings the Kintex-7 Mini Module Plus

Please also note that the 50MHz CCLK (Configuration Clock) bitgen switch settings currently prevent generation of a flash loader mcs file that will address Flash memory properly to load applications from Flash to DDR3. Default bitgen settings must be used.

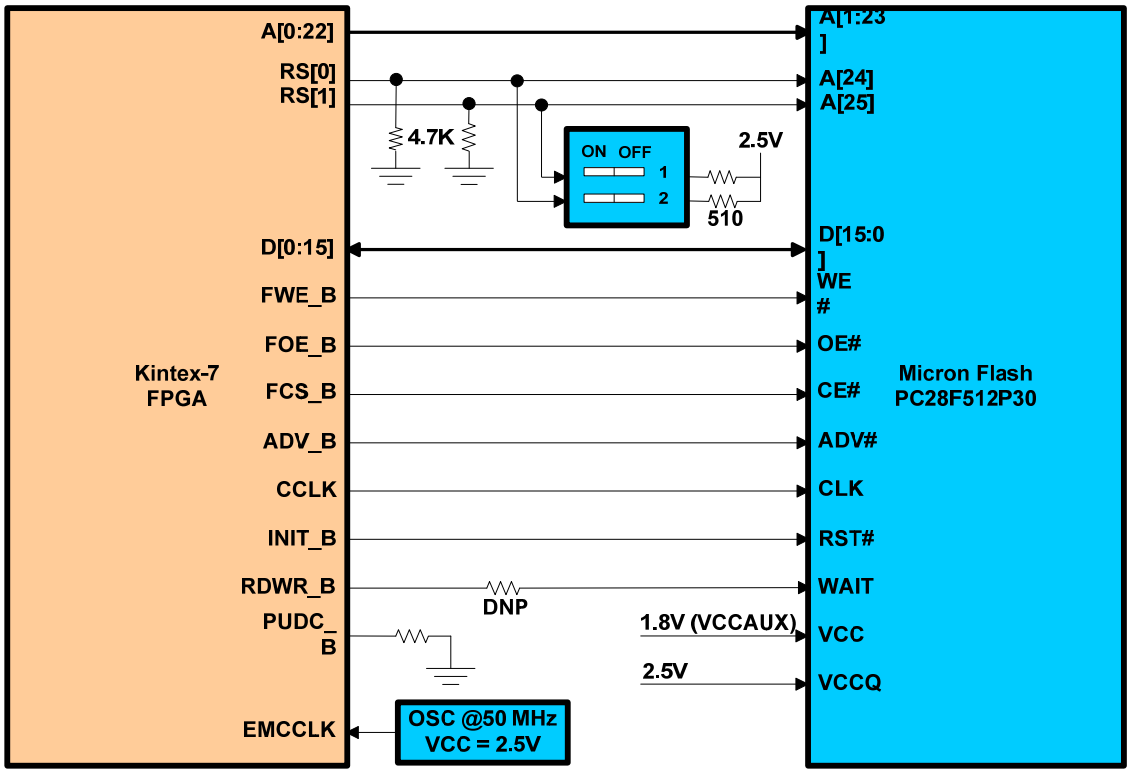


Figure 17 – Kintex-7 Mini Module Plus Parallel Flash Interface.

Note 1: Since the Flash interface on the Kintex-7 MMP runs at 2.5V, the Kintex-7 bank 0 VCCO must also run at 2.5V (bank 0 provides some of the configuration signals connected to the Flash).

Note 2: The Flash device A[1] must be connected to the FPGA BPI interface A[0] to prevent address misalignment.

Note 3: The DIP switch allows initial configuration from four different memory locations.

The following table shows the BPI Flash interface pinout for the Kintex-7 Mini Module Plus The XC7K160T / XC7K325T / XC7K410T -FFG676 banks 0 and 14 and 15 are used to implement the Flash interface.

Flash Signal	U10 FPGA Pin	U7 Flash Pin	Other Pins
FLASH_A1	L17	**A1**	
FLASH_A2	K18	**B1**	
FLASH_A3	K20	**C1**	
FLASH_A4	J20	**D1**	
FLASH_A5	J18	**D2**	
FLASH_A6	J19	**A2**	
FLASH_A7	L20	**C2**	
FLASH_A8	K16	**A3**	
FLASH_A9	K17	**B3**	
FLASH_A10	G26	**C3**	
FLASH_A11	F25	**D3**	
FLASH_A12	E26	**C4**	
FLASH_A13	J26	**A5**	
FLASH_A14	H26	**B5**	
FLASH_A15	H21	**C5**	
FLASH_A16	G21	**D7**	
FLASH_A17	H23	**D8**	
FLASH_A18	H24	**A7**	
FLASH_A19	H22	**B7**	
FLASH_A20	J24	**C7**	
FLASH_A21	J25	**C8**	
FLASH_A22	L22	**A8**	
FLASH_A23	K22	**G1**	
FLASH_A24	K23	**H8**	
FLASH_A25	J23	**B6**	
FLASH_CHIP_SEL_NOT (CE#)	C23	**B4**	
FLASH_OUTPUT_ENABLE_NOT (OE#)	M17	**F8**	
FLASH_WRITE_ENABLE_NOT (WE#)	L18	**G8**	
FLASH_D0	B21	**F2**	
FLASH_D1	C21	**E2**	
FLASH_D2	E22	**G3**	
FLASH_D3	A20	**E4**	
FLASH_D4	B20	**E5**	
FLASH_D5	C22	**G5**	
FLASH_D6	D21	**G6**	
FLASH_D7	C24	**H7**	
FLASH_D8	C26	**E1**	
FLASH_D9	D26	**E3**	
FLASH_D10	A24	**F3**	
FLASH_D11	A23	**F4**	
FLASH_D12	A22	**F5**	

FLASH_D13	B22	**H5**	
FLASH_D14	A25	**G7**	
FLASH_D15	B24	**E7**	
CLOCK_TO_FLASH (CCLK)(CLK)	**C8**	**E6**	
FLASH_ADDR_VALID_NOT (ADV#)	D20	**F6**	
FLASH_READ_WRITE (WAIT)	**E25**	**F7**	
FLASH_RESET_NOT (INITB)(RST#)	**G7**	**D4**	
EMCCLK	**B26**		U6.3
Flash Write Protect Not		**C6**	J5.1

Table 7 - Parallel Flash pinout for the Kintex-7 Mini Module Plus

2.1.4 I2C EEPROM

The Kintex-7 MMP will provide 8KB of EEPROM for storing board level parameters and system settings such as the MAC address for the MMP and MMP baseboard Ethernet ports. The **ST Microelectronics M24C08** is used to implement this interface. The EEPROM interfaces to the Kintex-7 FPGA via I2C bus. The **M24C08** VCC is connected to the **2.5V** rail. Note that shunt J4 must be installed for write access.

The following table shows the I2C EEPROM interface pinout for the Kintex-7 Mini Module Plus The XC7K160T / XC7K325T / XC7K410T -FFG676 bank 14 is used to implement the I2C interface.

EEPROM Signal	U10 FPGA Pin	U5 Flash Pin
IIC_EEPROM_SCL	E23	**6**
IIC_EEPROM_SDA	F22	**5**

Table 8 - EEPROM pinout for the Kintex-7 Mini Module Plus

2.1.5 10/100/1000 PHY Interface

The Mini Module Plus provides a 10/100/1000 Ethernet port. The **Marvell 88E1119R** device is used to implement this interface. All Ethernet GMII interface signals reside in bank 15 of the Kintex-7 FPGA. A high-level block diagram of the 10/100/1000 Ethernet interface is shown in the following figure.

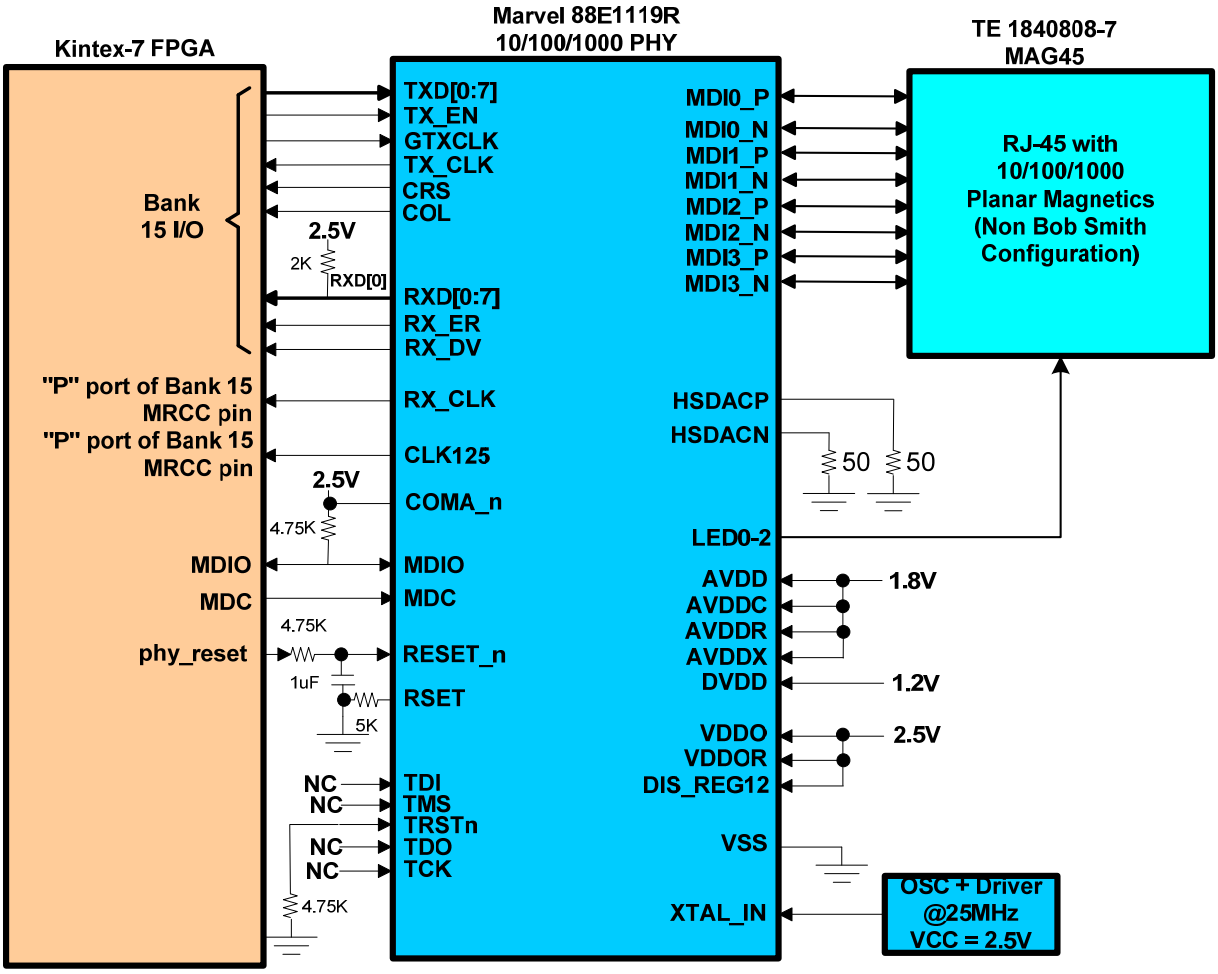


Figure 18 – Kintex-7 Mini Module Plus Ethernet Interface.

The following table shows the 10/100/1000 Ethernet Interface routing rules used to implement the GMII:

Trace Impedence = 40 Ohms
Length match to < 385 mil
Spacing is 10 mil for short runs, 4 mils for parallel runs < 500 mils.
Route RX and TX away from each other
Place series term resistor close to transmitter

Table 9 – Ethernet 10/100/1000 GMII routing rules for the Kintex-7 Mini Module Plus

The following table shows the 10/100/1000 Ethernet Interface routing rules used to implement the Twisted Pair Interface:

Differential Impedence is 100 Ohms.
Route pairs apart by 3X trace height from plane.
Match lengths as close as possible.
Do not use serpentines to make traces match.
Symetry is important.

Table 10 – Ethernet 10/100/1000 TPI routing rules for the Kintex-7 Mini Module Plus

The following table shows the 10/100/1000 Ethernet interface pinout for the Kintex-7 Mini Module Plus. The XC7K160T / XC7K325T / XC7K410T -FFG676 bank 15 is used to implement the GMII interface.

Ethernet Signal	U10 FPGA Pin	U3 PHY Pin	Other Pins
MDIO	G20	49	
MDC	H19	52	
CLK125	E18	9	
RESETn	K15	14	
CRS	G19	54	
COL	F20	53	
RX_CLK	F17	57	
RX_ER	G16	55	
RX_DV	H16	56	
RXD0	B17	59	
RXD1	A17	60	
RXD2	C19	61	
RXD3	B19	62	
RXD4	C17	63	
RXD5	C18	64	
RXD6	D15	65	
RXD7	D16	66	
GTX_CLK	E17	6	
TX_CLK	H17	67	
TX_EN	D18	69	
TXD0	G15	70	
TXD1	F15	71	
TXD2	J15	72	
TXD3	J16	1	
TXD4	E15	2	
TXD5	E16	3	
TXD6	G17	4	
TXD7	F18	5	
MDI0_P		34	J3.2
MDI0_N		33	J3.3
MDI1_P		29	J3.4
MDI1_N		28	J3.5
MDI2_P		27	J3.7
MDI2_N		26	J3.8
MDI3_P		23	J3.9
MDI3_N		22	J3.10
LED0		10	J3.13
LED1		11	J3.11
XTAL_IN		41	U4.8

Table 11 – Ethernet 10/100/1000 pinout for the Kintex-7 Mini Module Plus

2.1.6 CYUSB3014 USB 3.0 Controller Interface

The Kintex-7 Mini Module Plus provides a USB 3.0 interface using the **Cypress CYUSB3014 USB 3.0 Controller**. The following figure shows a high-level block diagram of the USB interface on the Kintex-7 Mini Module Plus.

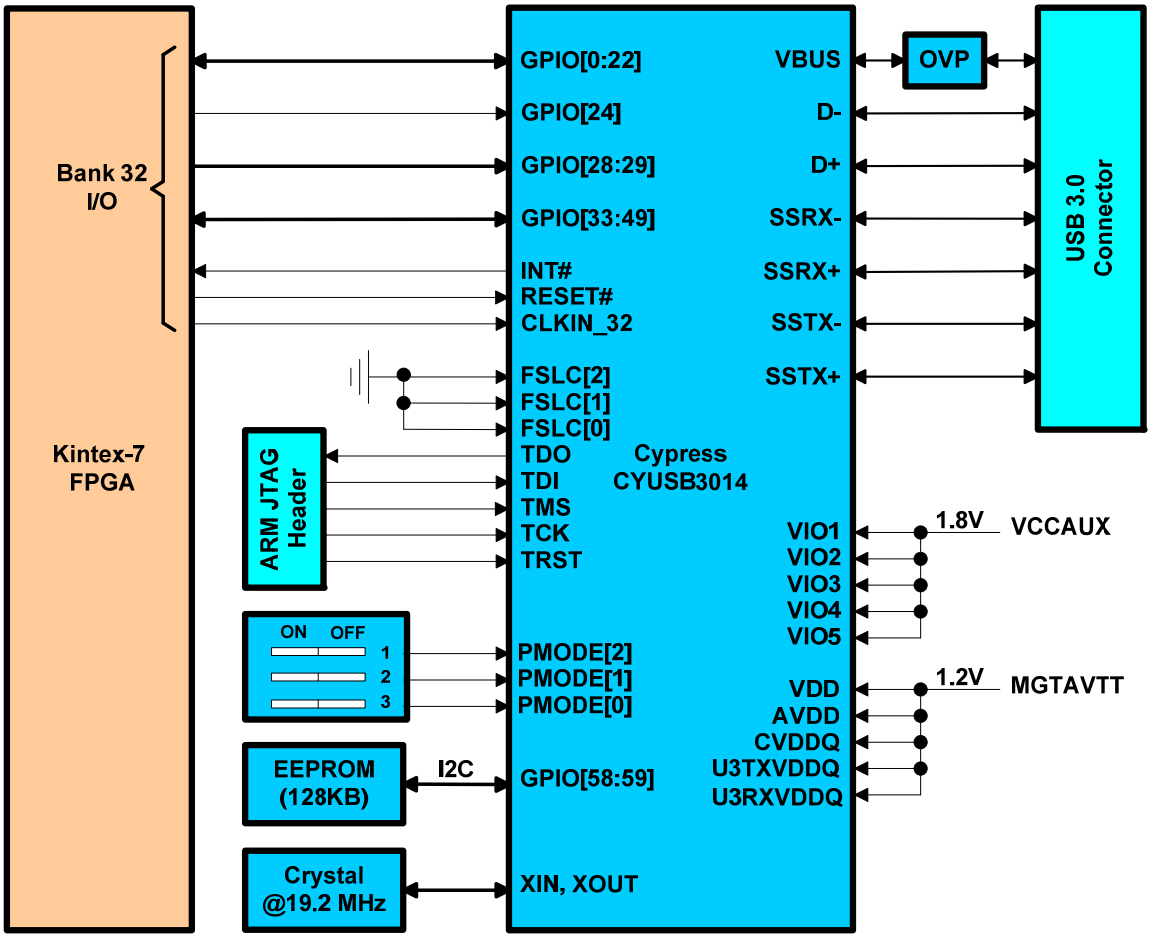


Figure 19 – Kintex-7 Mini Module Plus CYUSB3014 USB 3.0 Controller Interface.

2.1.6.1 CYUSB3014 USB 3.0 Controller EEPROM

The AT24C1024B provides 1,048,576 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 131,072 words of 8 bits each. This device is used to implement the IIC Boot EEPROM interface. The EEPROM interfaces to the USB controller via I2C bus and is used as an optional boot device. The AT24C1024B VCC is connected to the **1.8V** rail. Note that this EEPROM is programmed using the Cypress USB3 Control Center Windows application in conjunction with the bootloader firmware accessed through the USB3 boot configuration option with SW1[2:0] open, 1, 1. Once the EEPROM is programmed, it can be accessed by setting the SW1[2:0] open, 1, open. Note that the FX3 RESET# line needs to be toggled between each change, which can be done from the factory test console using “usbrst”.

Please note that the Cypress tools allow for user to build to types of images, a debug image and a non-debug image. Building a debug image results in an image size of greater than 128KB. User's must insure to build a non-debug version of the image to insure successful programming of the EEPROM.

Also please note that the Cypress tool target device default is Microchip I2C EEPROM, when in fact the Kintex-7 Mini-Module Plus implements an Atmel device. Users must be sure to select the proper Atmel device from the device target list to insure successful programming of the EEPROM.

2.1.6.2 CYUSB3014 USB 3.0 Controller ARM JTAG Header

The USB controller JTAG interface provides a "flywire" compatible five-pin interface for connecting to a JTAG debugger to debug firmware through the CPU-core's on-chip-debug circuitry. Industry standard debugging tools for the ARM926EJ-S core can be used for the USB controller application development.

2.1.6.3 CYUSB3014 USB 3.0 Controller Routing

The following table shows the CYUSB3014 USB 3.0 Controller Interface routing rules used to implement the GPIOII:

USB_GPIO may be swapped within the same bank.
GPIO Interface Impedence is 50 Ohms.
Length match to 200 mils.
Spacing is 10 mil min for short runs, 4 mils clearance for parallel runs less than 500 mils.
Place any series resistors close to FPGA drivers.

Table 12 – CYUSB3014 USB 3.0 Controller GPIOII routing rules for the Kintex-7 Mini Module Plus

The following table shows the CYUSB3014 USB 3.0 Controller Interface routing rules used to implement the Twisted Pair Interface:

Differential Impedence is 90 Ohms.
Do Not cross traces.
Differential Pairs can be polarity swapped.
SS pairs should be matched within 5 mils
D+/D- pairs should be matched within 50 mils
AC Coupling Caps:
Remove (cut-out) reference plane directly underneath capacitor body and pads.
Do not route traces under this cutout between the reference plane cutout and the next plane.
Circuit protection:
Remove (cut-out) reference plane directly underneath device body and pads.
Do not route traces under this cutout between the reference plane cutout and the next plane.

Table 13 – CYUSB3014 USB 3.0 Controller TPI routing rules for the Kintex-7 Mini Module Plus

2.1.6.4 CYUSB3014 USB 3.0 Controller Pinout

The following table shows the CYUSB3014 USB 3.0 Controller interface pinout for the Kintex-7 Mini Module Plus. The XC7K160T / XC7K325T / XC7K410T -FFG676 bank 32 is used to implement the GPIOII interface.

CYUSB3014 USB 3.0 Controller Signal	FPGA Interface Signal	U10 FPGA Pin	U1 PHY Pin	Other Pins
GPIO[0]	axi_usb_interface_0_USB_FIFODATA[0]	AF19	F10	
GPIO[1]	axi_usb_interface_0_USB_FIFODATA[1]	AD14	F9	
GPIO[2]	axi_usb_interface_0_USB_FIFODATA[2]	AA18	F7	
GPIO[3]	axi_usb_interface_0_USB_FIFODATA[3]	AF20	G10	
GPIO[4]	axi_usb_interface_0_USB_FIFODATA[4]	AF18	G9	
GPIO[5]	axi_usb_interface_0_USB_FIFODATA[5]	AB20	F8	
GPIO[6]	axi_usb_interface_0_USB_FIFODATA[6]	AE20	H10	
GPIO[7]	axi_usb_interface_0_USB_FIFODATA[7]	AD18	H9	
GPIO[8]	axi_usb_interface_0_USB_FIFODATA[8]	AF14	J10	
GPIO[9]	axi_usb_interface_0_USB_FIFODATA[9]	AD16	J9	
GPIO[10]	axi_usb_interface_0_USB_FIFODATA[10]	AE17	K11	
GPIO[11]	axi_usb_interface_0_USB_FIFODATA[11]	AE18	L10	
GPIO[12]	axi_usb_interface_0_USB_FIFODATA[12]	AE15	K10	
GPIO[13]	axi_usb_interface_0_USB_FIFODATA[13]	AD20	K9	
GPIO[14]	axi_usb_interface_0_USB_FIFODATA[14]	AC19	J8	
GPIO[15]	axi_usb_interface_0_USB_FIFODATA[15]	AD15	G8	
GPIO[16]	axi_usb_interface_0_USB_IFCLK_pin	AB16	J6	
GPIO[17]	axi_usb_interface_0_USB_SLCS_L_pin	AD19	K8	
GPIO[18]	axi_usb_interface_0_USB_SLWR_L_pin	AC16	K7	
GPIO[19]	axi_usb_interface_0_USB_SLOE_L_pin	AC18	J7	
GPIO[20]	axi_usb_interface_0_USB_SLRD_L_pin	AB17	H7	
GPIO[21]	axi_usb_interface_0_USB_FLAGA_FULL_L_pin	AF15	G7	
GPIO[22]	axi_usb_interface_0_USB_FLAGB_EMPTY_L_pin	AA19	G6	
GPIO[24]	axi_usb_interface_0_USB_PKTEND_L_pin	AF17	H8	
GPIO[28]	axi_usb_interface_0_USB_FIFOADDR_pin[1]	AB15	J5	
GPIO[29]	axi_usb_interface_0_USB_FIFOADDR_pin[0]	AA15	H5	
GPIO[33]		V19	K2	
GPIO[34]		Y16	J4	
GPIO[35]		V18	K1	
GPIO[36]		W18	J2	
GPIO[37]		W19	J3	
GPIO[38]		Y15	J1	
GPIO[39]		AB14	H2	
GPIO[40]		V17	H3	
GPIO[41]		W15	F4	
GPIO[42]		V16	G2	
GPIO[43]		AC14	G3	
GPIO[44]		AA17	F3	
GPIO[45]		V14	F2	
GPIO[46]		W16	F5	
GPIO[47]		AA14	E1	

GPIO[48]		AA20	E5	
GPIO[49]		W14	E4	
PMODE[0]_GPIO[30]			G4	SW1.8
PMODE[1]_GPIO[31]			H4	SW1.7
PMODE[2]_GPIO[32]			L4	SW1.6
INT#	USB_INT_N	AC17	L8	R96
RESET#	axi_usb_interface_0_USB_RESET_L_pin	AB19	C5	R95
CLKIN_32		Y17	D6	
XTALIN			C6	X1.1
XTALOUT			C7	x1.3
VBUS			E11	J1.1
DM			A10	J1.2
DP			A9	J1.3
OTG_ID			C9	J1.4
SSTXM			A6	J1.6
SSTXP			A5	J1.7
SSRXM			A3	J1.9
SSRXP			A4	J1.10
R_usb2			C8	R33
R_usb3			B3	R34
TDI			E7	P1.1
TDO			C10	P1.2
TRST#			B11	P1.3
TMS			E8	P1.4
TCK			F6	P1.5

Table 14 – CYUSB3014 USB 3.0 Controller pinout for the Kintex-7 Mini Module Plus

2.1.7 Kintex-7 Mini Module Plus GTX TX/RX and Clock Connections

The following tables show the FPGA GTX TX/RX and clock pin assignments to the MMP JX1/JX2 connectors (**this is required in order to comply with the PCIe pin assignments on the MMP baseboard**).

Kintex-7 GTX Bank / Tile	MMP Baseboard 2 Application	Kintex-7 Pin	Mini Module Plus Connector Signal Name	Mini Module Plus Connector Pin
Bank 116 GTX_X0Y4	PCIe Lane 2	D2	JX2_MGTTX0_P	JX2.44
		D1	JX2_MGTTX0_N	JX2.46
		E4	JX2_MGTRX0_P	JX2.43
		E3	JX2_MGTRX0_N	JX2.45
Bank 116 GTX_X0Y5	PCIe Lane 3	F2	JX2_MGTTX1_P	JX2.50
		F1	JX2_MGTTX1_N	JX2.52
		G4	JX2_MGTRX1_P	JX2.49

		G3	JX2_MGTRX1_N	JX2.51
Bank 116 GTX_X0Y6	PCIe Lane 0	A4	JX2_MGTTX2_P	JX2.56
		A3	JX2_MGTTX2_N	JX2.58
		B6	JX2_MGTRX2_P	JX2.55
		B5	JX2_MGTRX2_N	JX2.57
Bank 116 GTX_X0Y7	PCIe Lane 1	B2	JX2_MGTTX3_P	JX2.62
		B1	JX2_MGTTX3_N	JX2.64
		C4	JX2_MGTRX3_P	JX2.61
		C3	JX2_MGTRX3_N	JX2.63
Bank 115 GTX_X0Y0	FMC	P2	JX1_MGTTX0_P	JX1.44
		P1	JX1_MGTTX0_N	JX1.46
		R4	JX1_MGTRX0_P	JX1.43
		R3	JX1_MGTRX0_N	JX1.45
Bank 115 GTX_X0Y1	SFP	M2	JX1_MGTTX1_P	JX1.50
		M1	JX1_MGTTX1_N	JX1.52
		N4	JX1_MGTRX1_P	JX1.49
		N3	JX1_MGTRX1_N	JX1.51
Bank 115 GTX_X0Y2	DisplayPort	K2	JX1_MGTTX2_P	JX1.56
		K1	JX1_MGTTX2_N	JX1.58
		L4	JX1_MGTRX2_P	JX1.55
		L3	JX1_MGTRX2_N	JX1.57
Bank 115 GTX_X0Y3	SMA	H2	JX1_MGTTX3_P	JX1.62
		H1	JX1_MGTTX3_N	JX1.64
		J4	JX1_MGTRX3_P	JX1.61
		J3	JX1_MGTRX3_N	JX1.63

Table 15 – GTX TX/RX Pin Assignments for the Kintex-7 Mini Module Plus

Kintex-7 Bank / Clock	Kintex-7 Pin	Clock Source	Mini Module Plus Connector Pin
Bank116 / RefClock1	F6	MMP Connector JX2_MGTREFCLK_P Clock Input, PCIe	JX2.67
Bank116 / RefClock1	F5	MMP Connector JX2_MGTREFCLK_N Clock Input, PCIe	JX2.69
Bank115 / RefClock1	K6	MMP Connector JX1_MGTREFCLK_P Clock Input	JX1.67
Bank115 / RefClock1	K5	MMP Connector JX1_MGTREFCLK_N Clock Input	JX1.69
Bank115 / RefClock0	H6	On Board TI CDCM6001 Programmable LVDS Clock Source (Please see the Programmable LVDS Clock Source section of this document)	
Bank115 / RefClock0	H5		

Table 16 – GTX Clock Pin Assignments for the Kintex-7 Mini Module Plus

Note: The TI CDCM6001 programmable LVDS clock source provides a local reference clock input to the Kintex-7 GTX ports.

JX1 MGT: SFP, Display Port, SMA; JX2 MGT: PCIe
Differential Impedence is 85 Ohms.
Length Match to 10 mil within pair.
Length Match to 50 mil pair to pair within lane (TX to RX).
Use 4X Spacing between pairs.
No more than two layer to layer transitions (via's) are allowed.
Transitions must utilize GSSG via structure.
No foreign traces or planes may enter the GSSG structure.
Reference Clock length shall not exceed 4 inches total.
Length Match Reference Clock to 10 mil within pair.
Route MGT Signals in accordance with Xilinx 7 Series FPGAs GTX Transceivers User Guide UG476.
AC Coupling Caps:
Remove (cut-out) reference plane directly underneath capacitor body and pads.
Do not route traces under this cutout between the reference plane cutout and the next plane.

Table 17 – GTX routing rules for the Kintex-7 Mini Module Plus for the Kintex-7 Mini Module Plus

2.1.8 GTX Programmable LVDS Clock Source

The Kintex-7 MMP uses the **TI CDCM6001** clock synthesizer to provide a reference clock 0 input to the Kintex-7 Bank 115 GTX ports as shown in the following figure. The CDCM6001 device is powered by 3.3V which is inductively isolated from the off-board supply and the Analog section. The CDCM6001 control signals are “wire-or”ed to switches and the FPGA so that either can program the device. Not shown are external 4.7K pull-ups on the control lines.

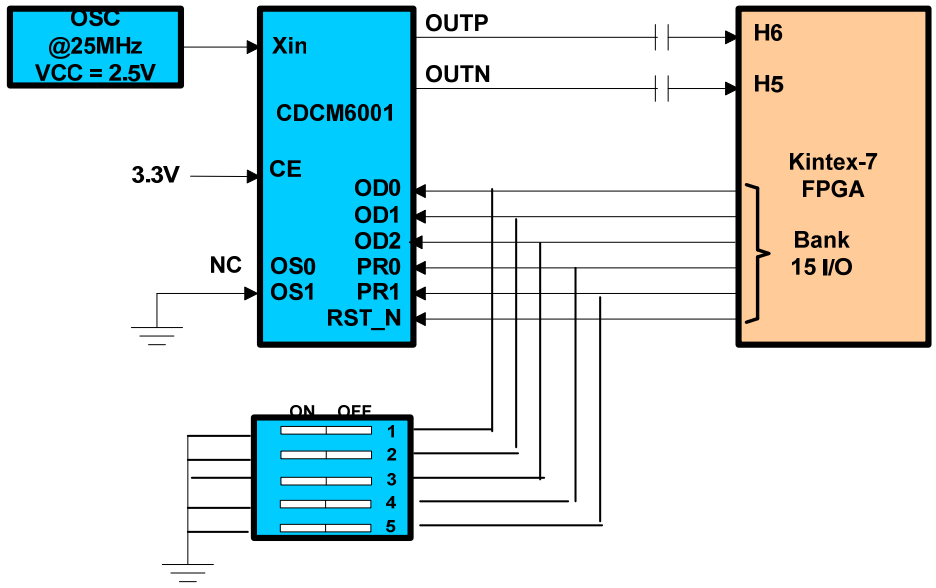


Figure 20 – Kintex-7 Mini Module Plus GTX Programmable LVDS Clock Source.

Note: The 25 MHz OSC on the MMP is used by the Marvel 88E1119R as well as the TI CDCM6001 device.

The following table shows the CDCM6001 GTX Programmable LVDS Clock Source for the Kintex-7 Mini Module Plus. The XC7K160T / XC7K325T / XC7K410T -FFG676 bank 14 is used to implement the CDCM6001 control interface.

CDCM6001 Signal	U10 FPGA Pin	U8 Clock Pin	Other Pins
XIN		21	U4.3
OUTN	H5	5	
OUTP	H6	6	
PR0	G24	25	SW4.1
PR1	F23	26	SW4.2
OD0	D23	13	SW3.1
OD1	D24	14	SW3.2
OD2	G22	15	SW3.3
RST_n	F24	12	

Table 18 – GTX Clock Pin Assignments for the Kintex-7 Mini Module Plus

The following table shows the CDCM6001 GTX Programmable LVDS Clock Source Settings for the Kintex-7 Mini Module Plus. The XC7K160T / XC7K325T / XC7K410T -FFG676 bank 14 is used to implement the CDCM6001 control interface.

CDCM61001	Common	Settings	Table								
INPUT	PRESCAL	FEEDBK	PR1	PR0	VCO	OUTPUT	OD2	OD1	OD0	OUTPUT	APPLICATION
(MHz)	DIVIDER	DIVIDER			(MHz)	DIVIDER				(MHz)	

25	4	20	1	1	2000	8	1	1	1	62.5	GigE
24.75	3	24	0	0	1782	8	1	1	1	74.25	HDTV
25	3	24	0	0	1800	8	1	1	1	75	SATA
24.8832	3	25	0	0	1866.24	8	1	1	1	77.76	SONET
25	3	24	0	0	1800	6	1	0	1	100	PCI Express
26.5625	3	24	0	0	1912.5	6	1	0	1	106.25	Fibre Channel
25	4	20	1	1	2000	4	0	1	1	125	GigE
25	3	24	0	0	1800	4	0	1	1	150	SATA
24.8832	3	25	1	0	1866.24	4	0	1	1	155.52	SONET
25	3	25	1	0	1875	4	0	1	1	156.25	10 GigE
26.5625	3	24	0	0	1912.5	4	0	1	1	159.375	10-G Fibre Channel
25	5	15	0	1	1875	2	0	0	1	187.5	12 GigE
25	3	24	0	0	1800	3	0	1	0	200	PCI Express
26.5625	3	24	0	0	1912.5	3	0	1	0	212.5	4-G Fibre Channel
25	4	20	1	1	2000	2	0	0	1	250	GigE
24.8832	3	25	1	0	1866.24	2	0	0	1	311.04	SONET
25	3	25	1	0	1875	2	0	0	1	312.5	XGMII
24.8832	3	25	1	0	1866.24	1	0	0	0	622.08	SONET
25	3	25	1	0	1875	1	0	0	0	625	10 GigE

Table 19 – GTX Clock Settings for the Kintex-7 Mini Module Plus

2.1.9 Kintex-7 GTX Power Sources

The following figure shows the power supply inputs to the Kintex-7 FPGA GTX ports. All supply inputs to the GTX are filtered using inductors and capacitors on the MMP.

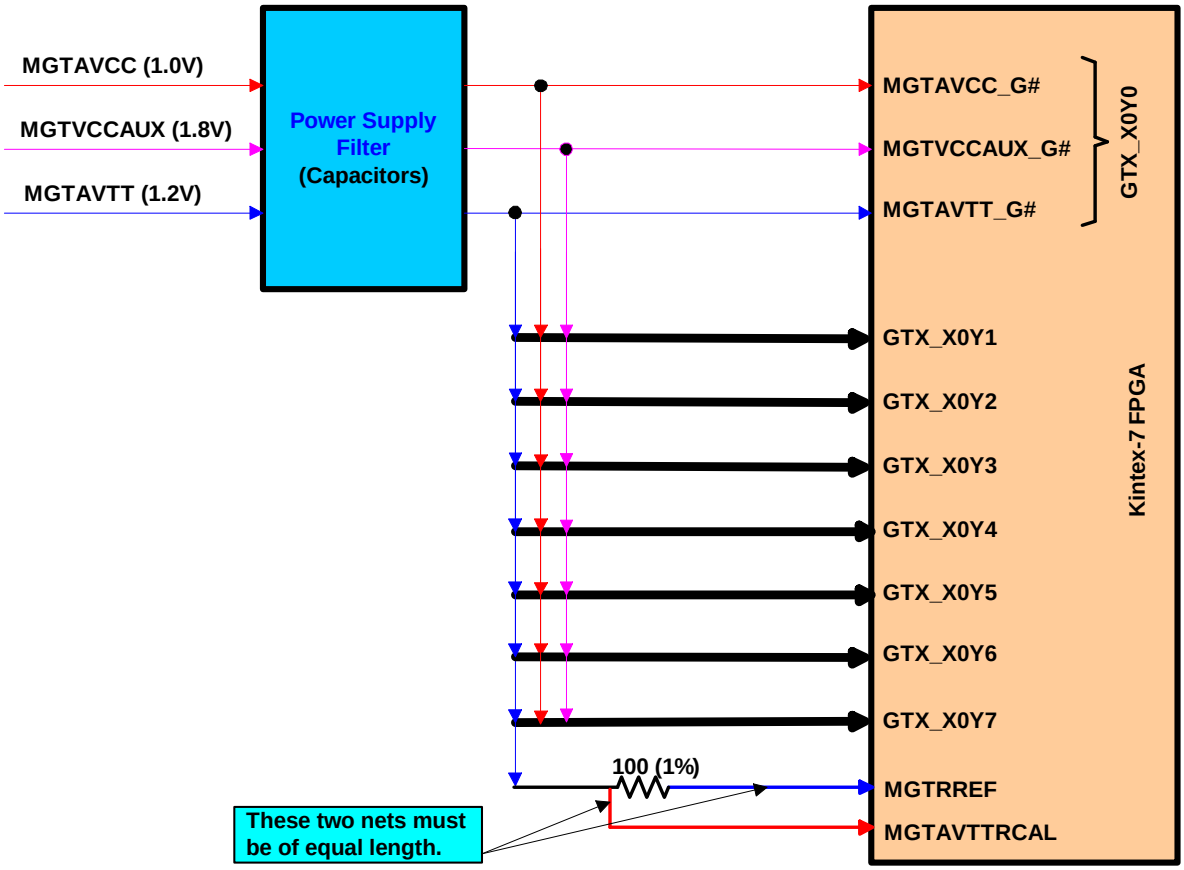


Figure 21 – GTX Power Connections for the Kintex-7 Mini Module Plus.

Note: The MGTVCCAUX rail is sourced from the MMP JX1/JX2 VCCAUX (1.8V) pins.

The following table shows the power supply inputs to the GTX ports for the Kintex-7 Mini Module Plus.

MGT Source	MGT Source Voltage	U10 FPGA Pin
MGTAVCC	1.0V	C6
MGTAVCC	1.0V	E6
MGTAVCC	1.0V	G6
MGTAVCC	1.0V	J6
MGTAVCC	1.0V	L6
MGTAVTT	1.2V	H3
MGTAVTT	1.2V	L2
MGTAVTT	1.2V	M3
MGTAVTT	1.2V	B3
MGTAVTT	1.2V	C2
MGTAVTT	1.2V	D3
MGTAVTT	1.2V	G2
MGTVCCAUX	1.8V	N6

MGTRREF		M6
MGTAVTTRCAL		M5

Table 20 – Power connections for the Kintex-7 Mini Module Plus

2.1.10 XADC Support

The Kintex-7 MMP supports XADC functionality as shown in the following figure.

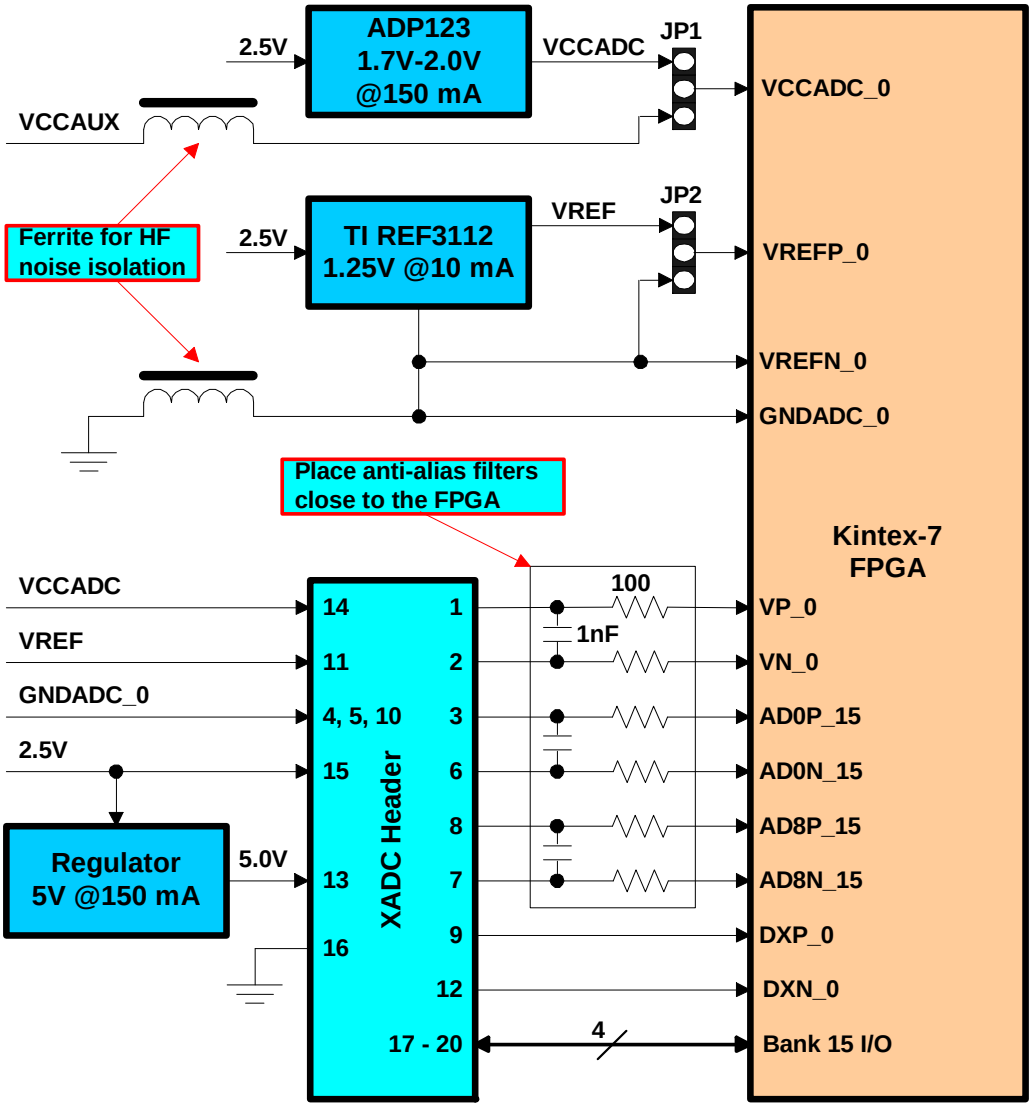


Figure 22 – XADC Support Circuitry for the Kintex-7 Mini Module Plus.

Note 1: The JP1 jumper selects between a fixed VCCADC_0 of 1.8V (VCCAUX) or a variable VCCADC_0 of 1.7V to 2.0V using the Analog Devices ADP123 regulator.

Note 2: The JP2 jumper can be used to set the VREFP for external (output of the REF3112) or internal operation.

Note 3: The XADC header is a 20 pin (2 x 10), 2.54mm male jumper header/connector.

The following table shows the ADC inputs, discrete outputs, and power sources, for the Kintex-7 Mini Module Plus XADC.

Analog Signal	U10 FPGA Pin	U10 FPGA Bank	P4 XADC Pin	Other Pins
VAUXP0	C16	Bank 15	P4.3	
VAUXN0	B16	Bank 15	P4.6	
VAUXP8	A18	Bank 15	P4.8	
VAUXN8	A19	Bank 15	P4.7	
VP_IN	N12	Bank 0	P4.2	
VN_IN	P11	Bank 0	P4.1	
AGND	M11, N11	Bank 0	P4.4, P4.5, P4.10	
DX_P	R12	Bank 0	P4.9	
DX_N	R11	Bank 0	P4.12	
VCCADC	M12	Bank 0	P4.14	
VREF_SEL	P12	Bank 0		P2.2
VREF_1V25			P4.11	U16.2, P2.1
DIO_0	D25	Bank 14	P4.17	
DIO_1	G25	Bank 14	P4.19	
DIO_2	J21	Bank 14	P4.18	
DIO_3	L23	Bank 14	P4.20	
AV_5V			P4.13	U15.2
VCC_2V5			P4.15	
DGND			P4.16	

Table 21 – XADC connections for the Kintex-7 Mini Module Plus

2.1.11 Kintex-7 FPGA JTAG Interface

The following figure shows the Kintex-7 FPGA JTAG connections to the MMP JX1/JX2 connectors. All configuration connections are through Bank 0.

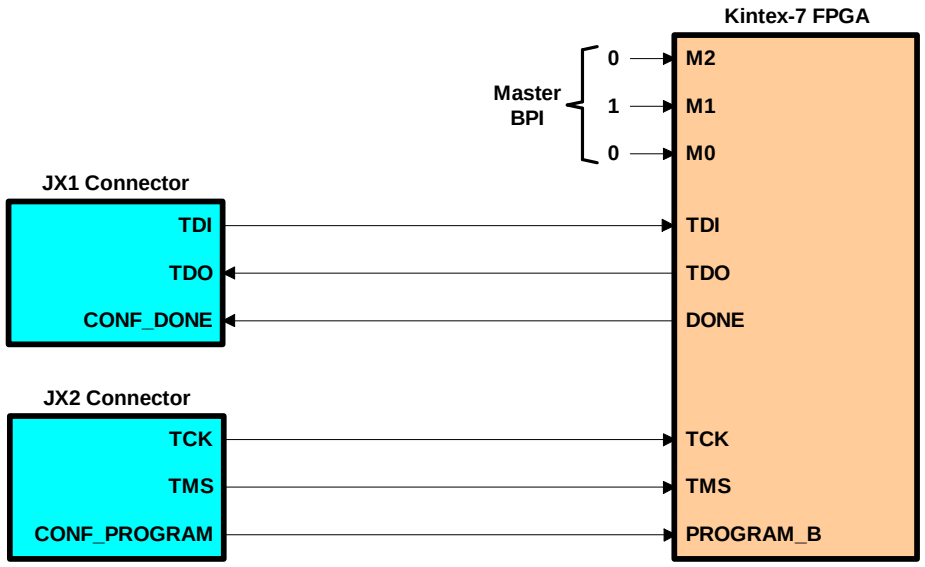


Figure 23 – JTAG Interface for the Kintex-7 Mini Module Plus.

The following table shows the JTAG inputs and outputs for the Kintex-7 Mini Module Plus.

JTAG Signal	U10 FPGA Pin	JX1 Pin	JX2 Pin
TDI	R6	JX1.1	
TDO	R7	JX1.2	
DONE	J7	JX1.38	
TCK	L8		JX2.1
TMS	N8		JX2.2
PROGRAM_B	P6		JX2.38
M0	T5		
M1	T2		
M2	P5		

Table 22 – JTAG connections for the Kintex-7 Mini Module Plus

2.1.12 Clock Connections to the Kintex-7 FPGA

The following figure shows clock connections to the Kintex-7 FPGA.

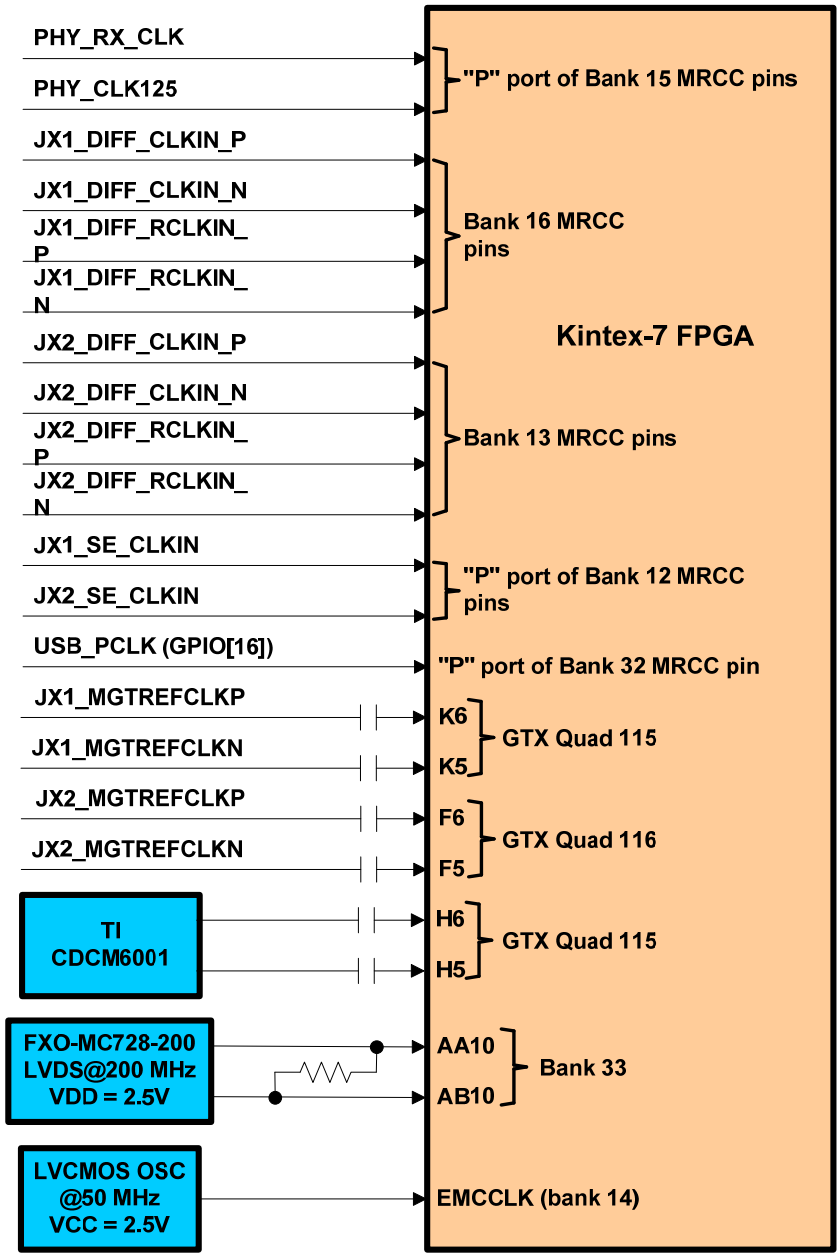


Figure 24 – MMP Clock Connections for the Kintex-7 Mini Module Plus.

The following table shows the Clock connections for the Kintex-7 Mini Module Plus.

FPGA Signal	U10 FPGA Pin	FPGA Bank / Type	Source Pin	Source / BB2 Description
RX_CLK	F17	Bank 15 MRCC P	U3.57	Ethernet PHY
CLK125	E18	Bank 15 MRCC P	U3.9	Ethernet PHY
JX1_DIFF_CLKIN_P	C12	Bank 16 MRCC	JX1.118	FMC1-CLK0-M2C_P
JX1_DIFF_CLKIN_N	C11	Bank 16 MRCC	JX1.120	FMC1-CLK0-M2C_N
JX1_DIFF_RCLKIN_P	E10	Bank 16 MRCC	JX1.117	FMC1-LA00-CC_P
JX1_DIFF_RCLKIN_N	D10	Bank 16 MRCC	JX1.119	FMC1-LA00-CC_N
JX2_DIFF_CLKIN_P	R21	Bank 13 MRCC	JX2.118	FMC1-CLK1-M2C_P

JX2_DIFF_CLKIN_N	P21	Bank 13 MRCC	JX2.120	FMC1-CLK1-M2C_N
JX2_DIFF_RCLKIN_P	N21	Bank 13 MRCC	JX2.117	FMC1-LA17-CC_P
JX2_DIFF_RCLKIN_N	N22	Bank 13 MRCC	JX2.119	FMC1-LA17-CC_N
JX1_SE_CLK	Y22	Bank 12 MRCC P	JX1.39	CDCE_Y1_OUT
JX2_SE_CLK	Y23	Bank 12 MRCC P	JX2.39	CDCE_Y2_OUT
USB_PCLK (GPIO_16)	AB16	Bank 32 MRCC P	U1.J6	USB3 FIFO Clock
JX1_MGTREFCLK_P	K6	GTX Quad 115 CLK1	JX1.67	FMC, SFP, DP, SMA
JX1_MGTREFCLK_N	K5	GTX Quad 115 CLK1	JX1.69	FMC, SFP, DP, SMA
JX2_MGTREFCLK_P	F6	GTX Quad 116 CLK1	JX2.67	PCIe
JX2_MGTREFCLK_N	F5	GTX Quad 116 CLK1	JX2.69	PCIe
CDCM_MGTREFCLK_P	H6	GTX Quad 115 CLK0	U8.6	CDCM6001
CDCM_MGTREFCLK_N	H5	GTX Quad 115 CLK0	U8.5	CDCM6001
SYSCLK_P	AA10	Bank 33 SRCC	X2.4	FXO-MC728-200 LVDS
SYSCLK_N	AB10	Bank 33 SRCC	X2.5	FXO-MC728-200 LVDS
EMCCLK	B26	Bank 14 EMCCLK	U8.3	KC2520B50

Table 23 – Clock connections for the Kintex-7 Mini Module Plus

2.1.13 Thermal Management and Power Connections to the Kintex-7 FPGA

An active heat sink is used to dissipate heat from the Kintex-7 FPGA. A Cool Innovations heat sink (PN: 3-121204UBFA) and an NMB 12V fan (PN: 1204KL-04W-B50-B00) are assembled together and shipped with the Kintex-7 Mini-Module Plus. The active heat sink is powered by connecting the three position connector (TE PN: 173977-3) to the mating connector on the Mini-Module Plus Baseboard 2.

For aggressive applications that utilize large amounts of FPGA resources it is recommended that an accurate worst-case power analysis be performed to avoid the pitfalls of overdesigning or under designing your product's power or cooling system, using the **Xilinx Power Estimator (XPE).**

The following figure shows the power connections to the Kintex-7 Mini Module Plus. Power is supplied to the Module from JX1 and JX2. Note that all power inputs are filtered using inductors and capacitors. Additionally, supplies to different function types are filtered / isolated from each other using a branching inductor scheme. This also gives a coarse means to measure circuit currents, or even isolate circuits by section. A "Point of Load" power scheme is employed with sense feedback from the most sensitive parts of the module provided to the Power Module via JX3.

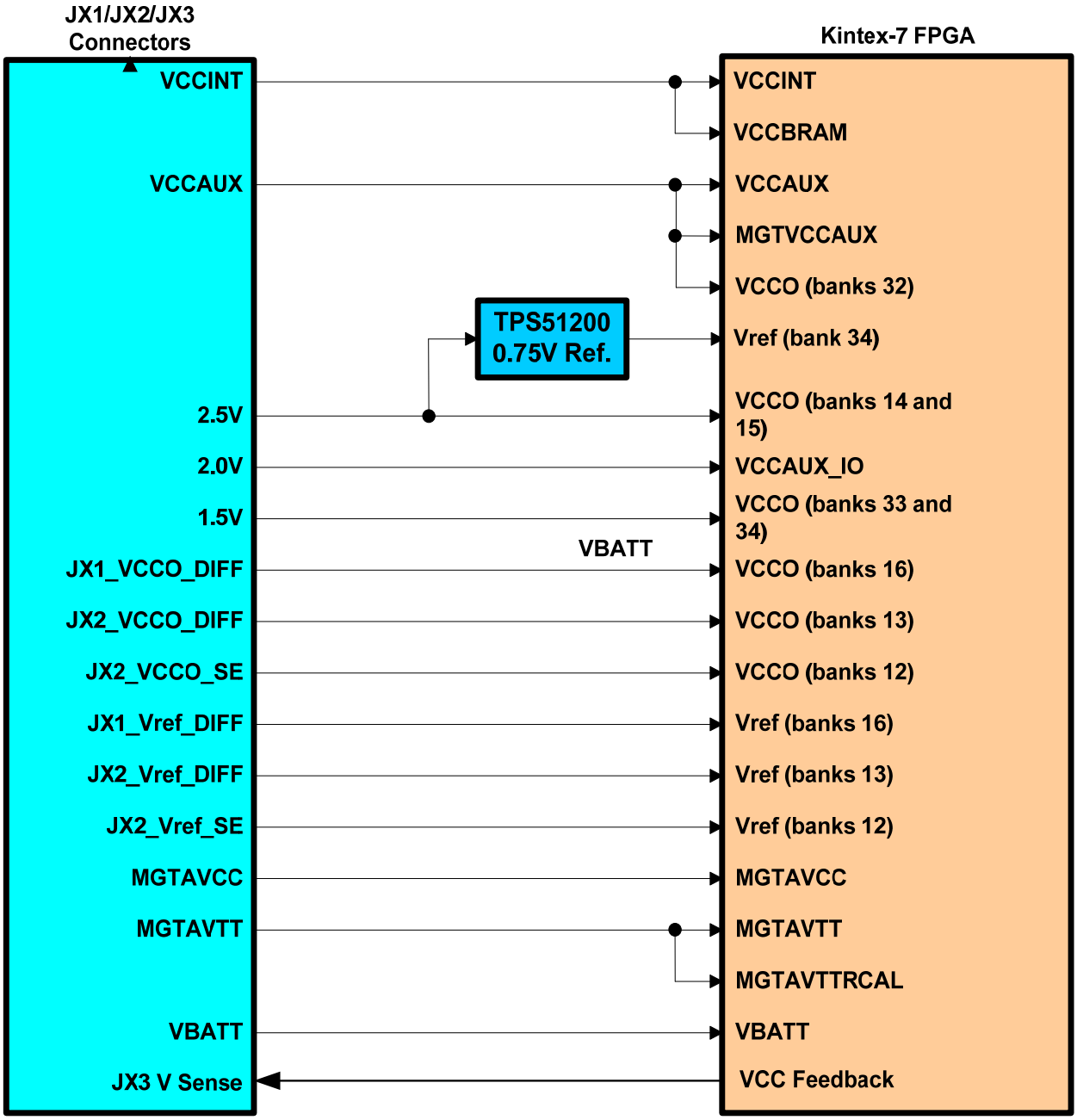


Figure 25 – MMP Power Connections for the Kintex-7 Mini Module Plus.

The following table shows the FPGA Power connections for the Kintex-7 Mini Module Plus.

FPGA Sink	FPGA Sink Voltage	U10 FPGA Pin	FPGA Function	JX1 Name	JX1 Pin	JX2 Name	JX2 Pin	JX3 Name	JX3 Pin
VCCINT	1V	L9	Internal	JX1_VCCINT	JX1.97	JX2_VCCINT	JX2.97	VINT_1V0	JX3.6
VCCINT	1V	L13		JX1_VCCINT	JX1.98	JX2_VCCINT	JX2.98		
VCCINT	1V	L15		JX1_VCCINT	JX1.103	JX2_VCCINT	JX2.103		
VCCINT	1V	M8							

VCCINT	1V	M14							
VCCINT	1V	N9							
VCCINT	1V	N15							
VCCINT	1V	P14							
VCCINT	1V	R15							
VCCINT	1V	T14							
VCCINT	1V	U15							
VCCINT	1V	J9							
VCCINT	1V	K8							
VCCINT	1V	K10							
VCCINT	1V	K12							
VCCINT	1V	K14							
VCCBRAM	1V	N13	BRAM						
VCCBRAM	1V	R13							
VCCBRAM	1V	T12							
VCCBRAM	1V	U13							
VCCAUX	1.8V	T10	AUXIO	JX1_VCCAUX	JX1.79	JX2_VCCAUX	JX2.79		
VCCAUX	1.8V	U11		JX1_VCCAUX	JX1.80	JX2_VCCAUX	JX2.80		
VCCAUX	1.8V	L11		JX1_VCCAUX	JX1.85	JX2_VCCAUX	JX2.85		
VCCAUX	1.8V	M10							
VCCAUX	1.8V	P10							
MGTVCCAUX	1.8V	N6						MGT_1V8	JX3.4
VCCO_32	1.8V	AB18	USB3						
VCCO_32	1.8V	AC15							
VCCO_32	1.8V	AE19							
VCCO_32	1.8V	AF16							
VCCO_32	1.8V	W17							
VCCO_32	1.8V	Y14							
VCCAUX_IO_G0	2V	T8	HSAUXIO	JX1_VBAT	JX1.116			VAUX_2V0	JX3.5
VCCAUX_IO_G0	2V	R9							
VCCAUX_IO_G0	2V	P8							
VBATT	2V	E8	VBATT						
VCCO_34	1.5V	AA1	DDR3	JX1_1V5	JX1.91	JX2_1V5	JX2.91	DDR_1V5	JX3.8
VCCO_34	1.5V	AC5			JX1.92		JX2.92		
VCCO_34	1.5V	AD2							
VCCO_34	1.5V	AF6							
VCCO_34	1.5V	U3							
VCCO_34	1.5V	Y4							
VREF_34	0.75V	W4	VTTREF U11.6						
VREF_34	0.75V	AD3	VTTREF U11.6						
VCCO_33	1.5V	AA11	DDR3						
VCCO_33	1.5V	AB8							

VCCO_33	1.5V	AD12							
VCCO_33	1.5V	AE9							
VCCO_33	1.5V	V10							
VCCO_33	1.5V	W7							
VCCO_16	2.5V/3.3V	A11	2V5/FMC_Vadj	JX1_VCCIO_DIFF	JX1.109				
VCCO_16	2.5V/3.3V	B8			JX1.110				
VCCO_16	2.5V/3.3V	C15							
VCCO_16	2.5V/3.3V	D12							
VCCO_16	2.5V/3.3V	E9							
VCCO_16	2.5V/3.3V	G13							
VCCO_16	2.5V/3.3V	H10							
VREF_16	NC-BB2	H11	REF	JX1_VREF_DIFF					
VREF_16	NC-BB2	C13							
VCCO_15	2.5V	B18	Enet, Flash	JX1_2V5	JX1.86	JX2_2V5	JX2.86	ENET_2V5	JX3.1
VCCO_15	2.5V	E19			JX1.104		JX2.104		
VCCO_15	2.5V	F16							
VCCO_15	2.5V	H20							
VCCO_15	2.5V	J17							
VCCO_15	2.5V	M18							
VCCO_14	2.5V	A21	Enet, Flash						
VCCO_14	2.5V	C25							
VCCO_14	2.5V	D22							
VCCO_14	2.5V	F26							
VCCO_14	2.5V	G23							
VCCO_14	2.5V	L21							
VCCO_0	2.5V	T6	Config						
VCCO_0	2.5V	L7							
VCCO_13	2.5V/3.3V	K24	2V5/FMC_Vadj			JX2_VCCIO_DIFF	JX2.109		
VCCO_13	2.5V/3.3V	N25					JX2.110		
VCCO_13	2.5V/3.3V	P22							
VCCO_13	2.5V/3.3V	R19							
VCCO_13	2.5V/3.3V	T16							
VCCO_13	2.5V/3.3V	T26							
VREF_13	NC-BB2	P25	REF			JX2_VREF_DIFF	JX2.115		
VREF_13	NC-BB2	T19							
VCCO_12	2.5V/3.3V	AA21	2V5/FMC_Vadj			JX2_VCCIO_SE	JX2.21		
VCCO_12	2.5V/3.3V	AC25					JX2.22		
VCCO_12	2.5V/3.3V	AD22							
VCCO_12	2.5V/3.3V	AF26							
VCCO_12	2.5V/3.3V	U23							
VCCO_12	2.5V/3.3V	V20							
VCCO_12	2.5V/3.3V	Y24							

VREF_12	NC-BB2	W21	REF			JX2_VREF_SE	JX2.40		
VREF_12	NC-BB2	AE21							
MGTAVCC	1.0V	C6	MGTAVCC	JX1_MGTAVCC	JX1.71	JX2_MGTAVCC	JX2.71	MGT_1V0	JX3.3
MGTAVCC	1.0V	E6			JX1.72		JX2.72		
MGTAVCC	1.0V	G6			JX1.73		JX2.73		
MGTAVCC	1.0V	J6			JX1.74		JX2.74		
MGTAVCC	1.0V	L6							
MGTAVTT	1.2V	H3	MGTAVTT	JX1_MGTAVTT	JX1.67	JX2_MGTAVTT	JX2.67	MGT_1V2	JX3.8
MGTAVTT	1.2V	L2			JX1.68		JX2.68		
MGTAVTT	1.2V	M3			JX1.69		JX2.69		
MGTAVTT	1.2V	B3			JX1.70		JX2.70		
MGTAVTT	1.2V	C2							
MGTAVTT	1.2V	D3							
MGTAVTT	1.2V	G2							
MGTRREF	1.2V	M6							
MGTAVTTRCAL	1.2V	M5							
MGT_3V3	3.3V		MGT Clock			JX2_3V3	JX2.116	MGT_3V3	JX3.2

Table 24 – FPGA Power connections for the Kintex-7 Mini Module Plus

The following figure shows convenient Voltage Measurement locations for the Kintex-7 Mini Module Plus

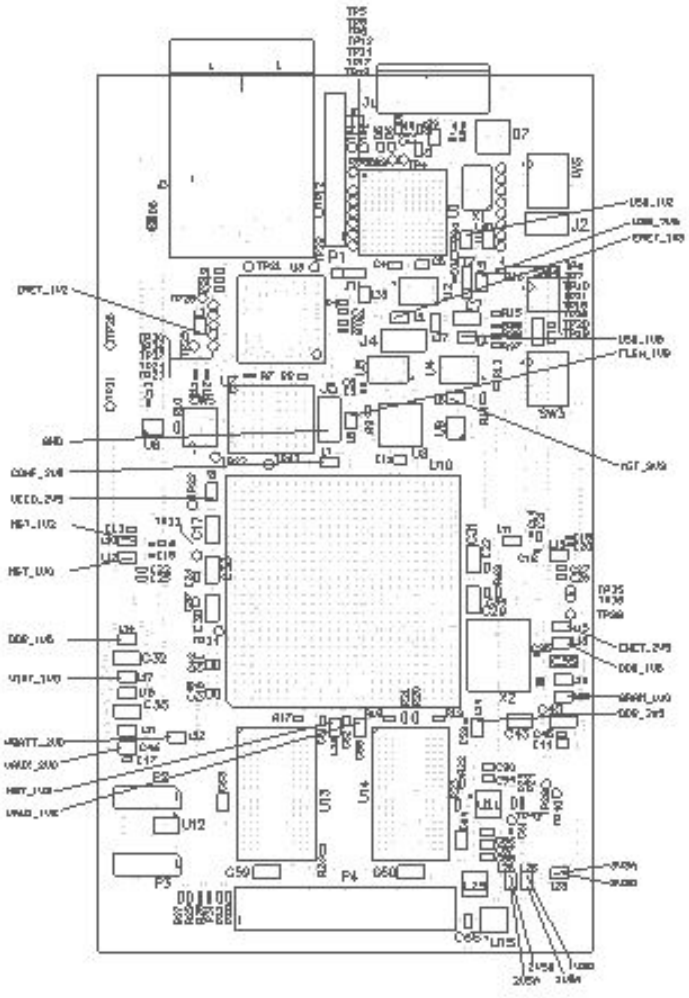


Figure 26 – Voltage Measurement locations for the Kintex-7 Mini Module Plus.

2.1.14 MMP JX1/JX2/JX3 Connectors

The following table shows the MMP JX1 and JX2 pin assignments (the JX1/JX2 connectors must be backward compatible with the existing V5FXT MMP).

BB2 Connector Signal Name	I/O Connector Signal Name	JX1 Pin #	FPGA Pin #	FPGA Pin #	JX1 Pin #	I/O Connector Signal Name	BB2 Connector Signal Name
JTAG_TDI	MMP_JTAG_TDI	1	R6	R7	2	MMP_JTAG_TDO	MMP_TDO
FMC1-LA29_P	JX1_SE_IO_0_P	3	B10	A10	4	JX1_SE_IO_0_N	FMC1-LA29_N
FMC1-LA31_P	JX1_SE_IO_2_P	5	B12	B11	6	JX1_SE_IO_2_N	FMC1-LA31_N
FMC1-LA30_P	JX1_SE_IO_4_P	7	A13	A12	8	JX1_SE_IO_4_N	FMC1-LA30_N

FMC1-LA33_P	JX1_SE_IO_6_P	9	E13	E12	10	JX1_SE_IO_6_N	FMC1-LA33_N
FMC1-LA32_P	JX1_SE_IO_8_P	11	B14	A14	12	JX1_SE_IO_8_N	FMC1-LA32_N
SDA_0_VT	JX1_SE_IO_10_P	13	A15	B15	14	JX1_SE_IO_10_N	SCL_0
FMC_TRST_L	JX1_SE_IO_12_P	15	T17	U17	16	JX1_SE_IO_12_N	FMC1-PRSNT-M2C_L_VT
SW0	JX1_SE_IO_14_P	17	R16	R17	18	JX1_SE_IO_14_N	SW1
SW2	JX1_SE_IO_16_P	19	P16	N17	20	JX1_SE_IO_16_N	SW3
FMC_VADJ	JX1_VCCIO_SE	21	NC	NC	22	JX1_VCCIO_SE	FMC_VADJ
SW4	JX1_SE_IO_18_P	23	N18	M19	24	JX1_SE_IO_18_N	SW5
SW6	JX1_SE_IO_20_P	25	U19	U20	26	JX1_SE_IO_20_N	SW7
LED0	JX1_SE_IO_22_P	27	R18	P18	28	JX1_SE_IO_22_N	LED1
LED2	JX1_SE_IO_24_P	29	U26	V26	30	JX1_SE_IO_24_N	LED3
LED4	JX1_SE_IO_26_P	31	U24	U25	32	JX1_SE_IO_26_N	DP_HPD
CDCE_SDA_VT	JX1_SE_IO_28_P	33	V23	V24	34	JX1_SE_IO_28_N	CDCE_SCL
UART_RX_VT	JX1_SE_IO_30_P	35	U22	V22	36	JX1_SE_IO_30_N	UART_TX
PCIe_PERST#_VT	JX1_SE_IO_32_P	37	Y20	J7	38	MMP_CONF_DONE	FPGA_DONE
CDCE_Y1_OUT	JX1_SE_CLK	39	Y22	NC	40	JX1_VREF_SE	NC
GND	GND	41			42	GND	GND
FMC1-DP0-M2C_p	JX1_MGTRX0_P	43	R4	P2	44	JX1_MGTTX0_P	FMC1-DP0-C2M_p
FMC1-DP0-M2C_n	JX1_MGTRX0_N	45	R3	P18	46	JX1_MGTTX0_N	FMC1-DP0-C2M_n
GND	GND	47			48	GND	GND
SFP0-RX_p	JX1_MGTRX1_P	49	N4	M2	50	JX1_MGTTX1_P	SFP0-TX_p
SFP0-RX_n	JX1_MGTRX1_N	51	N3	M1	52	JX1_MGTTX1_N	SFP0-TX_n
GND	GND	53			54	GND	GND
NC	JX1_MGTRX2_P	55	L4	K2	56	JX1_MGTTX2_P	DP_ML_L0_P
NC	JX1_MGTRX2_N	57	L3	K1	58	JX1_MGTTX2_N	DP_ML_L0_N
GND	GND	59			60	GND	GND
SMA_RX_P	JX1_MGTRX3_P	61	J4	H2	62	JX1_MGTTX3_P	SMA_TX_P
SMA_RX_N	JX1_MGTRX3_N	63	J3	H1	64	JX1_MGTTX3_N	SMA_TX_N
GND	GND	65			66	GND	GND
CLK_MUX_OUT_P	JX1_MGTREFCLK_P	67	K6		68	MGTAVTT (1.2V)	1V2
CLK_MUX_OUT_N	JX1_MGTREFCLK_N	69	K5		70	MGTAVTT (1.2V)	1V2
1V0	MGTAVCC (1.0V)	71			72	MGTAVCC (1.0V)	1V0

1V0	MGTAVCC (1.0V)	73			74	MGTAVCC (1.0V)	1V0
FMC1-LA01-CC_P	JX1_DIFF_IO_0_P	75	G12	J13	76	JX1_DIFF_IO_1_P	FMC1-LA02_P
FMC1-LA01-CC_N	JX1_DIFF_IO_0_N	77	F12	H13	78	JX1_DIFF_IO_1_N	FMC1-LA02_N
1V8	VCCAUX	79			80	VCCAUX	1V8
FMC1-LA04_P	JX1_DIFF_IO_2_P	81	E11	F14	82	JX1_DIFF_IO_3_P	FMC1-LA03_P
FMC1-LA04_N	JX1_DIFF_IO_2_N	83	D11	F13	84	JX1_DIFF_IO_3_N	FMC1-LA03_N
1V8	VCCAUX	85			86	2.5V	2V5
FMC1-LA05_P	JX1_DIFF_IO_4_P	87	F9	H14	88	JX1_DIFF_IO_5_P	FMC1-LA06_P
FMC1-LA05_N	JX1_DIFF_IO_4_N	89	F8	G14	90	JX1_DIFF_IO_5_N	FMC1-LA06_N
1V5	1.5V	91			92	1.5V	1V5
FMC1-LA07_P	JX1_DIFF_IO_6_P	93	A9	D14	94	JX1_DIFF_IO_7_P	FMC1-LA08_P
FMC1-LA07_N	JX1_DIFF_IO_6_N	95	A8	D13	96	JX1_DIFF_IO_7_N	FMC1-LA08_N
1V0	VCCINT	97			98	VCCINT	1V0
FMC1-LA11_P	JX1_DIFF_IO_8_P	99	D9	C9	100	JX1_DIFF_IO_9_P	FMC1-LA12_P
FMC1-LA11_N	JX1_DIFF_IO_8_N	101	D8	B9	102	JX1_DIFF_IO_9_N	FMC1-LA12_N
1V0	VCCINT	103			104	2.5V	2V5
FMC1-LA10_P	JX1_DIFF_IO_10_P	105	G10	H9	106	JX1_DIFF_IO_11_P	FMC1-LA09_P
FMC1-LA10_N	JX1_DIFF_IO_10_N	107	G9	H8	108	JX1_DIFF_IO_11_N	FMC1-LA09_N
2V5/FMC_Vadj	JX1_VCCIO_DIFF	109			110	JX1_VCCIO_DIFF	2V5/FMC_Vadj
FMC1-LA14_P	JX1_DIFF_IO_12_P	111	G11	J11	112	JX1_DIFF_IO_13_P	FMC1-LA13_P
FMC1-LA14_N	JX1_DIFF_IO_12_N	113	F10	J10	114	JX1_DIFF_IO_13_N	FMC1-LA13_N
NC	JX1_Vref_DIFF	115			116	VBAT	2V0
FMC1-LA00-CC_P	JX1_DIFF_RCLKIN_P	117	E10	C12	118	JX1_DIFF_CLKIN_P	FMC1-CLK0-M2C_P
FMC1-LA00-CC_N	JX1_DIFF_RCLKIN_N	119	D10	C11	120	JX1_DIFF_CLKIN_N	FMC1-CLK0-M2C_N

Table 25 – JX1 connections for the Kintex-7 Mini Module Plus

BB2 Connector Signal Name	I/O Connector Signal Name	JX2 Pin #	FPGA Pin #	FPGA Pin #	JX2 Pin #	I/O Connector Signal Name	BB2 Connector Signal Name
JTAG_TCK	MMP_JTAG_TCK	1	L8	N8	2	MMP_JTAG_TMS	JTAG_TMS
PB0	JX2_SE_IO_0_P	3	W26	W25	4	JX2_SE_IO_0_N	PB1
PB2	JX2_SE_IO_2_P	5	W23	W24	6	JX2_SE_IO_2_N	PB3
SFP0_TX_FAULT_VT	JX2_SE_IO_4_P	7	Y25	Y26	8	JX2_SE_IO_4_N	SFP0_TX_DISABLE
SFP0_MOD2_VT	JX2_SE_IO_6_P	9	AA23	AB24	10	JX2_SE_IO_6_N	SFP0_MOD1
SFP0_MOD0_VT	JX2_SE_IO_8_P	11	AA25	AB25	12	JX2_SE_IO_8_N	SFP0_RSEL

SFP0_LOS_VT	JX2_SE_IO_10_P	13	AB26	AC26	14	JX2_SE_IO_10_N	PMOD1_P1_VT
PMOD1_P2_VT	JX2_SE_IO_12_P	15	AC23	AC24	16	JX2_SE_IO_12_N	PMOD1_P3_VT
PMOD1_P4_VT	JX2_SE_IO_14_P	17	AE26	AD26	18	JX2_SE_IO_14_N	PMOD1_P7_VT
PMOD1_P8_VT	JX2_SE_IO_16_P	19	AE25	AD25	20	JX2_SE_IO_16_N	PMOD1_P9_VT
FMC_VADJ	JX2_VCCIO_SE	21			22	JX2_VCCIO_SE	FMC_VADJ
PMOD1_P10_VT	JX2_SE_IO_18_P	23	AD23	AD24	24	JX2_SE_IO_18_N	PMOD2_P1_VT
PMOD2_P2_VT	JX2_SE_IO_20_P	25	AF24	AF25	26	JX2_SE_IO_20_N	PMOD2_P3_VT
PMOD2_P4_VT	JX2_SE_IO_22_P	27	AF23	AE23	28	JX2_SE_IO_22_N	PMOD2_P7_VT
PMOD2_P8_VT	JX2_SE_IO_24_P	29	AF22	AE22	30	JX2_SE_IO_24_N	PMOD2_P9_VT
PMOD2_P10_VT	JX2_SE_IO_26_P	31	W20	Y21	32	JX2_SE_IO_26_N	SD1_D0_VT
SD1_D1_VT	JX2_SE_IO_28_P	33	AB21	AC21	34	JX2_SE_IO_28_N	SD1_D2_VT
SD1_D3_VT	JX2_SE_IO_30_P	35	AB22	AC22	36	JX2_SE_IO_30_N	SD1_CMD
SD1_CLK	JX2_SE_IO_32_P	37	U21	P6	38	MMP_CONF_PROGRAM	FPGA_PROG#
CDCE_Y2_OUT	JX2_SE_CLK	39	Y23		40	JX2_Vref_SE	NC
GND	GND	41			42	GND	GND
PCIe-RX2_P	JX2_MGTRX0_P	43	E4	D2	44	JX2_MGTTX0_P	PCIe-TX2_P
PCIe-RX2_N	JX2_MGTRX0_N	45	E3	D1	46	JX2_MGTTX0_N	PCIe-TX2_N
GND	GND	47			48	GND	GND
PCIe-RX3_P	JX2_MGTRX1_P	49	G4	F2	50	JX2_MGTTX1_P	PCIe-TX3_P
PCIe-RX3_N	JX2_MGTRX1_N	51	G3	F1	52	JX2_MGTTX1_N	PCIe-TX3_N
GND	GND	53			54	GND	GND
PCIe-RX0_P	JX2_MGTRX2_P	55	B6	A4	56	JX2_MGTTX2_P	PCIe-TX0_P
PCIe-RX0_N	JX2_MGTRX2_N	57	B5	A3	58	JX2_MGTTX2_N	PCIe-TX0_N
GND	GND	59			60	GND	GND
PCIe-RX1_P	JX2_MGTRX3_P	61	C4	B2	62	JX2_MGTTX3_P	PCIe-TX1_P
PCIe-RX1_N	JX2_MGTRX3_N	63	C3	B1	64	JX2_MGTTX3_N	PCIe-TX1_N
GND	GND	65			66	GND	GND
LJ-PCIe-REFCLK0_P	JX2_MGTREFCLK_P	67	F6		68	MGTAVTT (1.2V)	1V2
LJ-PCIe-REFCLK0_N	JX2_MGTREFCLK_N	69	F5		70	MGTAVTT (1.2V)	1V2
1V0	MGTAVCC (1.0V)	71			72	MGTAVCC (1.0V)	1V0
1V0	MGTAVCC (1.0V)	73			74	MGTAVCC (1.0V)	1V0
FMC1-LA15_P	JX2_DIFF_IO_0_P	75	R26	M25	76	JX2_DIFF_IO_1_P	FMC1-LA16_P

FMC1-LA15_N	JX2_DIFF_IO_0_N	77	P26	L25	78	JX2_DIFF_IO_1_N	FMC1-LA16_N
1V8	VCCAUX	79			80	VCCAUX	1V8
FMC1-LA18-CC_P	JX2_DIFF_IO_2_P	81	P23	P24	82	JX2_DIFF_IO_3_P	FMC1-LA20_P
FMC1-LA18-CC_N	JX2_DIFF_IO_2_N	83	N23	N24	84	JX2_DIFF_IO_3_N	FMC1-LA20_N
1V8	VCCAUX	85			86	2.5V	2V5
FMC1-LA23_P	JX2_DIFF_IO_4_P	87	K25	M24	88	JX2_DIFF_IO_5_P	FMC1-LA19_P
FMC1-LA23_N	JX2_DIFF_IO_4_N	89	K26	L24	90	JX2_DIFF_IO_5_N	FMC1-LA19_N
1V5	1.5V	91			92	1.5V	1V5
FMC1-LA21_P	JX2_DIFF_IO_6_P	93	N26	M21	94	JX2_DIFF_IO_7_P	FMC1-LA22_P
FMC1-LA21_N	JX2_DIFF_IO_6_N	95	M26	M22	96	JX2_DIFF_IO_7_N	FMC1-LA22_N
1V0	VCCINT	97			98	VCCINT	1V0
FMC1-LA24_P	JX2_DIFF_IO_8_P	99	T24	T20	100	JX2_DIFF_IO_9_P	FMC1-LA25_P
FMC1-LA24_N	JX2_DIFF_IO_8_N	101	T25	R20	102	JX2_DIFF_IO_9_N	FMC1-LA25_N
1V0	VCCINT	103			104	2.5V	2V5
FMC1-LA28_P	JX2_DIFF_IO_10_P	105	R22	P19	106	JX2_DIFF_IO_11_P	FMC1-LA27_P
FMC1-LA28_N	JX2_DIFF_IO_10_N	107	R23	P20	108	JX2_DIFF_IO_11_N	FMC1-LA27_N
2V5/FMC_Vadj	JX2_VCCIO_DIFF	109			110	JX2_VCCIO_DIFF	2V5/FMC_Vadj
FMC1-LA26_P	JX2_DIFF_IO_12_P	111	T22	N19	112	JX2_DIFF_IO_13_P	DP_AUX_CH_P
FMC1-LA26_N	JX2_DIFF_IO_12_N	113	T23	M20	114	JX2_DIFF_IO_13_N	DP_AUX_CH_N
NC	JX2_Vref_DIFF	115			116	3.3V	3V3
FMC1-LA17-CC_P	JX2_DIFF_RCLKIN_P	117	N21	R21	118	JX2_DIFF_CLKIN_P	FMC1-CLK1-M2C_P
FMC1-LA17-CC_N	JX2_DIFF_RCLKIN_N	119	N22	P21	120	JX2_DIFF_CLKIN_N	FMC1-CLK1-M2C_N

Table 26 – JX2 connections for the Kintex-7 Mini Module Plus

The following table shows the MMP JX3 connections for the Kintex-7 Mini Module Plus.

Voltage Sensed	JX3 Name	JX3 Pin
1V	VINT_1V0	JX3.6
1.8V	MGT_1V8	JX3.4
2V	VAUX_2V0	JX3.5
1.5V	DDR_1V5	JX3.8
2.5V	ENET_2V5	JX3.1
1.0V	MGT_1V0	JX3.3
1.2V	MGT_1V2	JX3.8

3.3V	MGT_3V3	JX3.2
GND	GND	JX3.9
GND	GND	JX3.10

Table 27 – JX3 connections for the Kintex-7 Mini Module Plus

2.1.15 Kintex-7 Mini Module Plus I/O Count

The following table shows the I/O count for the Kintex-7 FPGA on the Mini Module Plus. This module uses the XC7K160T, the XC7K325T, or the XC7K410T device in FFG676 package with 400 user I/O pins. The module utilizes 343 I/O pins leaving the other 57 pins for routing purposes.

- The unused pins in banks 12, 13, and 16 (JX1/JX2 signals) are not used on the MMP due to the JX1/JX2 VCCO dependencies.
- The unused pins in banks 33 and 34 (DDR3 signals) are not used for other functions due to 1.5V VCCO and also to allow easy routing of the DDR3 signals.

Device	I/O Pins	Comments
Mini Module Plus Connector	132	VADJ signal levels
MMP Connector Vref	6	VADJ signal levels
DDR3 SDRAM	77	1.5V signal levels (DDR3 + DCI + Vref)
Parallel Flash	47	2.5V signal levels
10/100/1000 PHY	16	2.5V signal levels
I2C EEPROM	2	2.5V signal levels
USB 3.0 MAC/PHY	46	1.8V signal levels
XADC Interface	8	2.5V signal levels
Clocks	2	1.5V signal levels (200 MHz LVDS OSC)
TI CDCM6001	6	2.5V signal levels
Configuration Clock (EMCCLK)	1	2.5V signal levels

Table 28 – I/O Count for the Kintex-7 Mini Module Plus

2.2 Avnet Mini-Module Plus Baseboard 2 Functional Description (From Mini Module Plus Baseboard 2 Users Guide)

A high-level block diagram of the Avnet Mini-Module Plus Baseboard 2 is shown below followed by a brief description of each sub-section.

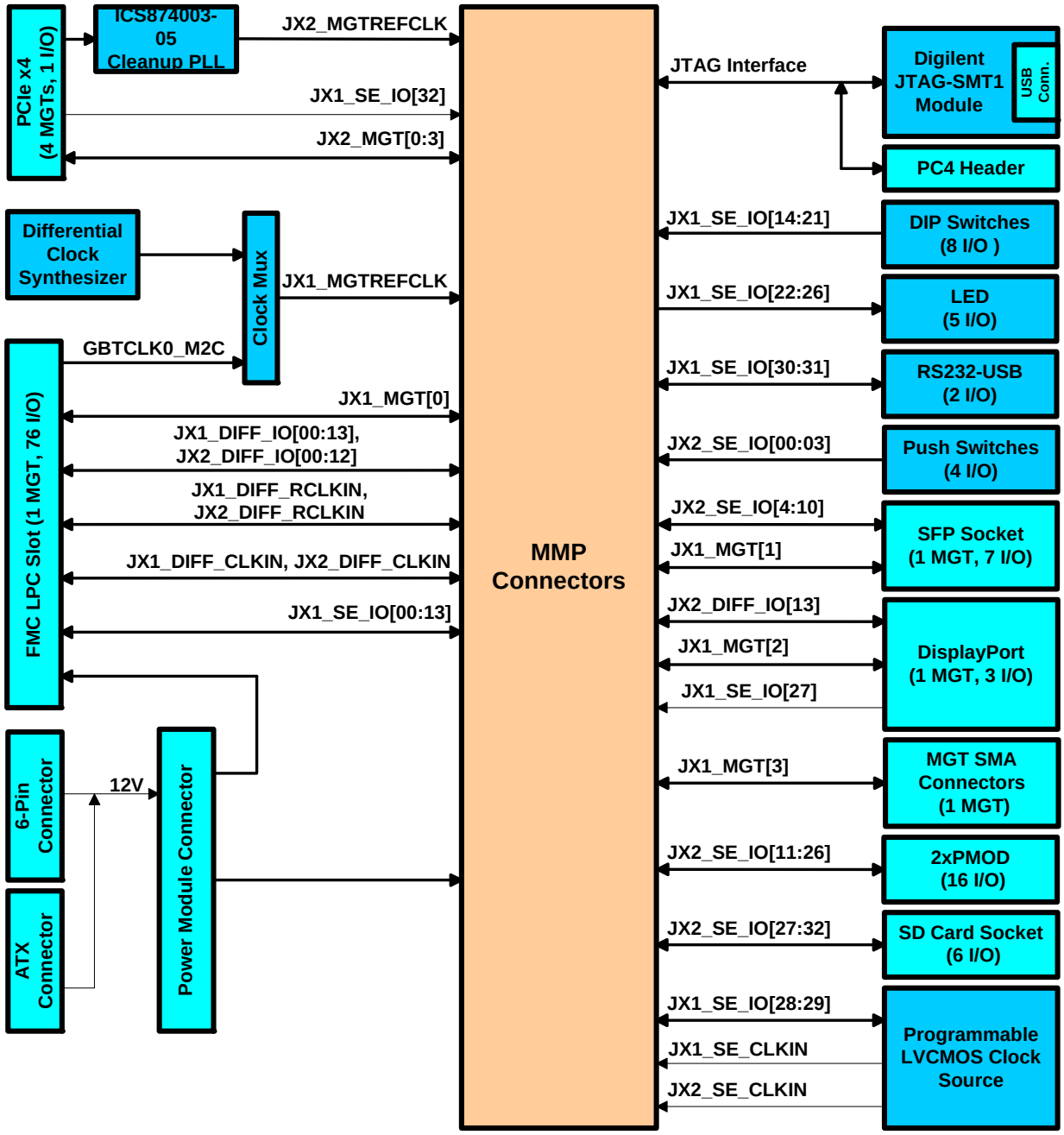


Figure 26 – Avnet Mini-Module Plus Baseboard 2 Block Diagram.

2.2.1 GTX (Gigabit Transceiver) Interfaces

The Mini-Module Plus Baseboard 2 supports a variety of Gigabit transceiver interfaces. GTX Transceivers are full-duplex serial transceivers for point-to-point transmission applications. The number of transceivers available is dependent on the model of Mini-Module that is installed on the baseboard. Refer to the Mini-Module's User Guide to get details on the number of transceivers available and performance details for a specific model of Mini-Module. The table below lists a sub-set of communication protocols supported by the Virtex-5 and Kintex-7 Mini-Modules.

Standards	I/O Bit Rate (Gb/s)
PCI Express	2.5
PCI Express 2.0	5.0
SFI-5	2.488 – 3.125
OC-12	0.622
OC-48	2.488
Fibre Channel	1.06
	2.12
Gigabit Ethernet	1.25
10-Gbit Fibre Channel	3.1875
Infiniband	2.5
HD-SDI	1.485
	1.4835
	3.0
Serial Rapid I/O	1.25
	2.5
	3.125
Aurora (Xilinx protocol)	0.100 – 3.75

Table 29 - Communications Standards

The Mini-Module Plus Baseboard 2 implements the following GTX interfaces:

GTX Interface	Lanes
SMA	x1
SFP	x1
FMC	x1
PCI Express	x4
DisplayPort	x1 (TX only)

Table 30 - GTX Interfaces Supported

2.2.1.1 2.1.1 GTX Reference Clock Inputs

GTX interfaces require a reference clock to operate. The Mini-Module Plus Baseboard 2 offers three sources for the GTX reference clocks.

A single programmable LVDS synthesizer (CDCM61001) is used to provide a variable clock source to the dedicated GTX clock inputs. The CDCM61001 is programmed by setting dip switches SW1 and SW2 on the board. The CDCM 61001 uses a 27MHz reference clock. The synthesizer provides reference clock frequencies that support the full range of line rates. The programmable LVDS clock source is routed through a 2:1 MUX, and is shared by the FMC slot's gigabit clock. The diagram below shows the architecture of these two GTX clock sources.

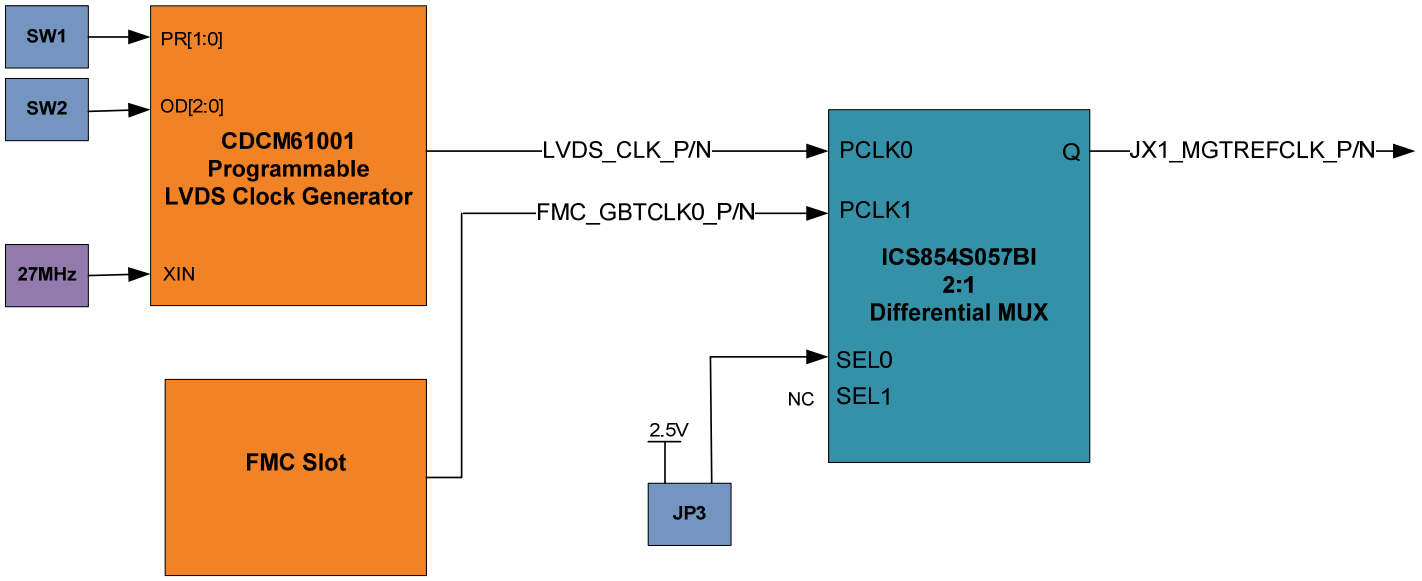


Figure 28 - GTX Reference Clock Sources

Placing a jumper shunt on JP3 will enable the MUX to pass the FMC_GBTCLK0 pair to the JX1_MGTREFCLK pins on the Mini-Module Plus mating connectors. The default configuration from the factory is no jumper placed, passing the clock generator's signal pair through to the connector JX1.

The table below shows the electrical connections of the JX1_MGTREFCLK pair to the Mini-Module Plus mating connector JX1.

Signal Name	Mini-Module Plus mating Connector (JX1)
JX1_MGTREFCLK_P	JX1.67
JX1_MGTREFCLK_N	JX1.69

Table 31 – JX1 GTX Reference Clock Pin Assignments

PCI Express applications use the 100 MHz reference clock provided over the card edge. The following figure shows the PCI Express reference clock architecture.

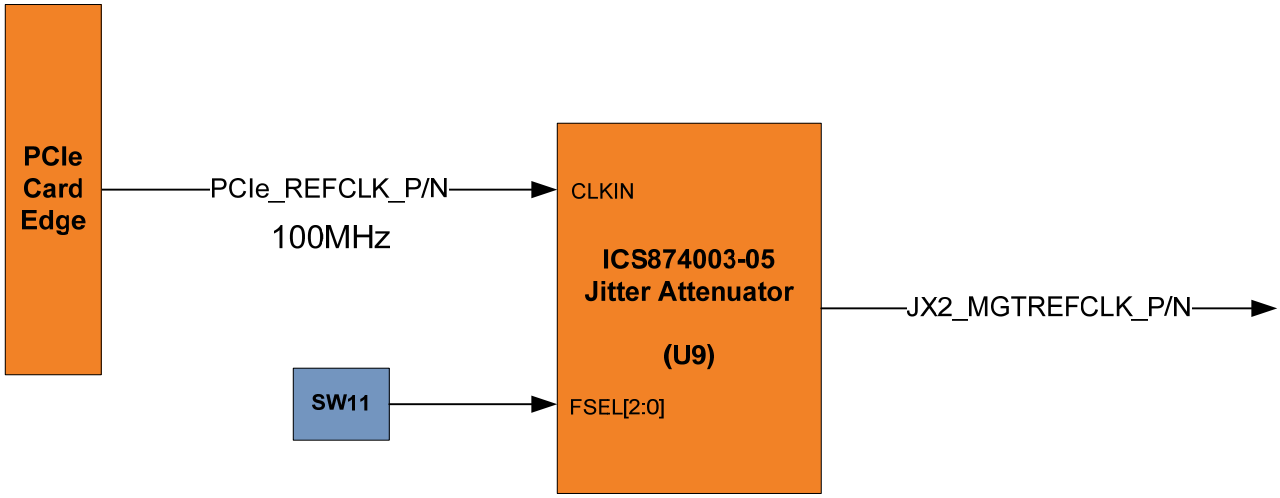


Figure 39 - PCI Express Reference Clock

The ICS874003 device can provide a 250MHz, 125MHz, or a 100MHz output by configuring the dip switch SW11.

The table below shows the appropriate dip switch settings for the valid output frequencies.

SW11[3:0]	Output Frequency
x000	250MHz
x010	125MHz
x101	100MHz

Table 32 – PCI Express Reference Clock Frequencies

The table below shows the electrical connections of the JX2_MGTREFCLK pair to the Mini-Module Plus mating connector JX2.

Signal Name	Mini-Module Plus mating Connector JX2)
JX2_MGTREFCLK_P	JX2.67
JX2_MGTREFCLK_N	JX2.69

Table 33 – PCI Express reference Clock Pin Assignments

2.2.1.2 PCI Express x4 Add-in Card

The PCI Express electrical interface on the Mini-Module Plus Baseboard 2 development board consists of 4 lanes, each lane having a unidirectional transmit and receive differential pair. Each lane supports both first generation data rate of 2.5 Gbps and PCI Express 2.0 data rate of 5.0Gbps. In addition to the 4 serial lanes there is a 100MHz reference clock that is provided from the system slot. In order to work in open systems, add-in cards must use the reference clock provided over the PCI Express card edge to be frequency locked with the host system.

To add clocking integrity and flexibility in the end user design the Mini-Module Plus Baseboard 2 development board utilizes the on board ICS874003-05 jitter attenuator. This device provides a stable, low jitter reference clock that is programmable. See the figure below for an illustration of how the PCI Express reference clock is connected to the target FPGA.

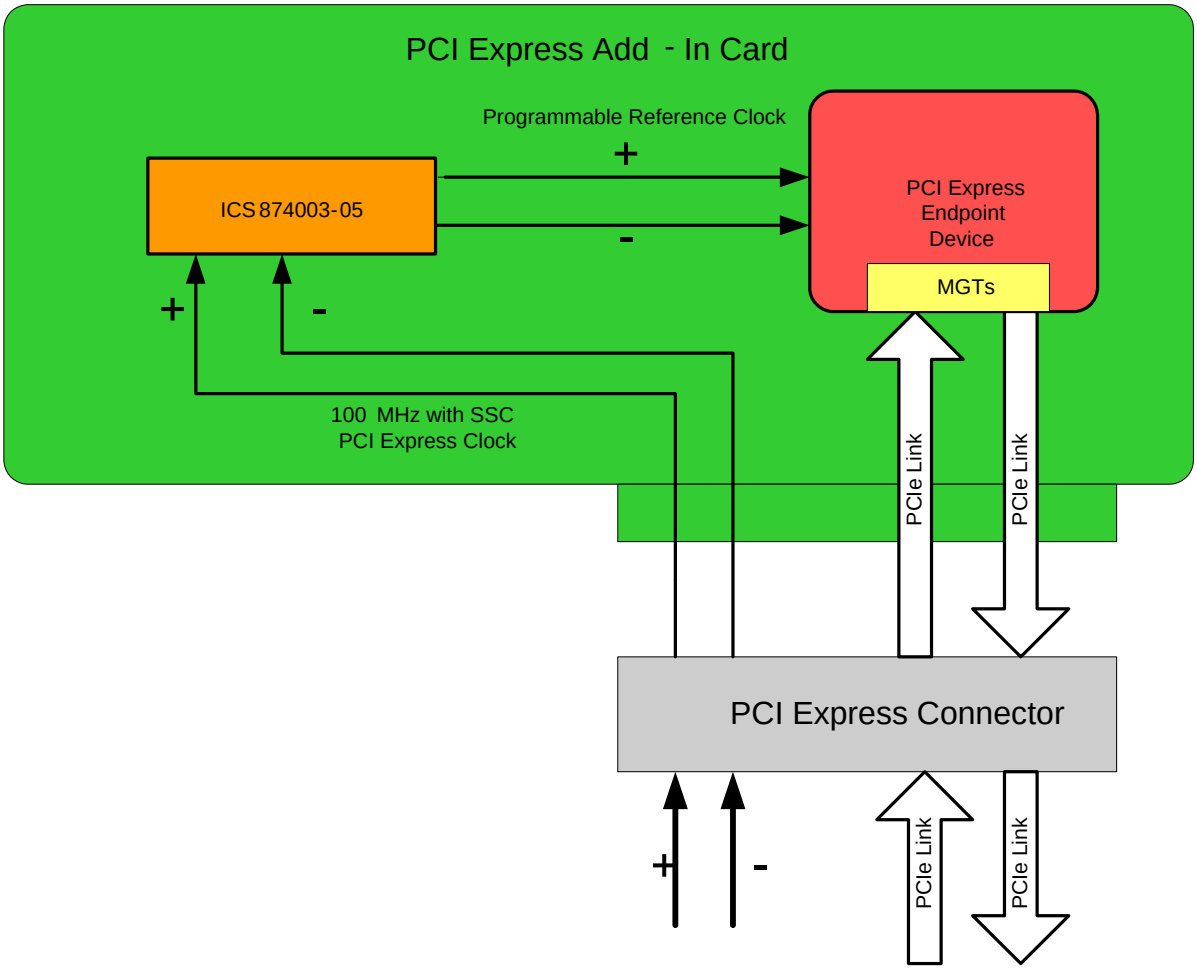


Figure 30 - PCI Express Electrical Interface

See **Section 2.1.1** for details about PCI Express programmable reference clock.

There is also a side band signal from the PCI Express card edge that connects to a regular I/O pin on the target endpoint device. The “PERST#” signal is an active low reset signal provided by the host PCI Express slot.

The lane width of the PCI Express interface is determined by the PRSNT1# and PRSNT2# connections. There are separate PRSNT2# pins for each of the lane options: one lane (x1) and four lanes (x4). These pins are pulled-up on the host motherboard. There is a single PRSNT1# pin that is pulled-low or tied to GND on the host motherboard. The add-in card connects the PRSNT1# pin to the PRSNT2# pin for the widest lane option in most applications, which effectively pulls the corresponding PRSNT2# pin low. This indicates to the host controller the lane width supported by the add-in card. The Mini-Module Plus Baseboard 2 development board provides the ability for the user to select the lane width by connecting the desired PRSNT2# pin with a jumper on **JP5**. See the figure below for an illustration of JP5

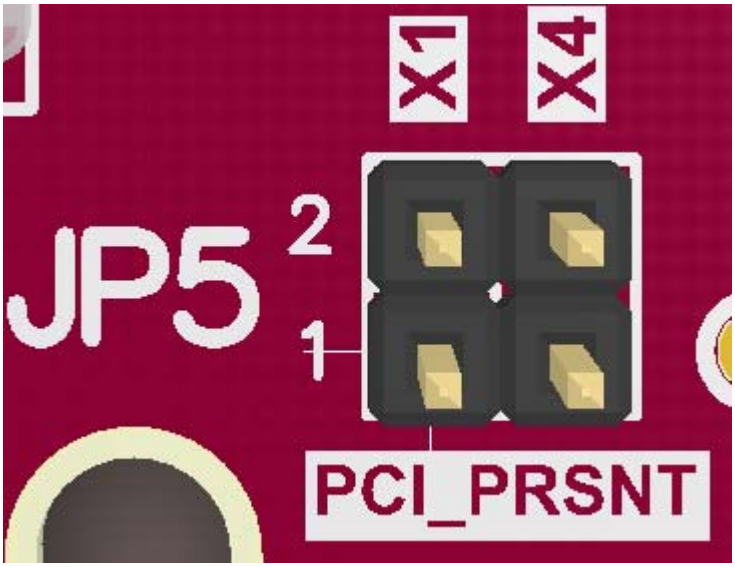


Figure 31 - PCI_PRSNT Configuration Jumper

Placing a jumper shunt across JP5 positions 1-2 indicates to the host system a x1 interface and placing a jumper shunt across JP positions 3-4 indicates a x4 interface.

The PCI Express receive lanes are AC coupled (DC blocking capacitors are included in the signal path) on the development board as required by the PCI Express specification. The Transmit pairs are AC coupled on the Mini-Module that is installed on the baseboard.

The table below shows the electrical connections to the Mini-Module Plus mating connector JX2.

Signal Name	Mini-Module Plus mating Connector (JX2)
PCIe_RX0P	JX2.55
PCIe_RX0N	JX2.57
PCIe_TX0P	JX2.56
PCIe_TX0N	JX2.58
PCIe_RX1P	JX2.61
PCIe_RX1N	JX2.63
PCIe_TX1P	JX2.62
PCIe_TX1N	JX2.64
PCIe_RX2P	JX2.43
PCIe_RX2N	JX2.45
PCIe_TX2P	JX2.44
PCIe_TX2N	JX2.46
PCIe_RX3P	JX2.49
PCIe_RX3N	JX2.51
PCIe_TX3P	JX2.50
PCIe_TX3N	JX2.52

Table 34 - PCI Express JX2 Pin Assignments

2.2.1.3 SFP Connector

The Mini-Module Plus Baseboard 2 provides for a Small Form-factor Pluggable (SFP) interface which provides the ability to support optical links with the addition of optical transceiver modules (not included in the kit). The following figure shows a high-level block diagram of the SFP interface on the development board. This interface utilizes one GTX channel and a set of low-speed control signals to interface to the SFP module. The programmable LVDS synthesizer on the board is used to provide the reference clock. The SFP interface on the Mini-Module Plus Baseboard 2 development board has been designed to support transceivers with transmission rates up to 3.75 Gbps operating over multimode or single mode fiber.

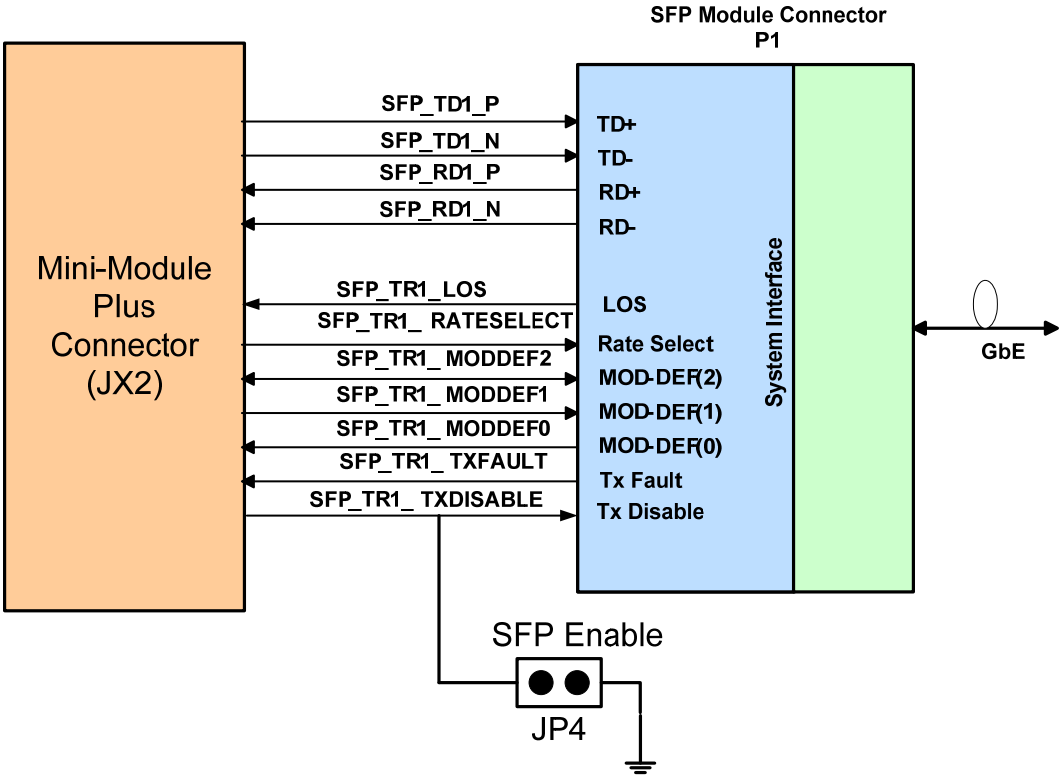


Figure 32 - SFP Module Interface

The SFP connector includes a Host Board Connector, and top and bottom EMI cage. The Host Connector is directly connected or DC coupled to the GTX port. SFP compliant modules include AC coupling capacitors in the modules for both transmit and receive signal paths so the AC coupling internal to the target GTX receiver may be bypassed.

The table below shows the electrical connections to the Mini-Module Plus mating connector JX2.

Signal Name	Mini-Module Plus mating Connector (JX1/JX2)
SFP0_RXP	JX1.49
SFP0_RXN	JX1.51
SFP0_TXP	JX1.50
SFP0_TXN	JX1.52
SFP_LOS	JX2.15
SFP_RATESEL	JX2.12
SFP_MODE0	JX2.11
SFP_MODE1	JX2.10
SFP_MODE2	JX2.9

SFP_TXFAULT	JX2.7
SFP_TXDISABLE	JX2.8

Table 35 - SFP JX1/JX2 Pin Assignments

SFP modules connect to the board via the Host Board Connector defined in the SFP Multi-Source Agreement (MSA). This 20-pin connector provides connections for power, ground, high-speed serial data, and the low-speed control signals for controlling the operation of the SFP module. The following figure shows the host connector used on the Mini-Module Plus Baseboard 2.

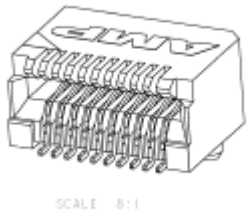


Figure 33 - Host Board Connector AMP 1367073-1 (photo taken from AMP Web Page)

The following table lists the Host Board Connector pin assignments and provides a brief description of each signal.

Pin Number	Signal Name	Function
1	VEET	Transmitter Ground
2	Tx Fault	Transmitter Fault Indication
3	Tx Disable	Transmitter Disable
4	MOD-DEF(2)	Module Definition 2 (Serial Interface Data Line)
5	MOD-DEF(1)	Module Definition 1 (Serial Interface Clock Line)
6	MOD-DEF(0)	Module Definition 0 (Module Present Signals, active low)
7	Rate Select	Not Connected
8	LOS	Loss of Signal
9	VEER	Receiver Ground
10	VEER	Receiver Ground
11	VEER	Receiver Ground
12	RD-	Inverse Received Data Out
13	RD+	Received Data Out
14	VEER	Receiver Ground
15	VCCR	Receiver Power
16	VCCT	Transmitter Power
17	VEET	Transmitter Ground
18	TD+	Transmitter Data In
19	TD-	Inverse Transmitter Data In
20	VEET	Transmitter Ground

Table 36 - SFP Host Connector Pin Description

2.2.1.4 2.1.4 GTX on FMC Expansion Connectors JX1 AND JX2

One GTX channel is interfaced to the target Mini-Module via the FMC slot JX3. Should a user want to connect an FMC daughter board to the Mini-Module Plus Baseboard 2 one gigabit channel is supported. The GTX channel is not AC coupled on the baseboard. The user must evaluate whether AC coupling is required on the daughter card to safely interface with the target Mini-Module.

Signal Name	Mini-Module Plus mating Connector (JX1/JX2)
FMC1_DP0_C2M_P	JX1.44
FMC1_DP0_C2M_N	JX1.46
FMC1_DP0_M2C_P	JX1.43
FMC1_DP0_M2C_N	JX1.45

Table 37 - FMC GTX JX1 Pin Assignments

2.2.1.5 2.1.5 SMA

One GTX channel is interfaced to the target Mini-Module via the on-board SMA connectors. The SMA connectors are referenced on the board as J11, J12, J13 and J14.

Signal Name	Mini-Module Plus mating Connector (JX1)
SMA_TXP	JX1.62
SMA_TXN	JX1.64
SMA_RXP	JX1.61
SMA_RXN	JX1.63

Table 38 - SMA GTX JX1 Pin Assignments

2.2.1.6 2.1.6 DisplayPort

One half of a GTX channel (transmit only) is interfaced to the target Mini-Module via the DisplayPort connector J9. This is a transmit only port that will allow the user to transmit DisplayPort data to the DisplayPort capable video monitor. The DisplayPort interface also utilizes one low speed differential auxiliary channel and a single DisplayPort HPD (Hot Plug Detect) single ended I/O signal.

Signal Name	Mini-Module Plus mating Connector (JX1/JX2)
DP_ML_L0_P	JX1.56
DP_ML_L0_N	JX1.58

DP_AUX_CH_P	JX2.112
DP_AUX_CH_N	JX2.114
DP_HPD	JX1.32

Table 39 – DisplayPort JX1/JX2 Pin Assignments

2.2.2 FMC Low Pin Count (LPC) Interface

The FMC specification defines the LPC interface to be a 160-pin connector arranged in a 4x40 array. The LPC connector is populates 160 of the 400 possible positions. The HPC (High Pin Count) version of the connector has all positions populated.

The FMC LPC configuration implemented on the Mini-Module Plus Baseboard 2 development board uses one LPC connector (SAMTEC part number ASP-134603-01), for a total of 68 user I/Os. The connector is referenced as **JX3** on the board.

The FMC specification defines five user signal types: Differential I/O, Differential Clock Inputs, Differential Clock Outputs, MGT I/O, and MGT Clock Inputs. Because the FPGA I/Os can be configured for either single-ended or differential use, the differential I/Os defined in the FMC specification can serve a dual role. All the differential I/O signals can be configured as either differential pairs or single-ended signals, as required by the end application. In providing differential signaling, higher performance LVDS interfaces can be implemented between the Mini-Module Plus Baseboard 2 development board and an FMC LPC module. Connection to high speed A/Ds, D/As, and flat panel displays are possible with this signaling configuration. Applications that require single-ended signals only can use each differential pair as two single-ended signals, for a total of 68 single-ended I/O per LPC connector.

Signal Names	Signal Description	Pins per Connector
FMC_LA**_P/N	34 Differential I/O Pairs	68
Total	**User I/O**	**68**
FMC_CLK0_C2M_P/N	1 Differential Clock Pair (Carrier to Mezzanine)	2
FMC_CLK0_M2C_P/N	1 Differential Clock Pair (Mezzanine to Carrier)	2
Total	**Clock I/O**	**4**
FMC_DP0_M2C_P/N	1 MGT Receive Differential Data Pair	2
FMC_DP0_C2M_P/N	1 MGT Transmit Differential Data Pair	2
FMC_GBTCLK0_M2C_P/N	1 MGT Differential Clock Pair	2
Total	**MGT I/O**	**6**

Table 40 - FMC LPC Connector Signals

	H	G	D	C
1	VREF_A_M2C	GND	PG_C2M	GND
2	PRSNT_M2C_L	CLK1_M2C_P	GND	DP0_C2M_P
3	GND	CLK1_M2C_N	GND	DP0_C2M_N
4	CLK0_M2C_P	GND	GBTCLK0_M2C_P	GND
5	CLK0_M2C_N	GND	GBTCLK0_M2C_N	GND
6	GND	LA00_P_CC	GND	DP0_M2C_P
7	LA02_P	LA00_N_CC	GND	DP0_M2C_N
8	LA02_N	GND	LA01_P_CC	GND
9	GND	LA03_P	LA01_N_CC	GND
10	LA04_P	LA03_N	GND	LA06_P
11	LA04_N	GND	LA05_P	LA06_N
12	GND	LA08_P	LA05_N	GND
13	LA07_P	LA08_N	GND	GND
14	LA07_N	GND	LA09_P	LA10_P
15	GND	LA12_P	LA09_N	LA10_N
16	LA11_P	LA12_N	GND	GND
17	LA11_N	GND	LA13_P	GND
18	GND	LA16_P	LA13_N	LA14_P
19	LA15_P	LA16_N	GND	LA14_N
20	LA15_N	GND	LA17_P_CC	GND
21	GND	LA20_P	LA17_N_CC	GND
22	LA19_P	LA20_N	GND	LA18_P_CC
23	LA19_N	GND	LA23_P	LA18_N_CC
24	GND	LA22_P	LA23_N	GND
25	LA21_P	LA22_N	GND	GND
26	LA21_N	GND	LA26_P	LA27_P
27	GND	LA25_P	LA26_N	LA27_N
28	LA24_P	LA25_N	GND	GND
29	LA24_N	GND	TCK	GND
30	GND	LA29_P	TDI	SCL
31	LA28_P	LA29_N	TDO	SDA
32	LA28_N	GND	3P3VAUX	GND
33	GND	LA31_P	TMS	GND
34	LA30_P	LA31_N	TRST_L	GA0
35	LA30_N	GND	GA1	12P0V
36	GND	LA33_P	3P3V	GND
37	LA32_P	LA33_N	GND	12P0V
38	LA32_N	GND	3P3V	GND
39	GND	VADJ	GND	3P3V
40	VADJ	GND	3P3V	GND
	LPC Connector	LPC Connector	LPC Connector	LPC Connector

Figure 34 - FMC LPC Connector Pin Out

Note: For the FMC LPC, the connector columns K, J, F, E, B, and A are not used and not shown in the above table.

The SAMTEC connector plug on the board (CC-LPC-10 part number: ASP-134603-01) mates with the SAMTEC low pin count receptacle (MC-LPC-10 part number: ASP-134604-01), located on FMC modules.

Since the FMC connectors are connected to the I2C bus a geographical address must be given to the connector. The GA[1:0] inputs provide a means to give the connector an I2C address. For JX3 the address is hard wired to 0x00 by tying these inputs low through pull-down resistors.

The following diagram and table shows how FMC LPC connector JX3 is connected to the Mini-Module Plus mating connectors JX1 and JX2.

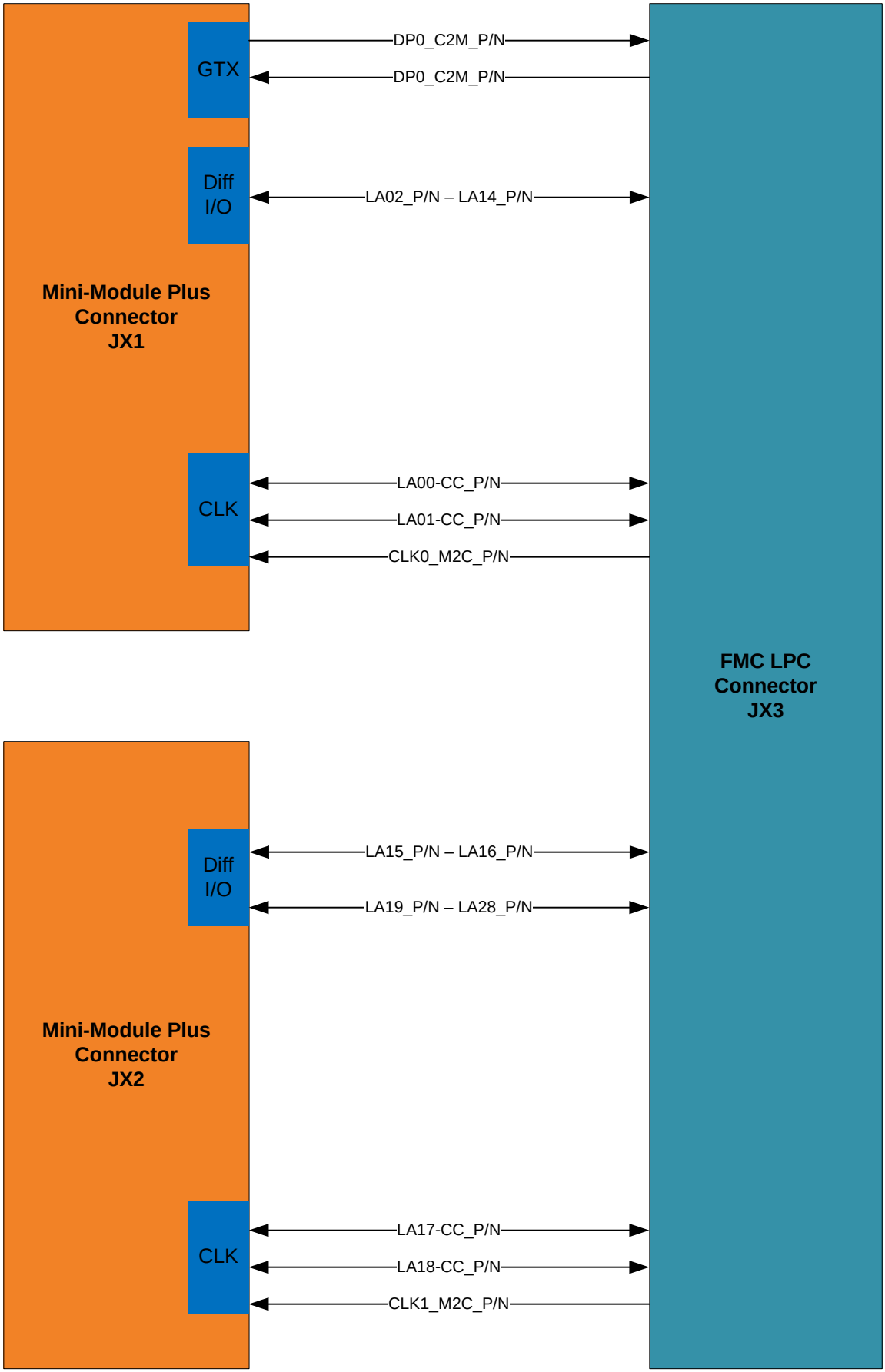


Figure 35 - FMC LPC Connector JX3 Block Diagram

Mini-Module Plus mating Connector (JX1/JX2)	Schematic Net Name	FMC Connector Pin Location (JX1)	FMC Connector Symbol Name
-	GND	C1	GND
JX1.44	**FMC1_DP0_C2M_P**	**C2**	**DP0_C2M_P**
JX1.46	**FMC1_DP0_C2M_N**	**C3**	**DP0_C2M_N**
-	GND	C4	GND
-	GND	C5	GND
JX1.43	**FMC1_DP0_M2C_P**	**C6**	**DP0_M2C_P**
JX1.45	**FMC1_DP0_M2C_N**	**C7**	**DP0_M2C_N**
-	GND	C8	GND
-	GND	C9	GND
JX1.88	**FMC1_LA06_P**	**C10**	**LA06_P**
JX1.90	**FMC1_LA06_N**	**C11**	**LA06_N**
-	GND	C12	GND
-	GND	C13	GND
JX1.105	**FMC1_LA10_P**	C14	LA10_P
JX1.107	**FMC1_LA10_N**	C15	LA10_N
-	GND	C16	GND
-	GND	C17	GND
JX1.111	**FMC1_LA14_P**	**C18**	**LA14_P**
JX1.113	**FMC1_LA14_N**	**C19**	**LA14_N**
-	GND	C20	GND
-	GND	C21	GND
JX2.81	**FMC1_LA18_CC_P**	**C22**	**LA18_P_CC**
JX2.83	**FMC1_LA18_CC_N**	**C23**	**LA18_N_CC**
-	GND	C24	GND
-	GND	C25	GND
JX2.106	**FMC1_LA27_P**	**C26**	**LA27_P**
JX2.108	**FMC1_LA27_N**	**C27**	**LA27_N**
-	GND	C28	GND
-	GND	C29	GND
JX1.14	**SCL_0**	**C30**	**SCL**
JX1.13	**SDA_0_VT**	**C31**	**SDA**
-	GND	C32	GND
-	GND	C33	GND
-	**PULL-DOWN**	**C34**	**GA0**
-	12V	C35	12P0V
-	-	C36	GND
-	12V	C37	12P0V
-	-	C38	GND
-	3.3V	C39	3P3V
-	-	C40	GND
-	**FMC_VADJ(PULL-UP)**	**D1**	**PG_C2M**
-	GND	D2	GND
-	GND	D3	GND
JX1.67	**CLK_MUX_OUT_P**	**D4**	**GBTCLK0_M2C_P**
JX1.69	**CLK_MUX_OUT_N**	**D5**	**GBTCLK0_M2C_N**
-	GND	D6	GND
-	GND	D7	GND
JX1.75	**FMC1_LA01_CC_P**	**D8**	**LA01_P_CC**
JX1.77	**FMC1_LA01_CC_N**	**D9**	**LA01_N_CC**
-	GND	D10	GND
JX1.87	**FMC1_LA05_P**	**D11**	**LA05_P**
JX1.89	**FMC1_LA05_N**	**D12**	**LA05_N**
-	GND	D13	GND
JX1.106	**FMC1_LA09_P**	**D14**	**LA09_P**
JX1.108	**FMC1_LA09_N**	**D15**	**LA09_N**
-	GND	D16	GND
JX1.112	**FMC1_LA13_P**	**D17**	**LA13_P**
JX1.114	**FMC1_LA13_N**	**D18**	**LA13_N**
-	GND	D19	GND
JX2.117	**FMC1_LA17_CC_P**	**D20**	**LA17_P_CC**
JX2.119	**FMC1_LA17_CC_N**	**D21**	**LA17_N_CC**
-	GND	D22	GND
JX2.87	**FMC1_LA23_P**	**D23**	**LA23_P**
JX2.89	**FMC1_LA23_N**	**D24**	**LA23_N**
-	GND	D25	GND
JX2.111	**FMC1_LA26_P**	**D26**	**LA26_P**
JX2.113	**FMC1_LA26_N**	**D27**	**LA26_N**
-	GND	D28	GND
JX2.1	**JTAG_TCK**	**D29**	**TCK**
JX1.2	**MMP_TDO**	**D30**	**TDI**
-	**FMC1_TDO**	**D31**	**TDO**

-	FMC_3.3V	D32	3P3VAUX
JX2.2	**JTAG_TMS**	**D33**	**TMS**
JX1.15	**FMC_TRST_L**	**D34**	**TRST_L**
-	**PULLD-DOWN**	**D35**	**GA1**
-	3.3V	D36	3P3V
-	GND	D37	GND
-	3.3V	D38	3P3V
-	GND	D39	GND
-	3.3V	D40	3P3V
-	GND	G1	GND
JX2.118	**FMC1_CLK1_M2C_P**	**G2**	**CLK1_M2C_P**
JX2.120	**FMC1_CLK1_M2C_N**	**G3**	**CLK1_M2C_N**
-	GND	G4	GND
-	GND	G5	GND
JX1.117	**FMC1_LA00_CC_P**	**G6**	**LA00_P_CC**
JX1.119	**FMC1_LA00_CC_N**	**G7**	**LA00_N_CC**
-	GND	G8	GND
JX1.82	**FMC1_LA03_P**	**G9**	**LA03_P**
JX1.84	**FMC1_LA03_N**	**G10**	**LA03_N**
-	GND	G11	GND
JX1.94	**FMC1_LA08_P**	**G12**	**LA08_P**
JX1.96	**FMC1_LA08_N**	**G13**	**LA08_N**
-	GND	G14	GND
JX1.100	**FMC1_LA12_P**	**G15**	**LA12_P**
JX1.102	**FMC1_LA12_N**	**G16**	**LA12_N**
-	GND	G17	GND
JX2.76	**FMC1_LA16_P**	**G18**	**LA16_P**
JX2.78	**FMC1_LA16_N**	**G19**	**LA16_N**
-	GND	G20	GND
JX2.82	**FMC1_LA20_P**	**G21**	**LA20_P**
JX2.84	**FMC1_LA20_N**	**G22**	**LA20_N**
-	GND	G23	GND
JX2.94	**FMC1_LA22_P**	**G24**	**LA22_P**
JX2.96	**FMC1_LA22_N**	**G25**	**LA22_N**
-	GND	G26	GND
JX2.100	**FMC1_LA25_P**	**G27**	**LA25_P**
JX2.102	**FMC1_LA25_N**	**G28**	**LA25_N**
-	GND	G29	GND
JX1.3	**FMC1_LA29_P**	**G30**	**LA29_P**
JX1.4	**FMC1_LA29_N**	**G31**	**LA29_N**
-	GND	G32	GND
JX1.5	**FMC1_LA31_P**	**G33**	**LA31_P**
JX1.6	**FMC1_LA31_N**	**G34**	**LA31_N**
-	GND	G35	GND
JX1.9	**FMC1_LA33_P**	**G36**	**LA33_P**
JX1.10	**FMC1_LA33_N**	**G37**	**LA33_N**
-	GND	G38	GND
-	FMC_VADJ	G39	VADJ_2.5V
-	GND	G40	GND
-	-	H1	VREF_A_M2C
JX1.16	**FMC1_PRSNT_M2C_L_VT**	**H2**	**PRSNT_M2C_L**
-	GND	H3	GND
JX1.118	**FMC1_CLK0_M2C_P**	**H4**	**CLK0_M2C_P**
JX1.120	**FMC1_CLK0_M2C_N**	**H5**	**CLK0_M2C_N**
-	GND	H6	GND
JX1.76	**FMC1_LA02_P**	**H7**	**LA02_P**
JX1.78	**FMC1_LA02_N**	**H8**	**LA02_N**
-	GND	H9	GND
JX1.81	**FMC1_LA04_P**	**H10**	**LA04_P**
JX1.83	**FMC1_LA04_N**	**H11**	**LA04_N**
-	GND	H12	GND
JX1.93	**FMC1_LA07_P**	**H13**	**LA07_P**
JX1.95	**FMC1_LA07_N**	**H14**	**LA07_N**
-	GND	H15	GND
JX1.99	**FMC1_LA11_P**	**H16**	**LA11_P**
JX1.101	**FMC1_LA11_N**	**H17**	**LA11_N**
-	GND	H18	GND
JX2.75	**FMC1_LA15_P**	**H19**	**LA15_P**
JX2.77	**FMC1_LA15_N**	**H20**	**LA15_N**
-	GND	H21	GND
JX2.88	**FMC1_LA19_P**	**H22**	**LA19_P**
JX2.90	**FMC1_LA19_N**	**H23**	**LA19_N**
-	GND	H24	GND
JX2.93	**FMC1_LA21_P**	**H25**	**LA21_P**
JX2.95	**FMC1_LA21_N**	**H26**	**LA21_N**
-	GND	H27	GND

JX2.99	**FMC1_LA24_P**	**H28**	**LA24_P**
JX2.101	**FMC1_LA24_N**	**H29**	**LA24_N**
-	GND	H30	GND
JX2.105	**FMC1_LA28_P**	**H31**	**LA28_P**
JX2.107	**FMC1_LA28_N**	**H32**	**LA28_N**
-	GND	H33	GND
JX1.7	**FMC1_LA30_P**	**H34**	**LA30_P**
JX1.8	**FMC1_LA30_N**	**H35**	**LA30_N**
-	GND	H36	GND
JX1.11	**FMC1_LA32_P**	**H37**	**LA32_P**
JX1.12	**FMC1_LA32_N**	**H38**	**LA32_N**
-	GND	H39	GND
-	FMC_VADJ	H40	VADJ_2.5V

Table 41 - FMC LPC Connector JX1 Pin Assignments

NOTE: The signal pairs highlighted in orange denote pairs that are routed differentially on the Mini-Module Plus Baseboard 2 but may NOT be on the target Mini-Module. Mini-Module specification defines these pins as single ended signals.

2.2.3 Clock Sources

This section describes the clock sources that are available on the Mini-Module Plus Baseboard 2.

2.2.3.1 2.3.1 CDCM61001 Programmable Clock Synthesizer

There is an on-board TI CDCM61001 LVDS clock synthesizer that is connected to the MGT_REFCLK inputs on the Mini-Module Plus connector JX1 and can be used to generate the reference clock for the target Mini-Module's GTX circuit(s).

A list of features included in the CDCM61001 device is shown below.

- Output frequency range: 43.75 MHz to 683.264 MHz
- RMS period jitter: 0.509 ps @ 625 MHz
- Output rise and fall time: 255 ps (maximum)
- Output duty cycle: varies dependant on output frequency

The following figure shows a high-level block diagram of the CDCM61001 programmable clock synthesizer. Inputs OS0 and OS1 are hard wired to use the LVDS mode of the CDCM61001 device.

Design Note: The CDCM61001 is sourced by a 27 MHz clock oscillator U10.

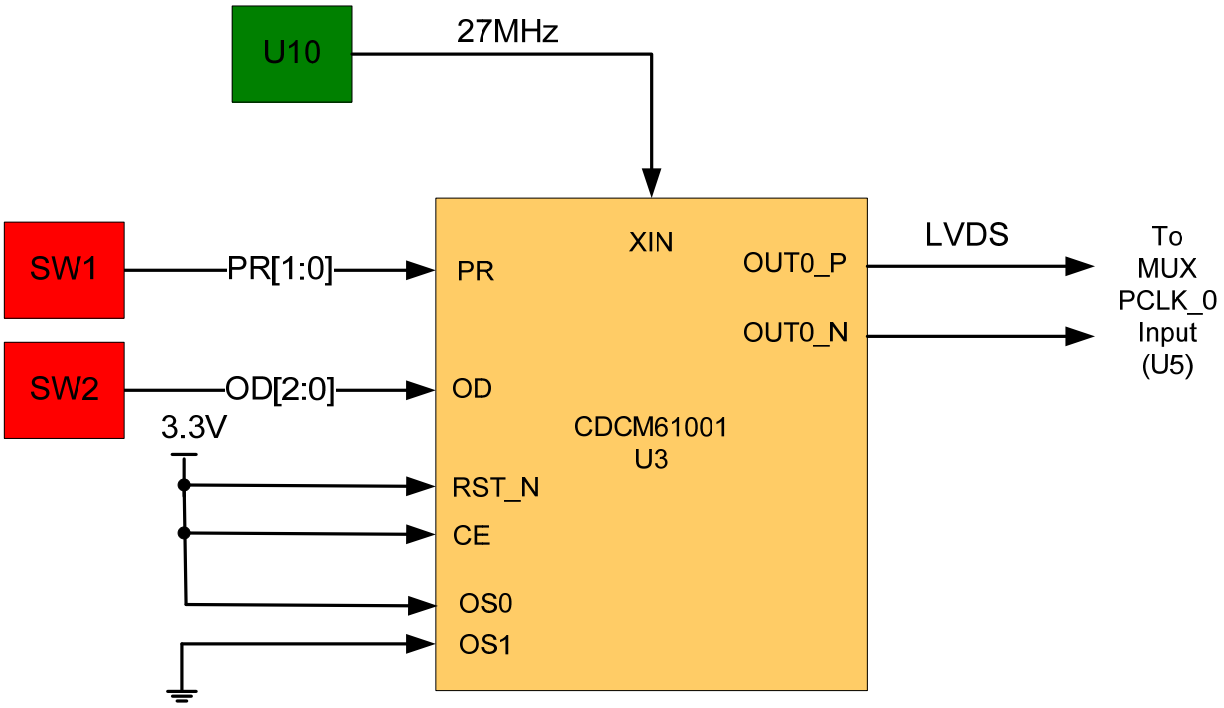


Figure 36 - CDCM61001 Clock Synthesizer

Signal Name	Direction	Pull up/Pull down (Internal)	Description
PR[1:0]	Input	Pull up	Prescaler and Feedback divider control pins.
OD[2:0]	Input	Pull up	Output divider control pins.
OS[1:0]	Input	Pull up	Output type select control pins.
CE	Input	Pull up	Chip enable.
RST_N	Input	Pull up	Device reset (active low).
XIN	Input	Pull up	Parallel resonant crystal/LVCMOS input.
OUT0 P/N	Output		Differential output pair.

Table 42 - CDCM61001 Clock Synthesizer Pin Description

2.2.3.2 CDCM61001 Clock Generation

The CDCM61001 output clocks are generated based on the following formula:

FOUT = (FIN) (FD) / OD

Equation Variables:

FOUT = Output Frequency

FIN = Clock Input Frequency

FD = Feedback Divider Value

OD = Output Divider Value

Please refer to the CDCM61001 datasheet for detailed tables regarding the Feedback Divider and Output Divider values. The CDCM61001 FD and OD values are programmed via dipswitches SW1 and SW2. These dipswitches should be configured prior to powering up the board.

2.2.3.3 CDCM61001 Programming Mode

The Mini-Module Plus Baseboard 2 development board allows programming of the PR and OD values in parallel mode. This is the only mode allowed by the device. In parallel mode, PR and OD values are programmed into the device upon power-on. The switches should be set into the correct position prior to turning on power to the board. Should the switch settings change after power up the board will have to be power cycled to reset the device

2.2.3.4 CDCE913 Programmable Clock

The CDCE913 is a modular PLL-based low-cost, high-performance, programmable clock synthesizer, multiplier, and divider. It can generate up to 3 output clocks from a single input frequency. Each output can be programmed via an SDA / SCL, SMBus / I2C interface, for any clock frequency up to 230 MHz, using the integrated configurable PLL. The input crystal frequency for the CDCE913 is 27MHz.

Only two of the outputs on the CDCE913 are used on the Mini-Module Plus Baseboard 2. The CDCE913 clock outputs will connect to global clock inputs on the target Mini-Module. The Y3 output is left floating.

The table below shows the electrical connection between the CDCE913 clock generator and the Mini-Module Plus connectors.

Signal Name	Mini-Module Plus mating Connector (JX1/JX2)
CDCE_SCL	JX1.34
CDCE_SDA	JX1.33
CDCE_Y1_OUT	JX1.39
CDCE_Y2_OUT	JX2.39

Table 43 – CDCE913 Pin Assignments

2.2.4 Communication

The Mini-Module Plus Baseboard 2 Implements a Silicon Labs CP2102 device that provides a USB-to-RS232 bridge. The USB physical interface is brought out on a USB Type-B connector labeled “J8”.

The USB-to-RS232 bridge interface connects to the Mini-Module Plus connectors at the following pins:

Signal Name	Mini-Module Plus mating Connector (JX1/JX2)

UART_TX	JX1.36
UART_RX	JX1.35

Table 44 – USB-to-RS232 Pin Assignments

2.2.5 Memory

The Mini-Module Plus Baseboard 2 implements a Micro-SD Card interface. The table below shows how the Micro-SD Card connector connects to the Mini-Module Plus connectors.

Signal Name	Mini-Module Plus mating Connector (JX1/JX2)
SD1_D0	JX2.32
SD1_D1	JX2.33
SD1_D2	JX2.34
SD1_D3	JX2.35
SD1_CMD	JX2.36
SD1_CLK	JX2.37

Table 45 – Micro-SD Card Pin Assignments

2.2.6 PMOD Headers

Two vertical, 12-pin (2 x 6 female) Peripheral Module (PMOD) headers (J2, J5) are connected to the Mini-Module Plus connectors, with each header providing 3.3 V power, ground, and eight I/O's. These headers may be utilized as general-purpose I/Os or may be used to interface to PMODs. J2 and J5 are placed in close proximity (0'9"-centers) on the PCB in order to support dual PMODs**.** Tables 19 and 20 provide the connector and FPGA pin out. For Digilent PMODs see: **http://www.digilentinc.com/Products/Catalog.cfm?Nav1=Products&Nav2=Peripheral&Cat=Peripheral**

Mini-Module Plus mating Connector (JX2)	I/O Signal	Connector Pin #	Connector Pin #	I/O Signal	Mini-Module Plus mating Connector (JX2)
JX2.14	PMOD1_P1	1	2	PMOD1_P2	JX2.15
JX2.16	PMOD1_P3	3	4	PMOD1_P4	JX2.17
-	**GND**	5	6	**3.3V**	-
JX2.18	PMOD1_P7	7	8	PMOD1_P8	JX2.19
JX2.20	PMOD1_P9	9	10	PMOD1_P10	JX2.23
-	**GND**	11	12	**3.3V**	-

Table 46 - Peripheral Module Pin Assignments – J2

Mini-Module Plus mating Connector (JX2)	Signal Name	Connector Pin #	Connector Pin #	Signal Name	Mini-Module Plus mating Connector (JX2)
JX2.24	PMOD2_P1	1	2	PMOD2_P2	JX2.25
JX2.26	PMOD2_P3	3	4	PMOD2_P4	JX2.27
-	**GND**	5	6	**3.3V**	-
JX2.28	PMOD2_P7	7	8	PMOD2_P8	JX2.29
JX2.30	PMOD2_P9	9	10	PMOD2_P10	JX2.31
-	**GND**	11	12	**3.3V**	-

Table 47 - Peripheral Module Pin Assignments – J5

2.2.7 User Push Buttons and Switches

Four momentary closure push buttons have been installed on the board and connected to the Mini-Module Plus connectors. These buttons can be programmed by the user on the target Mini-Module's FPGA and are ideal for logic reset and similar functions. Pull down resistors hold the signals low until the switch closure pulls them high (active high signals).

Signal Name	Reference	Mini-Module Plus mating Connector (JX2)
PB0	SW7	JX2.3
PB1	SW8	JX2.4
PB2	SW9	JX2.5
PB3	SW10	JX2.6

Table 48 - Push Button Pin Assignments

An eight-position dipswitch (SPST) has been installed on the board and connected to the Mini-Module Plus connectors. These switches provide digital inputs to user logic as needed. The signals are pulled low by 4.7K ohm resistors when the switch is open and tied high to FMC_VADJ (see "Power" section) when closed as shown in the following table.

Signal Name	Reference	Voltage when closed	Mini-Module Plus mating Connector (JX1)
SW0	SW6 – 1	FMC_VADJ	JX1.17
SW1	SW6 – 2		JX1.18
SW2	SW6 – 3		JX1.19
SW3	SW6 – 4		JX1.20
SW4	SW6 – 5		JX1.23

SW5	SW6 – 6		JX1.24
SW6	SW6 – 7		JX1.25
SW7	SW6 – 8		JX1.26

Table 49 - DIP Switch Pin Assignments

2.2.8 User LEDs

Five discrete LEDs are installed on the board and can be used to display the status of the target Mini-Module FPGA's internal logic. These LEDs are attached as shown below and are lit by forcing the associated FPGA I/O pin to a logic '1' and are off when the pin is either low (0) or not driven.

Net Name	Reference	Mini-Module Plus mating Connector (JX1)
LED0	D20	JX1.27
LED1	D21	JX1.28
LED2	D22	JX1.29
LED3	D23	JX1.30
LED4	D24	JX1.31

Table 50 - LED Pin Assignments

2.2.9 Configuration

The Mini-Module Plus Baseboard 2 supports two methods of configuring the target Mini-Module's FPGA. Both configuration sources use Boundary-scan and use either the Xilinx platform JTAG cable (J1) or the Digilent HS1 USB-JTAG module (U1). The blue "DONE" LED (D1) on the board illuminates to indicate when the FPGA has been successfully configured.

2.2.9.1 JTAG Chain

The Mini-Module Plus Baseboard 2 has two connectors in the JTAG chain, the Mini-Module plus mating connectors and the FMC LPC connector. The following figure shows a high-level block diagram of the JTAG Chain on the development board.

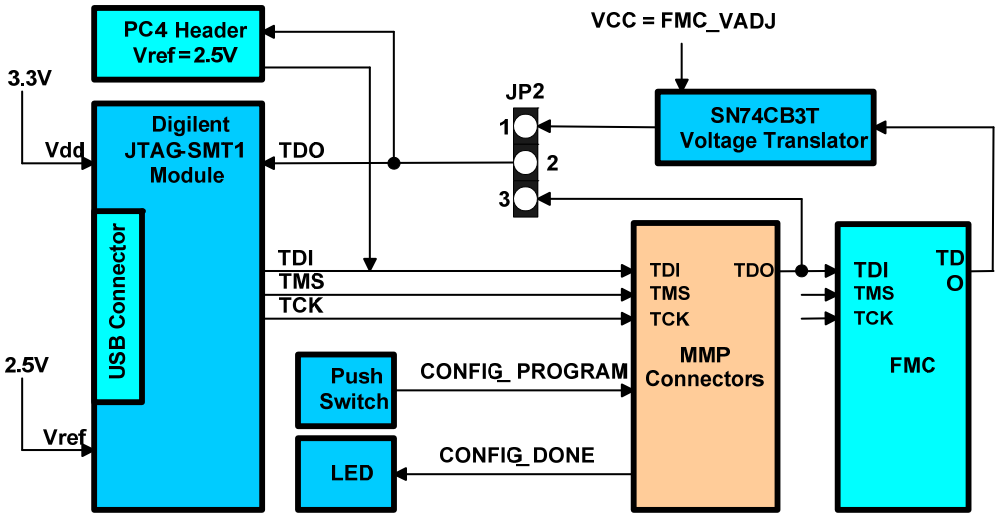


Figure 37 - JTAG Chain on the Mini-Module Plus Baseboard 2

Configuring the JTAG chain to include one or both can be done using jumper JP2. Setting the jumper position to 1-2 will include both connectors, while placing the jumper to position 2-3 includes only the Mini-Module Plus connectors.

Programming the FPGA on the target Mini-Module via Boundary-scan mode requires either JTAG download cable (not included in the kit). The Xilinx PC4 download cable plugs into the J1 connector on the board. Alternately, a standard USB A-Micro-B cable can be used to configure the target FPGA by plugging it into the Micro-B connector located at U1.

2.2.10 Power

The Mini-Module Plus Baseboard 2 power is derived from a +12 V input provided by the furnished power supply at J4 or from the 4-pin ATX power connector JP1. No power is available to the baseboard through the PCI Express edge connector. All of the voltage rails used on the board are derived from the 12V source. The 12V source is used to supply the input voltages to a variety of power solutions that reside power modules that are available from Avnet for the baseboard. This modular power approach allows the user to pick the best power solution for the end application and also allows the user flexibility to design their own power module if desired.

Avnet currently offers pre-designed power module solutions from Texas Instruments, Maxim, General Electric, ST Micro and Analog Devices. Click on the following link to the Avnet Design resource Center (DRC) to get more details.

http://www.em.avnet.com/en-us/design/drc/Pages/Xilinx-Kintex-7-Mini-Module-Plus.aspx

The voltage rails produced by the power modules are: 1.5V/1.35V (jumper selectable on the power modules), 1.8V, 2.0V, 3.3V, 1.0V, 1.0V_MGT, and 1.2V_MGT.

In stand-alone mode the board is connected to the external power supply via the six pin right angle connector J4**.** The power supply shipped with the Mini-Module Plus Baseboard 2 can supply 12 V @ 5 Amps.

NOTICE!!! NOTICE!!! NOTICE!!!

THE 6-PIN CONNECTOR "J4" SHOULD NEVER BE PLUGGED INTO A PC'S ATX 6-PIN PCI EXPRESS POWER CONNECTOR!

THE TWO CONNECTORS ARE NOT COMPATIBLE AND WILL CAUSE DAMAGE TO THE PC POWER SUPPLY, MINI-MODULE PLUS BASEBOARD 2, MINI-MODULE, POWER MODULE OR ALL OF THE ABOVE!

THE CONNECTOR "J4" WILL HAVE THE FOLLOWING LABEL ADHERED TO ITS TOP SIDE:

NOTICE!!! NOTICE!!! NOTICE!!!

When the Mini-Module Plus Baseboard 2 is plugged into a PCI Express slot within the PC's chassis it is recommended that the 4-pin ATX power connector JP1 is used to supply 12V to the board.

The main power switch to for the development board is SW5 and must be turned ON to supply any power to the board.

The figure below shows a high-level block diagram of the power architecture on the development board.

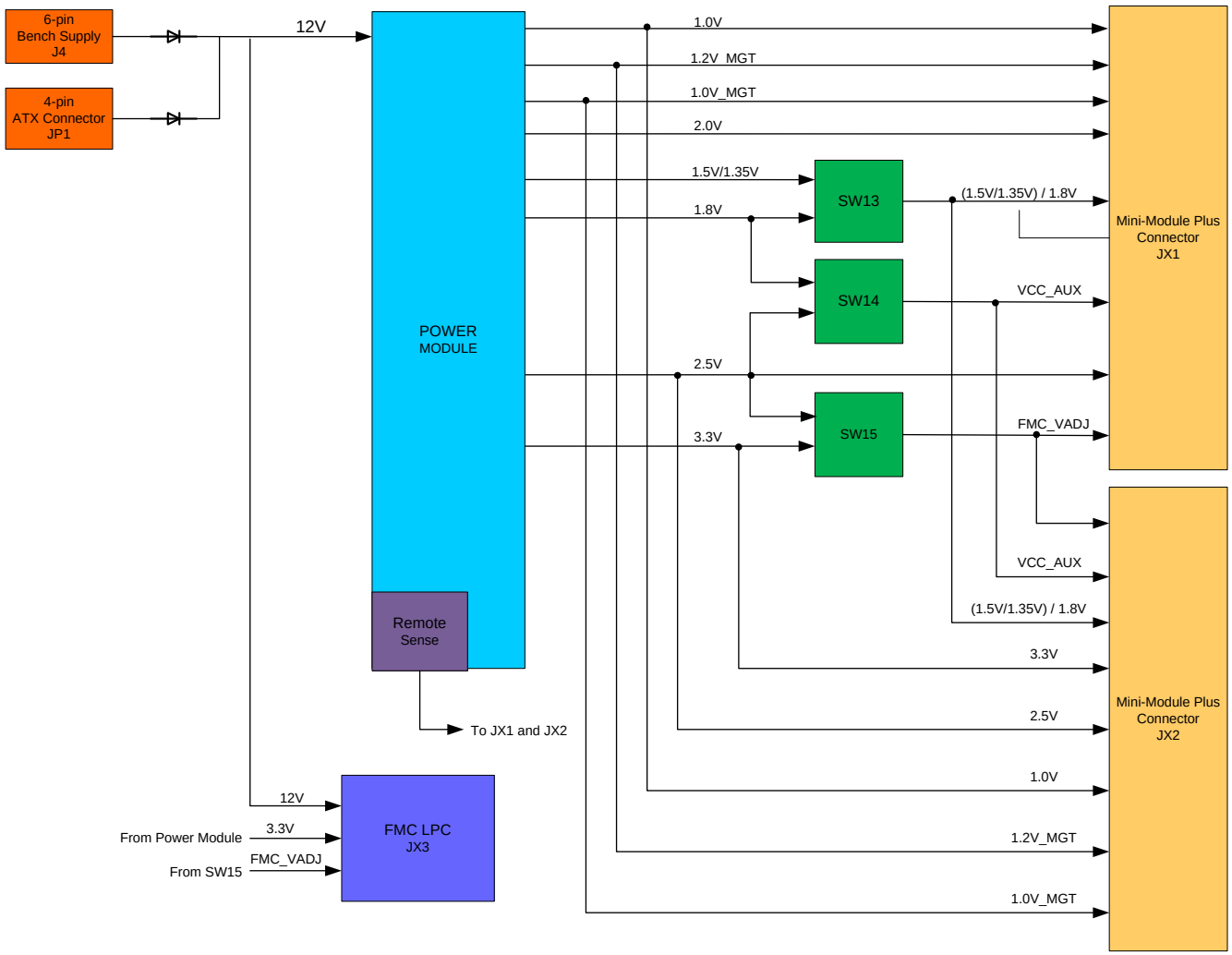


Figure 38 - Board Power

SW13 controls the voltage for the DDR circuits on a given target Mini-Module. Mini-Modules that implement DDR2 memory will utilize the 1.8V rail. Mini-Modules implementing DDR3 memory will use the 1.35/1.5V rail. Since DDR3 core voltage can be either 1.35V or 1.5V, the power modules have a jumper that can be placed to switch between 1.35V and 1.5V. Placing SW13 in the DOWN position selects 1.8V, while placing the switch in the UP position selects 1.35V/1.5V.

NOTE: SW13 is not installed on Rev C boards. The SW13 setting has been hardwired to support K7 Mini-Modules. See the bottom part of this section for details on the hardwired settings and how to modify the setting to support Virtex-5 Mini-Modules.

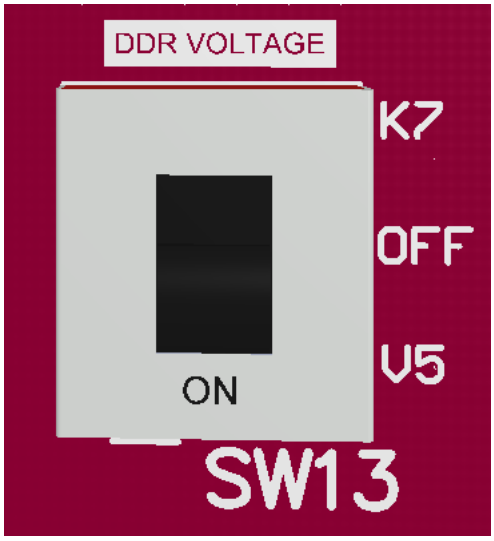


Figure 39 - DDR Voltage SW13

SW14 controls the VCC_AUX voltage being supplied to the target Mini-Module's FPGA. The Mini-Module Plus Baseboard 2 is backward compatible with the Virtex-5 Mini-Module, and thus the reason for this switch. Setting SW14 in the DOWN position sets VCC_AUX = 2.5V for Virtex-5 Mini-Modules. Setting the switch in the UP position sets the VCC_AUX = 1.8V, supporting the Kintex-7 mini-Module.

WARNING! WARNING! WARNING!

SW14 MUST BE SET PROPERLY WHEN INSTALLING A KINTEX-7 MINI-MODULE!! THE SWITCH MUST BE SET IN THE "UP" POSITION TO PREVENT DAMAGE TO THE KINTEX-7 FPGA. INSURE THE PROPER SWITCH SETTING PRIOR TO APPLYING POWER TO THE BOARD!!!

SEVERE DAMAGE TO THE MINI-MODULE CAN OCCUR IF THIS SWITCH IS NOT SET PROPERLY!!!

WARNING! WARNING! WARNING!

NOTE: SW14 is not installed on Rev C boards. The SW14 setting has been hardwired to support K7 Mini-Modules. See the bottom part of this section for details on the hardwired settings and how to modify the setting to support Virtex-5 Mini-Modules.

Figure 40 - VCC_AUX Voltage SW14

SW15 controls the FMC_VADJ voltage. The setting is either 2.5V or 3.3V. This setting is completely application specific. If an FMC module is installed on the baseboard that utilizes 3.3V I/O then setting this switch to the 3.3V position insures that the I/O routed to the FPGA banks connected to the FMC module will operate at the correct I/O voltage for the application.

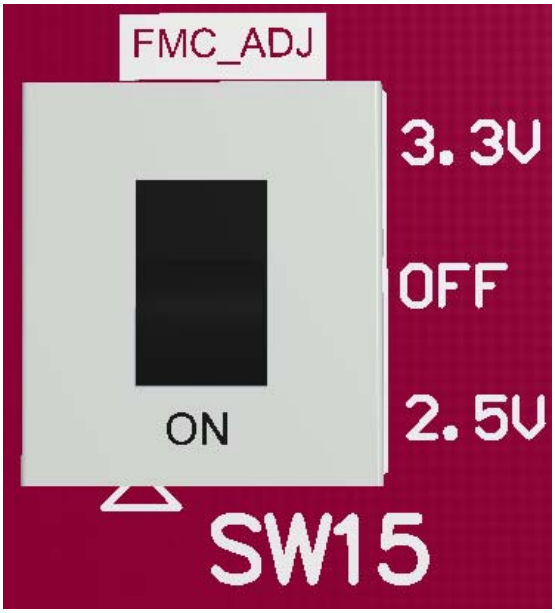


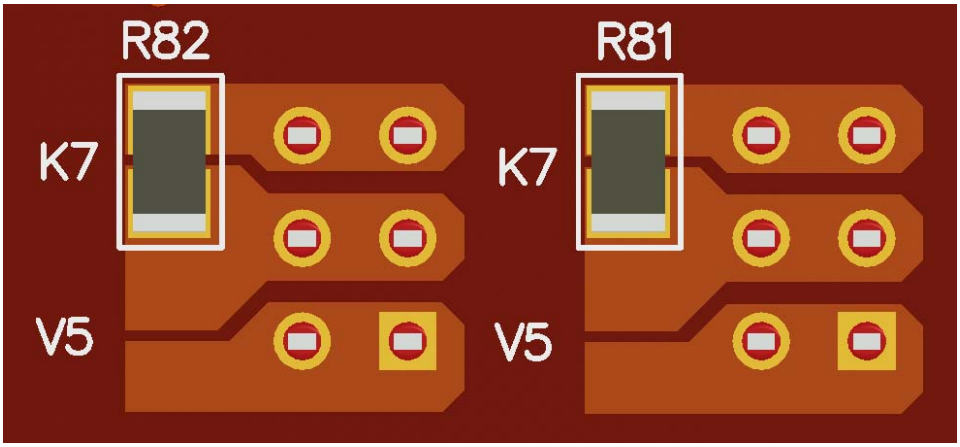
Figure 41 - FMC VADJ Voltage SW15

SW13 and SW14 Rev C Hardwired Settings

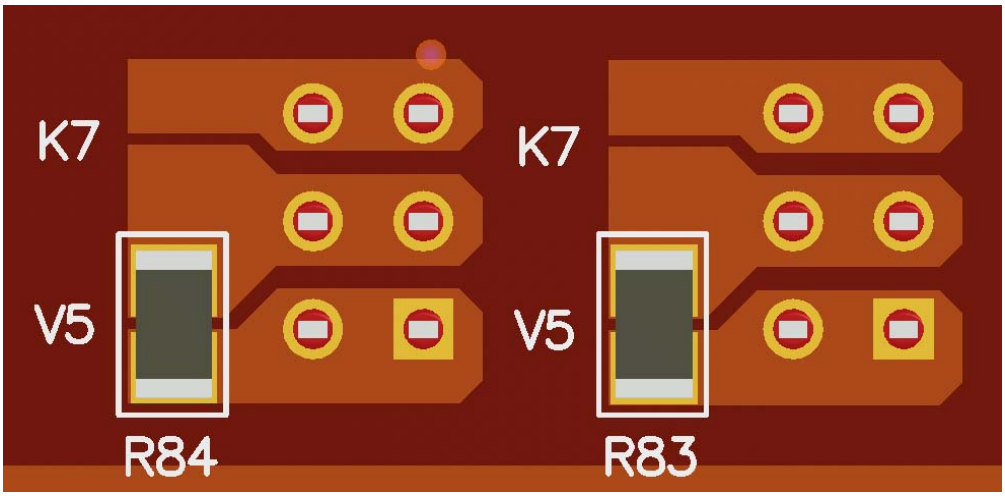
As mentioned in the above notes, SW13 and SW14 have been removed on Rev C Mini-Module Plus Baseboard's 2. The switches have jumper pads on the bottom side of the board directly below the switches that allow the user to hardwire the appropriate voltages for the DDR3 and VCC_AUX voltage rails depending on which platform is being used; Kintex-7 or Virtex-5. The jumpers used for Rev C boards are 0-ohm resistors in a 2512 package. The change on the Rev C boards came as a result of users inadvertently causing damage to the Kintex-7 Mini-Modules and/or DDR3 memory by having the switches set or inadvertently moved to the wrong position.

The default circuits for SW13 and SW14 is set to support the Kintex-7 platform which supplies 1.8V to VCC_AUX (SW14) and 1.5 or 1.35V to the DDR3 memory (SW13). The DDR3 memory voltage is determined by a jumper on the power modules.

See the picture below for an illustration of the default (K7) jumper positions as shipped from the factory.



If the user intends to support the Virtex-5 Mini-Module Plus platform, the jumpers must be moved to change the voltage settings for VCC_AUX (2.5V) and DDR2 memory (1.8V). The illustration below shows the proper implementation of the jumpers to support the Virtex-5 platform.



2.2.10.1 Remote Sense

The Mini-Module Plus Baseboard 2 implements remote sense in its power architecture using two connectors. One is located near the power module and plugs directly into the power module and is designated by J7. The other is located near the Mini-Module plus connectors and is designated J10.

Remote sense is implemented to insure more accurate voltage regulation at the loads of the target Mini-Module. The Kintex-7 Mini-Module from Avnet implements the remote sense connector. The Virtex-5 Mini-Module does not support the remote sense feature.

For Mini-Modules that implement remote sense feedback, the remote sense signals are placed at strategic and/or critical places at the various Mini-Module loads. Those signals are then routed down to the J10 connector on the baseboard and fed back to the power module for precise load regulation on a per rail basis.

Remote sense can be disabled by the user by moving or removing the 0-ohm jumper resistors on the baseboard. The default position of the resistor jumpers is in position 1-2, which enables the remote sense

feedback path to the power module regulators. Moving the resistor jumpers to the 2-3 position ties the remote sense feedback loop directly to the regulated output voltage per rail. This may or may not be desirable depending on the implementation of power module's remote sense feedback loop.

It is recommended that the remote sense feature be left enabled. For Mini-Modules that implement the remote sense feedback the voltages on each rail will be much more stable and efficient. For Mini-Modules that do not use the remote sense feedback the circuits on the power module will remain unaffected.

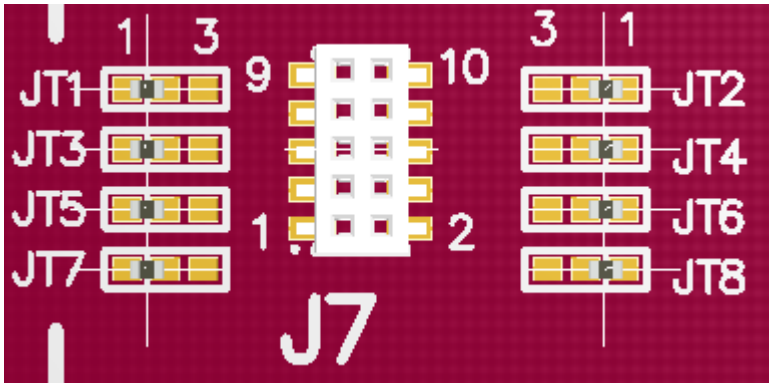


Figure 42 - Remote Sense Configuration Resistors

2.3 Customer Selected Power Module Functional Description

2.3.1 Introduction

The purpose of this section is to describe the functionality and contents of the Mini-Module Plus TI power supply module from Avnet Electronics Marketing. This document includes instructions for operating the board, descriptions of the hardware features and explanations of the header signals and functionality.

2.3.1.1 Description

The Mini-Module Plus (MMP) power module is designed to be used with the Avnet Mini-Module Plus development system. The power module operates off a 12VDC input provided from the Mini-Module Plus Baseboard. The following table shows the output voltages generated by the power module, as well as the voltage banks each rail is tied to through the baseboard.

Xilinx power bank / FMC Voltage	Voltage (V)	Max Current (A)	Tolerance
Vccint/Vccbram	1	6	3.00%
Vcco	1.5 / 1.35	4	5.00%
Vccaux/Vccaux_io/Vccadc/Vcco/MGTVccaux	1.8	6	5.00%
Vccaux_io	2	2	3.00%
Vcco	2.5	8	5.00%
Vcco	3.3	8	5.00%

MGTAVcc	1	6	3.00%
MGTAVtt/MGTAVTTrcal	1.2	4	2.50%

Table 51 – Output Voltages

2.3.1.2 Features

The MMP Power Module provides a complete power solution through the use of 3 headers. 2 headers are used to provide power between the Power Module and the MMP Baseboard. The 3rd header is used to provide access to remote sensing for increased regulation accuracy. There is one configurable supply provided on the board which is selectable to be either 1.5V output or 1.35V output. This supply configurability allows the MMP Power Module to work with Mini Module cards populated with either 1.5V or 1.35V DDR3 memory.

2.3.1.3 Reference Design

Reference design files for this board are available at:

www.avnet.com/MMPpowermodules

2.3.2 Functional Description

2.3.2.1 Block Diagram

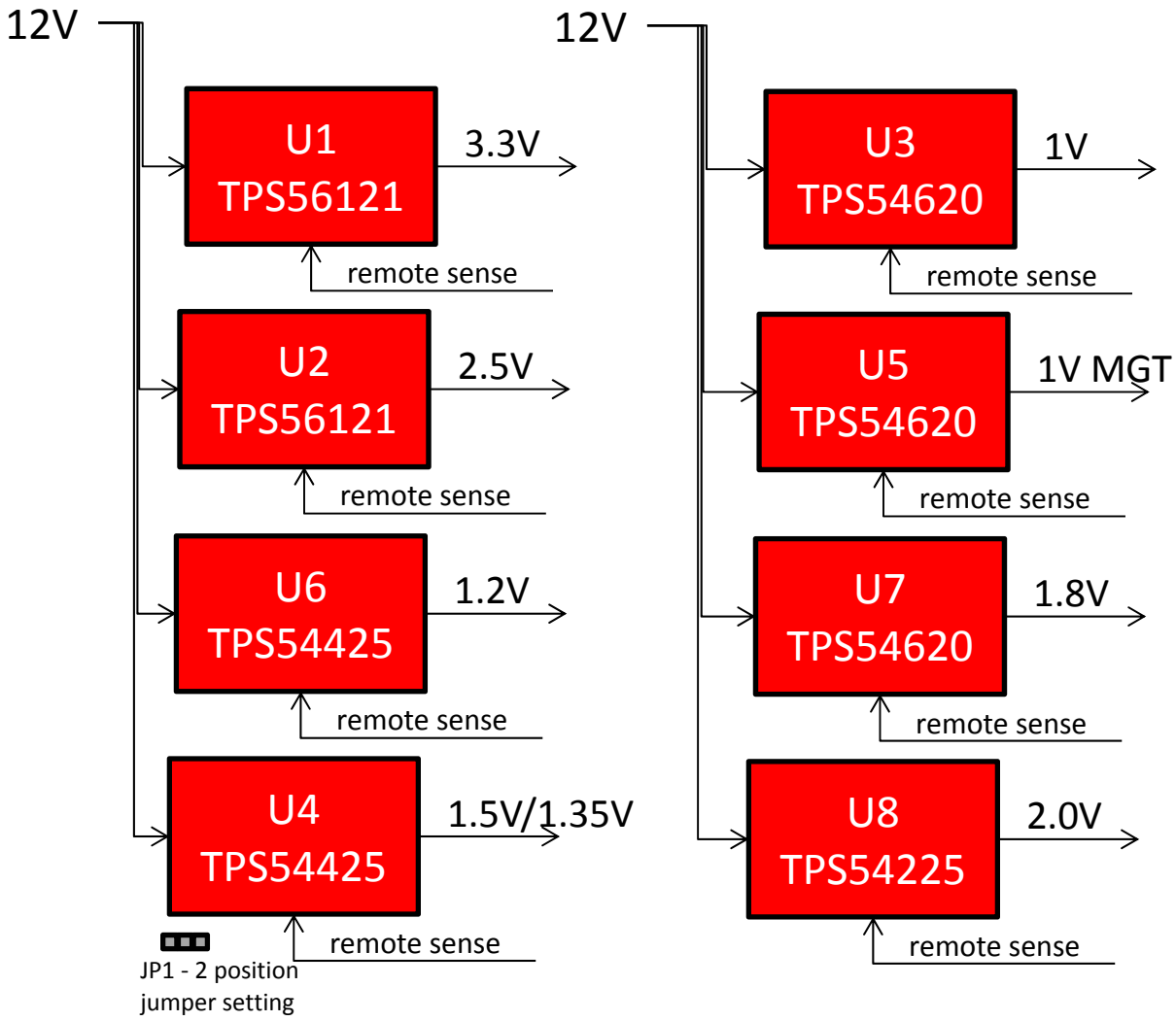


Figure 43 – Power Module Block Diagram

2.3.2.2 Header Pin Outs

The following tables show the pinouts for J1, J2 and J3. J1 and J2 provide power and ground to and from the MMP baseboard. J1 (Samtec part # HPM-10-05-T-S) and J2 (Samtec part # HPM-08-05-T-S) provide power to and from the board. On the baseboard, J1 mates with Samtec part # HPF-10-01-T-S and J2 mates with Samtec part # HPF-08-01-T-S.

Pin	1	2	3	4	5	6	7	8	9	10
Signal	GND	1.5V/1.35V	GND	1.8V	GND	2V	GND	3.3V	GND	12V

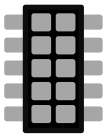
Table 52 – J1 Pinout

Pin	1	2	3	4	5	6	7	8

Signal	GND	1V	GND	1V(MGT)	GND	1.2V	GND	2.5V

Table 53 – J2 Pinout

J3 (Samtec part # FW-05-05-F-D-361-085) is in place to provide access for remote voltage sense. The mating connector on the Mini-Module Plus baseboard is Samtec part # CLP-105-02-F-D. The signals on this header are tied directly to the FPGA voltage pins. This header is pinned out left to right down the header as illustrated below:



1	2
3	4
5	6
7	8
9	10

Table 54 – J3 Diagram

Pins are defined as follows:

Pin	2	4	6	8	10
Signal	2.5Vrm	1Vmgtrm	2Vrm	1.2Vrm	GND
Pin	1	3	5	7	9
Signal	3.3Vrm	1.8Vrm	1Vrm	1.5Vrm	GND

Table 55 – J3 Pinout

Pin 1 location on J3 is indicated on the silk screen on the PCB. Pin 1 on J1 and J2 are the right most pins when viewing the board header side up. Refer to Figure 1 for an illustration of these pin positions.

2.3.2.3 Jumper Settings

Typically JP1 sets the output of the 1.5V / 1.35V regulator. (Not all cards have a JP1, named JP1. The user is advised to consult the user guide for their particular User Module.) JP1 is a 3 pin header with a jumper used to connect pins 1-2 or pins 2-3. Place the jumper on pins 1-2 to set the voltage to 1.5V. Set the jumper on pins 2-3 to set the voltage to 1.35V. The table below shows the jumper settings and corresponding output voltage.

Jumper setting	Output voltage
1-2	1.5V
2-3	1.35V

Table 56 – JP1 Jumper Settings

Setting the voltage to 1.5V or 1.35V is dependent on the type of memory utilized on the Mini-Module target board. In the case of the K7 Mini-Module for example, the DDR memory used is 1.5V.

WARNING: Do NOT power up the Power Module without the jumper set to either 1.5V or 1.35V. Powering the board without the jumper in place can result in board failure.

2.3.2.4 Normal operation

The power module provides 8 sequenced output voltages with controlled rise times from a 12VDC input. The supplies are designed to meet the current and regulation tolerances outlined in table 1.

2.3.2.5 Remote Sense

Remote sense is used to compensate for the power supplies being located far from the load. J3 provides a low impedance path directly to the voltage pins on the FPGA. By allowing access to the voltage actually being seen by the load, the regulator can adjust the output to be more accurate and compensate for impedance losses through components and the PCB.

When using remote sense, the signals tied to the header are traces that are terminated right at the pin of the target load. In our case, these voltage pins are terminated right at the pin on the FPGA. The signal is then routed as a trace back to the remote sense header. It is important that this signal originate from as close to the target load as possible. The signals on these pins are then used as the set point by the regulators to regulate the output voltage. By using a signal directly tied to the load as the set point, the power supplies are able to better regulate the voltage at the intended load.

2.3.2.6 Sequencing and Startup

Sequencing of the output voltages follows Xilinx specification for 7 Series devices as follows:

Vccint (1V) -> Vccaux (1.8V) -> Vccaux_io (2V) -> Vcco

The power module is designed to start all remaining supplies after the 2V rail has come up.
The diagram below illustrates the start up sequencing of the power module.

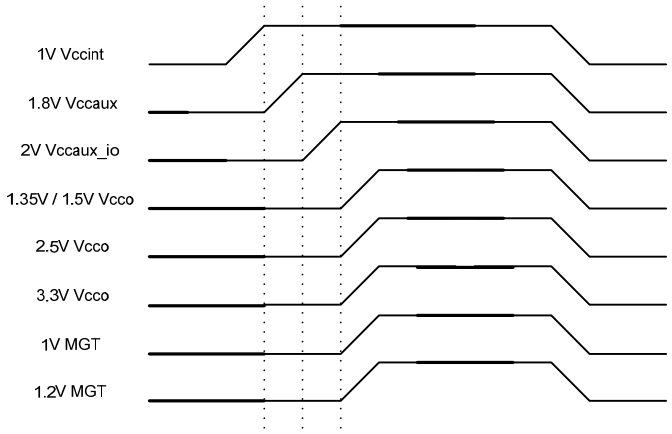


Figure 44 – Power Timing Diagram

Timing Diagram

Each rail must start up between 0.2ms and 50ms to meet ramp requirements, as well as have a monotonic rise. The requirement for power down sequencing states that the 3.3V Vcco rail cannot exceed the 1.8V Vccaux rail during shut down by more than 2.625V for longer than 500ms. No additional power down circuitry is needed in the power module to meet this requirement.

3 Mechanical Requirements

3.1 Kintex-7 MMP Mechanical

The following figure shows the Mini Module Plus physical dimensions and a suggested component placements. The suggested FPGA orientation will allow optimal routing of the Kintex-7 GTX ports to the JX1/JX2 connectors.

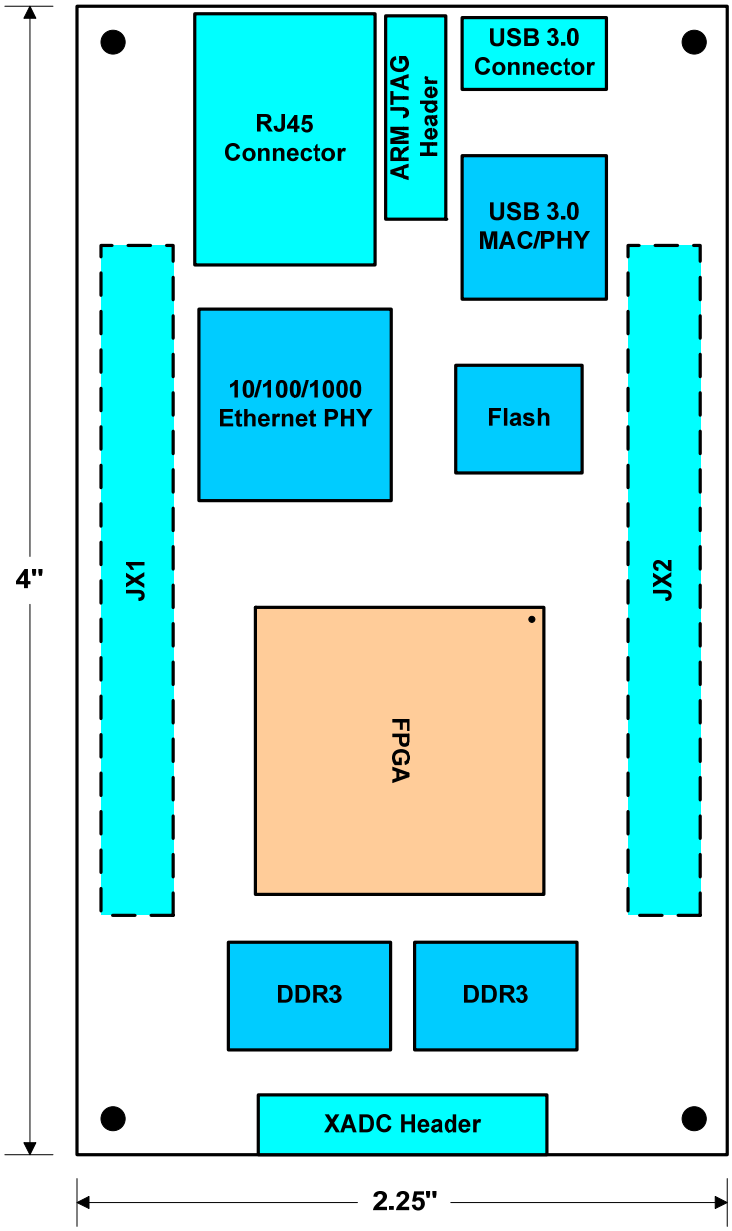


Figure 45 – Kintex-7 MMP Component Placements

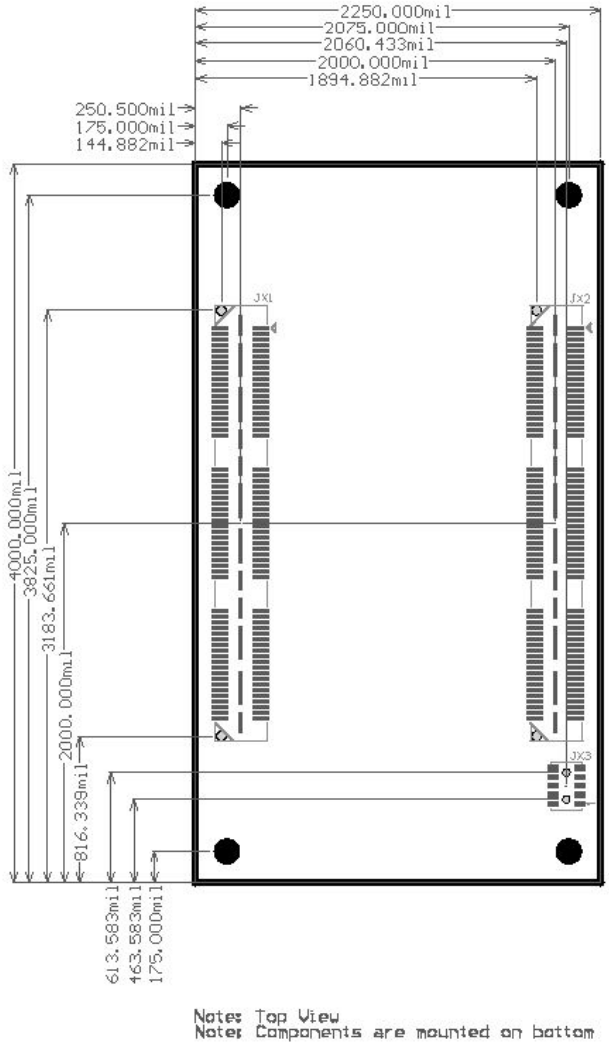


Figure 46 – Kintex-7 MMP Connectors Mechanical Locations

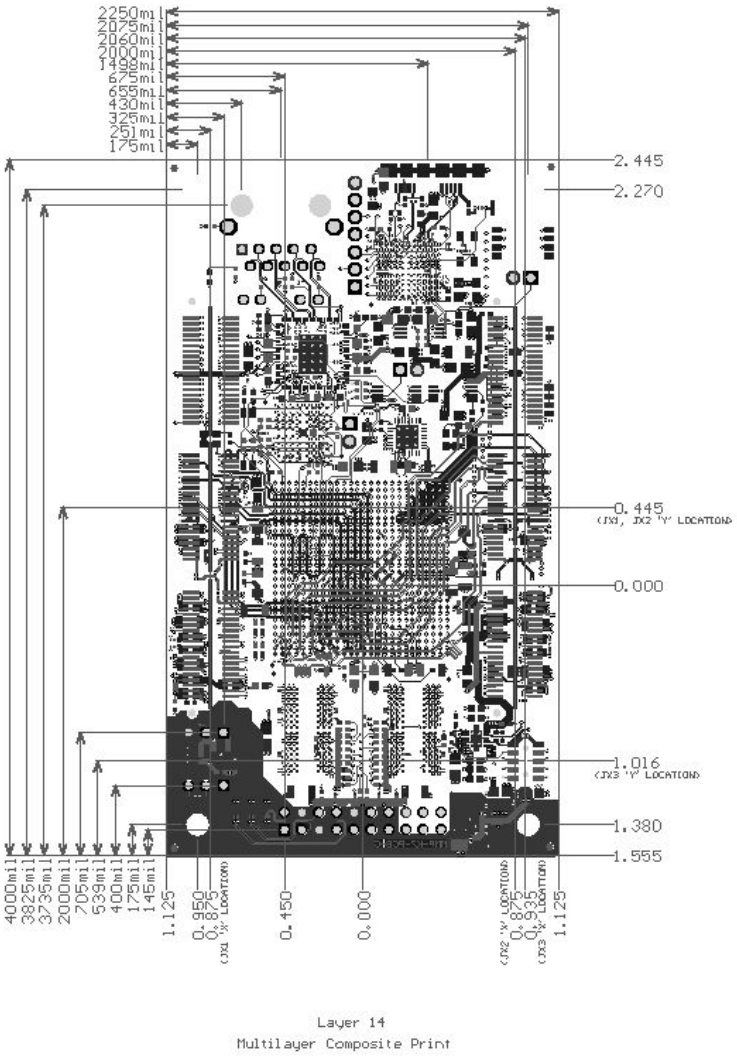


Figure 47 – Kintex-7 MMP Mechanical Drawing

3.2 Baseboard Mechanical

A mechanical diagram of the Avnet Mini-Module Plus Baseboard 2 is shown.

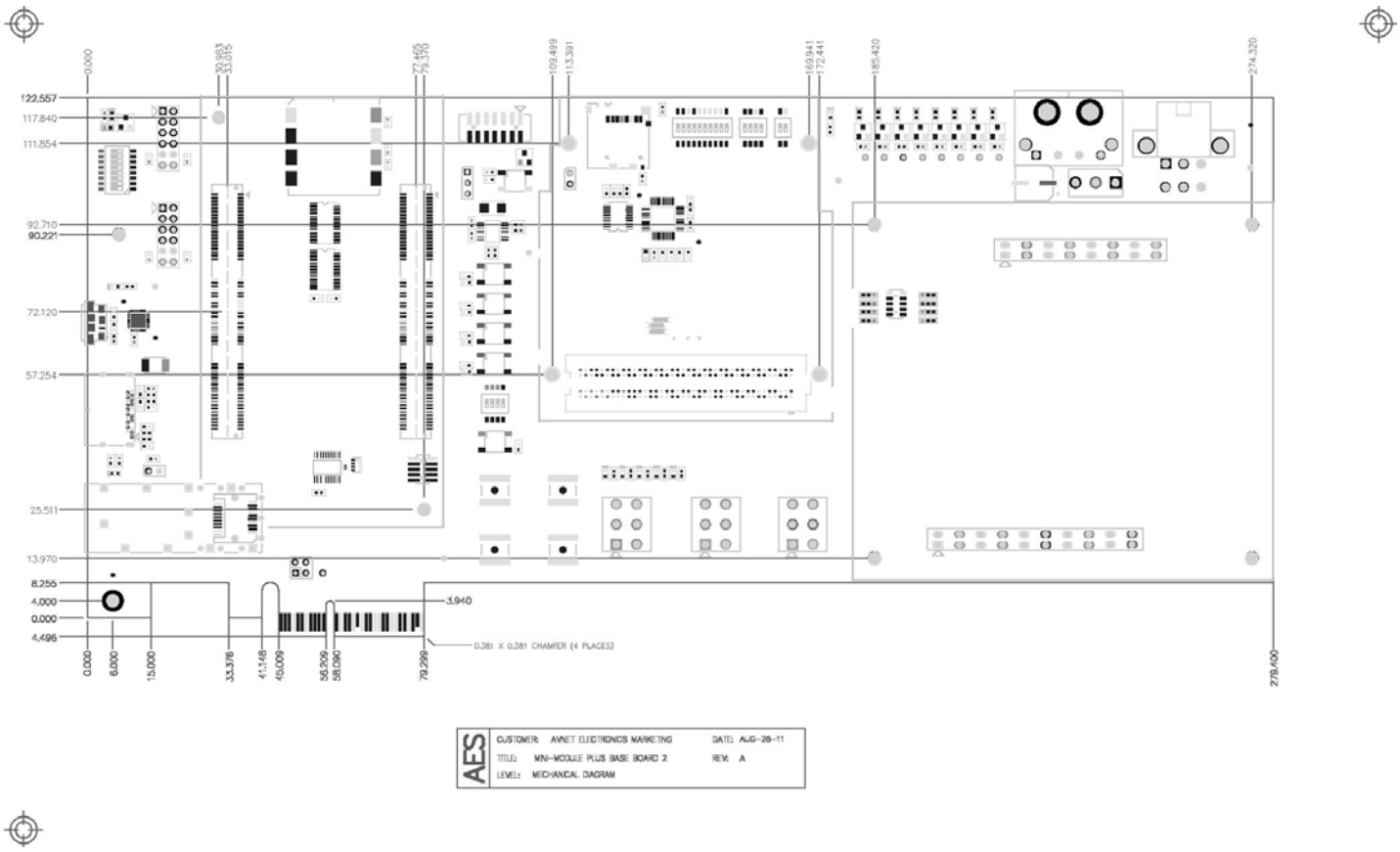


Figure 48 – Avnet Mini-Module Plus Baseboard 2 Mechanical Diagram

3.3 Power Module Mechanical

The Power Module meets the following geometry requirements:

Max Component Height	0.4”
Max Board Width	3.5”
Max Board Length	5.5”
Clearance Between Mated Boards (power module and baseboard)	0.45”

Table 57 – Power Module Geometry

The component height requirement is for both sides of the board, meaning dual side population is acceptable. Along with meeting these geometry requirements, headers J1, J2, and J3 must be placed on the bottom of the board according to the definition below:

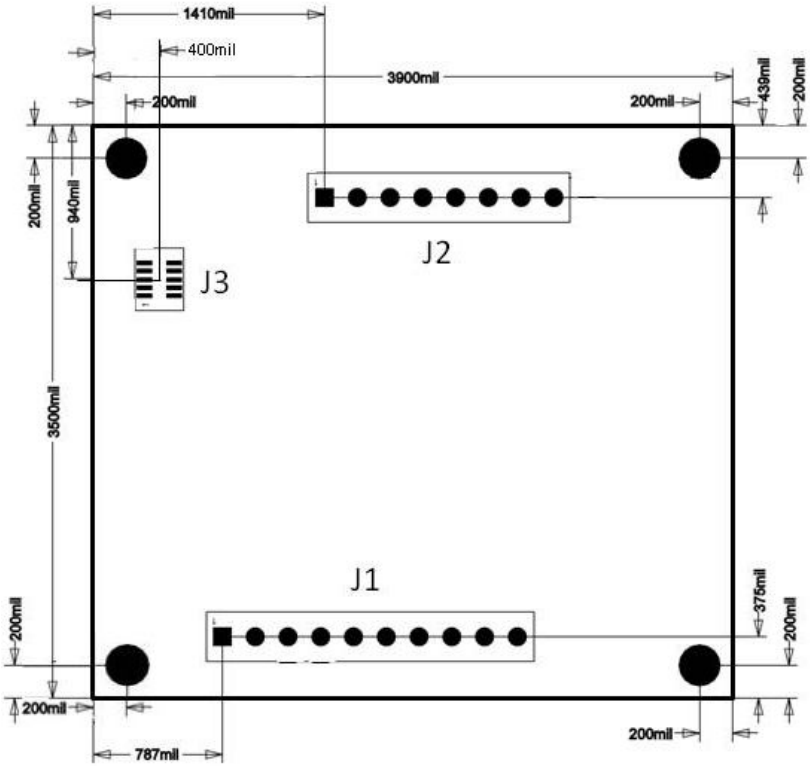


Figure 49 – Power Module Mechanical Header and Mounting Hole Locations

These locations are based on a topside view looking through the board. The headers should be placed on the bottom. J3 is measured to the center of the connector. The right side of the board can grow up to 5500mils if necessary, however all header locations and mounting holes must remain fixed. The mounting holes should be plated through holes with a 125mil diameter. The mounting holes should not be electrically connected on the module.

4 Revisions

Date	Version	Revision
20 June 2012	1.0	Release
23 October 2012	1.1	Added heat sink info (2.1.13) and Cypress EEPROM programming info (2.1.6.1)
5 September 2013	1.2	Corrected table 41 for FMC1_LA10_P/N pin numbers
7 January 2015	1.3	- Corrected SW7 statement in Section 1.1 (now SW6) - Added clarification and illustrations for removal of SW13 and SW14 in Section 2.2.10

5 Acknowledgements

Avnet would like to acknowledge the following key partners for their key contributions to this project.

Texas Instruments (**www.ti.com/xilinxfpga**)
- Clock PLL
- Power Management Unit for voltage regulation

Micron
- Multi-I/O SPI Flash
- LPDDR Memory

Tyco
- RJ45 connector
- USB-A connector
- Micro-B USB connector
- DIP switch
- Push buttons
- USB Protection for electro-static discharge and over-voltage

Xilinx
- Spartan-6 FPGA
  - **www.xilinx.com/spartan6**
- Xilinx ISE® Design Suite (IDS) 12.4 DVD WebPACK edition
- ChipScope™ Pro and SDK license voucher (device-locked to XC6SLX9)

Programmable Logic
Xilinx
Actel
Lattice

Logic
TI
ST
Fairchild

Analog Converters
TI
ADI

Analog Power
TI
National
ST

Analog Power Modules
Emerson
TI

Connectors
Tyco
Molex
FCI

Passive - Resistors
Vishay
Panasonic
NIC
Bourns (arrays)

Passive - Capacitors
AVX
Kemet

Passive - Timing
Fox

Electromechanical - switches
Tyco

Electomagnetics - Magnetics

Pulse

Discretes

OnSemi
ST
NXP

Optoelectronics

Avago
Everlight

Memory - DRAM

Micron
Samsung

Communication - USB

Cypress
TI

Memory Flash

Numonix
Spansion

Communication - Ethernet

National
Broadcom

6 Getting Help and Support

The Kintex-7 Mini Module Plus home page with Documentation and Reference Designs is located at:

Xilinx Kintex-7 FPGA Mini-Module Plus

Additional support is located at:

Design Resource Center

Mini-Module Plus Development Kit Supporting the Kintex-7 FPGA Family

Xilinx Kintex-7 FPGA Mini-Module Plus

Mini-Module Plus Baseboard 2

Analog Devices Power Module

GE Energy Power Module

Maxim Power Module

STMicroelectronics Power Module

Texas Instruments Power Module

Texas Instruments SIMPLE SWITCHER® Power Module

The Avnet Kintex-7 Mini Module Plus forum:

http://community.em.avnet.com/t5/Avnet-Development-Boards/ct-p/Avtbds

For Xilinx technical support, you may contact Xilinx Online Technical Support at www.support.xilinx.com.

On this site you will also find the following resources for assistance:

- Software, IP, and Documentation Updates
- Access to Technical Support Web Tools
- Searchable Answer Database with Over 4,000 Solutions
- User Forums
- Training - Select instructor-led classes and recorded e-learning options

Contact Avnet Support for any questions regarding the Kintex-7 Mini Module Plus reference designs or kit hardware:

http://www.em.avnet.com/techsupport

You can also contact your local Avnet/Silica FAE.

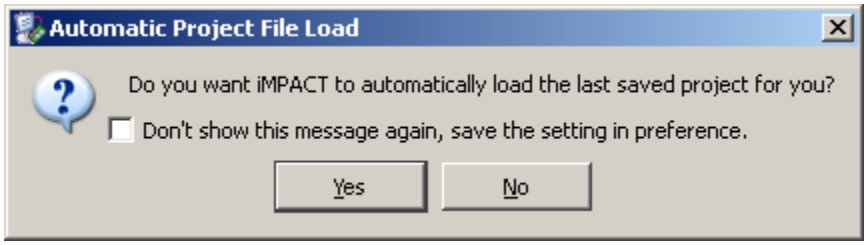
7 Appendix

7.1 How to Create an MCS file and Program the Flash using Impact

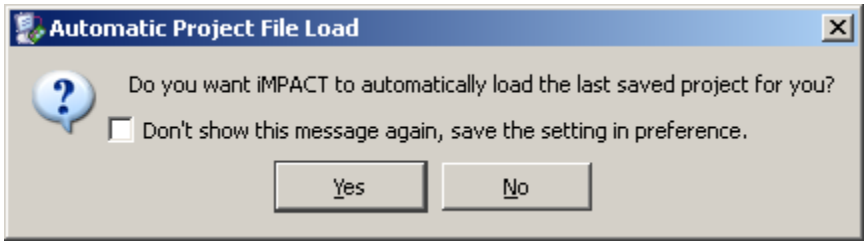
The following steps describe how to create an MCS file from a project BIT file, and then load that MCS file to Flash. This example uses iMPACT 13.4 and the K7_MMP_PCIeEndpoint_Gen2.bit file.

1) Start Impact:
   a. Start -> Impact -> Xilinx ISE Design Suite 13.4 -> ISE Design Tools -> Tools -> iMPACT
   b. Impact launches using a shell and takes a few seconds for the Application to start

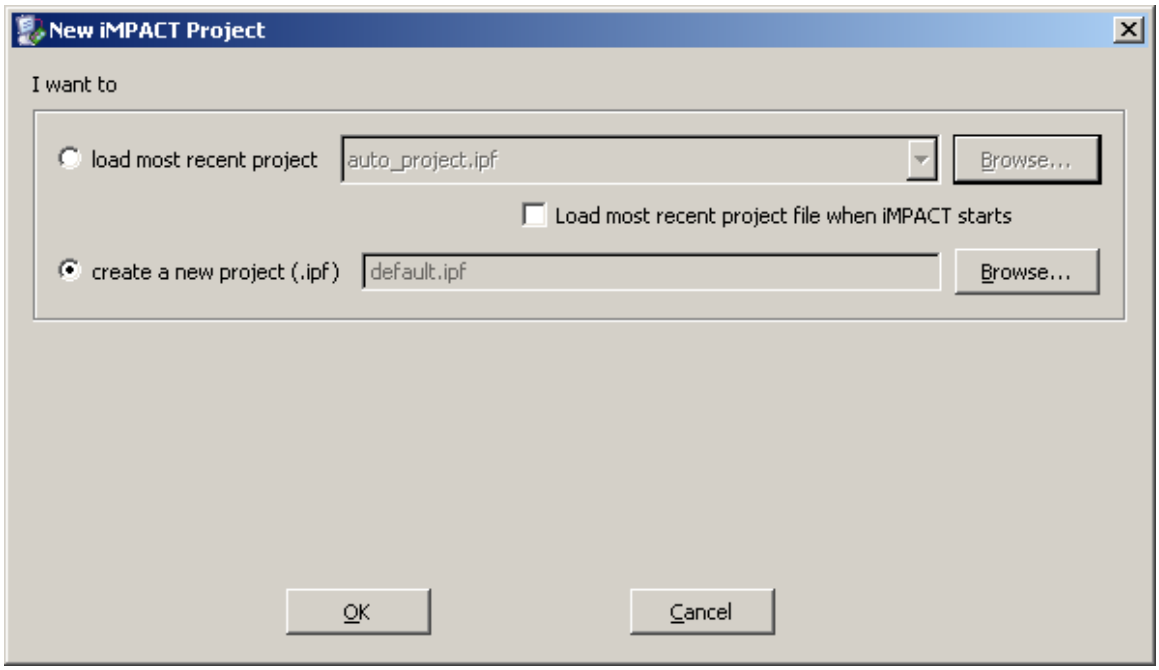
2) An initial project screen will appear, select No.



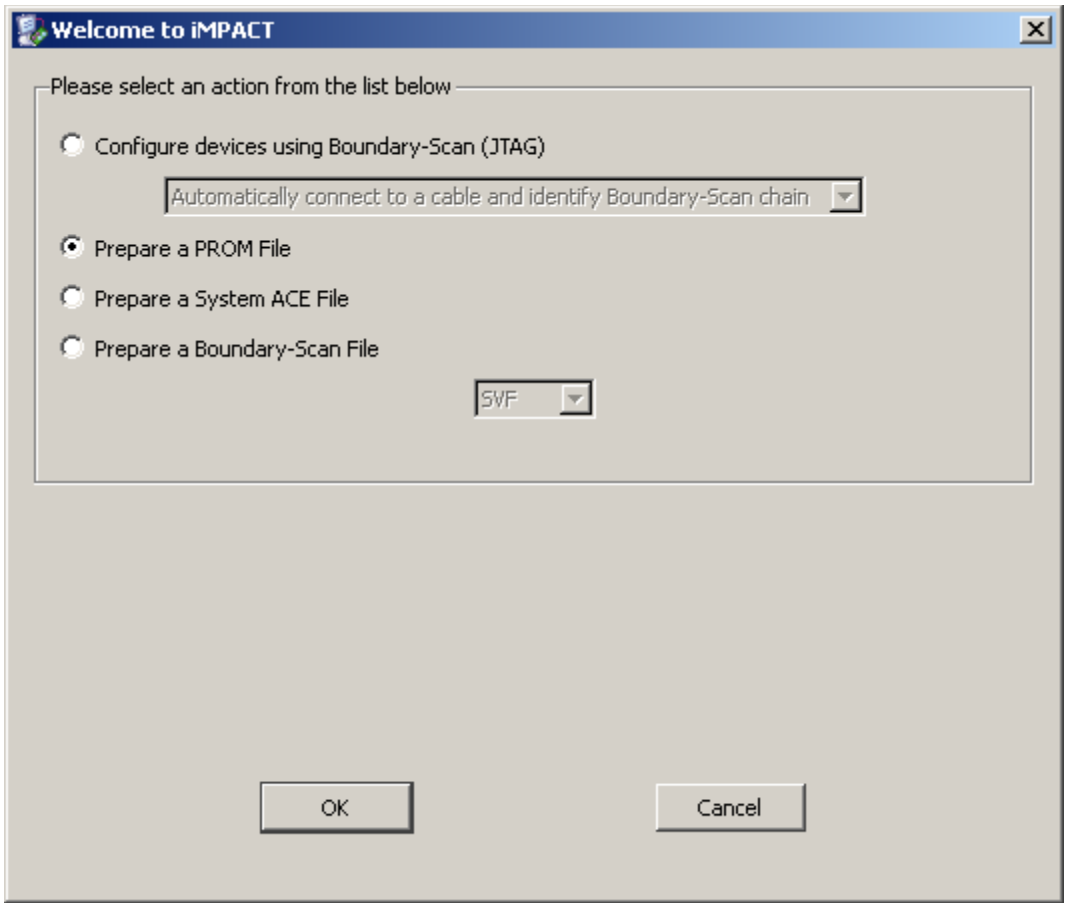
3) A second project screen will appear, select No.



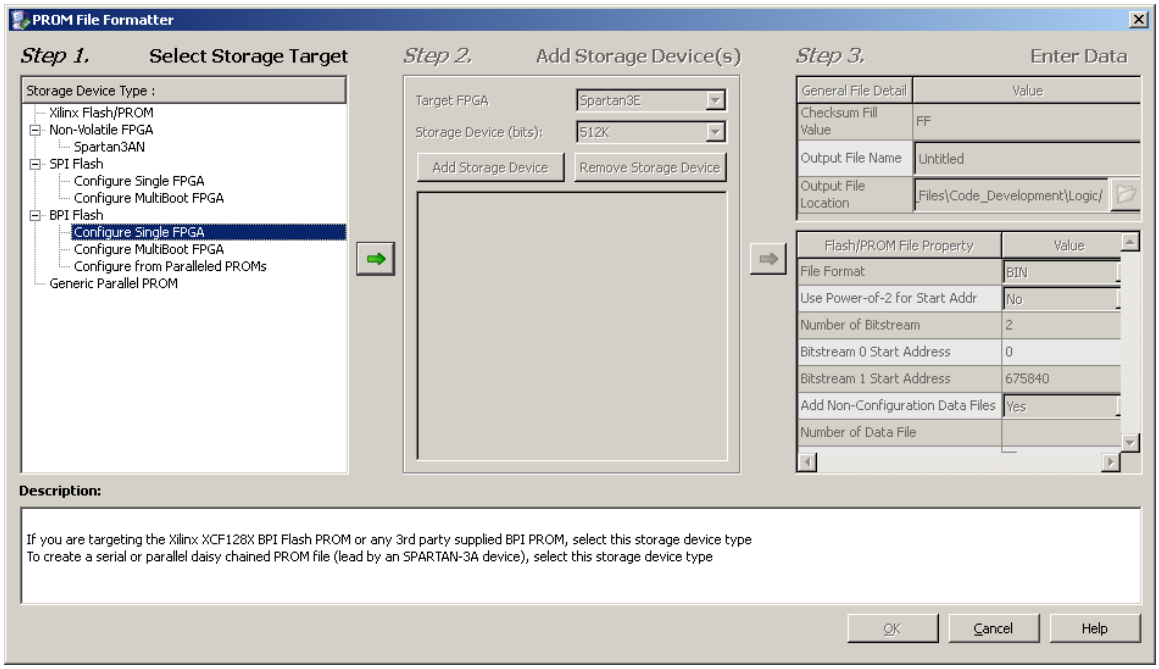
4) A third project screen will appear, select “create”, then “OK”.



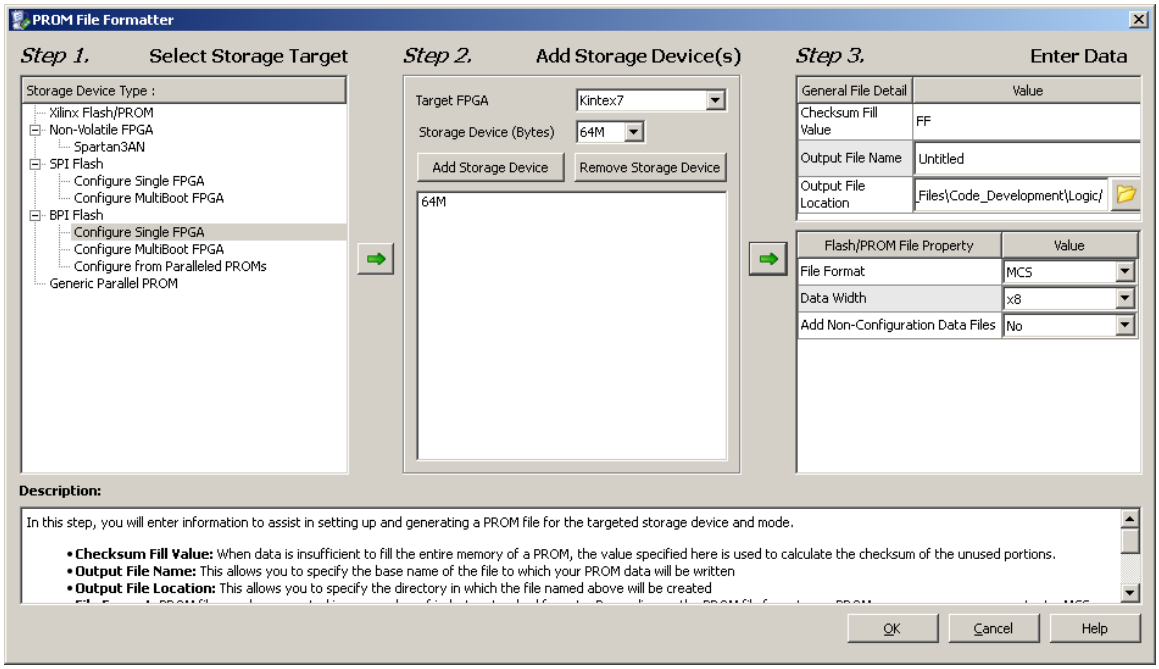
5) A welcome screen will appear, select “Prepare a PROM File”, then “OK”



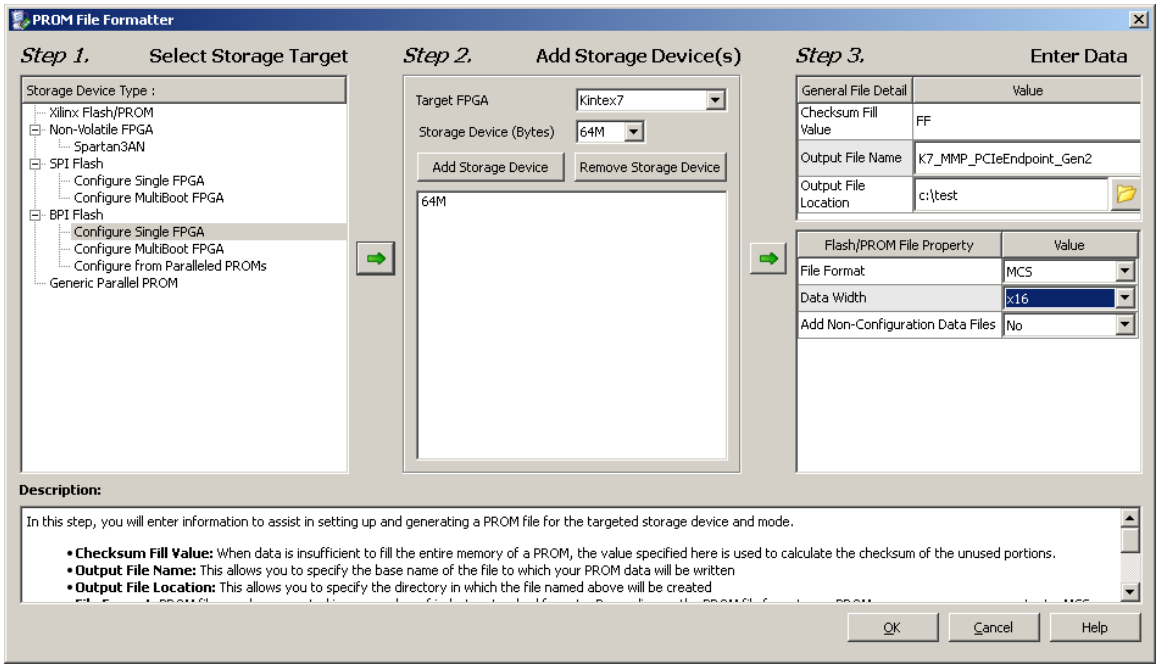
6) A PROM File Formatter Screen will appear. Select under Step 1, “BPI Flash” – “Configure Single FPGA” then select the first arrow.



7) Continue with the PROM File Formatter Screen. Select under Step 2, Target FPGA “Kintex7”, Storage Device “64M”, “Add Storage Device”, then select the second arrow.

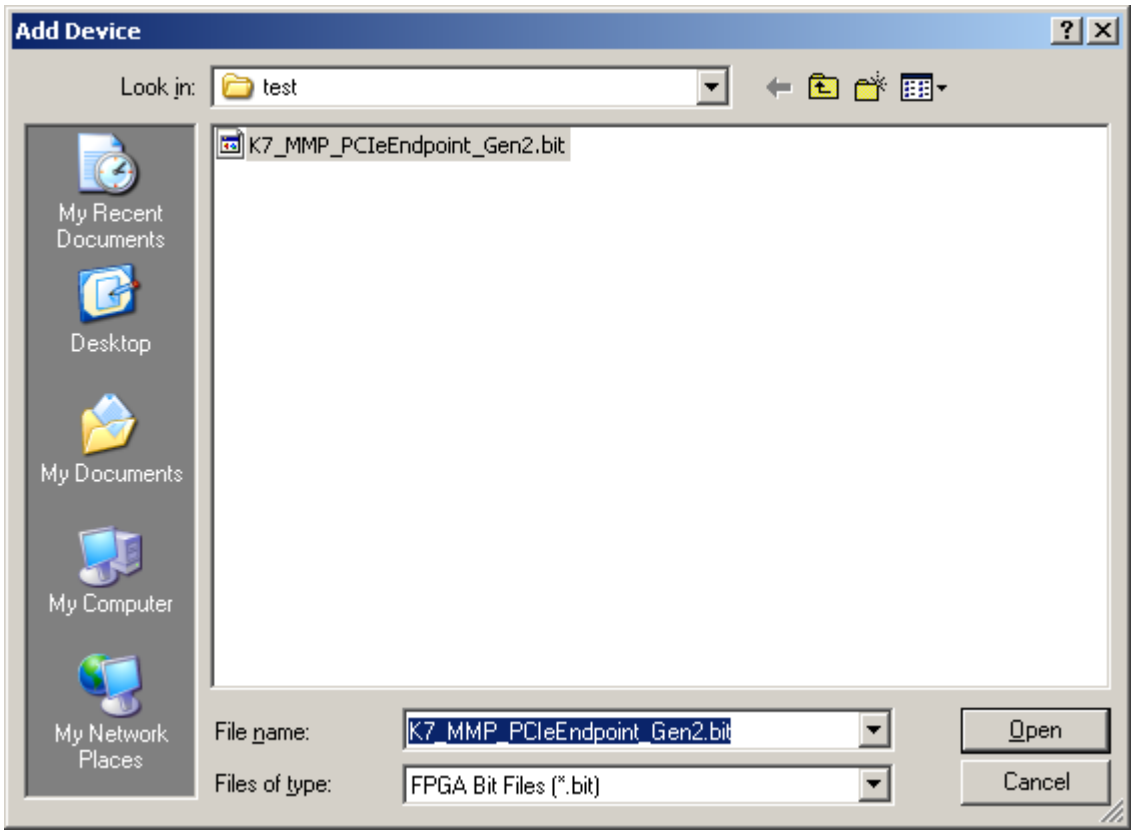


8) Continue with the PROM File Formatter Screen. Select under Step 3, Checksum fill value “FF”, an output file name and location, for this example choose the bit file name K7_MMP_PCIeEndpoint_Gen2, and an output file location c:\test. Choose a File Format “MCS”, Data Width “x16”, and Add Non-Configuration Data Files “No”. Then Press “OK”.

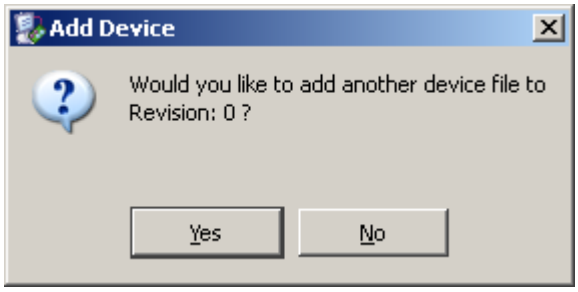


9) A new screen will appear with a prompt to “Add Device”, select “OK”

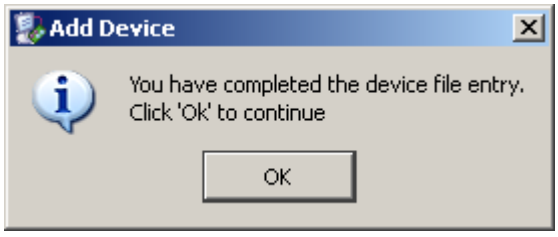
10) Navigate to and open the K7_MMP_PCIeEndpoint_Gen2.bit file



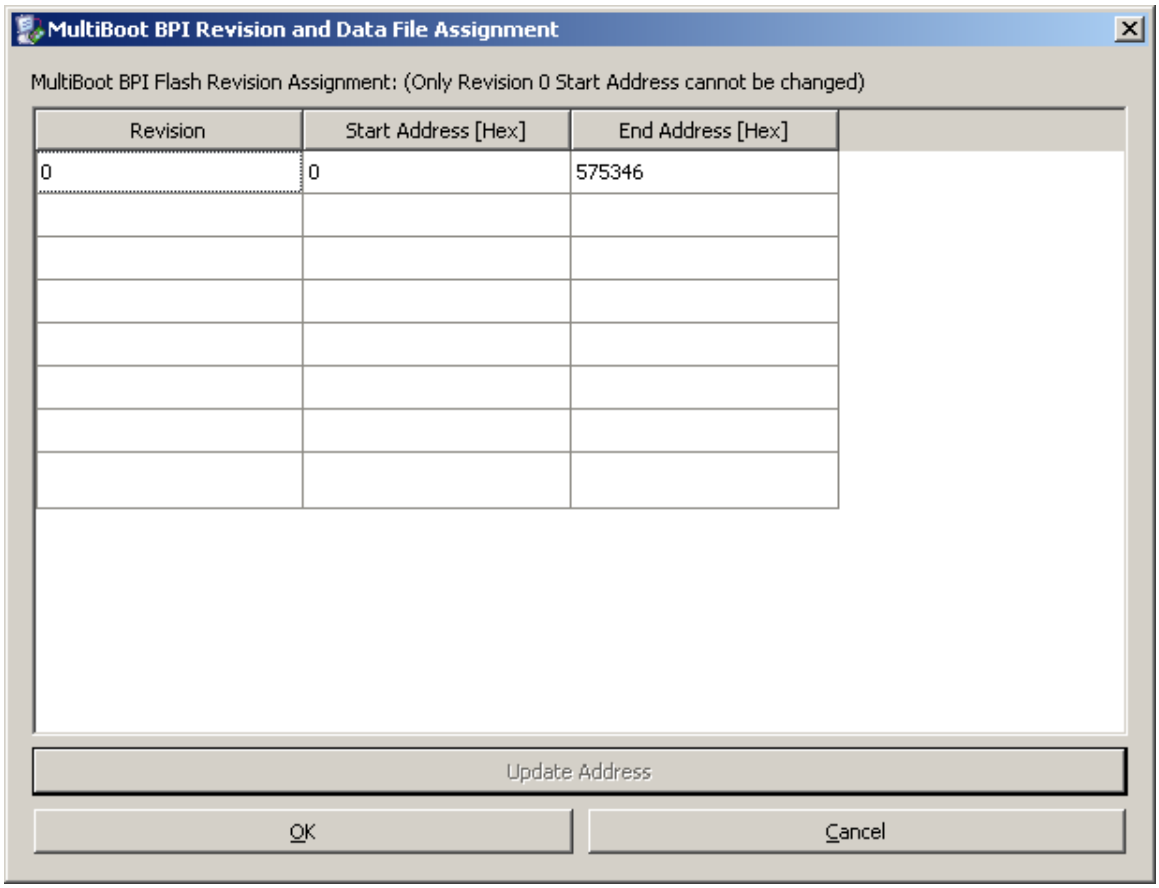
11) After a few seconds, a small screen will appear asking if you would like to add another device file, select "No":



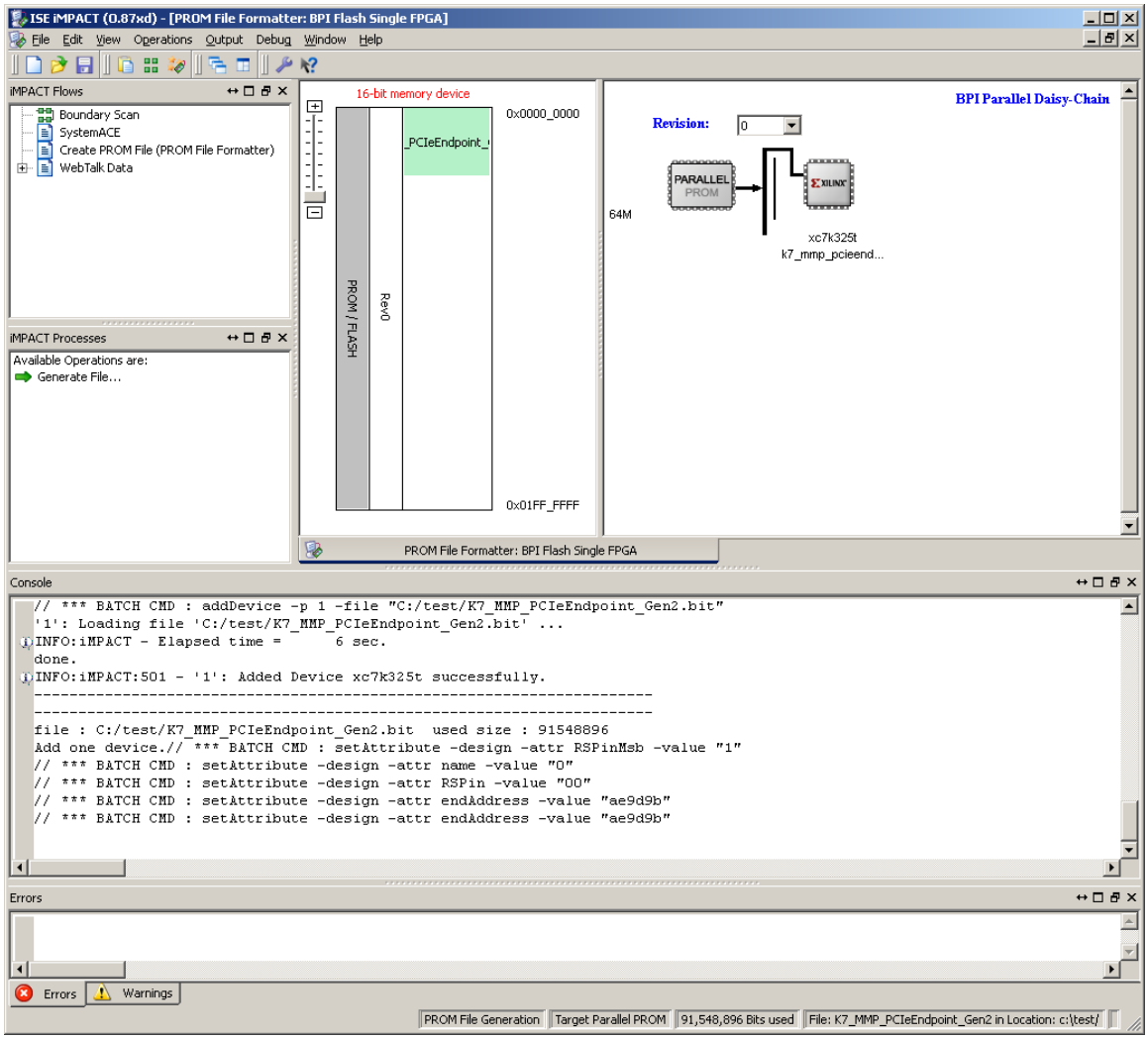
12) A small notification screen will appear, "You have completed the device file entry", select OK:



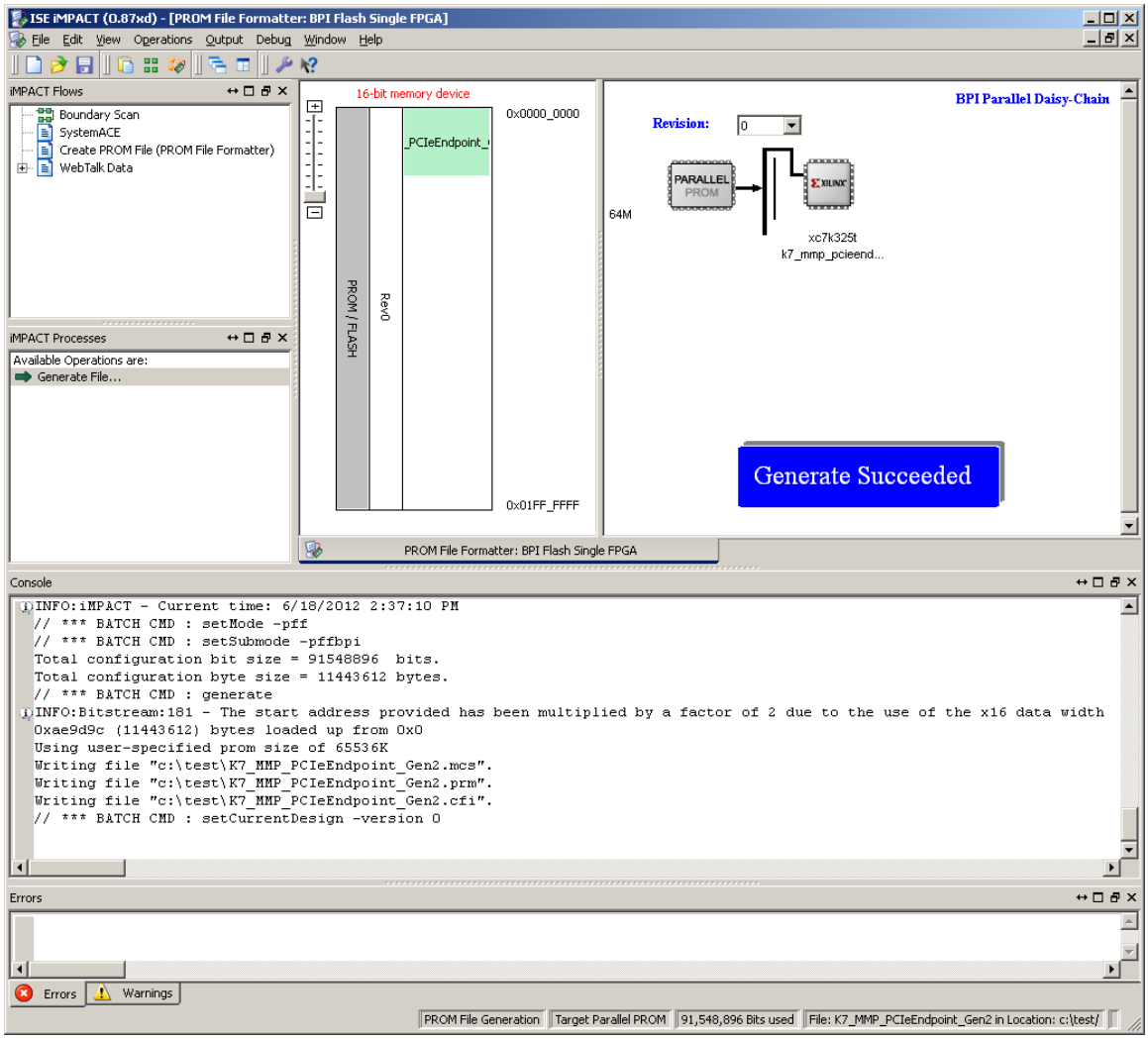
13) A data file assignment map will appear, select OK:



14) After the data file assignment map goes away, select (under iMPACT Processes on the left half way down) “Generate File”



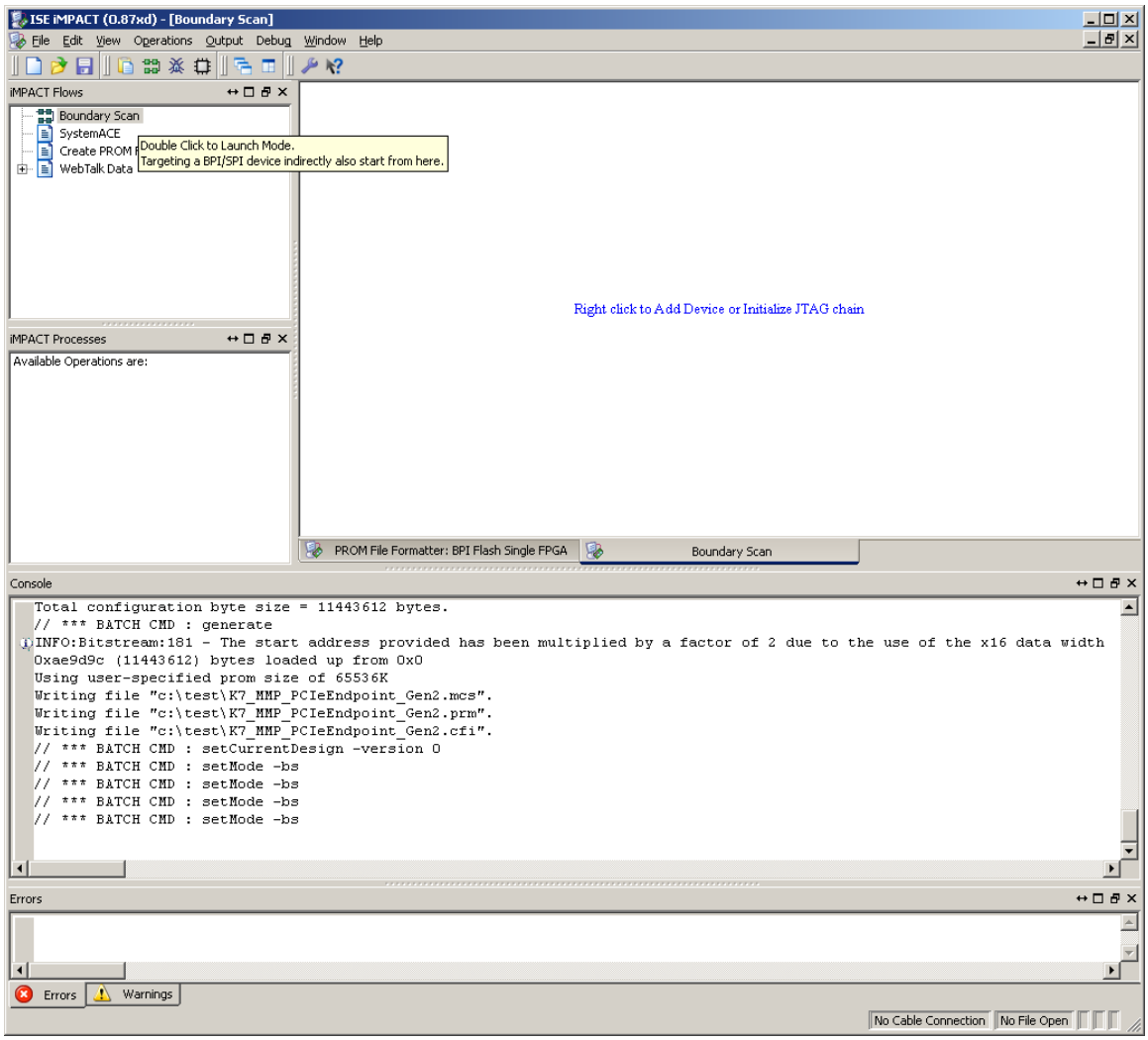
15) After several seconds the screen should indicate “Generate Succeeded”



16) Make sure the Digilent USB programming cable is attached between Baseboard U1 and the PC Host.

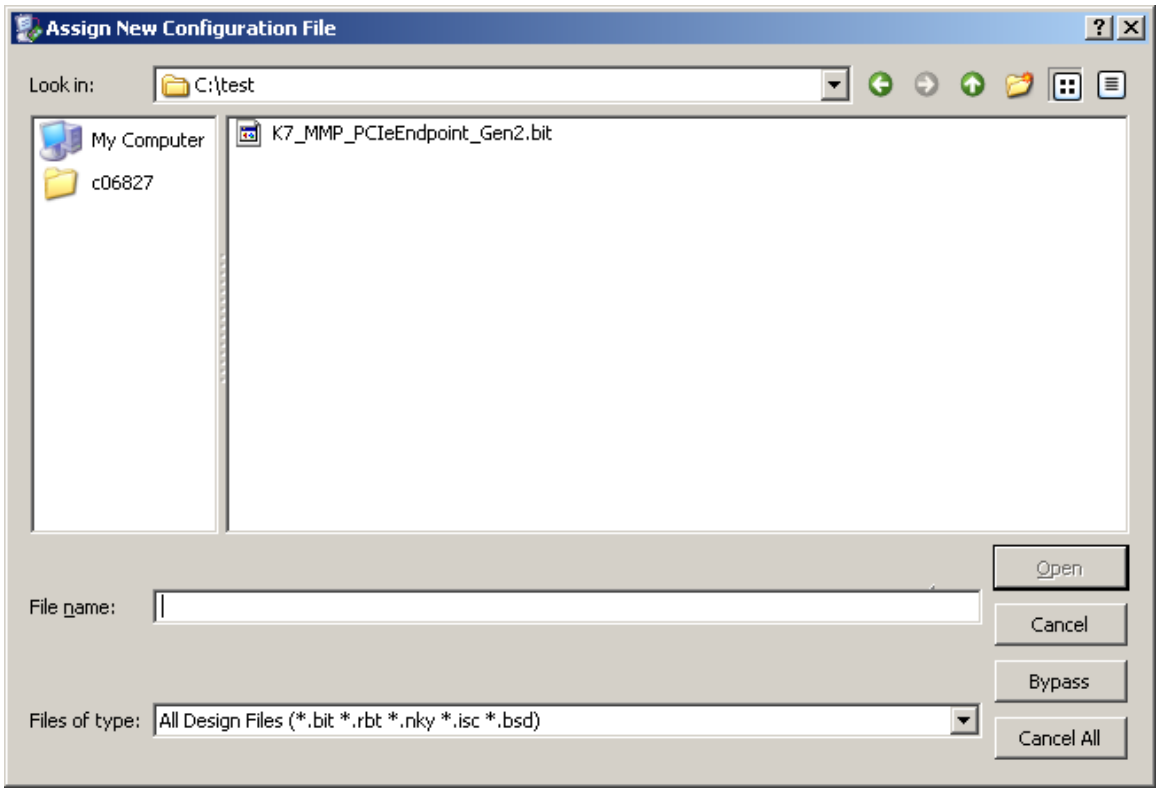
17) Make sure power is applied to the boards (All the power LED’s D3-10 should be lit).

18) Under “iMPACT Flows” select “Boundary Scan”.

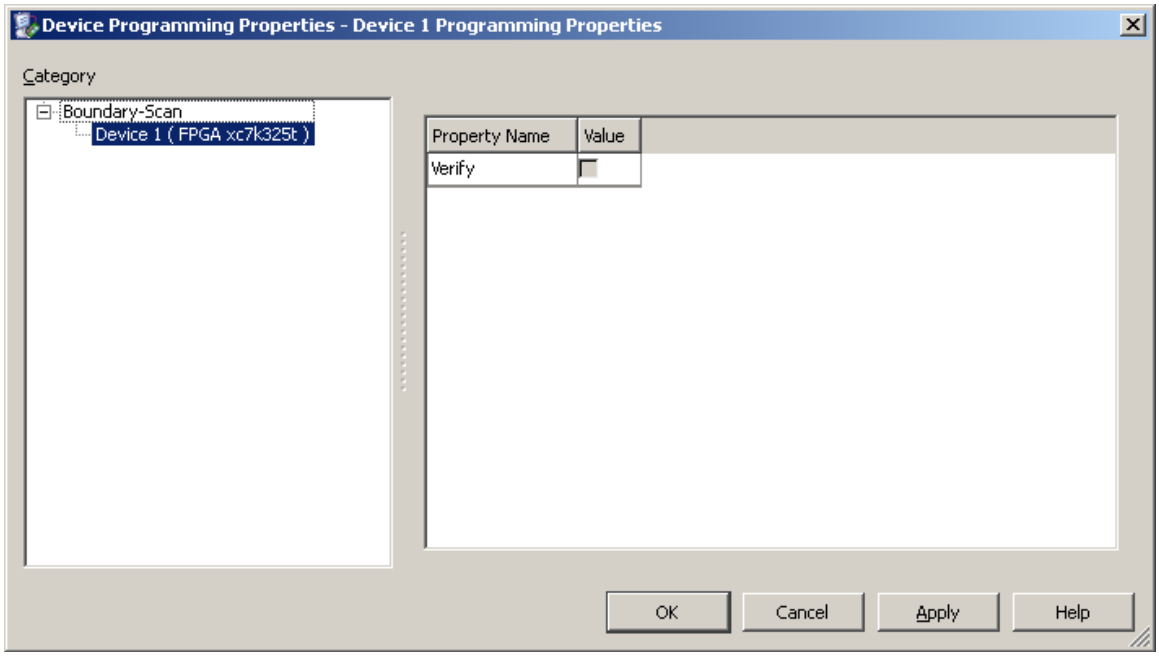


19) Right Click in the window where indicated, select “Initialize Chain”

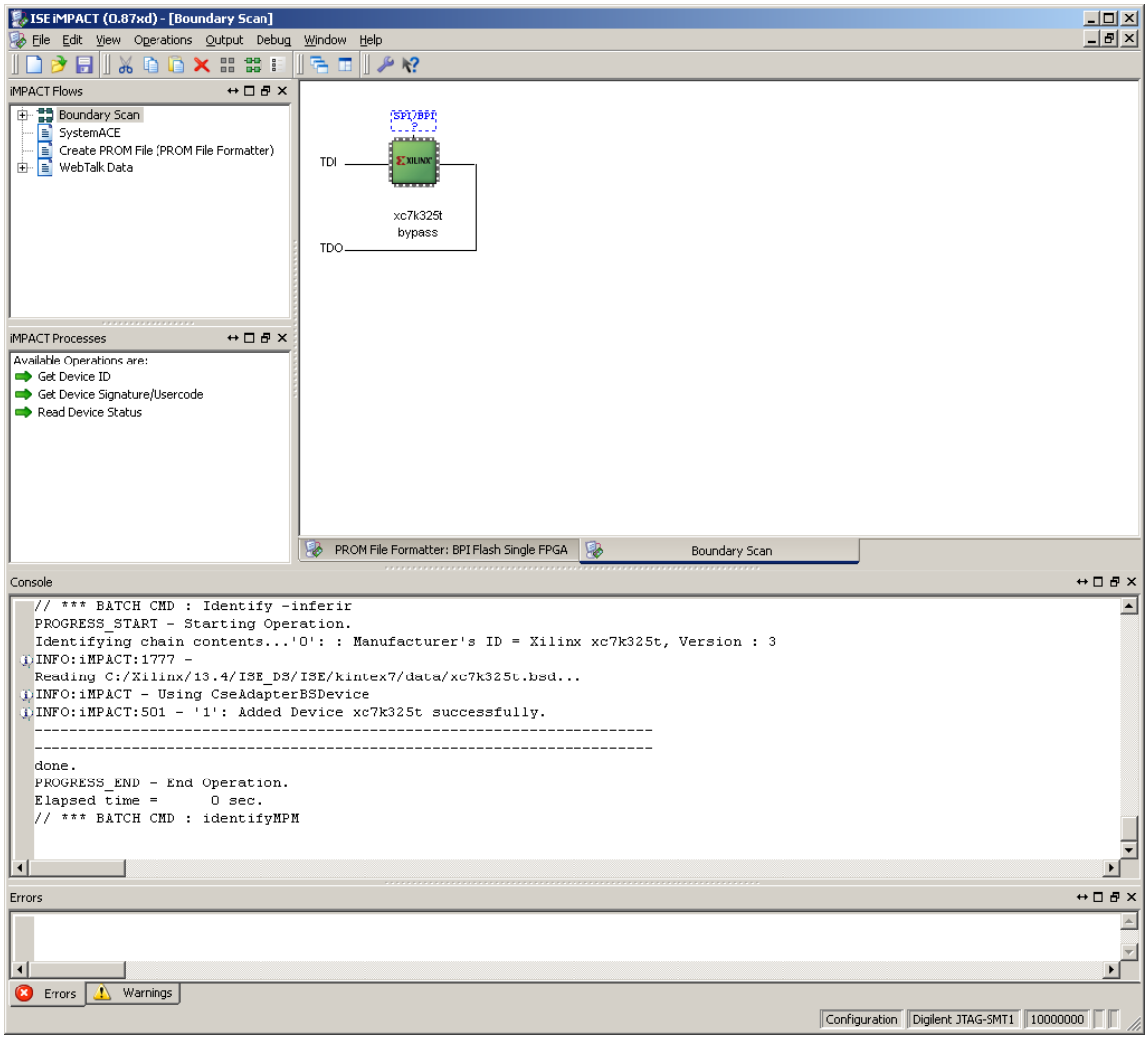
19) An assign configuration file window will appear, select “Bypass”

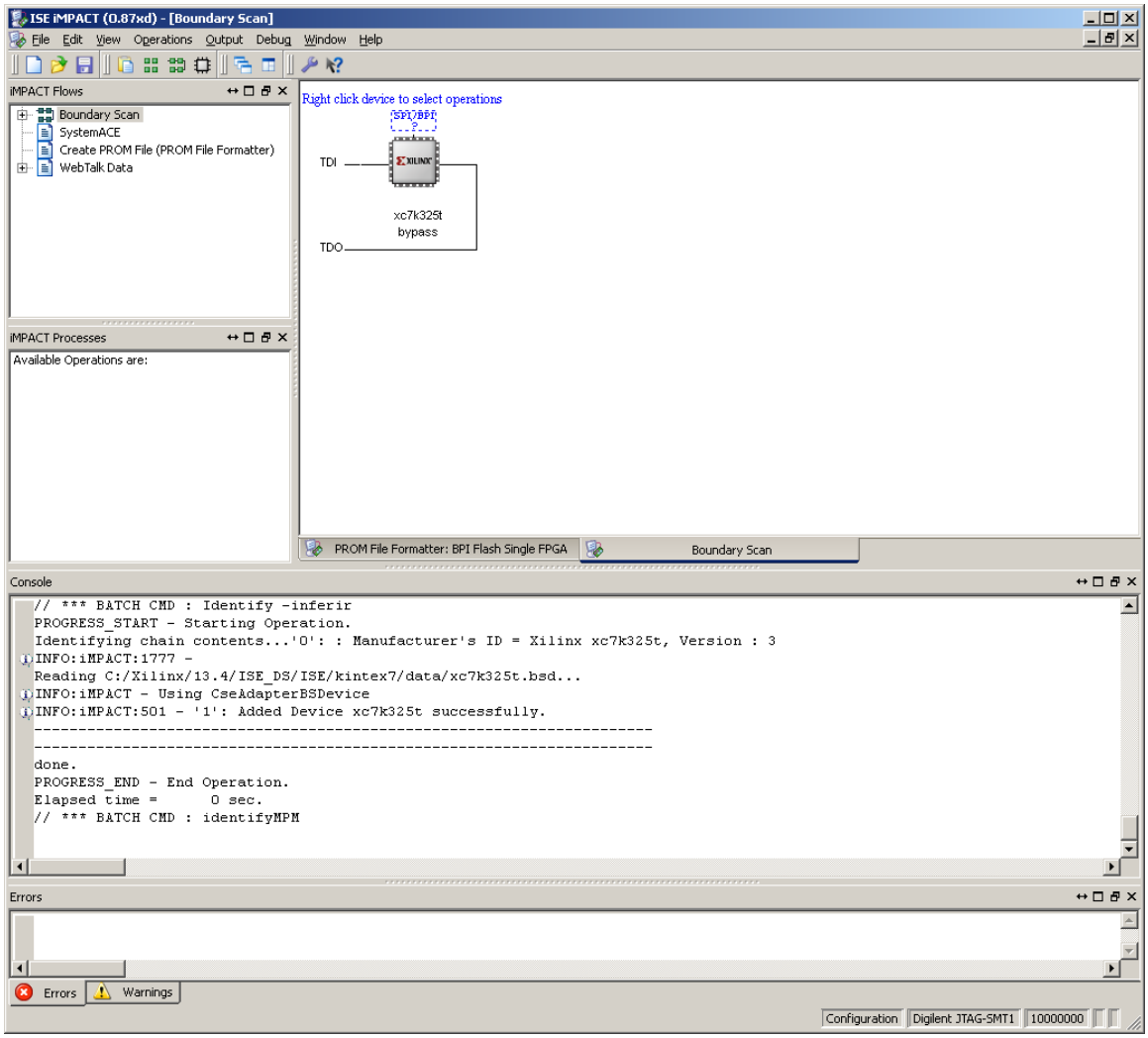


19) A device programming properties window will appear, select OK



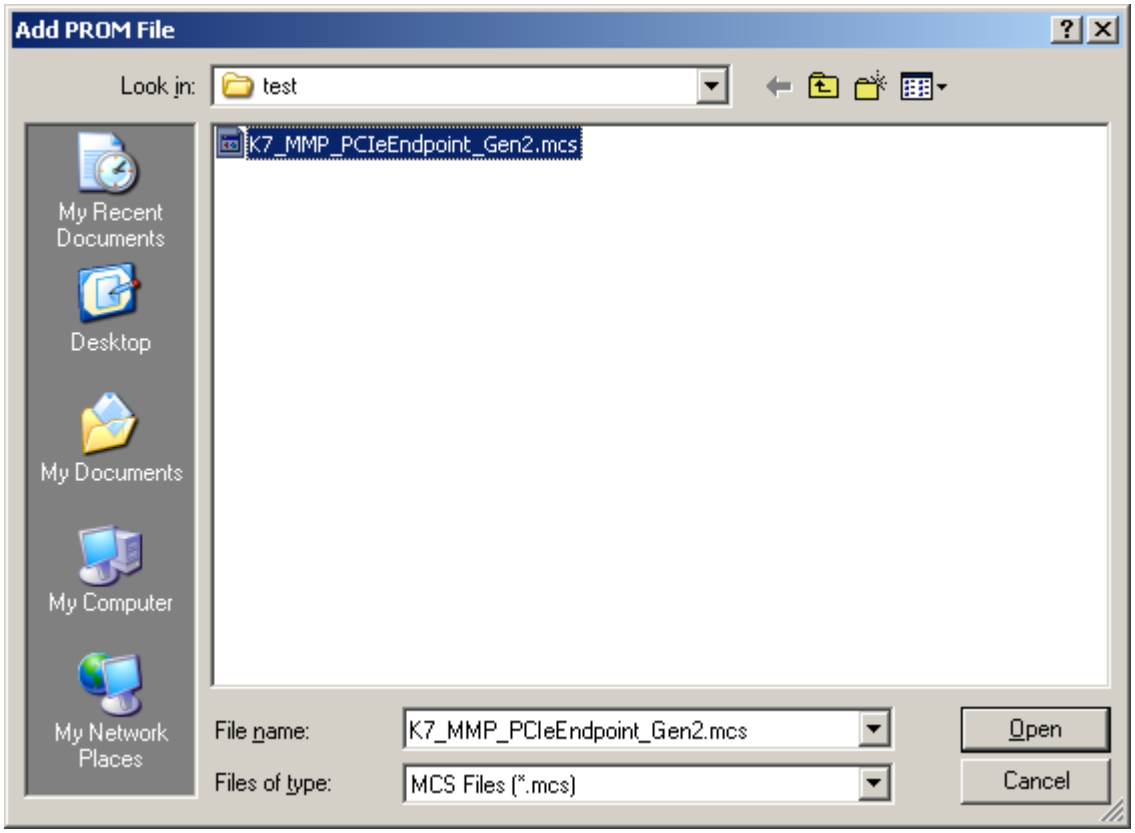
19) The iMPACT window should now show the FPGA with a dotted line box for the BPI Flash. Click the box so the FPGA is no longer hi-lighted green. Right click on this dotted box.



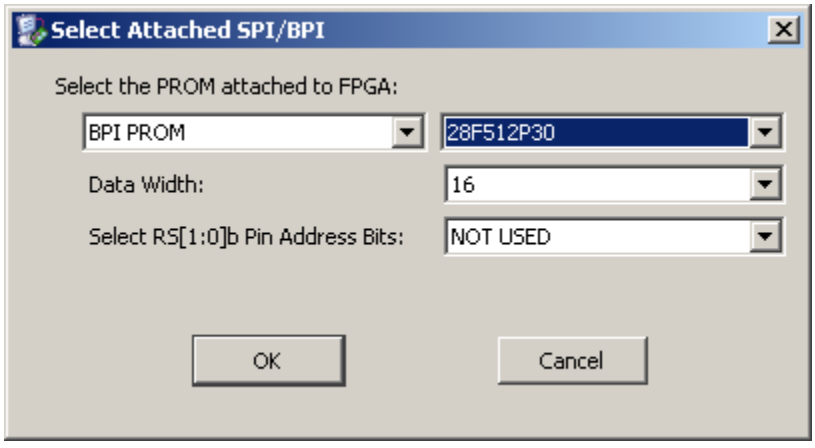


20) A small box will appear Add SPI/BPI Flash… Click on the box.

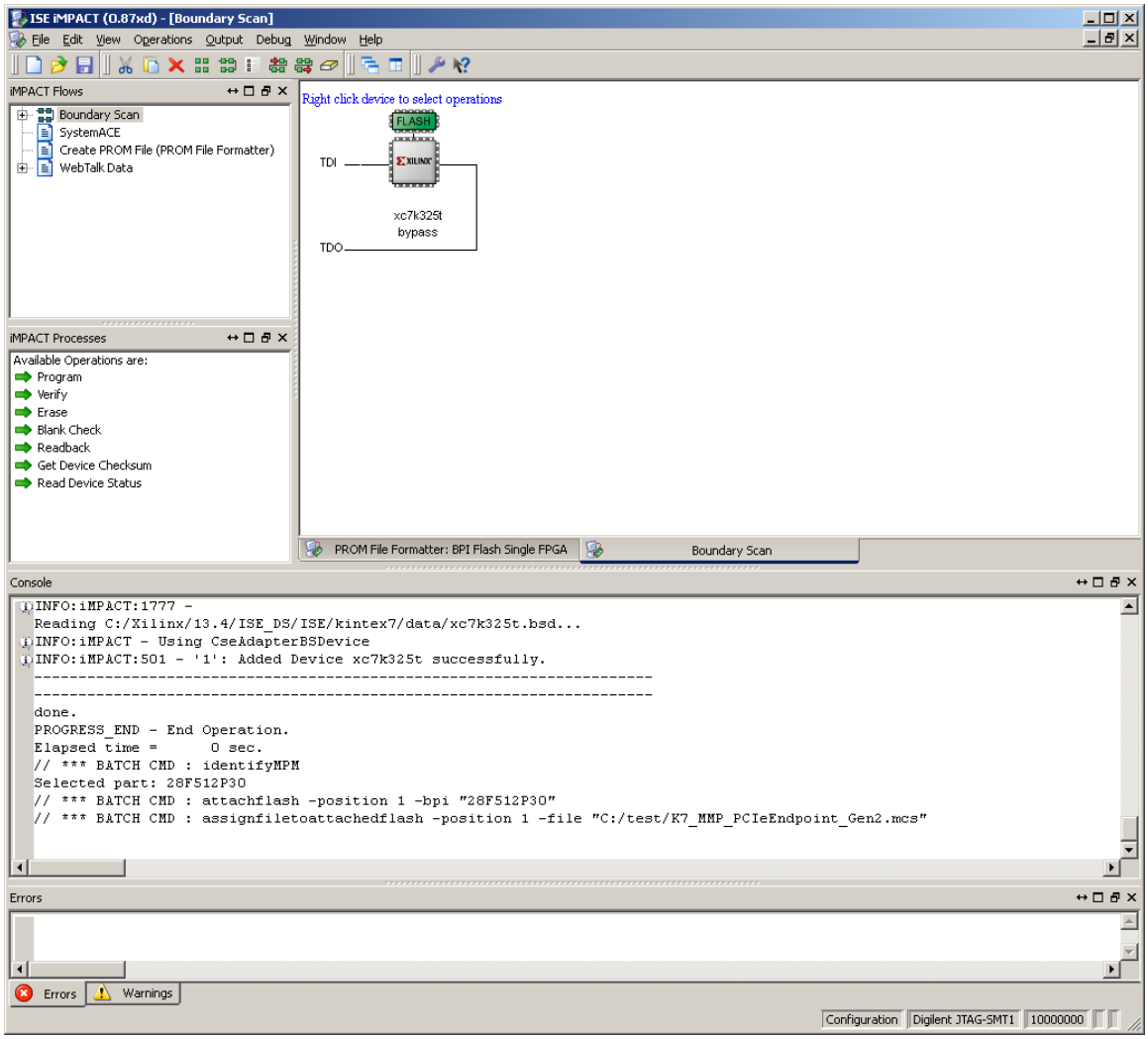
21) An Add PROM File window will appear. Navigate to the output file location entered previously and open the K7_MMP_PCIeEndpoint_Gen2.mcs file.



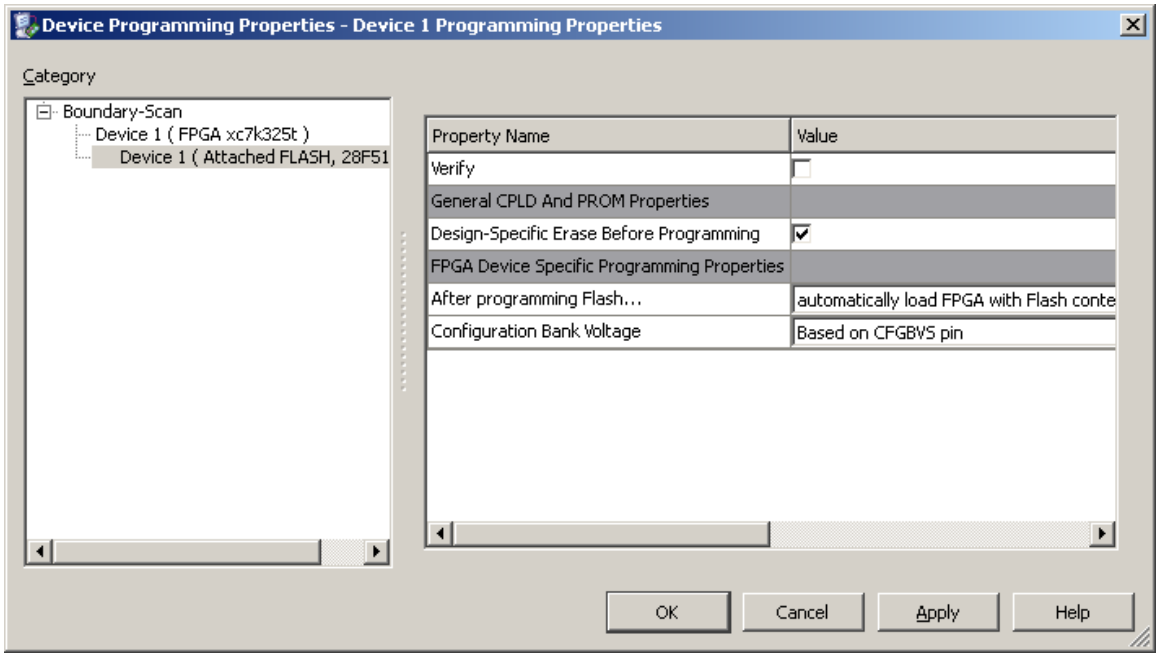
21) A select attached SPI/BPI file window will appear. Select the PROM attached to the FPGA. Select BPI PROM, 28F512P30, Data Width 16, and RS[1:0]b Not Used.
Select OK.



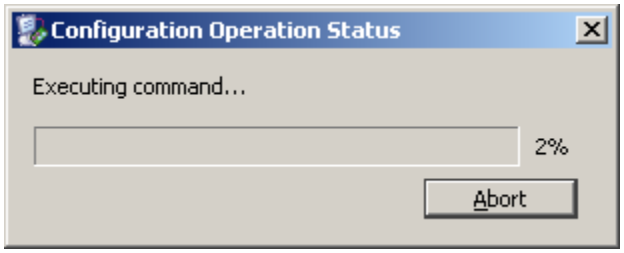
22) The Flash can now be highlighted:

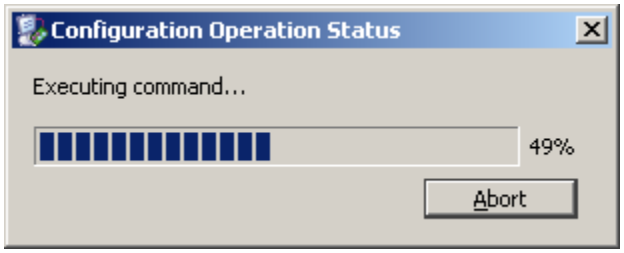


23) Right Click the Flash and select Program. A device programming screen will appear. De-select verify, select design specific erase, select OK.



24) A small Status screen will appear which will track Flash Programming:





25) After the Status reaches 50% the main window should indicate program succeeded!