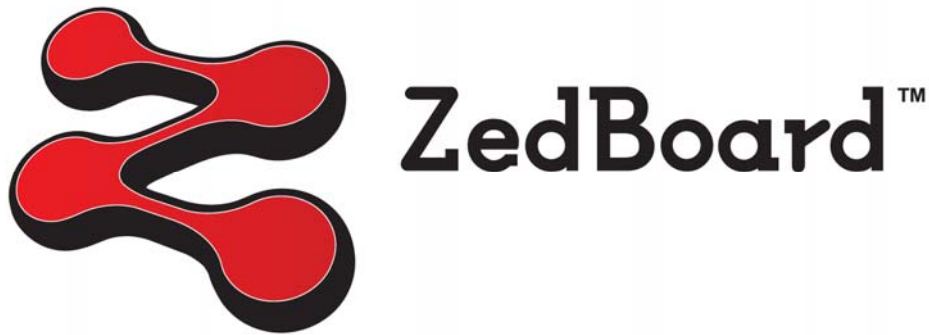


ZedBoard Power Distribution and Decoupling System



September 14, 2012

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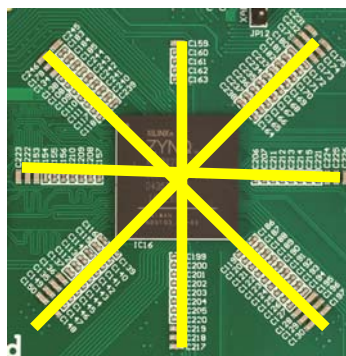
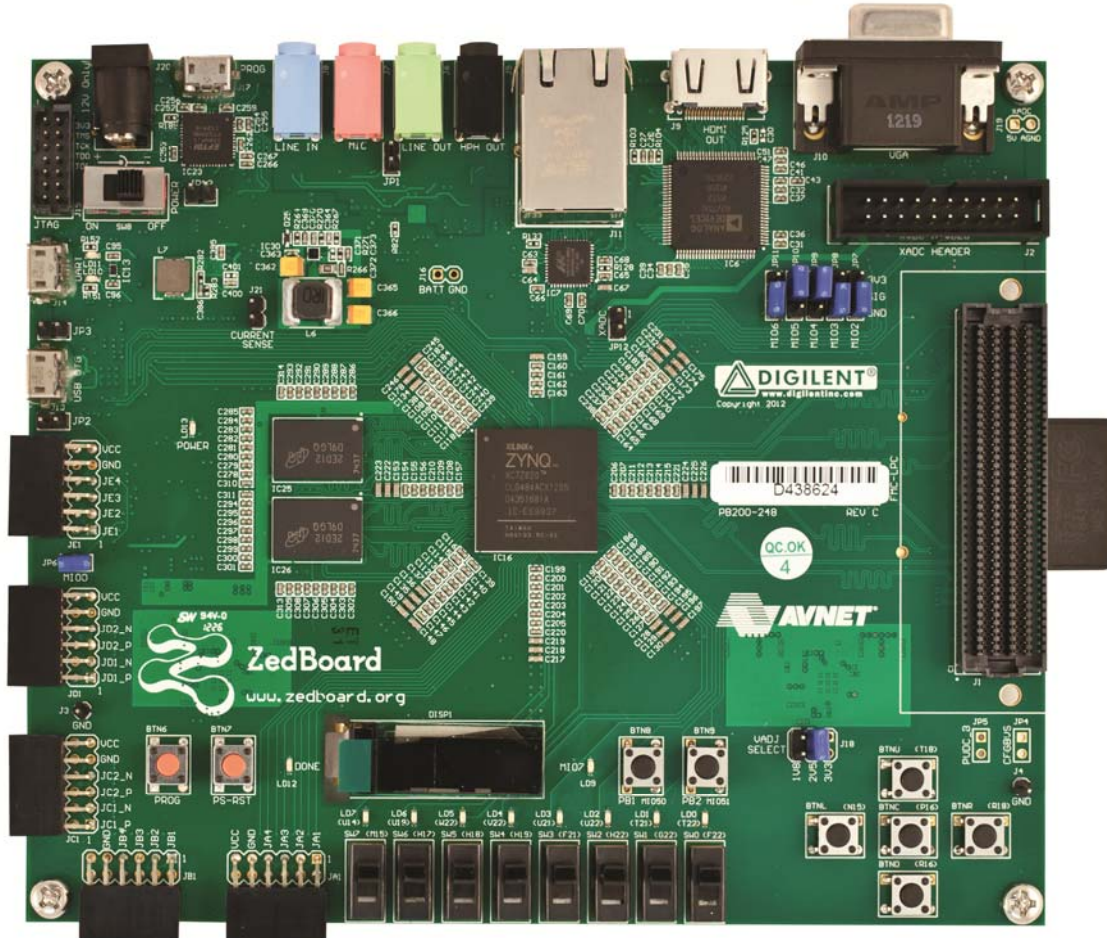
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Introduction

This document describes the design of the ZedBoard power distribution system in support of the Zynq-7000 All Programmable System on Chip device. A common observation when looking at the board is that the decoupling network ends up producing a star like pattern around the Zynq device. The perception is sometimes that this pattern was for appearance. This document will illustrate the design purpose behind the decoupling of the Zynq device.



Overview

The ZedBoard is designed to be a low cost development platform for the Zynq-7000 AP SoC device. Provided on the board are key peripherals to fully exercise the device and provide an adequate development and evaluation environment while maintaining an overall lower cost than platforms providing more expandability.

In order to achieve the lower price points, additional efforts had to be made up front to ensure that low cost measures implemented on the board would not cause performance issues in the system.

A common reaction to seeing the board is that the decoupling network around the Zynq device looks like a deliberate star pattern. While this pattern for component placement was intentional, it was for function, not form. This document focuses on the low cost implementations surrounding the power system, which includes the decoupling network.

Reference Design Requirements

The requirements for the power system were focused on providing adequate power to the system in a small footprint, low cost solution. In addition to regulator and component cost, a large cost adder that often gets overlooked during the design process is the cost of a higher layer count PCB. The cost of the PCB is critical since in most cases, even if a board is redesigned for cost reduction reasons, very rarely is the PCB stackup or layer count changed since it requires extensive redesign and in some cases a complete “do-over.”

In order to maximize your cost advantage, it’s important to choose a PCB stackup and layer count that provides the access and performance needed, while delivering the lowest layer count possible. For reference, each additional layer pair (going from 10-12, 12-14, etc) can result in a 25% cost increase for the PCB. The ZedBoard was designed to be a 10 layer board. In comparison, the ZC702 platform from Xilinx is a 16 layer board. One example that illustrates this cost increase is the calculator available online from Sanmina-SCI, which you can find in the appendix. This calculator allows you to change parameters of a PCB to show costs of changing different attributes. By only increasing the layer count and keeping all other variables the same, going from 10 to 16 layers results in a 69% PCB cost increase. While this example is specific to Sanmina-SCI, the relative cost increase is common among all PCB manufacturers.

The first priority of any design is that it meets the performance goals of the intended system. The challenge then becomes minimizing the costs to get there. Simulation and analysis must be done up front to minimize your initial risk, and validation testing must be done after boards have been built to ensure the actual board performs as expected.

Up Front Analysis

So how does all of this PCB talk relate to the “star” on ZedBoard? Designing a stack up requires defining signal and power planes, priority routing layers as well as plans for fanning out signals from BGA packages like the CLG484 package of the Zynq device on ZedBoard. Typically more layers are used to provide enough “break out” paths from underneath the BGA through vias. As discussed in the previous section, a goal of the ZedBoard design was to provide a low cost solution.

The fewer number of layers you have, the fewer planes you have for ground and power. Due to the lower layer count, dedicated layers for each voltage are not feasible. In this case, the power planes can be split with different floods for different voltages. These splits must be done carefully since signals crossing plane cuts can experience slight impedance changes and could pick up noise coupled from the different voltage floods.

The ZedBoard uses a 10-layer PCB with no blind or buried vias and 5-mil minimum spacing for trace width and separation. The stack-up of six signal layers alternating with power and ground planes is driven by cost and by signal impedance requirements.



ZedBoard Layer Stackup

Diagram 1 ZedBoard Layer Stackup

All six signal layers are densely routed, including the top and bottom layers. Power supply pins on the Zynq device are connected to power plane polygons on two layers that provide the required voltage. These polygons connect to Zynq supply pins and to bypass capacitors located beyond the edge or immediately under the Zynq device. The series of images below illustrate the plane floods and corresponding voltages for the two power planes on the ZedBoard.



Figure 1 – Power Plane one 1.8V Vccaux Flood

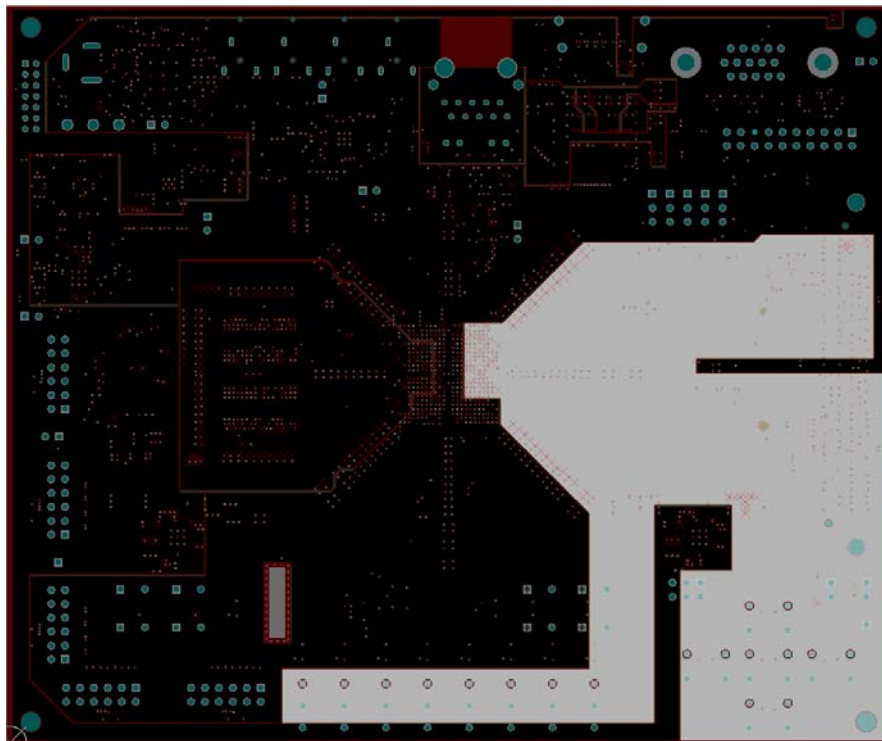


Figure 2 – Power Plane one Vadj Flood

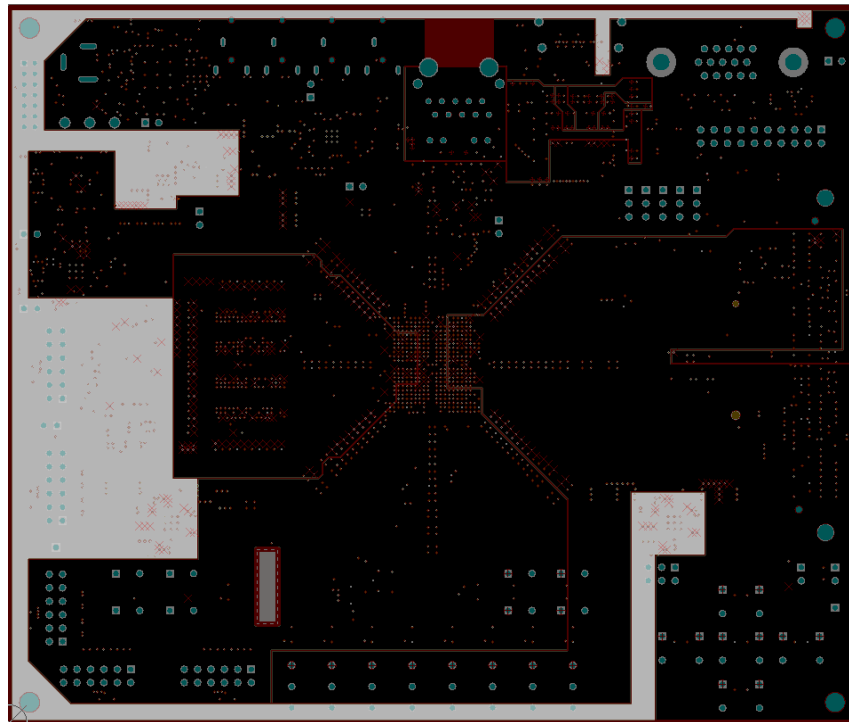


Figure 3 – Power Plane one 5V Flood

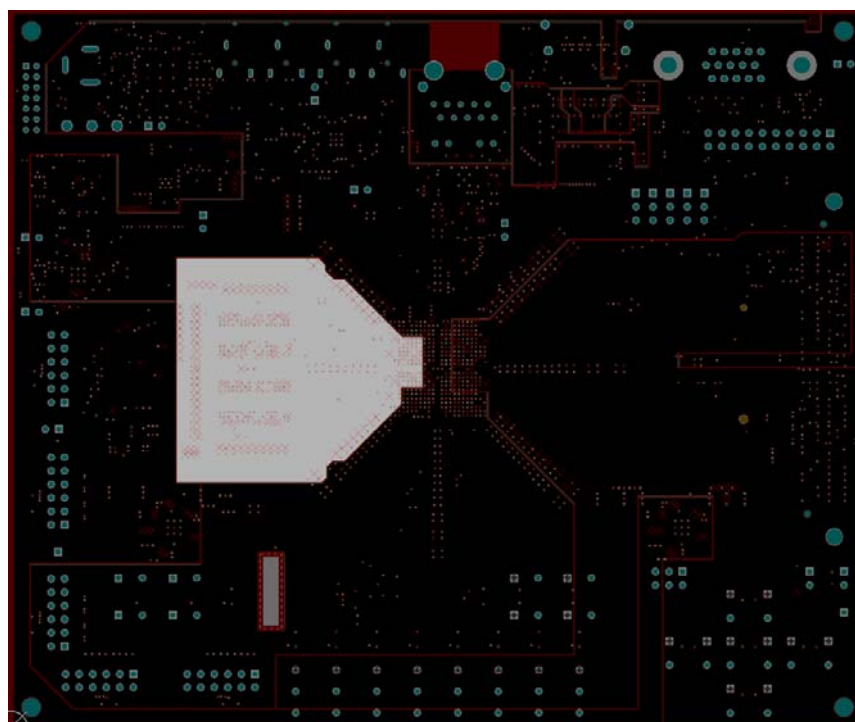


Figure 4 – Power Plane one 1.5V DDR Flood

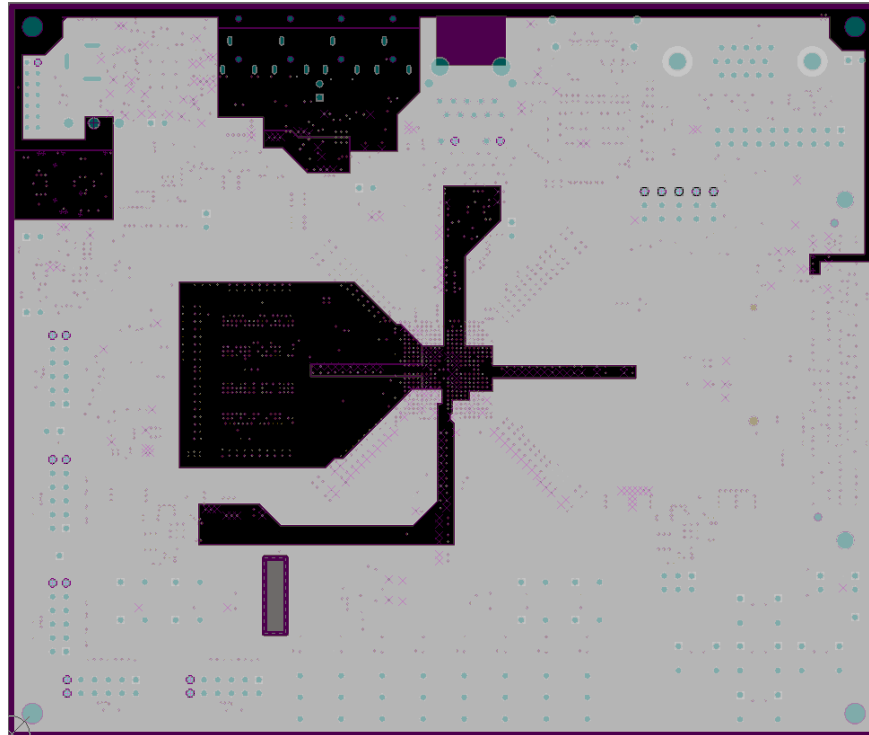


Figure 5 – Power Plane two 3.3V Flood

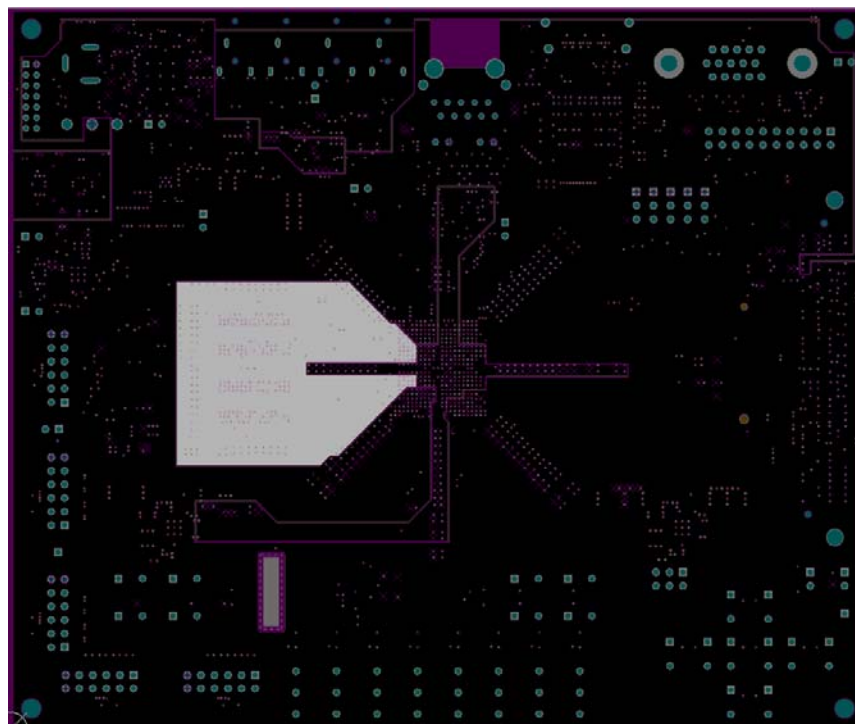


Figure 6 – Power Plane two 1.5V DDR Flood

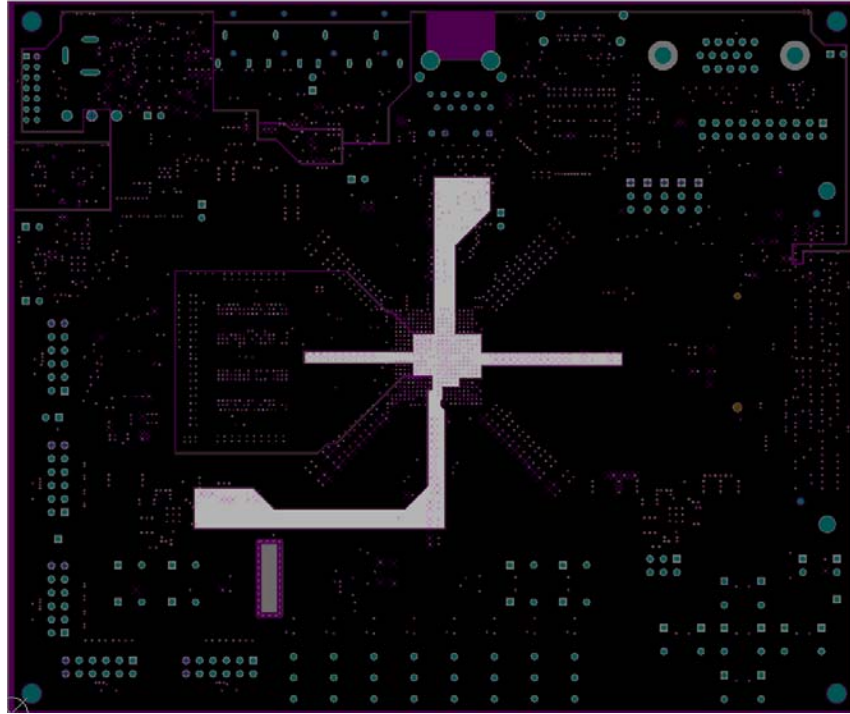
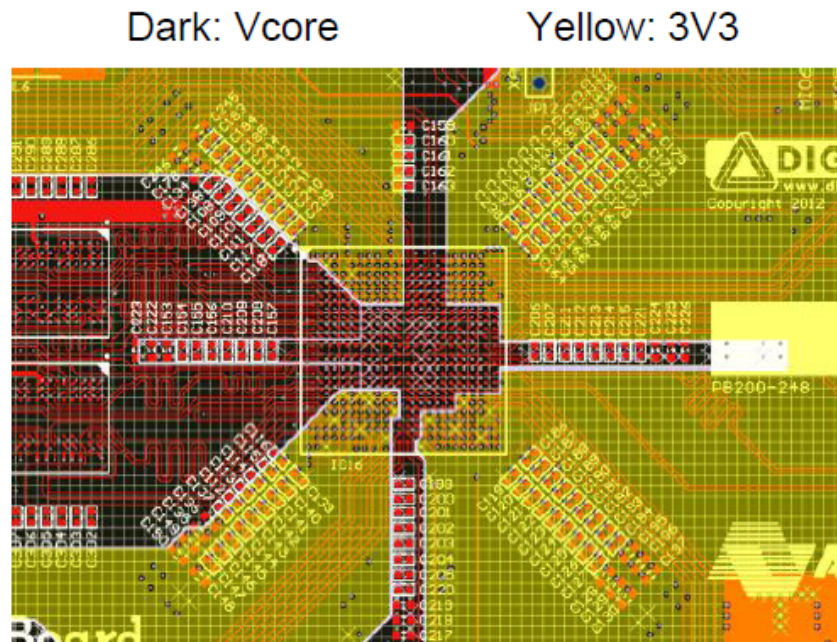
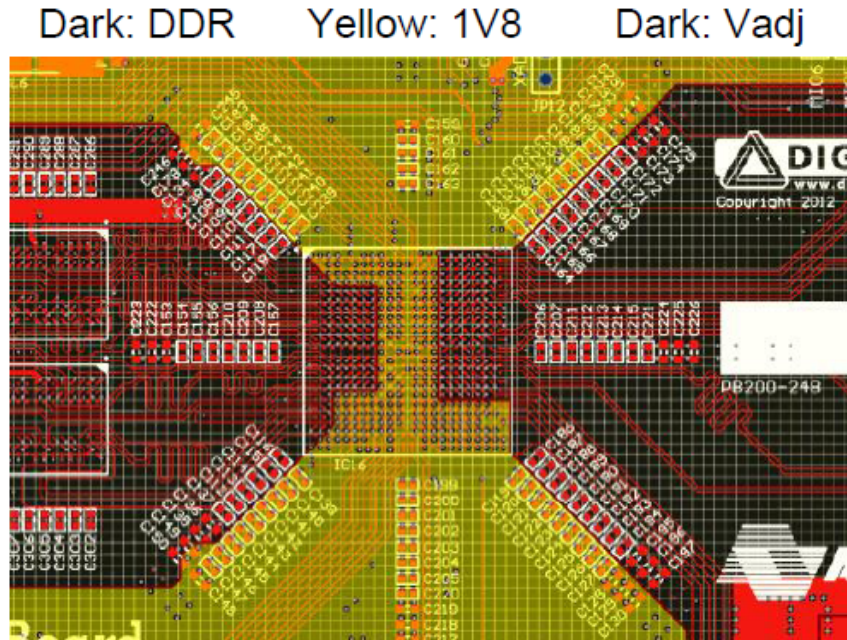


Figure 7 – Power Plane two 1.0V Vccint Flood

Ideally, all bypass capacitors would be placed immediately adjacent to the Zynq package to minimize impedance and maximize decoupling effect. However, the same PCB area adjacent to the Zynq is also valuable for routing signals, so tradeoffs (including PCB cost) must be evaluated.

The vias connecting bypass capacitors to internal planes contribute anywhere from 1.5nH to 3nH of inductance depending on via size, plating thickness, layer thickness, and other factors. The planar inductance of internal planes ranges between 30pH/mm and 60pH/mm. For bypass capacitors that are less than 25mm from the pins they supply, inductance is dominated by vias.

On the ZedBoard, bypass capacitors were located near the corners of the Zynq device, to leave room for signal traces on the sides of the device. The ZedBoard uses a range of bypass capacitor values in several package sizes to offer good bypassing at all frequencies. The smallest package, most effective high-frequency decoupling capacitors are placed closest to the Zynq device to minimize their impedance (this includes about 1/3 of the total capacitors). The larger package, lower-frequency bulk decoupling capacitors are less affected by increased inductance and are placed further away.



These images show the two power planes and their respective polygons underneath the Zynq and bypass capacitor banks. The capacitors that are not optimally close to the pins they supply are an average of 6mm further from the pins they supply, contributing up to an additional 400pH of inductance that would otherwise not be present. This additional planar inductance is only a fraction of the overall inductance, and does not significantly degrade bypass effectiveness. Restricting the capacitors to locations near the Zynq device corners allowed enough signal density on the top and bottom layers to limit the ZedBoard to only 10 layers.

Test Results

Test setup

- Rigol DS1104B oscilloscope
- ZedBoard Rev B running Ubuntu
- Xilinx ZC702 Rev B running Ubuntu



Each power supply rail feeding the Zynq device was measured for ripple noise close to the FPGA. Measurements were taken across decoupling capacitors located near the device. The tests were run while the ZedBoard was running Ubuntu which exercises the Zynq and DDR3 at a high enough power level that the measurements should reflect real world usage situations. While running the software, the ZedBoard draws roughly 4.5-5W from the 12V input. The picture shown illustrates the scope probe. Note the tightly coupled ground lead required to get accurate measurements.

The following captures with white backgrounds show the measurements on ZedBoard.

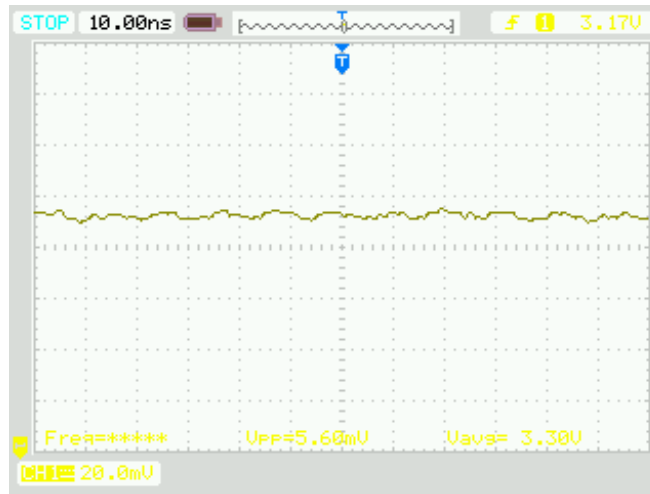


Figure 8 – 3.3V measured across C119 – 5.6mV

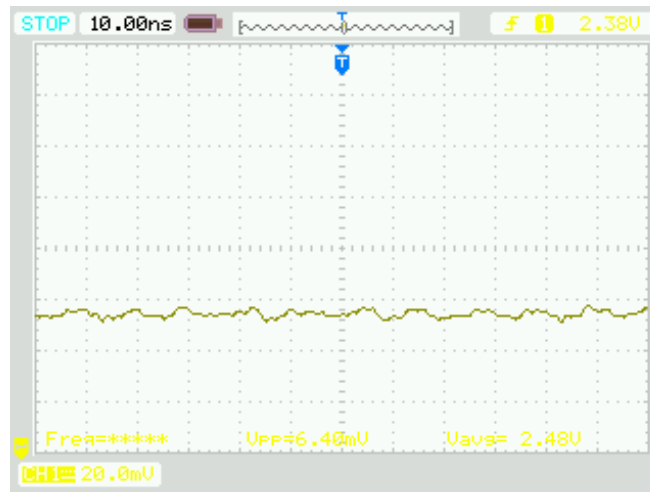


Figure 9 – 2.5V measured across C186 – 6.4mV

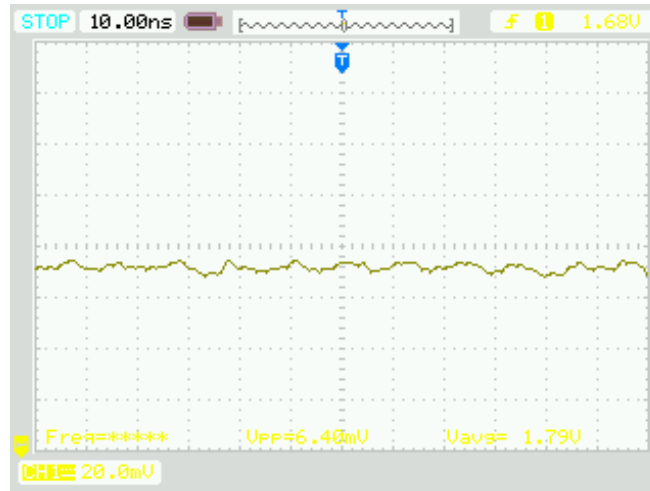


Figure 10 – 1.8V measured across C239 – 6.4mV

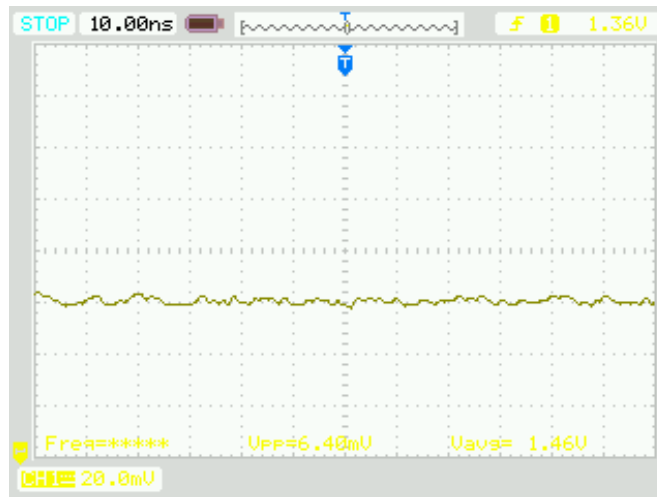


Figure 11 – 1.5V measured across C118 – 6.4mV

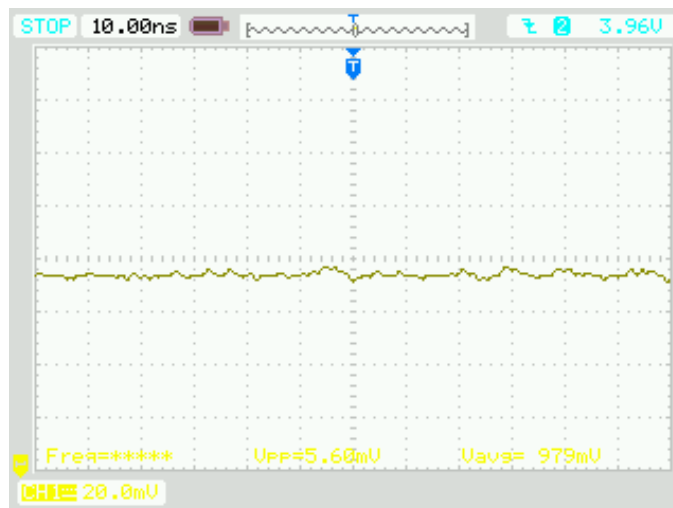


Figure 12 – 1V measured across C206 – 5.6m

*Note – each measurement was taken after observing the waveform for abnormal spikes. There was slight variation due to the difficulty in maintaining proper contact with the probe. The captures reflect the most common settling point.

For comparison, the ZC702 was also measured running similar Ubuntu software. Note the direct comparison is somewhat flawed due to the ZC702 board having more features resulting in a higher power system. Measurements were taken to get relative noise figures. The captures below with black backgrounds were taken of the ZC702.

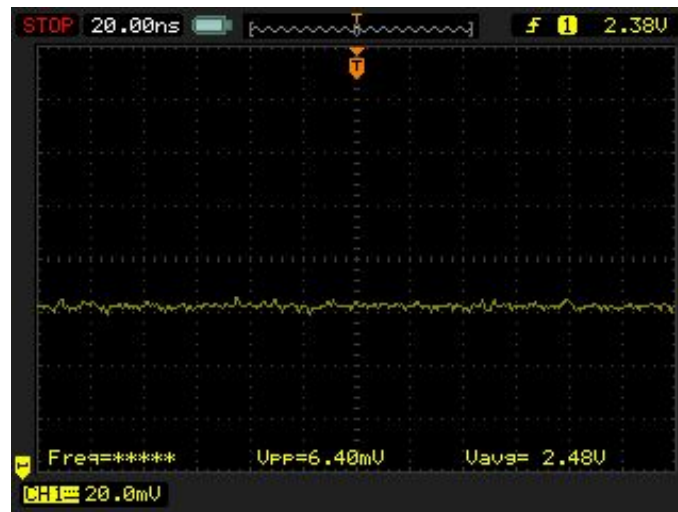


Figure 13 – 2.5V (Vadj) Measured across C384 – 6.4mV



Figure 14 – 1.8V (Vccpau) measured across C339 – 7.2mV



Figure 15 – 1.5V measured across C480 – 7.2mV



Figure 16 – 1V (Vccpint) measured across C366 – 6.4mV



Figure 17 – 1V (Vccint) measured across C357 – 7.2mV



Figure 18 – 1.8V (Vccpaux) measured across C222 – 8.0mV



Figure 19 – 1V (Vccbram) measured across C348 – 7.2mV



Figure 20 – 1.8V (Vccmio) measured across C344 – 6.4mV

As shown by the captures above of both the ZedBoard and the ZC702, the ZedBoard produces slightly better noise performance on the power system at the Zynq device. This testing was performed to alleviate concerns about layout and stackup on the ZedBoard. Results are somewhat expected since the ZC702 is much more densely populated. Each load introduces more noise onto the voltage rails.

Another major decoupling design goal is the transient response. However, limitations of the test setup prevented transient response testing from being performed.

Reference Material

ZedBoard

www.zedboard.org

Sanmina-SCI PCB cost calculator

<http://www.sanmina.com/sections/components/printed-circuit-boards/cost-ratio-calculator/index.php>

Xilinx Zynq-7000 AP SoC

<http://www.xilinx.com/products/silicon-devices/soc/Zynq-7000/index.htm>

Xilinx Zynq-7000 Packaging and Pinout Specifications

http://www.xilinx.com/support/documentation/user_guides/ug865-Zynq-7000-Pkg-Pinout.pdf

Xilinx Zynq-7000 All Programmable SoC PCB Design and Pin Planning Guide

http://www.xilinx.com/support/documentation/user_guides/ug933-Zynq-7000-PCB.pdf

Revision History

Version	Date	Author	Details
1.0	09/12/2012	CA	Initial release
2.0	09/26/2012	CA	Feedback revision