



# ZedBoard Rev C.1 Errata



## Table of Contents

1	Introduction .....	3
2	Identifying Affected Kits.....	3
3	Errata.....	4
3.1	Xilinx Zynq-7000 ES.....	4
3.2	TUSB1210 Cvbus Value is out of specification for Host mode .....	5
3.3	DDR3 CKE Termination .....	6
3.4	SD Card Clock Series Termination.....	7
3.5	DDR3 Missing Connections for Pins F1 and G7 .....	8
3.6	Zynq Applications Fail Due to Heat.....	9
3.7	USB-UART VBUS connection.....	11
3.8	Zynq-7000 USB timing parameter is incompatible with TUSB1210 PHY.....	12
3.9	Zynq-7000 SD voltage parameter is incompatible with TXS02612 .....	14
3.10	ZedBoard Resets when Hot-Plugging a Cable.....	16
3.11	ZedBoard Routing Does Not Account for Package Delays.....	17
3.12	ZedBoard DDR3 Single-Ended Trace Impedance Does Not Match UG933 Recommendation .....	17
	New Erratum .....	19
4	Additional Support.....	19
5	Revision History .....	19

# 1 Introduction

Thank you for your interest in the ZedBoard. Although Avnet and Digilent have made every effort to ensure the highest possible quality, these kits and associated software are subject to the limitations described in this errata notification.

Be aware that any of the optional workarounds requiring physical modifications to the board are done at the User's own risk. Neither Avnet nor Digilent is liable for any user performed rework.

# 2 Identifying Affected Kits

The kits affected by these errata are Revision C.2. Kits can be identified by the Revision of the ZedBoard in the kit and the additional pictures provided in the explanations below. The Revision of the ZedBoard can be found just below the barcode.

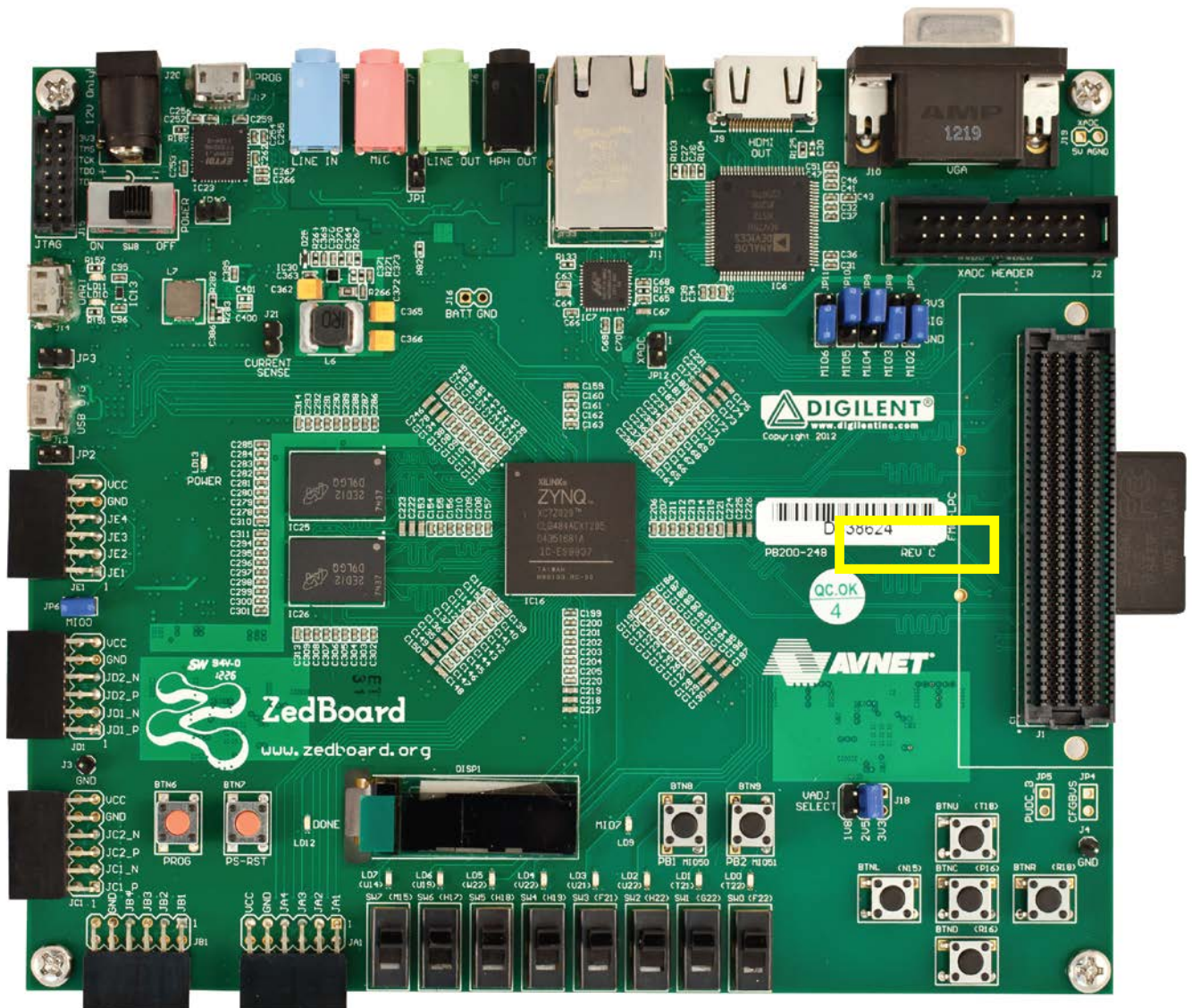


Figure 1 – Identifying ZedBoard Revision (Rev C shown)

## 3 Errata

### 3.1 Xilinx Zynq-7000 ES

#### Applications Affected

The errata for the Xilinx 7Z020 ES device may affect applications.

#### Description

The Rev C ZedBoard contains the CES version of the Xilinx ZC7Z020. Therefore, the XC7Z020 errata apply to this kit. You can verify that your board has a CES device by examining the Zynq package markings. Note in the image below that the last line states “1C-ES9937.” The “ES” in this line indicates that this is Engineering Sample silicon.

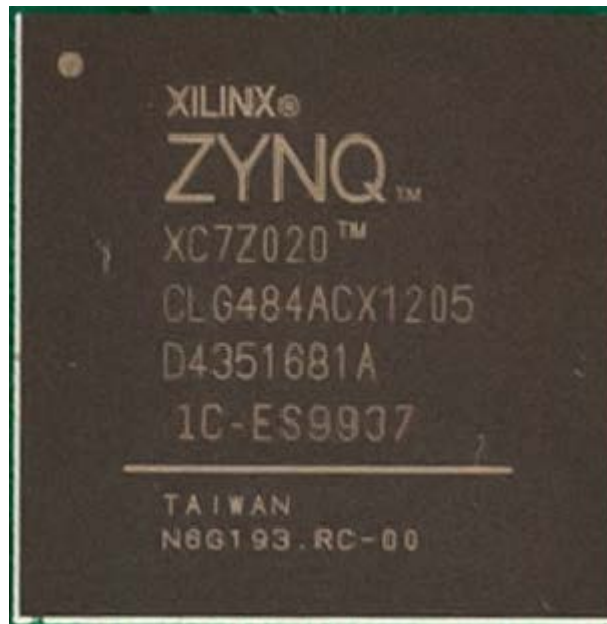


Figure 2 – Identifying ES Zynq Silicon

#### Workaround

Please refer to the Errata on the Xilinx website:

[http://www.xilinx.com/support/documentation/zynq-7000\\_errata.htm](http://www.xilinx.com/support/documentation/zynq-7000_errata.htm) → [Zynq-7000 XC7Z020 CES Errata](#)

## 3.2 USB1210 Cvbus Value is out of specification for Host mode

### Applications Affected

There are no known field failures due to this issue.

### Description

The first ~5000 Rev C ZedBoards populated a 100uF capacitor at location C89, although the schematics show 120uF. C89 is used as the USB1210 Cvbus when jumper JP3 is installed. JP3 is installed when the user desires to put the ZedBoard in Host USB mode.

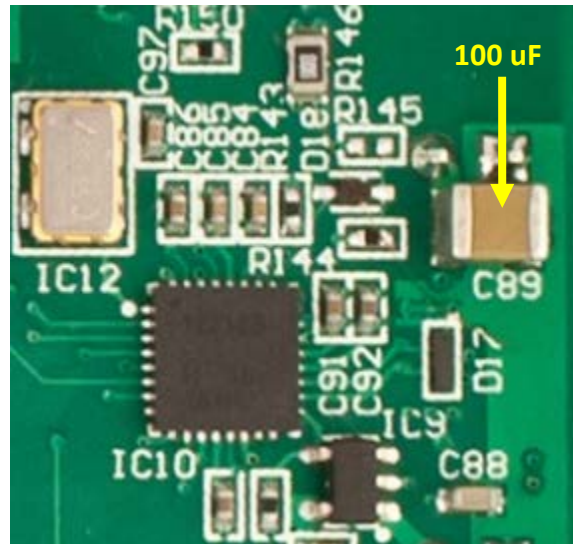


Figure 3 – Identifying affected ZedBoards

According to Table 8-2 in the USB1210 datasheet for VBUS – HOST, Cvbus should be larger than 120uF.

Table 8-2. USB1210 V<sub>BUS</sub> Capacitors

FUNCTION	COMPONENT	REFERENCE	VALUE	NOTE	LINK
VBUS - HOST	Capacitor	CVBUS	>120 $\mu$ F		<a href="#">Figure 10-1</a>
VBUS – DEVICE	Capacitor	CVBUS	4.7 $\mu$ F	Range: 1.0 $\mu$ F to 10.0 $\mu$ F	<a href="#">Figure 10-1</a>
VBUS - OTG	Capacitor	CVBUS	4.7 $\mu$ F	Range: 1.0 $\mu$ F to 6.5 $\mu$ F	<a href="#">Figure 10-1</a>

### Workaround

Replace C89 with a capacitor that is 120uF or larger.

## 3.3 DDR3 CKE Termination

### Applications Affected

Those users that exercise self-refresh may find poor signal integrity on CKE. All Rev C boards are affected.

### Description

Micron's DDR3 specification requires CKE to be low 10ns before RESET# goes high. DDR2 designs required CKE to be held low longer. To achieve the CKE low on DDR2, it was recommended that CKE be pulled low to GND through a 4.7K-ohm resistor. This design practice carried over into the early release Zynq PCB recommendations. However, since the Zynq controller drives CKE low, the 10ns requirement is met, and it is not necessary to pull-down the CKE signal.

Xilinx has now changed the recommended PCB design for DDR3 CKE to be a 40-ohm termination to VTT. This matches what Micron does on their SODIMMs.

For typical users, the termination of CKE makes no difference. For users exercising self-refresh, the 4.7k-ohm pull-down may result in poor signal integrity as CKE could potentially be a higher frequency signal in this scenario.

### Workaround

There is no work-around. Users desiring to use DDR3 self-refresh on ZedBoard should be aware that the signal integrity on CKE in this situation may be poor.

Designers that use ZedBoard schematics as a reference should terminate CKE through 40-ohms to VTT.

## 3.4 SD Card Clock Series Termination

### Applications Affected

There are no known field failures due to this issue. However, it is listed here for designers referencing the Rev C ZedBoard schematics and layout.

### Description

Since the original release of the Rev C ZedBoard, Xilinx has updated the recommendation for termination on the SD peripheral clock, which affects the SD Card on ZedBoard. The *Zynq PCB Design and Pin Planning Guide (UG993)* now states:

The SDIO clock (SDx\_CLK) needs to be terminated with a  $40\Omega - 60\Omega$  series resistor. The resistor shall be placed as close to the MIO pin as possible.

### Workaround

None

Designers that use ZedBoard schematics as a reference should terminate the SD Card clock with a  $40\Omega - 60\Omega$  series resistor.

### 3.5 DDR3 Missing Connections for Pins F1 and G7

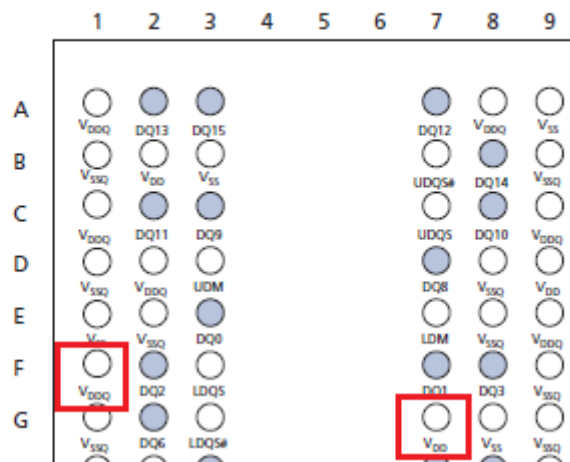
#### Applications Affected

There are no known field failures due to this issue. However, it is listed here for designers referencing the Rev C ZedBoard schematics and layout.

#### Description

The DDR3 symbol used in the Rev C ZedBoard has a mistake that improperly leaves Pins F1 and G7 disconnected. This affects IC25 and IC26. Pins F1 and G7 of the DDR3 are not shown on the Rev C ZedBoard schematic. An examination of the Rev C ZedBoard layout will show that these two pins are No-Connects. The Micron datasheet shows these as VDDQ and VDD.

Figure 7: 96-Ball FBGA – x16 (Top View)



#### Workaround

None

Designers that use ZedBoard schematics as a reference should connect F1 to Vddq and G7 to Vdd.



## 3.6 Zynq Applications Fail Due to Heat

### Applications Affected

Designs that exercise the Zynq on the ZedBoard at the highest performance (especially FMC card applications) or high ambient temperatures may experience a heat-related failure. Similar applications may not fail on the ZC702, which has the same 7z020 device.

### Description

The Rev C ZedBoard ships with a Commercial temperature grade Zynq device. According to the Zynq datasheet, the maximum operating junction temperature is specified at 85° C. When the junction temperature exceeds 85° C, the Zynq device may experience failures.

Table 2: Recommended Operating Conditions<sup>(1)</sup> (Cont'd)

Symbol	Description	Min	Typ	Max	Units
<b>Temperature</b>					
T <sub>j</sub>	Junction temperature operating range for commercial (C) temperature devices	0	–	85	°C
	Junction temperature operating range for extended (E) temperature devices	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices	–40	–	100	°C

The Zynq junction temperature is a function of the ambient temperature, internally generated heat due to operation, and the ability of the Zynq package and ZedBoard PCB to dissipate that heat. Applications that utilize the Zynq at higher operating frequencies or fuller capacity or more I/O will consume more power and thus generate more heat. Applications that make use of an FMC may be particularly susceptible to more heat due to the extra logic and I/Os to interface to the card. In some cases, the ZedBoard Zynq T<sub>j</sub> may exceed 85° C and fail. ChipScope was used to access the XADC to measure T<sub>j</sub> and verify that T<sub>j</sub> did exceed 85° C during demanding applications.

Given the same Zynq application with FMC running under similar conditions, field failures have occurred on ZedBoard that do not occur on ZC702. This is attributed to the ZC702's better ability to dissipate heat. The ZedBoard was designed to be lower cost. For this reason, several cost-cutting measures were taken related to the PCB, outlined below. The trade-off for these decisions is ZedBoard's decreased capacity to dissipate heat out of the Zynq device in demanding applications.

- Thinner dielectric layers
- Fewer copper plane (power and ground) layers
- Fewer total layers
- Reduced copper thickness

For these reasons, ZedBoard may be susceptible to heat-related failures with demanding applications, especially applications utilizing FMC. High ambient temperatures may also cause problems with ZedBoard.

## Workaround

A heatsink applied to the ZedBoard's Zynq device is recommended for all applications. Starting in October 2012, all ZedBoard's are populated with a CTS BDN09-3CB/A01. Additionally, the most demanding applications will benefit from a fan to produce airflow over the ZedBoard. For example, the [Zynq-7000 SoC / Analog Devices Software-Defined Radio Kit](#) will ship with Sunon fan UF3H3-700, which can be operated from 3.3V power available through one of the Pmod connectors.

Both the heatsink and the fan are listed on the [ZedBoard Accessories](#) page.

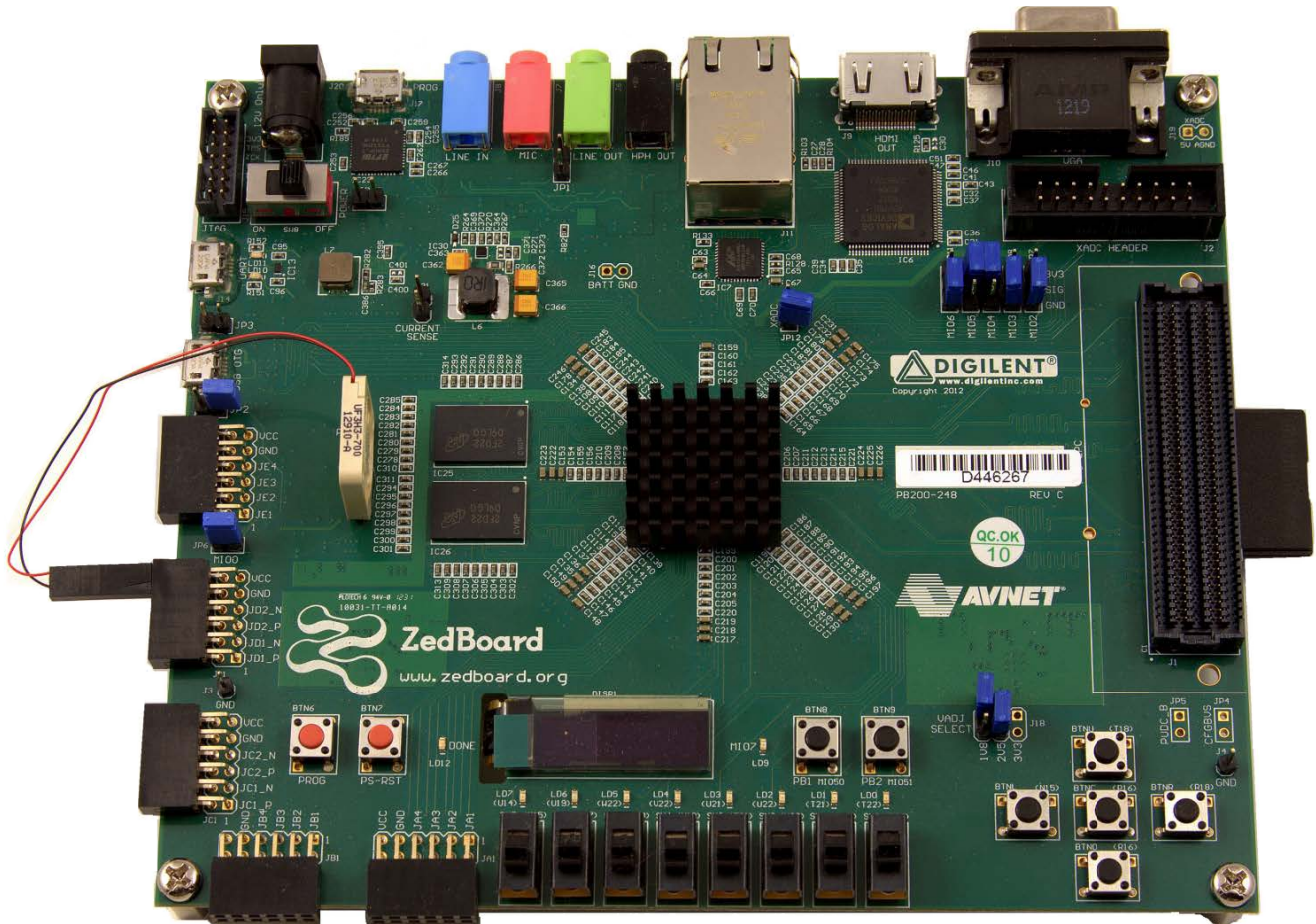


Figure 4 – ZedBoard with Heatsink and Auxiliary Fan attached

## 3.7 USB-UART VBUS connection

### Applications Affected

There are no known field failures due to this issue. However, it is listed here for designers referencing the Rev C ZedBoard schematics and layout.

### Description

The Cypress CY7C64225 USB-UART circuit on the ZedBoard is designed to allow experimentation either in a self-powered or a bus-powered configuration.

The default is self-powered, with R146 being installed, and R147 is depopulated

In bus-powered mode, R147 should be installed and R146 depopulated.

When in self-powered mode (R146 installed and R147 depopulated), the CY7C64225 VBUS pin connects through a 1K-ohm resistor (R150) to VCC3V3. This is incorrect. VBUS should be connected through a 1K-ohm resistor to the USB connector Pin V, regardless of the mode.

### Workaround

Switch to bus-powered mode by depopulated R146 and installing R147.

### 3.8 Zynq-7000 USB timing parameter is incompatible with TUSB1210 PHY

#### Applications Affected

There are no known field failures due to this issue. However, as Zynq moves to production, it is possible based on a datasheet analysis that USB data transfers will fail. The worst-case conditions occur at hot temperatures and low voltage range of the two devices.

#### Description

The Xilinx Zynq has a hold time requirement for ULPI input data, which is given by  $T_{ULPICKD} \text{ MIN} = 1.0 \text{ ns}$ . This specification can be found in the *Zynq-7000 AP SoC (XC7Z010 and XC7Z020: DC and AC Switching Characteristics, DS187 (v1.2) September 12, 2012*, as shown below.

Symbol	Description	Min	Max	Units
$T_{ULPICK}$	Input setup to ULPI clock, all inputs	10.67		ns
$T_{ULPICKD}$	Input hold to ULPI clock, all inputs	1.0		ns
$T_{ULPICKO}$	ULPI clock to output valid, all outputs		8.86	ns
$F_{ULPICKL}$	ULPI reference clock frequency	59.97	60.03	MHz

The Texas Instrument's TUSB1210 does not specify the MIN (fastest) Output Delay ( $T_{DC}, T_{DD}$ ) with ULPI Output Clock. This is observed in *TUSB1210 Standalone USB Transceiver Chip Silicon Data Manual, SLLSE09F, August, 2012*, as shown below.

PARAMETER	INPUT CLOCK		OUTPUT CLOCK		UNIT
	MIN	MAX	MIN	MAX	
$T_{SC}, T_{SD}$ Set-up time (control in, 8-bit data in)		3		6	ns
$T_{SC}, T_{HD}$ Hold time (control in, 8-bit data in)	1.5		0		ns
$T_{DC}, T_{DD}$ Output delay (control out, 8-bit data out)		6		9	ns

According to internal sources at TI, this could be as fast as 0.1ns.

This results in a possible 900ps window where data could be lost.

#### Workaround

The worst-case scenario is when the Zynq needs the full 1.0ns of Hold Time at the same time that the TUSB1210 outputs data at the fastest possible clock-to-output. According to sources at Xilinx and TI, each chip experiences this worst-case potential under high temperature and low-voltage conditions. It may be possible to prevent an issue by maintaining the devices at lower temperatures. It is recommended that ZedBoard not be operated above room temperature for this reason.

For those designing their own boards based on ZedBoard, it is recommended that the ZedBoard TUSB1210 circuitry NOT be copied. Xilinx recommends interfacing Zynq to SMSC USB PHYs. As an example, the [Xilinx ZC702](#) uses the SMSC USB3320 PHY.

As shown in *USB3320 Highly Integrated Full Featured Hi-Speed USB 2.0 ULPI Transceiver Datasheet*, Revision 1.0 (07-14-09), the USB3320 Output Delay shows a MIN = 1.0 ns, which is compatible with Zynq-7000.

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
60MHz ULPI Output Clock <a href="#">Note 4.4</a>					
Setup time (STP, data in)	$T_{SC}, T_{SD}$	Model-specific REFCLK	5.0		ns
Hold time (STP, data in)	$T_{HC}, T_{HD}$	Model-specific REFCLK	0.0		ns
Output delay (control out, 8-bit data out)	$T_{DC}, T_{DD}$	Model-specific REFCLK	1.0	3.5	ns

### 3.9 Zynq-7000 SD voltage parameter is incompatible with TXS02612

After further analysis and documentation from Xilinx, this is not expected to be an issue.

#### Description

The Xilinx Zynq has a PS MIO  $V_{OL}$  of 0.45V. This specification can be found in the *Zynq-7000 AP SoC (XC7Z010 and XC7Z020: DC and AC Switching Characteristics, DS187 (v1.5) March 19, 2013*, as shown below.

Table 8: PS DC Input and Output Levels<sup>(1)</sup>

Bank	I/O Standard	$V_{IL}$		$V_{IH}$		$V_{OL}$	$V_{OH}$	$I_{OL}$ mA	$I_{OH}$ mA
		V, Min	V, Max	V, Min	V, Max	V, Max	V, Min		
MIO	LVC MOS18	-0.300	35% $V_{CCO\_MIO}$	65% $V_{CCO\_MIO}$	$V_{CCO\_MIO} + 0.300$	0.450	$V_{CCO\_MIO} - 0.450$	8	-8

The Texas Instrument's TXS02612 shows a  $V_{IL}$  MAX of 0.15V in document SCES682C, February 2009, as shown below.

#### RECOMMENDED OPERATING CONDITIONS

		$V_{CCA}$	$V_{CCBx}$ <sup>(1)</sup>	MIN	MAX	UNIT	
$V_{CCA}$ $V_{CCB0}$ $V_{CCB1}$	Supply voltage			1.1	3.6	V	
$V_{IH}$	High-level input voltage	A-port I/Os	1.1 V to 3.6 V	1.1 V to 3.6 V	$V_{CCI} - 0.2$	$V_{CCI}$	V
		B-port I/Os			$V_{CCI} - 0.2$	$V_{CCI}$	
		SEL, CLKA			$V_{CCA} \times 0.65$ V	3.6	
$V_{IL}$	Low-level input voltage	A-port I/Os	1.1 V to 3.6 V	1.1 V to 3.6 V	0	0.15	V
		B-port I/Os			0	0.15	
		SEL, CLKA			0	$V_{CCA} \times 0.35$	
$\Delta t/\Delta v$	Input transition rise or fall rate	CLK, SEL			10	ns/V	
$T_A$	Operating free-air temperature			-40	85	°C	

(1)  $V_{CCBx}$  refers to  $V_{CCB0}$  and  $V_{CCB1}$ .

The Zynq  $V_{OL}$  is greater than the TXS02612  $V_{IL}$  MAX.

#### Workaround

No workaround is necessary. Either the MAX13035E or the TXS02612 are recommended for new SD Card designs with Zynq, based on the following justification.

Xilinx now has an additional answer record that describes how the use of the Maxim MAX13035E device was justified, which has the same apparent voltage incompatibility as the TI TXS02612.

<http://www.xilinx.com/support/answers/55253.htm>

The key point is that the Zynq  $V_{OL}$  is specified at  $I_{OL}$  of -8mA. It doesn't take -8mA for either the MAX or TI devices when driven low. In the AR, Xilinx based their  $V_{OL}$  max simulation on 30 uA sink, which was determined based on the input characteristics for the MAX13035E that was obtained directly from Maxim. In the TI datasheet excerpts below, the maximum sink current required is -12uA. Xilinx' simulation showed

a  $V_{ol} = 0.15V$  for  $I_{ol} = 30\mu A$ . The TI device has a  $V_{il-max} = 0.15V$  for  $I_{ccb-sink-max}$  of  $-12\mu A$ . Therefore, the justification shown in AR55253 also applies to the TI device.

### RECOMMENDED OPERATING CONDITIONS

		$V_{CCA}$	$V_{CCBx}^{(1)}$	MIN	MAX	UNIT	
$V_{CCA}$ $V_{CCB0}$ $V_{CCB1}$	Supply voltage			1.1	3.6	V	
$V_{IH}$	High-level input voltage	A-port I/Os	1.1 V to 3.6 V	1.1 V to 3.6 V	$V_{CCI} - 0.2$	$V_{CCI}$	V
		B-port I/Os			$V_{CCI} - 0.2$	$V_{CCI}$	
		SEL, CLKA			$V_{CCA} \times 0.65 V$	3.6	
$V_{IL}$	Low-level input voltage	A-port I/Os	1.1 V to 3.6 V	1.1 V to 3.6 V	0	0.15	V
		B-port I/Os			0	0.15	
		SEL, CLKA			0	$V_{CCA} \times 0.35$	
$\Delta t/\Delta v$	Input transition rise or fall rate	CLK, SEL			10	ns/V	
$T_A$	Operating free-air temperature			-40	85	$^{\circ}C$	

(1)  $V_{CCBx}$  refers to  $V_{CCB0}$  and  $V_{CCB1}$ .

### ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CCA}$	$V_{CCBx}$	$T_A = 25^{\circ}C$		$T_A = -40^{\circ}C$ to $85^{\circ}C$		UNIT
				TYP	MIN	MAX		
$I_I$	SEL, CLKA	1.1 V to 3.6 V	1.1 V to 3.6 V	$\pm 1$			$\pm 2$	$\mu A$
	DAT, CMD			$\pm 1$			$\pm 2$	
$I_{CCA}$	$V_I = V_O = \text{Open}$ , $I_O = 0$ , SEL, CLK = High or Low	1.1 V to 3.6 V	1.1 V to 3.6 V				12	$\mu A$
		3.6 V	0 V				12	
		0 V	3.6 V				-1	
$I_{CCB0}$ or $I_{CCB1}$	$V_I = V_O = \text{Open}$ , $I_O = 0$ , SEL, CLK = High or Low	1.1 V to 3.6 V	1.1 V to 3.6 V				24	$\mu A$
		3.6 V	0 V				-12	
		0 V	3.6 V				24	
$C_I$	SEL, CLKA	3.3 V	3.3 V	2.5			3.5	pF
$C_{IO}$	A port	3.3 V	3.3 V	7			7.5	pF
	B port			9.5			10	

## 3.10 ZedBoard Resets when Hot-Plugging a Cable

### Applications Affected

After ZedBoard is booted, plugging in a USB or Ethernet cable immediately resets the board. This is visible by the blue "DONE" LED going to the off state.

The board may also reset when touching the Ethernet shield, the usb shield, or other metal on the board, including the screws in the mounting holes of the board.

### Description

When the ZedBoard is "on" and powered from the included supply there is no reference to earth ground (the system is floating). When a device that references/connects its shield pins to earth-ground is attached using a shielded cable (like HDMI), a reference/connection to earth-ground is established and the ZedBoard may be reset as the board ground stabilizes.

It is also possible for the ZedBoard to reset in response to ESD events, but this is a separate issue from the hot-plugging reset described above.

### Workaround

The only way to solve the floating ground issue is to not introduce a new ground reference while the board is on and operating. If hot-plugging is required for your application, a reference to earth-ground can be established prior to powering on the board by either attaching it to a grounded device, or by using a three-prong power supply that provides a ground reference.

All of the ZedBoard's cable connectors (HDMI, USB, and Ethernet) have their shields connected to a "shield ring" within the PCB that is then connected to board ground through a 1Mohm resistor and ESD-suppression cap. Replacing the 1Mohm resistor with a shunt decreases the likelihood of an ESD event causing a board reset. If you are experiencing excessive ESD related resets in your environment, then you have the option of shunting resistor R281 to suppress the problem.



### 3.11 ZedBoard Routing Does Not Account for Package Delays

#### Applications Affected

There are no known field failures due to this issue. However, it is listed here for designers referencing the Rev C ZedBoard schematics and layout.

#### Description

Xilinx document *Zynq-7000 All Programmable SoC PCB Design and Pin Planning Guide* (UG933 v1.6 December 4, 2013) makes several statements related to routing of high-speed circuits (emphasis added):

- All trace lengths must also include the package delay
- DDR signals also require matched trace lengths
- Differential traces should be length matched to  $\pm 5$  mil if possible

**Table 5-9: DDR Trace Length Match**

Signal Group	LPDDR2	DDR2	DDR3	Comments
DQ/DM to DQS_P/N in data group	$\pm 10$ ps	$\pm 20$ ps	$\pm 10$ ps	
Address/Control to CK_P/N	$\pm 10$ ps	$\pm 25$ ps	$\pm 10$ ps	

- PHYs that support RGMII v2.0 with internal delays (RGMII-ID)
  - Delay skew for DATA[3:0] and CTL to clock delay should be less than  $\pm 50$  ps including package time

#### Workaround

No work-around is possible. ZedBoard ships with a -1 speed-grade Zynq device which is capable of a DDR3 interface speed of 533 MHz. The ZedBoard DDR3 has been tested at frequencies higher than this and passed. Ethernet has also been tested and passed. However, for those designers looking to duplicate the ZedBoard design, you should carefully consider what Xilinx specifies in UG933 as well as your own design objectives to determine how best to route your own board.

For those interested in evaluating the package flight times, these can be obtained using the *partgen* utility in the Xilinx tools. From a Xilinx command prompt, use the following command to obtain the flight times for the Zynq device on the ZedBoard:

```
partgen -v xc7z020clg484
```

### 3.12 ZedBoard DDR3 Single-Ended Trace Impedance Does Not Match UG933 Recommendation

#### Applications Affected

There are no known field failures due to this issue. However, it is listed here for designers referencing the Rev C ZedBoard schematics and layout.

## Description

The ZedBoard DDR3 single-ended PCB traces targeted a 50 ohm impedance. Xilinx document *Zynq-7000 All Programmable SoC PCB Design and Pin Planning Guide* (UG933 v1.6 December 4, 2013) specifies a 40 ohm impedance:

**Table 5-10: DDR Trace Impedance**

Signal Group	LPDDR2	DDR2	DDR3/3L	Comments
Single-ended	40Ω	50Ω	40Ω	±10% tolerance
Differential	80Ω	100Ω	80Ω	±10% tolerance

## Workaround

No work-around is possible. ZedBoard ships with a -1 speed-grade Zynq device which is capable of a DDR3 interface speed of 533 MHz. The ZedBoard DDR3 has been tested at frequencies higher than this and passed. However, for those designers looking to duplicate the ZedBoard design, you should carefully consider what Xilinx specifies in UG933 as well as your own design objectives to determine how best to route your own board.

## New Erratum

Any new erratum found will first be posted in the ZedBoard Forums:

<http://zedboard.org/forum>

Since this document will only be updated periodically, it is recommended that the ZedBoard Forum also be checked for other, recently found erratum.

## 4 Additional Support

For additional support, please review the discussions and post your questions to the ZedBoard Forum at

<http://zedboard.org/forum>

You can also contact your local Avnet/Silica FAE for commercial users and Digilent for academic users.

## 5 Revision History

Date	Version	Revision
21 Oct 2012	1.0	Initial Version, ZedBoard Rev C
16 Jan 2013	1.1	Added TUSB1210
01 Apr 2013	1.2	Added TXS02612
26 May 2013	1.3	Added TXS02612 justification; Added ESD reset issue; Added non-consideration of package flight times
27 Jan 2014	1.4	Added DDR3 trace impedance section