Zynq PicoZed 7015/7030	
Avnet Engineering Services	
www.microzed.org	
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PicoZed 7015/7030

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Title: 01 - Lead Sheet.SchDoc		
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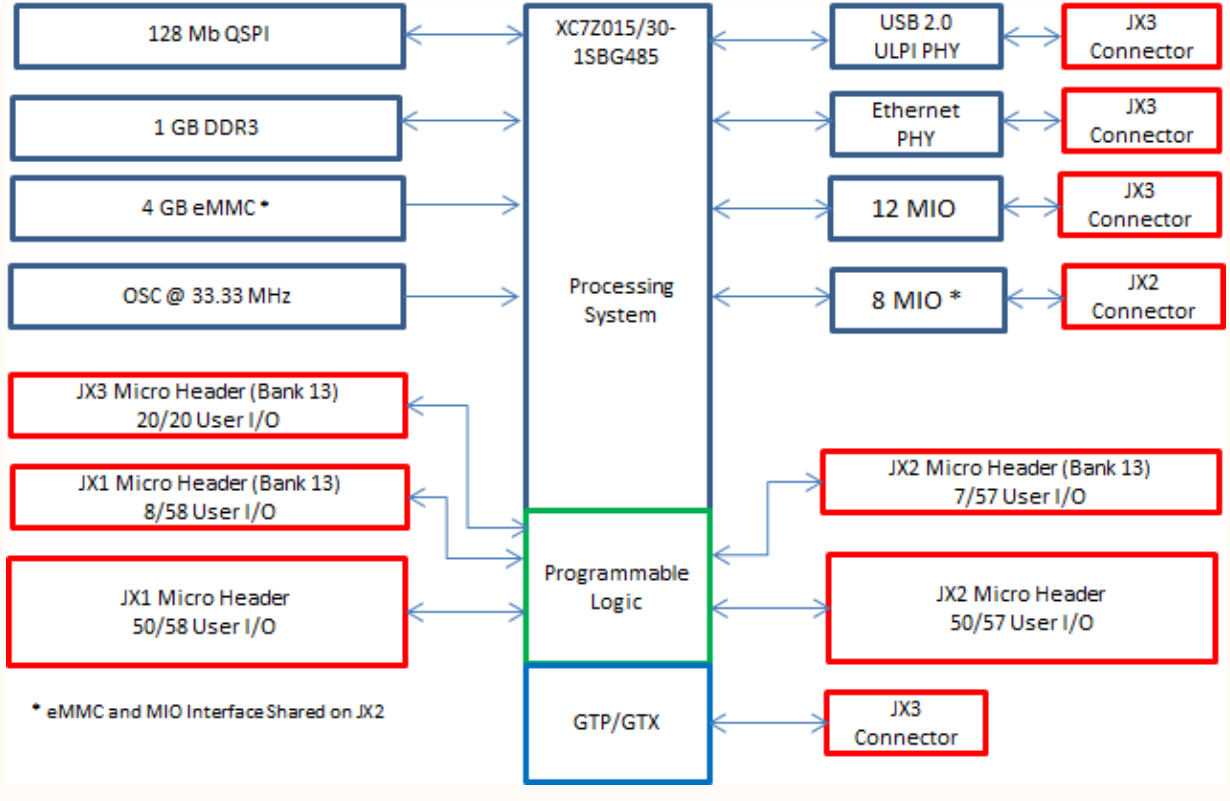

AVNET Avnet Engineering Services		
Title: 02 - Block Diagram.SchDoc		
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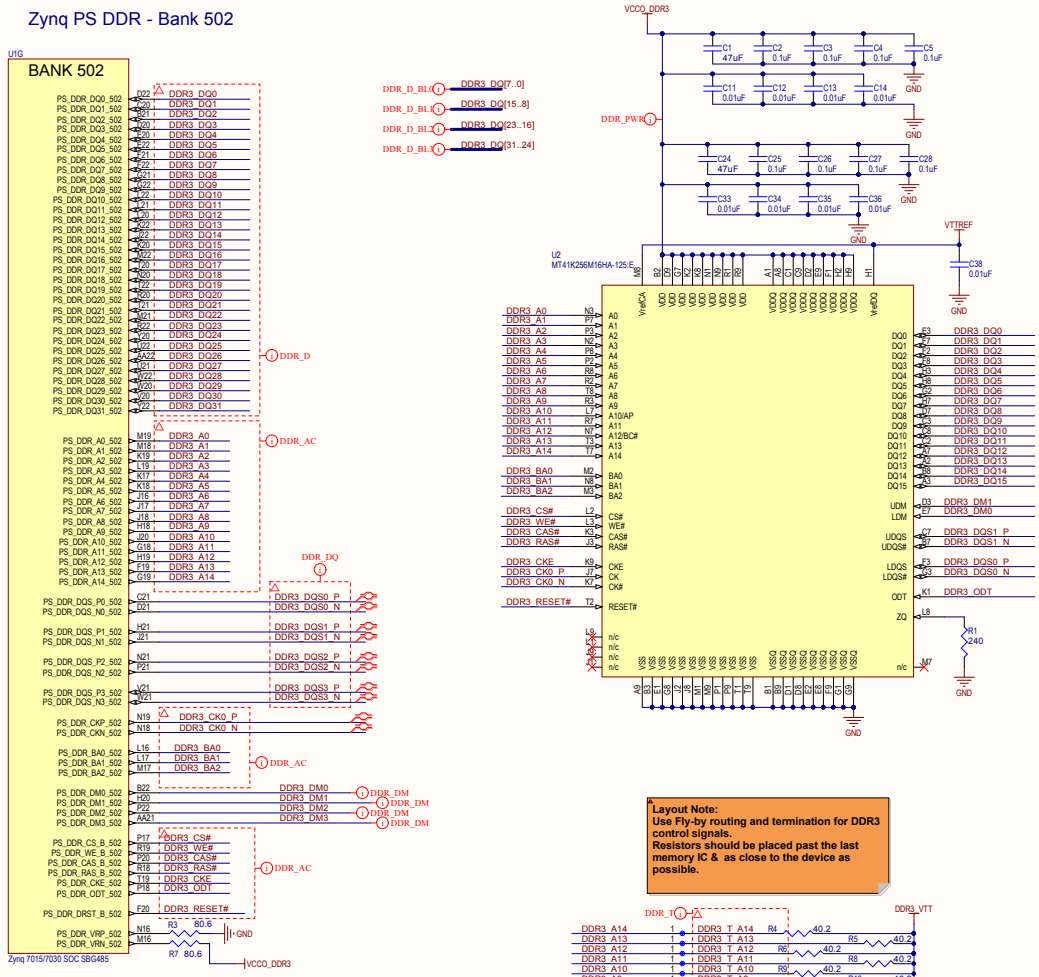
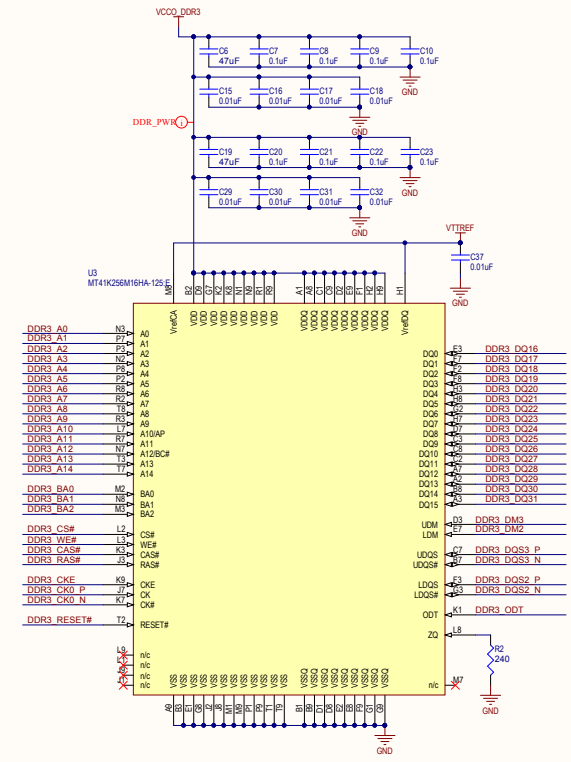
Date: 12/3/2014	Sheet 2 of 12	

Zynq PS DDR - Bank 502



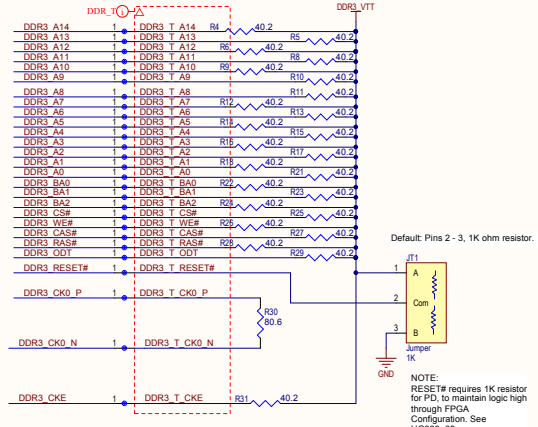
DDR3



Layout Note:
Use Fly-by routing and termination for DDR3 control signals.
Resistors should be placed past the last memory IC & as close to the device as possible.

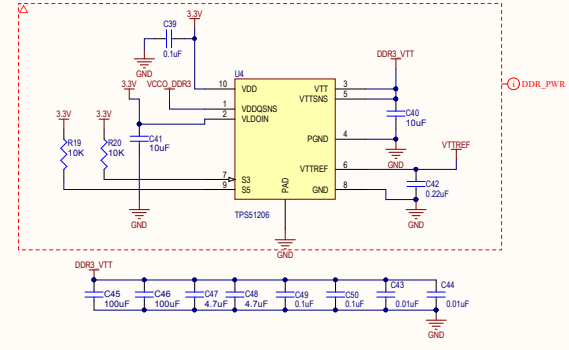
Layout Note:
DDR3 trace lengths must include Zynq package flight times.
See UG933 and Layout Guidelines.

Layout Note:
DDR3 target trace impedances are as follows:
Single Ended Signals = 40 ohms
Differential Signals = 80 ohms



NOTE:
RESET# requires 1K resistor for PD, to maintain logic high through FPGA Configuration. See UG933p62

DDR3 Termination Supply



Avnet Engineering Services			
Title: 03 - DDR3.SchDoc			
Size: C	Document Number: PicoZed 7015/7030		Rev: C
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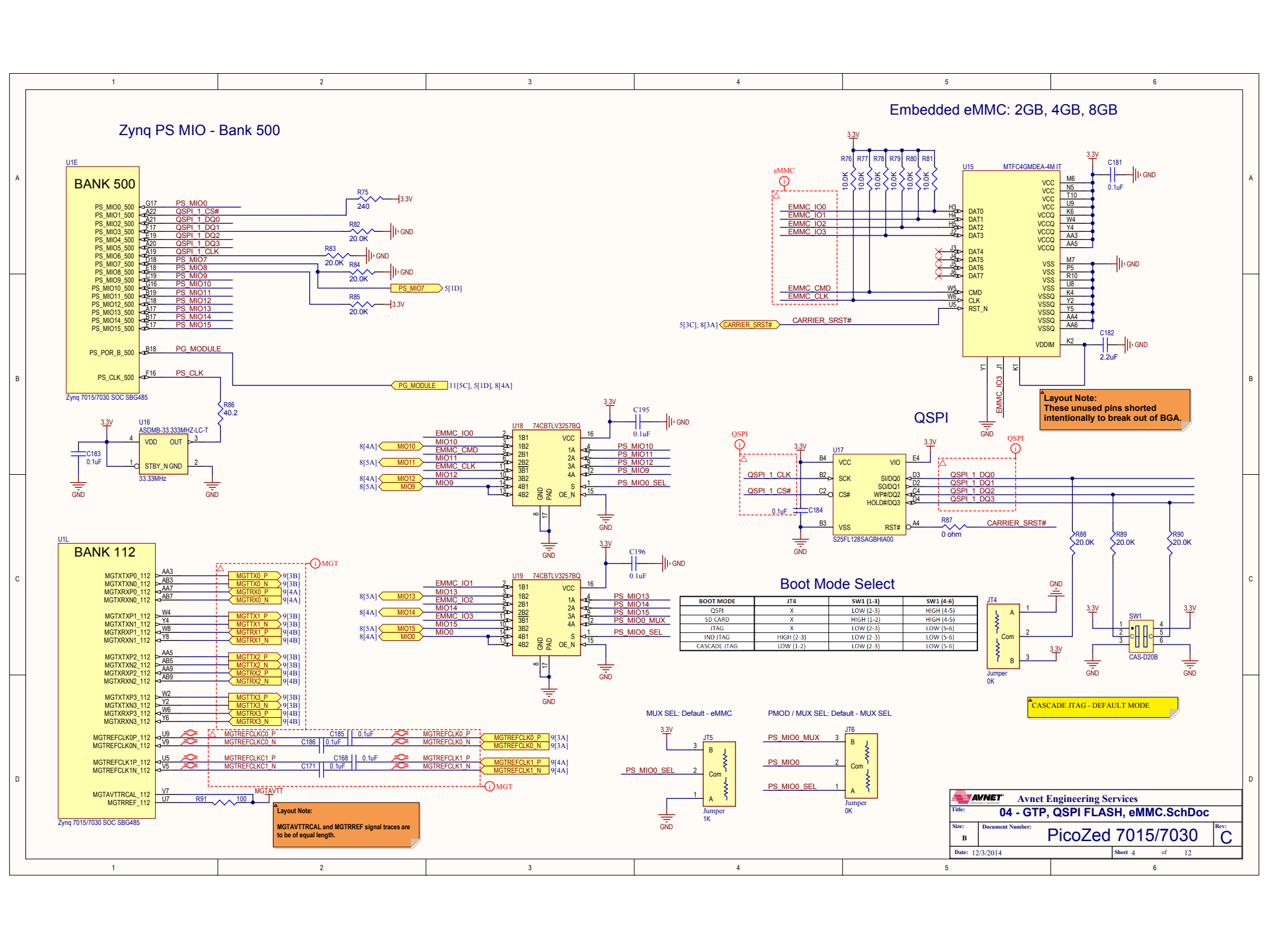
Zynq PS MIO - Bank 500
Embedded eMMC: 2GB, 4GB, 8GB
QSPI
Boot Mode Select
BOOT MODE | JT4 | SW1 (1-3) | SW1 (4-6)
QSPI | X | LOW (2-3) | HIGH (4-5)
SD CARD | X | HIGH (1-2) | HIGH (4-5)
JTAG | X | LOW (2-3) | LOW (5-6)
IND JTAG | HIGH (2-3) | LOW (2-3) | LOW (5-6)
CASCADE JTAG | LOW (1-2) | LOW (2-3) | LOW (5-6)
Layout Note:
These unused pins shorted intentionally to break out of BGA.
Layout Note:
MGTAVTTRCAL and MGTRREF signal traces are to be of equal length.
CASCADE JTAG - DEFAULT MODE
MUX SEL: Default - eMMC
PMOD / MUX SEL: Default - MUX SEL
Avnet Engineering Services
Title: 04 - GTP, QSPI FLASH, eMMC.SchDoc
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Date: 12/3/2014
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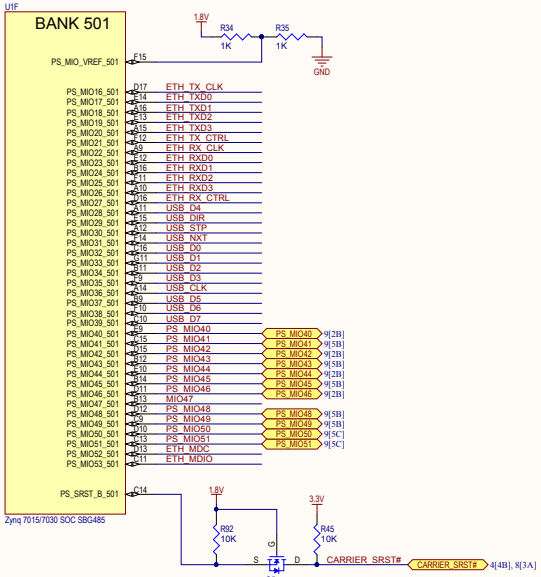
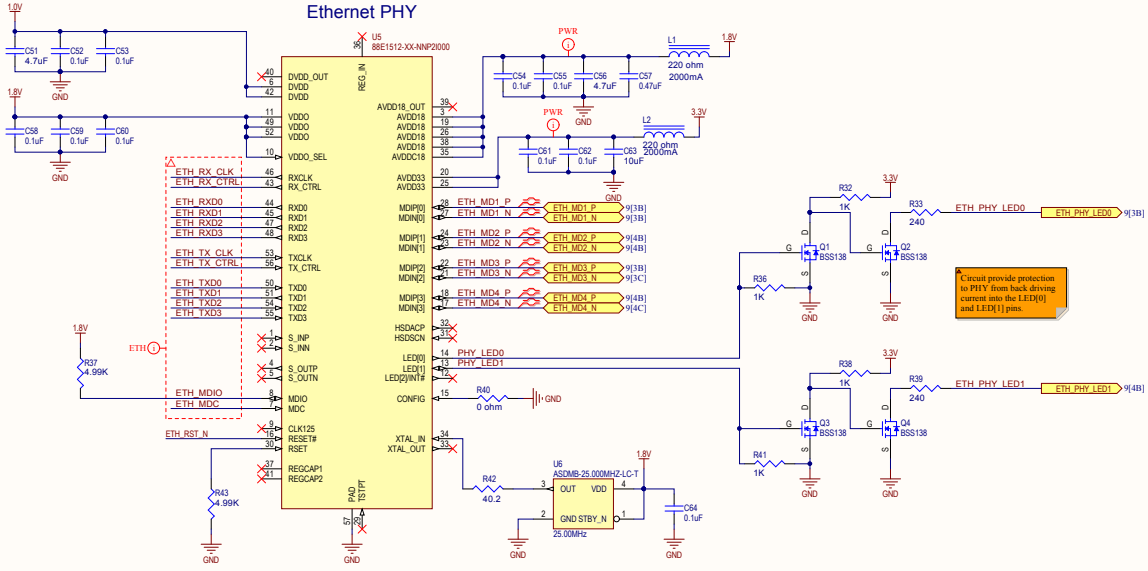
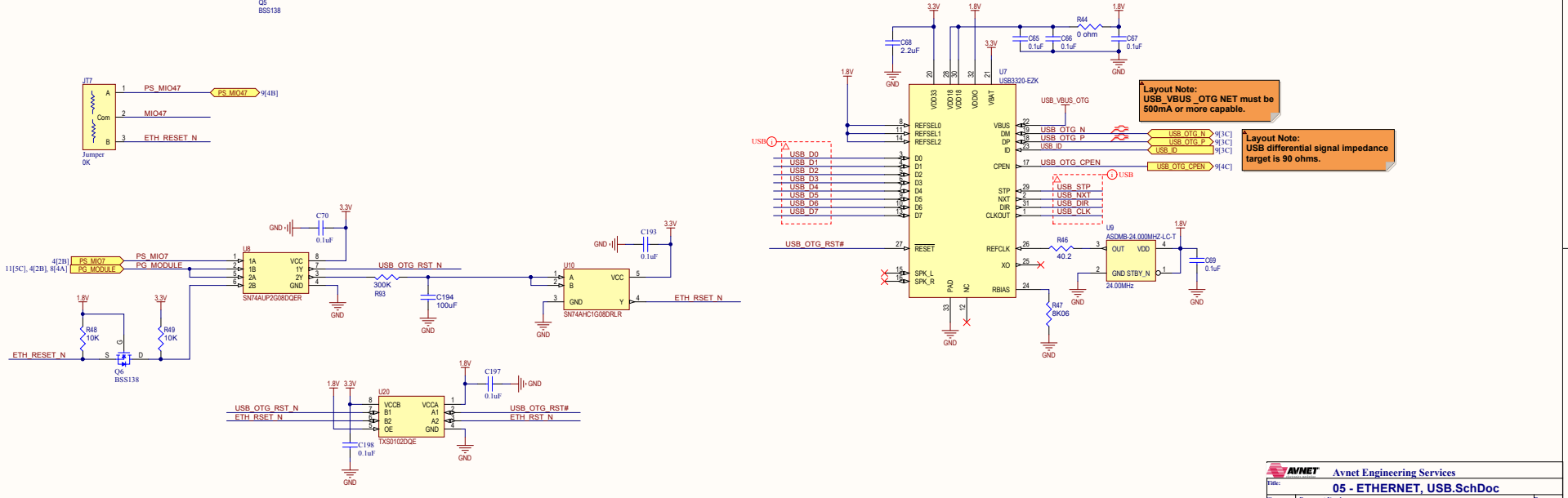
Zynq PS MIO - Bank 501



Ethernet PHY



USB 2.0 OTG



Layout Note:
Circuit provide protection to PHY from back driving current into the LED[0] and LED[1] pins.

AVNET	Avnet Engineering Services		
Title:	05 - ETHERNET, USB.SchDoc		
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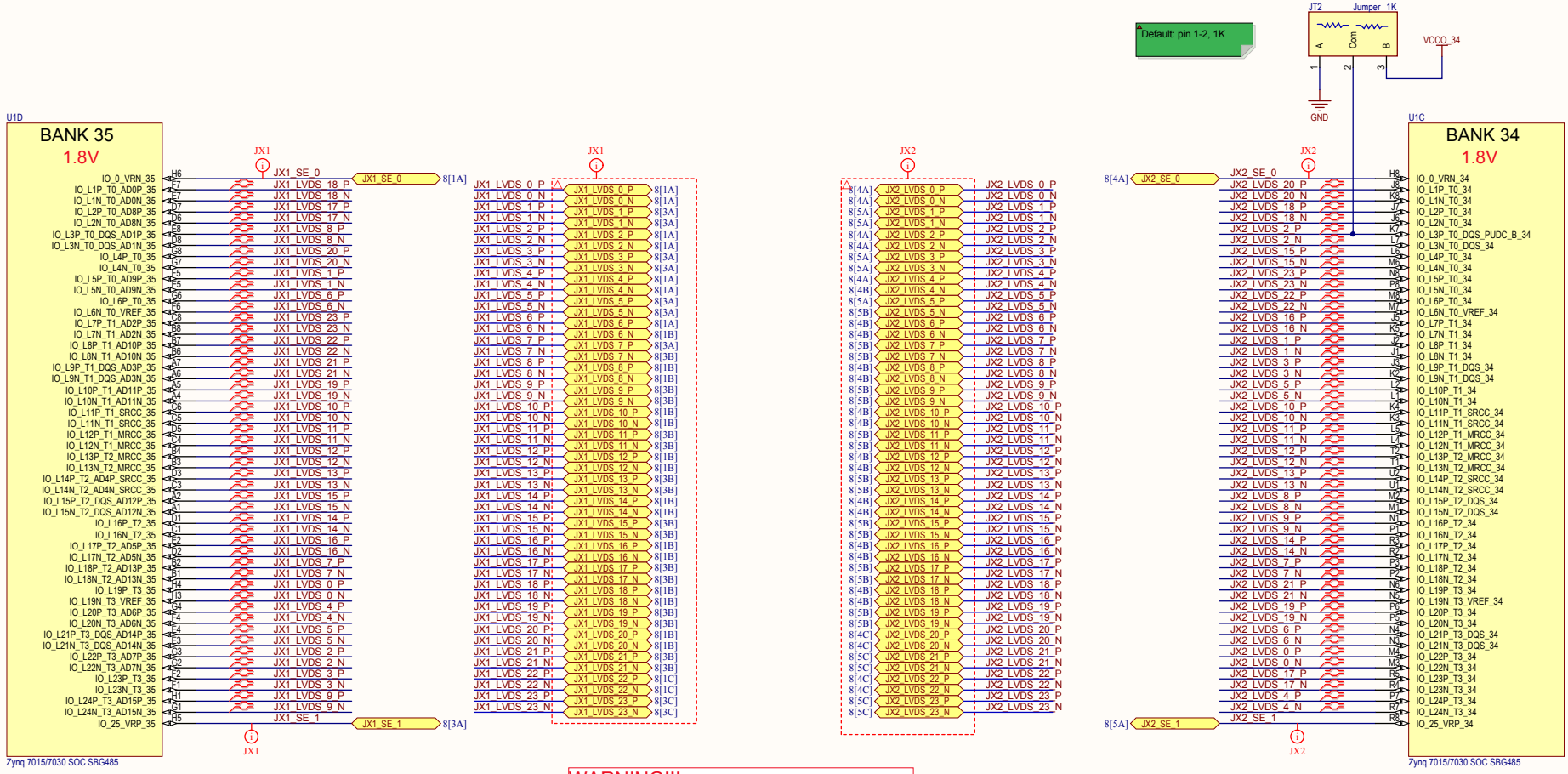
U1D
BANK 35
1.8V
Zynq 7015/7030 SOC SBG485
JX1
JX1_SE_0
JX1_SE_1
JX1_LVDS_0_P
JX1_LVDS_0_N
JX1_LVDS_1_P
JX1_LVDS_1_N
JX1_LVDS_2_P
JX1_LVDS_2_N
JX1_LVDS_3_P
JX1_LVDS_3_N
JX1_LVDS_4_P
JX1_LVDS_4_N
JX1_LVDS_5_P
JX1_LVDS_5_N
JX1_LVDS_6_P
JX1_LVDS_6_N
JX1_LVDS_7_P
JX1_LVDS_7_N
JX1_LVDS_8_P
JX1_LVDS_8_N
JX1_LVDS_9_P
JX1_LVDS_9_N
JX1_LVDS_10_P
JX1_LVDS_10_N
JX1_LVDS_11_P
JX1_LVDS_11_N
JX1_LVDS_12_P
JX1_LVDS_12_N
JX1_LVDS_13_P
JX1_LVDS_13_N
JX1_LVDS_14_P
JX1_LVDS_14_N
JX1_LVDS_15_P
JX1_LVDS_15_N
JX1_LVDS_16_P
JX1_LVDS_16_N
JX1_LVDS_17_P
JX1_LVDS_17_N
JX1_LVDS_18_P
JX1_LVDS_18_N
JX1_LVDS_19_P
JX1_LVDS_19_N
JX1_LVDS_20_P
JX1_LVDS_20_N
JX1_LVDS_21_P
JX1_LVDS_21_N
JX1_LVDS_22_P
JX1_LVDS_22_N
JX1_LVDS_23_P
JX1_LVDS_23_N
JX2
JX2_LVDS_0_P
JX2_LVDS_0_N
JX2_LVDS_1_P
JX2_LVDS_1_N
JX2_LVDS_2_P
JX2_LVDS_2_N
JX2_LVDS_3_P
JX2_LVDS_3_N
JX2_LVDS_4_P
JX2_LVDS_4_N
JX2_LVDS_5_P
JX2_LVDS_5_N
JX2_LVDS_6_P
JX2_LVDS_6_N
JX2_LVDS_7_P
JX2_LVDS_7_N
JX2_LVDS_8_P
JX2_LVDS_8_N
JX2_LVDS_9_P
JX2_LVDS_9_N
JX2_LVDS_10_P
JX2_LVDS_10_N
JX2_LVDS_11_P
JX2_LVDS_11_N
JX2_LVDS_12_P
JX2_LVDS_12_N
JX2_LVDS_13_P
JX2_LVDS_13_N
JX2_LVDS_14_P
JX2_LVDS_14_N
JX2_LVDS_15_P
JX2_LVDS_15_N
JX2_LVDS_16_P
JX2_LVDS_16_N
JX2_LVDS_17_P
JX2_LVDS_17_N
JX2_LVDS_18_P
JX2_LVDS_18_N
JX2_LVDS_19_P
JX2_LVDS_19_N
JX2_LVDS_20_P
JX2_LVDS_20_N
JX2_LVDS_21_P
JX2_LVDS_21_N
JX2_LVDS_22_P
JX2_LVDS_22_N
JX2_LVDS_23_P
JX2_LVDS_23_N
JX2_SE_0
JX2_SE_1
JT2
Jumper 1K
Default: pin 1-2, 1K
VCCO_34
GND
U1C
BANK 34
1.8V
Zynq 7015/7030 SOC SBG485
WARNING!!!
Bank 34 and Bank 35 are High Performance banks (7030 only) and will only accept 1.8V level signals.
Failure to limit Bank 34 and 35 to 1.8V signals can damage the Zynq 7030 AP SoC.
AVNET
Avnet Engineering Services
Title: 06 - BANKS 34 and 35.SchDoc
Size: B
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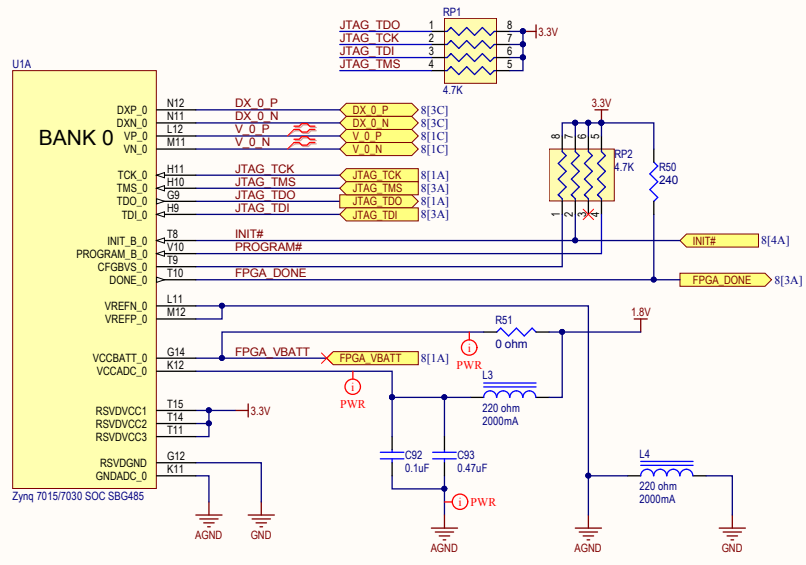

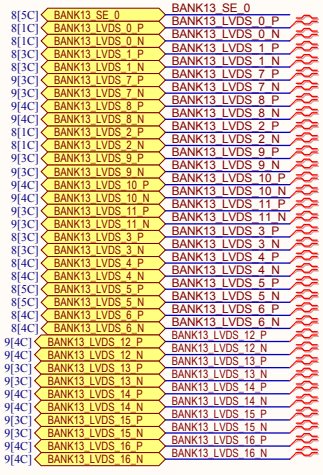

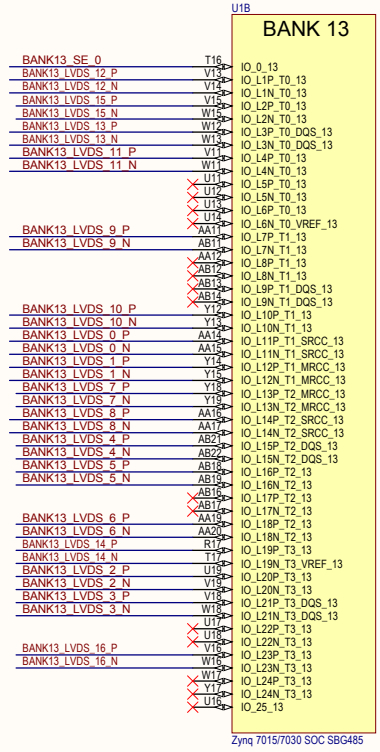

AVNET Avnet Engineering Services			
Title: 07 - BANK 0, BANK13, JTAG.SchDoc			
Size: B	Document Number: PicoZed 7015/7030		Rev: C
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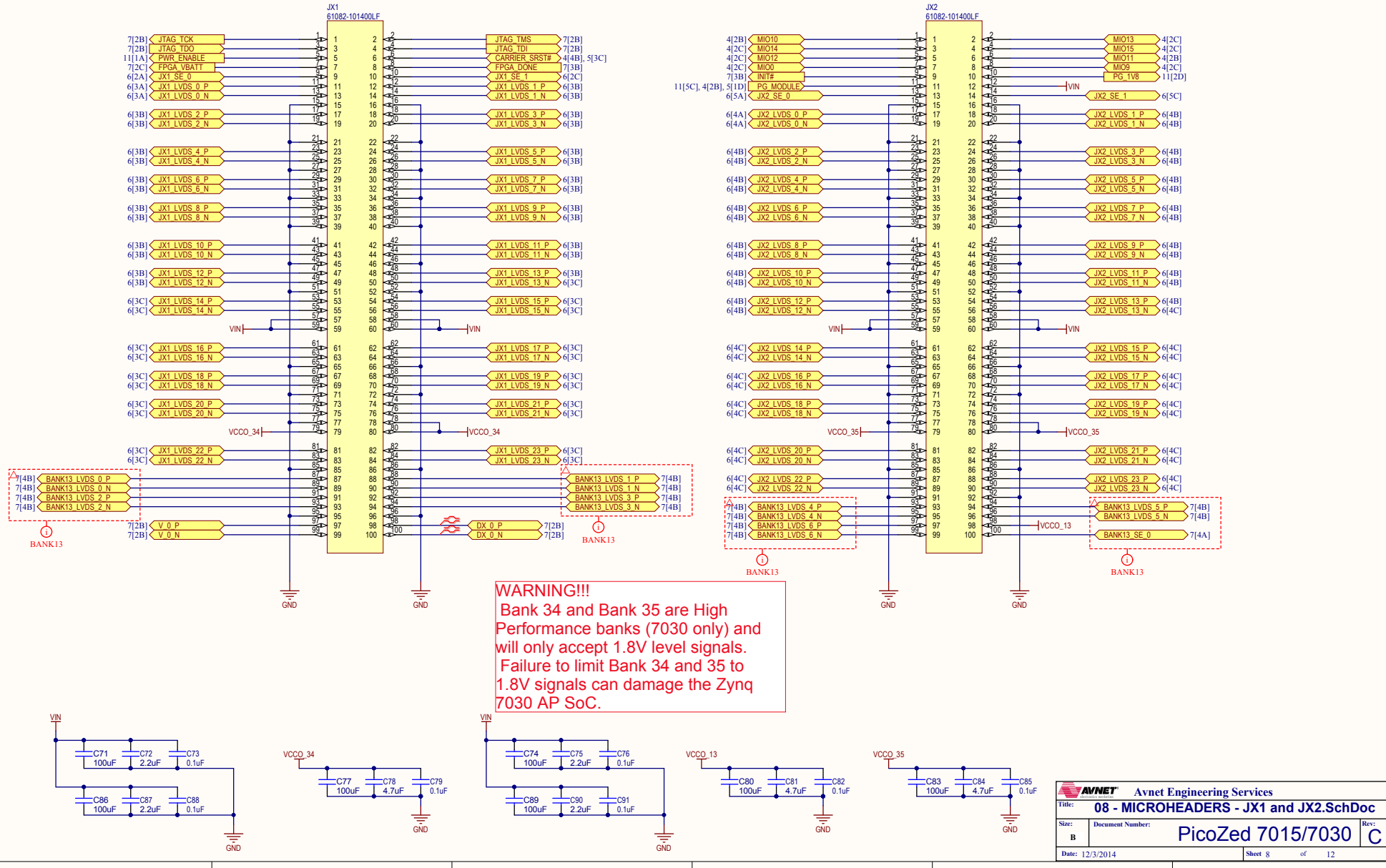
JX1
61082-101400LF
JX2
61082-101400LF
JTAG_TCK
JTAG_TDO
PWR_ENABLE
FPGA_VBATT
JX1_SE_0
JX1_LVDS_0_P
JX1_LVDS_0_N
JTAG_TMS
JTAG_TDI
CARRIER_SRST#
FPGA_DONE
JX1_SE_1
JX1_LVDS_1_P
JX1_LVDS_1_N
JX1_LVDS_2_P
JX1_LVDS_2_N
JX1_LVDS_3_P
JX1_LVDS_3_N
JX1_LVDS_4_P
JX1_LVDS_4_N
JX1_LVDS_5_P
JX1_LVDS_5_N
JX1_LVDS_6_P
JX1_LVDS_6_N
JX1_LVDS_7_P
JX1_LVDS_7_N
JX1_LVDS_8_P
JX1_LVDS_8_N
JX1_LVDS_9_P
JX1_LVDS_9_N
JX1_LVDS_10_P
JX1_LVDS_10_N
JX1_LVDS_11_P
JX1_LVDS_11_N
JX1_LVDS_12_P
JX1_LVDS_12_N
JX1_LVDS_13_P
JX1_LVDS_13_N
JX1_LVDS_14_P
JX1_LVDS_14_N
JX1_LVDS_15_P
JX1_LVDS_15_N
JX1_LVDS_16_P
JX1_LVDS_16_N
JX1_LVDS_17_P
JX1_LVDS_17_N
JX1_LVDS_18_P
JX1_LVDS_18_N
JX1_LVDS_19_P
JX1_LVDS_19_N
JX1_LVDS_20_P
JX1_LVDS_20_N
JX1_LVDS_21_P
JX1_LVDS_21_N
JX1_LVDS_22_P
JX1_LVDS_22_N
JX1_LVDS_23_P
JX1_LVDS_23_N
BANK13_LVDS_0_P
BANK13_LVDS_0_N
BANK13_LVDS_2_P
BANK13_LVDS_2_N
BANK13_LVDS_1_P
BANK13_LVDS_1_N
BANK13_LVDS_3_P
BANK13_LVDS_3_N
V_0_P
V_0_N
DX_0_P
DX_0_N
VIN
VCCO_34
BANK13
GND
MIO10
MIO14
MIO12
MIO0
INIT#
PG_MODULE
JX2_SE_0
JX2_LVDS_0_P
JX2_LVDS_0_N
JX2_LVDS_2_P
JX2_LVDS_2_N
JX2_LVDS_4_P
JX2_LVDS_4_N
JX2_LVDS_6_P
JX2_LVDS_6_N
JX2_LVDS_8_P
JX2_LVDS_8_N
JX2_LVDS_10_P
JX2_LVDS_10_N
JX2_LVDS_12_P
JX2_LVDS_12_N
JX2_LVDS_14_P
JX2_LVDS_14_N
JX2_LVDS_16_P
JX2_LVDS_16_N
JX2_LVDS_18_P
JX2_LVDS_18_N
JX2_LVDS_20_P
JX2_LVDS_20_N
JX2_LVDS_22_P
JX2_LVDS_22_N
BANK13_LVDS_4_P
BANK13_LVDS_4_N
BANK13_LVDS_6_P
BANK13_LVDS_6_N
MIO13
MIO15
MIO11
MIO9
PG_1V8
JX2_SE_1
JX2_LVDS_1_P
JX2_LVDS_1_N
JX2_LVDS_3_P
JX2_LVDS_3_N
JX2_LVDS_5_P
JX2_LVDS_5_N
JX2_LVDS_7_P
JX2_LVDS_7_N
JX2_LVDS_9_P
JX2_LVDS_9_N
JX2_LVDS_11_P
JX2_LVDS_11_N
JX2_LVDS_13_P
JX2_LVDS_13_N
JX2_LVDS_15_P
JX2_LVDS_15_N
JX2_LVDS_17_P
JX2_LVDS_17_N
JX2_LVDS_19_P
JX2_LVDS_19_N
JX2_LVDS_21_P
JX2_LVDS_21_N
JX2_LVDS_23_P
JX2_LVDS_23_N
BANK13_LVDS_5_P
BANK13_LVDS_5_N
BANK13_SE_0
VCCO_35
VCCO_13
WARNING!!!
Bank 34 and Bank 35 are High Performance banks (7030 only) and will only accept 1.8V level signals.
Failure to limit Bank 34 and 35 to 1.8V signals can damage the Zynq 7030 AP SoC.
C71 100uF
C72 2.2uF
C73 0.1uF
C86 100uF
C87 2.2uF
C88 0.1uF
C77 100uF
C78 4.7uF
C79 0.1uF
C74 100uF
C75 2.2uF
C76 0.1uF
C89 100uF
C90 2.2uF
C91 0.1uF
C80 100uF
C81 4.7uF
C82 0.1uF
C83 100uF
C84 4.7uF
C85 0.1uF
Avnet Engineering Services
Title: 08 - MICROHEADERS - JX1 and JX2.SchDoc
Size: B
Document Number: PicoZed 7015/7030
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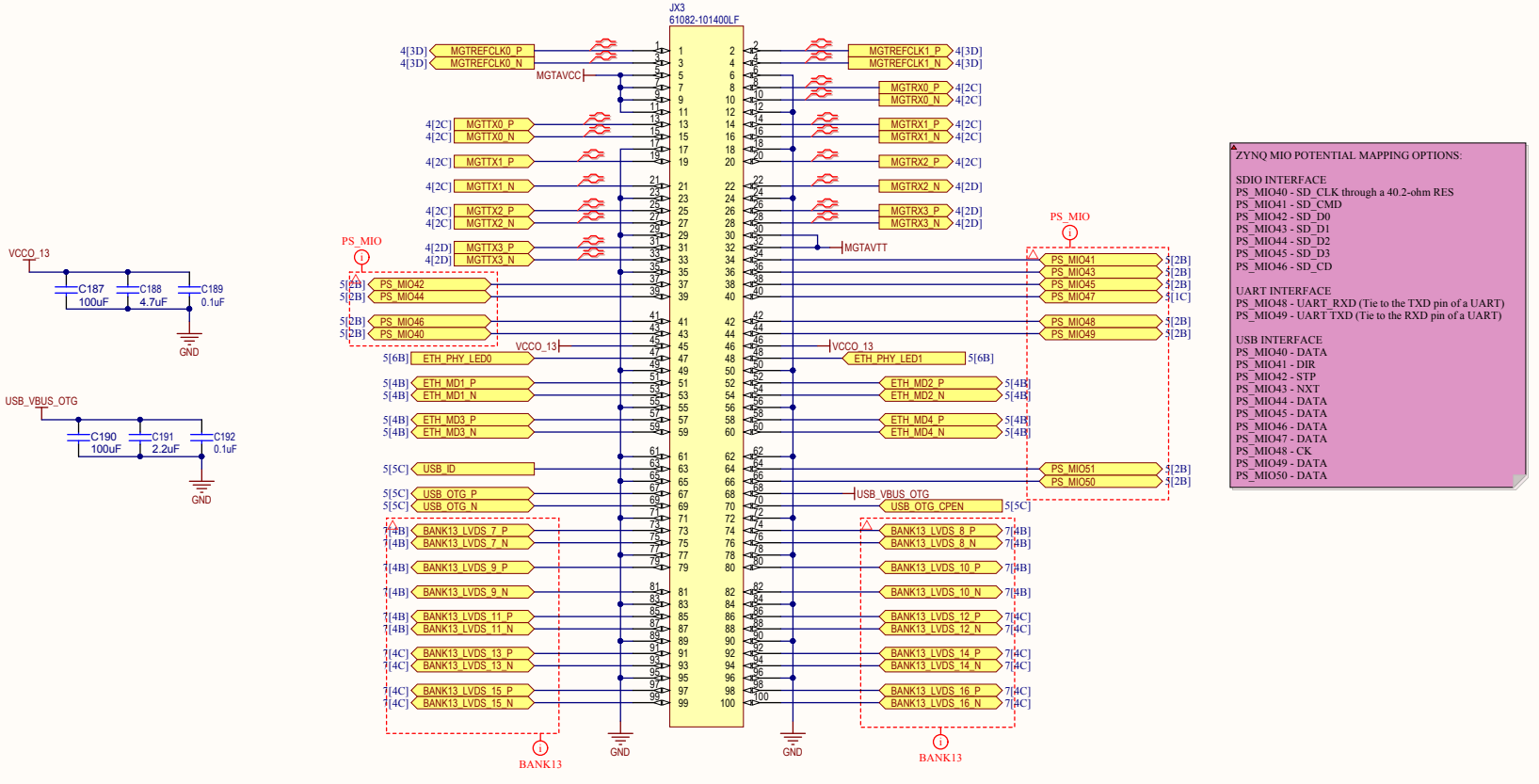

ZYNQ MIO POTENTIAL MAPPING OPTIONS:

SDIO INTERFACE
PS_MIO40 - SD_CLK through a 40.2-ohm RES
PS_MIO41 - SD_CMD
PS_MIO42 - SD_D0
PS_MIO43 - SD_D1
PS_MIO44 - SD_D2
PS_MIO45 - SD_D3
PS_MIO46 - SD_CD

UART INTERFACE
PS_MIO48 - UART_RXD (Tie to the TXD pin of a UART)
PS_MIO49 - UART TXD (Tie to the RXD pin of a UART)

USB INTERFACE
PS_MIO40 - DATA
PS_MIO41 - DIR
PS_MIO42 - STP
PS_MIO43 - NXT
PS_MIO44 - DATA
PS_MIO45 - DATA
PS_MIO46 - DATA
PS_MIO47 - DATA
PS_MIO48 - CK
PS_MIO49 - DATA
PS_MIO50 - DATA

AVNET Avnet Engineering Services		
Title: 09 - MICROHEADER - JX3.SchDoc		
Size: B	Document Number: PicoZed 7015/7030	Rev: C
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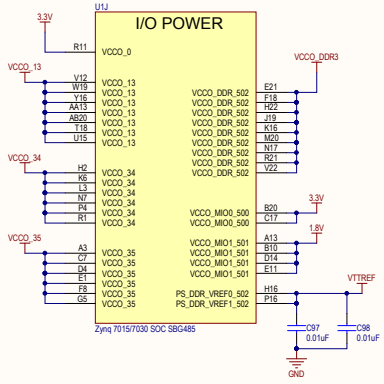

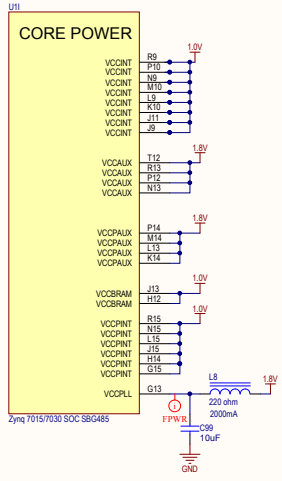

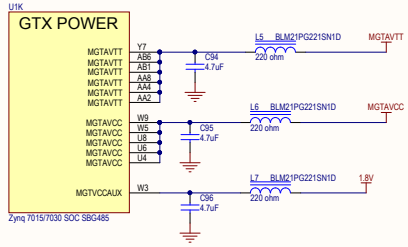

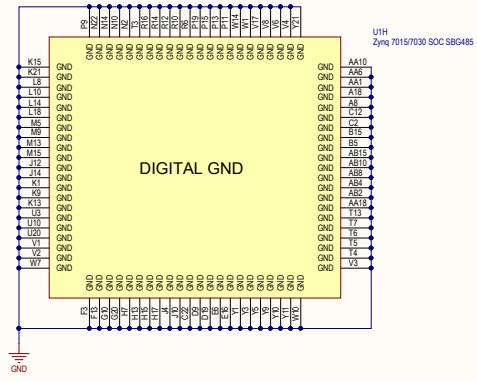

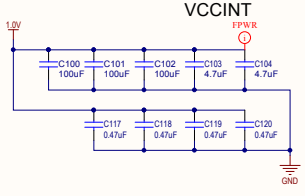

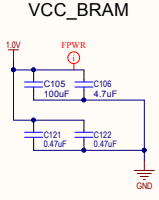

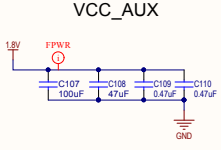

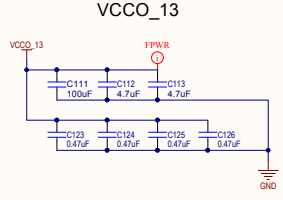

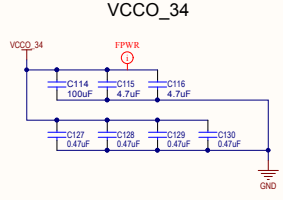

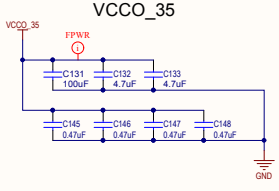

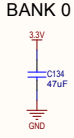

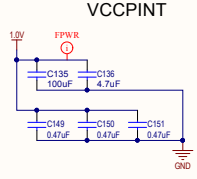

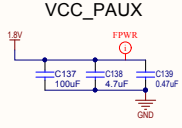

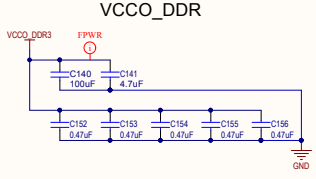

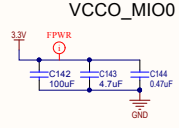

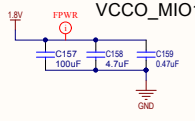

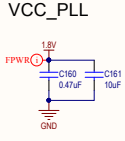

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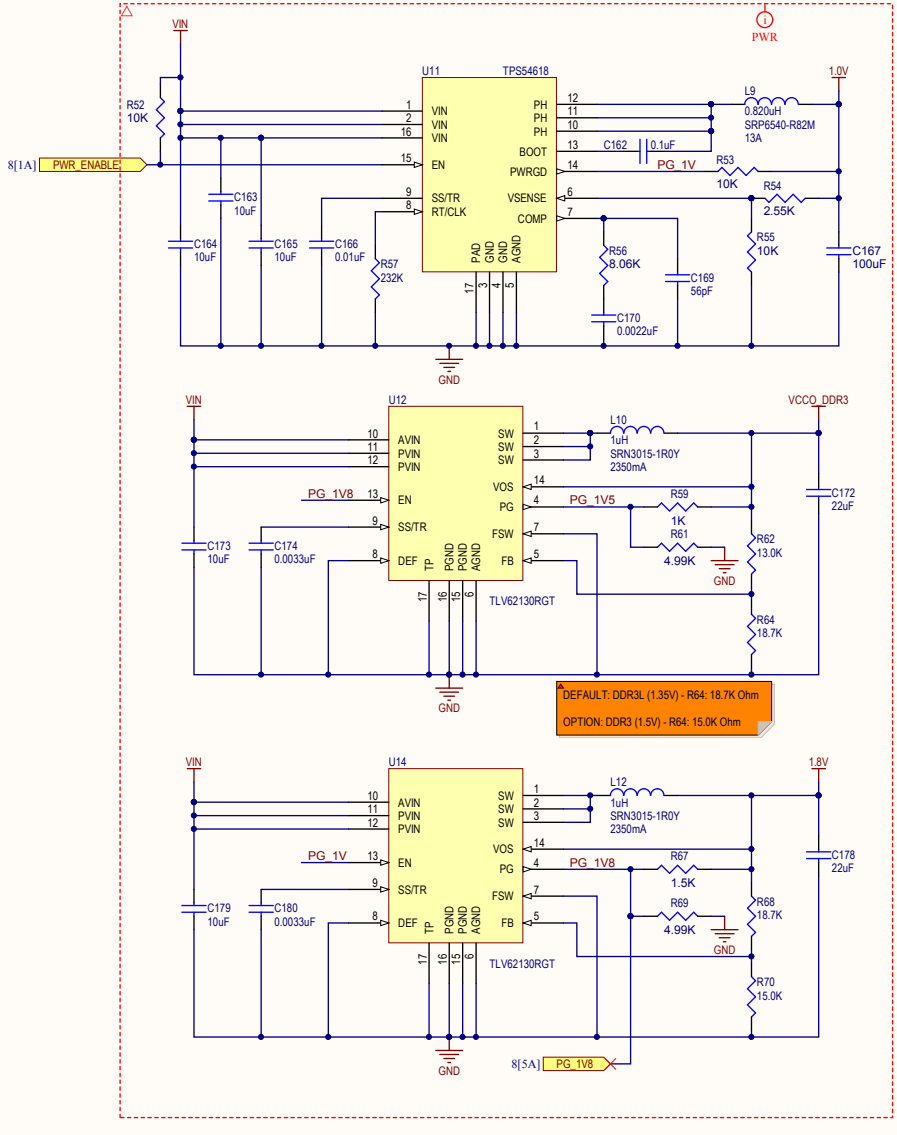

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Size: B	Document Number: PicoZed 7015/7030 Rev: C
Date: 12/3/2014	Sheet 11 of 12

Revision History

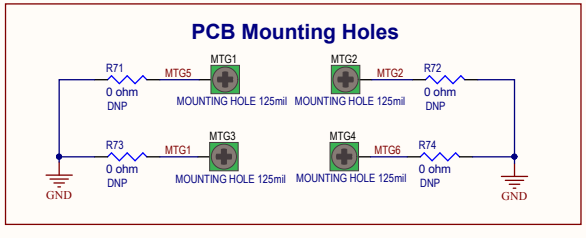
Rev B

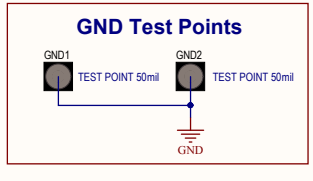
Original release

Rev C

1) Updated Block Diagram
2) Added shared circuit MIO47 to JX3 and ETHERNET RESET
3) Added RC time constant to ETHERNET RESET
4) DDR3L/DDR3 option note added
5) Renamed 1.5V and DDR3_0V75 power nets
6) Changed U4.2 connection from 1.8V to 3.3V
7) Changed JX1/JX2 connections to Zynq Bank 34/35 Clock Capable Pins

Mechanicals:





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