PicoZed 7Z015 / 7Z030 SOM

(System-On Module)

Hardware User Guide

Version 1.1
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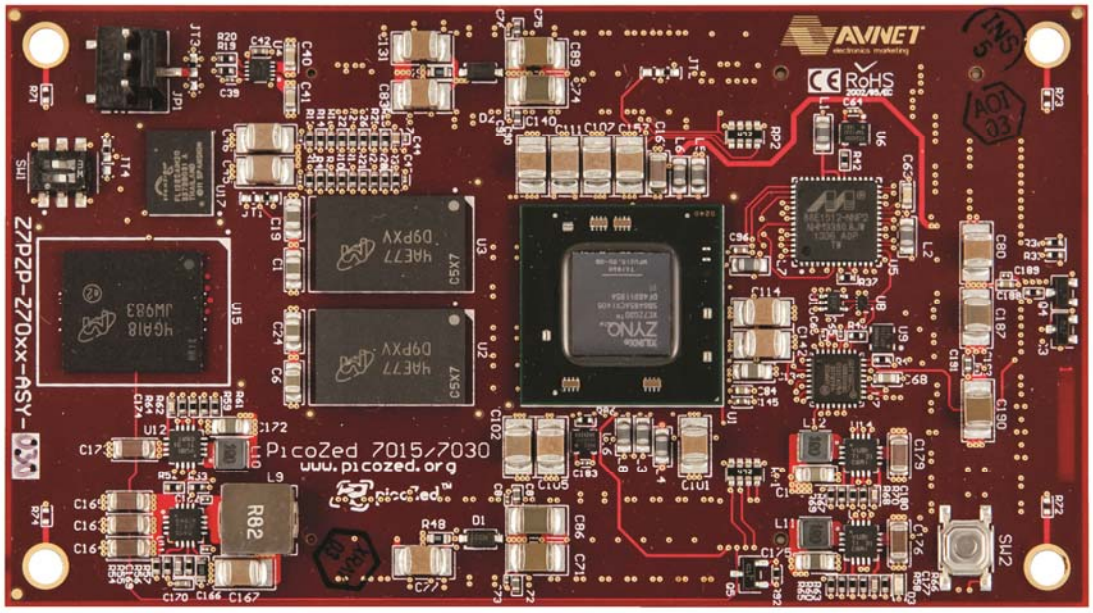

(XC7Z030 Model Shown)

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1 Introduction

The PicoZed 7Z015 / 7Z030 SOM (System-On Module) is a low cost evaluation board targeted for broad use in many applications. The features provided by the PicoZed SOM consist of:

- Xilinx XC7Z015-1CLG485C or Xilinx XC7Z030-1SBG485C AP SOC
  - Primary configuration = QSPI Flash
  - Auxiliary configuration options via Carrier Card
    - JTAG
    - microSD Card
- Four Gigabit Transceivers
  - 3.75Gbps Max Line rate for 7Z015 (GTP)
  - 6.6Gbps Max Line rate for 7Z030 (GTX)
- Memory
  - 1 GB DDR3 (x32)
  - 128 Mb QSPI Flash
  - 4GB eMMC
- Interfaces
  - 10/100/1000 Ethernet
  - USB 2.0 OTG
  - Three 100-pin Micro Headers
- On-board Oscillator
  - 33.333 MHz
- Power
  - High-efficiency regulators for Vccint, Vccpint, Vccbram, Vccaux, Vccpaux, Vccpll, Vcco_0, Vcco_ddr, Vcco_mio, MGT_Vccaux
  - Vcc0_34, Vcco_35 Vcco_13, MGTavtt and MGTavcc are powered from Carrier Card via Two 100-pin Micro Headers

- Software
  - Vivado Design Suite
    - Download from www.xilinx.com/support/download.html
    - Request a free DVD from www.xilinx.com/onlinestore/dvd_fulfillment_request.htm

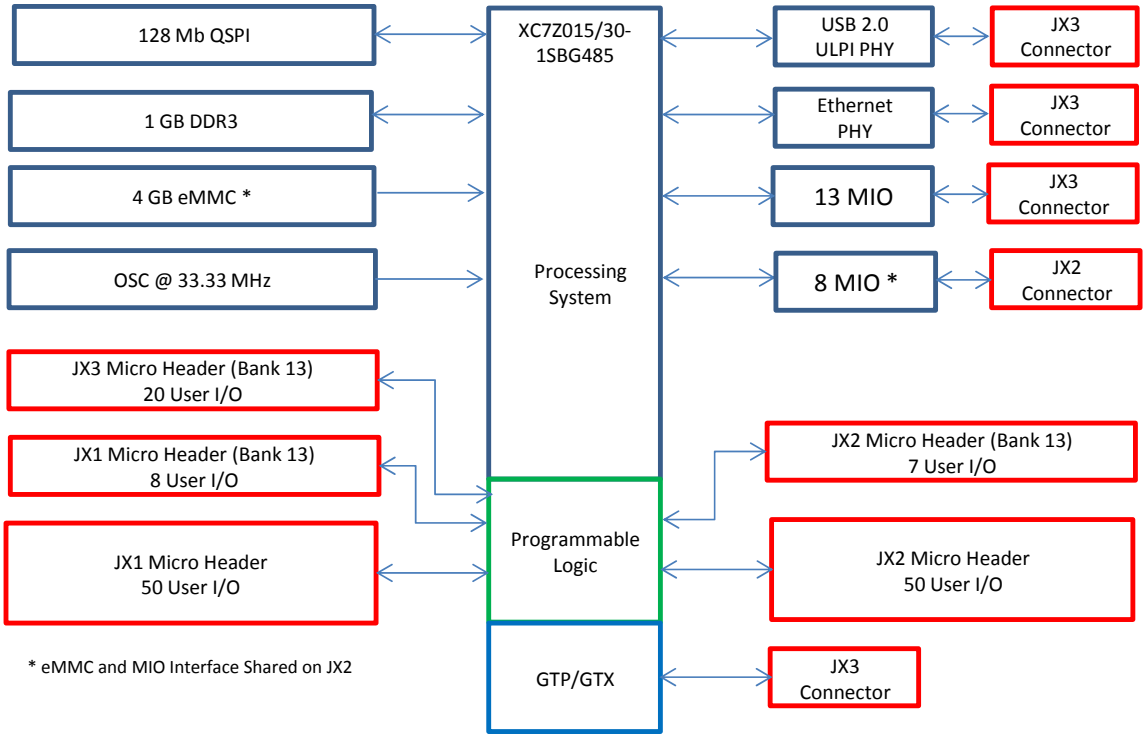

Figure 1 – PicoZed 7015/7030 Block Diagram

2 Functional Description

2.1 All Programmable SoC

PicoZed 7015/7030 includes a Xilinx Zynq XC7Z015-1CLG485 or Zynq XC7Z030-1SBG485 AP SoC. The PicoZed 7015/7030 is available in both commercial and industrial temperature grade options.

2.2 Memory

Zynq contains a hardened PS memory interface unit. The memory interface unit includes a dynamic memory controller and static memory interface modules. PicoZed 7015/7030 takes advantage of these interfaces to provide system RAM as well as two different non-volatile memory sources.

2.2.1 DDR3

PicoZed 7015/7030 includes two Micron MT41K256M16HA-125:E DDR3 memory components creating a 256M x 32-bit interface, totaling 1 GB of random access memory. The DDR3 memory is connected to the hard memory controller in the PS of the Zynq AP SoC. The PS incorporates both the DDR controller and the associated PHY, including its own set of dedicated I/Os.

Speed of up to 1,066 MT/s for DDR3 is supported.

The DDR3L interface uses 1.35V SSTL-compatible inputs by default. There is an option to support 1.5V capable DDR3 devices via a resistor change on the PicoZed 7015/7030. This option is provided as a note on the PicoZed 7015/7030 schematics.

DDR3L Termination is utilized on the PicoZed 7015/7030 and configured for fly-by routing topology, as recommended in UG933. Additionally the board trace lengths are matched, compensating for the XC7Z015-SBG485 internal package flight times, to meet the requirements listed in the Zynq-7000 AP SoC PCB Design and Pin Planning Guide (UG933).

All single-ended signals are routed with 40 ohm trace impedance. DCI resistors (VRP/VRN), as well as differential clocks, are set to 80 ohms. DDR3-CKE0 is terminated through 40 ohms to VTT as described in UG933. DDR3-ODT has the same 40 ohm to VTT termination.

Each DDR3 chip has its own 240-ohm pull-down on ZQ. Note DDR-VREF is not the same as DDR-VTT.

Table 1 – DDR3 Connections

Signal Name	Description	Zynq AP SOC pin	DDR3 pin
DDR_CK_P	Differential clock output	N19	J7
DDR_CK_N	Differential clock output	N18	K7
DDR_CKE	Clock enable	T19	K9
DDR_CS_B	Chip select	P17	L2
DDR_RAS_B	RAS row address select	R18	J3
DDR_CAS_B	RAS column address select	P20	K3
DDR_WE_B	Write enable	R19	L3
DDR_BA[2:0]	Bank address	PS_DDR_BA[2:0]	BA[2:0]
DDR_A[14:0]	Address	PS_DDR_A[14:0]	A[14:0]
DDR_ODT	Output dynamic termination	P18	K1
DDR_RESET_B	Reset	F20	T2
DDR_DQ[31:0]	I/O Data	PS_DDR_[31:0]	DDR3_DQ pins [15:0] x2
DDR_DM[3:0]	Data mask	PS_DDR_DM[3:0]	LDM/UDM x2
DDR_DQS_P[3:0]	I/O Differential data strobe	PS_DDR_DQS_P[3:0]	UDQS/LDQS x2
DDR_DQS_N[3:0]	I/O Differential data strobe	PS_DDR_DQS_N[3:0]	UDQS#/LDQS# x2
DDR_VRP	I/O Used to calibrate input termination	N16	N/A
DDR_VRN	I/O Used to calibrate input termination	M16	N/A
DDR_VREF[1:0]	I/O Reference voltage	H16, P16	VTTREF

2.2.2 Quad SPI Flash

PicoZed 7015/7030 features a 4-bit SPI (quad-SPI) serial NOR flash. The Spansion S25FL128S (S25FL128SAGBHIA00) is used on this board. The Multi-I/O SPI Flash memory is used to provide non-volatile boot, application code, and data storage. It can be used to initialize the PS subsystem as well as configure the PL subsystem (bitstream). Spansion provides Spansion Flash File System (FFS) for use after booting the Zynq-7000 AP SoC.

The relevant device attributes are:

- 128Mbit
- x1, x2, and x4 support
- Speeds up to 104 MHz, supporting Zynq configuration rates @ 100 MHz
  - In Quad-SPI mode, this translates to 400Mbs
- Powered from 3.3V

The SPI Flash connects to the Zynq PS QSPI interface. This requires connection to specific pins in MIO Bank 0/500, specifically MIO[1:6,8] as outlined in the Zynq TRM. Quad-SPI feedback mode is used, thus qspi_sclk_fb_out/MIO[8] is connected to a 20K pull-up resistor to 3.3V and nothing else. This allows a QSPI clock frequency greater than FQSPICLK2. The 20K pull-up straps VMODE[1], setting the Bank 1 Voltage to 1.8V.

Table 2 – QSPI Flash Pin Assignment and Definitions

Signal Name	Description	Zynq Pin	MIO	Quad-SPI Pin
CS	Chip Select	A22 (MIO Bank 0/500)	1	1
DQ0	Data0	A21 (Bank MIO0/500)	2	5
DQ1	Data1	F17 (MIO Bank 0/500)	3	2
DQ2	Data2	E19 (MIO Bank 0/500)	4	3
DQ3	Data3	A20 (MIO Bank 0/500)	5	7
SCK	Serial Data Clock	A19 (MIO Bank 0/500)	6	6
FB Clock	QSPI Feedback	D5 (MIO Bank 0/500)	8	N/A

Note: The QSPI data and clock pins are shared with the VMODE and BOOT_MODE jumpers JT4 and SW1.

2.2.3 eMMC (Multi-Media Card)

PicoZed 7015/7030 features a Micron MTFC4GMDEA-4M IT eMMC Multi Media Controller and NAND Flash IC. The eMMC is used to provide non-volatile user data storage.

The relevant device attributes are:

- 4GB (default)
- Optional densities available via customization
- Industrial temperature range (-40 to +85 C)
- 4-bit data interface
- 50MHz max clock speed
- 25MHz standard Zynq operation
  See Xilinx Answer Record #59999:
  http://www.xilinx.com/support/answers/59999.html

The eMMC connects to the Zynq PS via seven signals by way of 2 4-bit MUXs.

The eMMC I/O is MUXed with direct connections to the Zynq MIO PS_MIO[0, 15:9] pins allowing the user to use the JX2 MIO[0, 15:9] pins as standard I/O or have access to the eMMC I/O. The Zynq PS_MIO0 pin can be used as a MUX select to give the user software control to select either interface in real time. Software control and hardware control of the multiplexer select line is discussed in further detail below.

Software Control of Multiplexer Select

If the user wishes to use software to control the multiplexer select the Zynq PS_MIO0 pin is utilized. When software controls the multiplexer select signal, the running application can select either eMMC accesses for the Zynq or standard MIO interfaces via the JX2 connector. When using software to control the multiplexer select signal, the JX2 MIO interface becomes limited to 7 I/O pins, MIO[15:9] since the Zynq PS_MIO0 pin is being used to control the multiplexer select signal. This option offers the user the most flexibility to connect either interface to the Zynq when needed by the application.

Software control of the Multiplexer Select signal is the default setting for the PicoZed 7015/7030 System-On-Module from the factory, and is enabled by the jumper resistor position at JT6 position 1-2.

In position 1-2 the Zynq PS_MIO0 pin is connected to the multiplexer select pins of U18 and U19.

In position 2-3 the Zynq PS_MIO0 pin is connected to the JX2 MIO0 pin via the multiplexer channel 4 on device U19.

Hardware Control of Multiplexer Select (Interface Strapping)
Another user option available is to “hard-wire” one of the two interfaces, JX2 MIO[0,15:9] or eMMC I/O to the Zynq PS_MIO[0,15:9] pins. This can be done by modifying the resistor jumper position at JT5, which sets the desired interface and JT6, which controls the use of PS_MIO0.

The default resistor jumper position for JT5 is 1-2, which selects the eMMC as the selected interface.

If JT5 resistor jumper position is changed to position 2-3, JX2 MIO pins become selected by the multiplexers. In this case, it is best to also change the JT6 jumper position to 2-3 to ensure that a full 8-bit peripheral can be connected through the JX2 MIO interface if so desired.

The diagram below shows how the eMMC and JX2 MIO signals are connected to the Zynq via the multiplexer ICs U18 and U19.

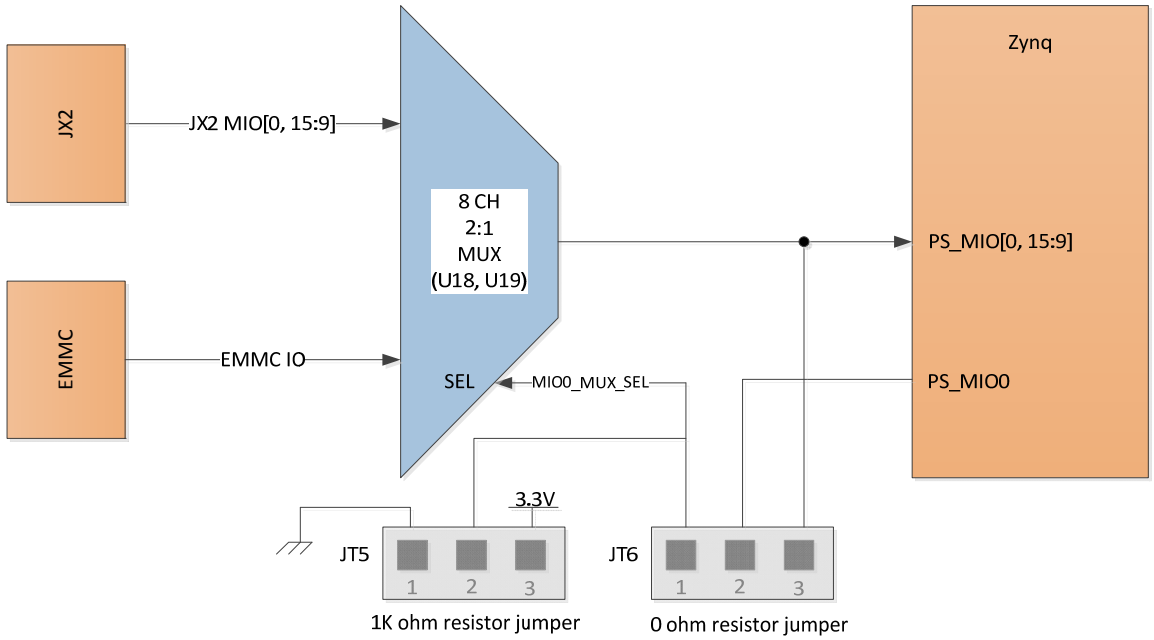

Figure 2 – eMMC / JX2 MIO Multiplexer Block Diagram

2.3 USB 2.0 OTG

2.3.1 USB Host 2.0

Zynq contains a hardened PS USB 2.0 controller. PicoZed 7015/7030 takes advantage of the USB 2.0 controller to provide USB 2.0 On-The-Go signaling to the JX3 connector.

PicoZed 7015/7030 implements one of the two available PS USB 2.0 interfaces. An external PHY with an 8-bit ULPI interface is required. A SMSC USB3320 Standalone USB Transceiver Chip is used as the PHY. The PHY features a complete HS-USB Physical Front-End supporting speeds of up to 480Mbs. VDDIO for this device can be 1.8V or 3.3V, and on the PicoZed 7015/7030 it is powered at 1.8V. The PHY is connected to MIO Bank 1/501, which is also powered at 1.8V. This is critical since a level translator cannot be used as it would impact the tight ULPI timing required between the PHY and the Zynq device.

Additionally the USB chip must clock the ULPI interface which requires a 24 MHz crystal or oscillator (configured as ULPI Output Clock Mode). On the PicoZed 7015/7030, the 24 MHz oscillator is an Abracon ASDMB CMOS oscillator.

The USB connector is not populated on the PicoZed 7015/7013 System-on-Module and is designed to have the USB connector reside on the mating carrier card. The four USB connector signals (USB_P, USB_N, USB_ID and USB_OTG_CPEN) are connected to the JX3 Micro Header. The table below shows the connections of these four signals at JX3.

Table 3 - USB 2.0 JX3 Pin Assignments

Signal Name	JX3 Pin
USB_OTG_N	69
USB_OTG_P	67
USB_ID	63
USB_OTG_CPEN	70

If using the Avnet PicoZed Carrier Card as the mating carrier card, a Micro-AB connector provided by FCI is used. The FCI part number is 10104111-0001LF.

The usb0 peripheral is used on the PS, connected through MIO[28-39] in MIO Bank 1/501. The USB Reset signal connected to MIO[7]. Signal PS_MIO7 is a 3.3V signal. It is AND-ed with the power-on reset (PG_MODULE) signal and then level shifted to 1.8V through a TI TXS0102 level translator before connecting to the USB3320 Pin 27 RESET.

PicoZed 7015/7030 is configured such that either Host Mode (OTG) or Device Mode can used depending on the circuitry of the carrier card. With a standard connection to a baseboard (no power supply used to provide USB power to the connector) the device will operate in Device Mode. Using the USB_OTG_CPEN signal on JX3 allows the user to control an external power source for USB VBUS on the carrier board. Other considerations need to be made to accommodate Host Mode. Refer to the Avnet PicoZed Carrier Card design for an example design for configuring the carrier card for either Host Mode or Device Mode.

Table 4 - USB Host Pin Assignment and Definitions

Signal Name	Description	Zynq Bank	MIO	SMSC 3320 Pin
Data[7:0]	USB Data lines	MIO Bank 1/501	28:39	Data[7:0]
REFCLOCK	USB Clock	MIO Bank 1/501		26
DIR	ULPI DIR output signal	MIO Bank 1/501		31
STP	ULPI STP input signal	MIO Bank 1/501		29
NXT	ULPI NXT output signal	MIO Bank 1/501		2
REFSEL[2:0]	USB Chip Select	N/C	N/C	8,11,14
DP	DP pin of USB Connector			18
DM	DM pin of USB Connector			19
ID	Identification pin of the USB connector			23
RESET_B	Reset	MIO Bank 1/501	7**	27**

** Connected through AND-gate with PG_MODULE through level translator (TI TXS0102DQE).

2.4 10/100/1000 Ethernet PHY

PicoZed 7015/7030 implements a 10/100/1000 Ethernet port for network connection using a Marvell 88E1512 PHY. This part operates at 1.8V. The PHY connects to MIO Bank 1/501 (1.8V) and interfaces to the Zynq-7000 AP SoC via RGMII.

The RJ-45 interface signals are connected to the JX3 Micro Header.

A high-level block diagram the 10/100/1000 Ethernet interface is shown in the following figure.

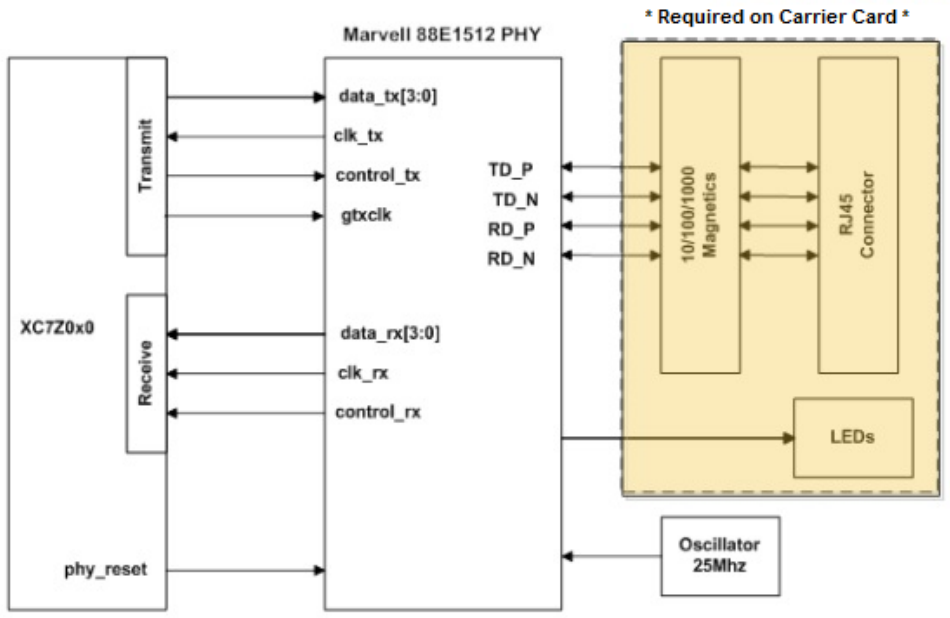

Figure 3 – 10/100/1000 Ethernet Interface

Zynq requires a voltage reference for RGMII interfaces. Thus PS_MIO_VREF, F15, is tied to 0.9V, half the bank voltage of MIO Bank 1/501. The 0.9V is generated through a resistor divider.

The 88E1512 also requires a 25 MHz input clock. An ABRACON ASDMB-25.000MHZ-LC-T is used as this reference.

Table 5 - Ethernet PHY Pin Assignment and Definitions

Signal Name	Description	Zynq pin	MIO	88E1512 pin
RX_CLK	Receive Clock	A9	16:27	46
RX_CTRL	Receive Control	D16		43
RXD[3:0]	Receive Data	RXD0: E12 RXD1: B16 RXD2: F11 RXD3: A10		44 45 47 48
TX_CLK	Transmit Clock	D17		53
TX_CTRL	Transmit Control	F12		56
TXD[3:0]	Transmit Data	TXD0: E14 TXD1: A16 TXD2: E13 TXD3: A15		50 51 54 55
MDIO	Management Data	C11	53	8
MDC	Management Clock	D13	52	7
ETH_RST_N	PHY Reset	B13	47 **	16**

****** Controlled via level translator U8 and can be held low using PG_MODULE signal.

The datasheet for the Marvell 88E1512 is not available publicly. An NDA is required for this information. Please contact your local Avnet or Marvell representative for assistance.

2.5 User I/O

2.5.1 Available PS MIO User Pins

PicoZed 7015/7030 provides 8 user PS MIO pins from bank 500 and 11 user PS MIO pins from bank 501 of the Zynq-7000 AP SoC. The 19 PS MIO pins connect to the Zynq Processor Sub-System for the implementation of peripherals such as SPI, SDIO, CAN, UART, and I2C. These I/O pins can also be used as general purpose IO to connect push buttons, LEDs and/or switches to the Zynq from the carrier card.

Note: The bank 500 PS MIO are shared with the eMMC interface and proper operation of these 8 user PS MIO pins depends on the multiplexer implemented to support the shared interface. Please review section 2.2.3 eMMC (Multi-Media Controller) for details on the multiplexer interface.

Table 6 - PS MIO User Interface

Signal Name	Zynq Pin	JX Pin
PS_MIO0	G17 (MIO Bank 500)	JX2.7
PS_MIO9	C19 (MIO Bank 500)	JX2.8
PS_MIO10	G16 (MIO Bank 500)	JX2.1
PS_MIO11	B19 (MIO Bank 500)	JX2.6
PS_MIO12	C18 (MIO Bank 500)	JX2.5
PS_MIO13	A17 (MIO Bank 500)	JX2.2
PS_MIO14	B17 (MIO Bank 500)	JX2.3
PS_MIO15	E17 (MIO Bank 500)	JX2.4
PS_MIO40	E9 (MIO Bank 501)	JX3.43
PS_MIO41	C15 (MIO Bank 501)	JX3.34
PS_MIO42	D15 (MIO Bank 501)	JX3.37
PS_MIO43	B12 (MIO Bank 501)	JX3.36

PS_MIO44	E10 (MIO Bank 501)	JX3.39
PS_MIO45	B14 (MIO Bank 501)	JX3.38
PS_MIO46	D11 (MIO Bank 501)	JX3.41
PS_MIO47	B13 (MIO Bank 501)	JX3.40
PS_MIO48	D12 (MIO Bank 501)	JX3.42
PS_MIO49	C9 (MIO Bank 501)	JX3.44
PS_MIO50	D10 (MIO Bank 501)	JX3.64
PS_MIO51	C13 (MIO Bank 501)	JX3.66

Note: PS_MIO47 is not implemented on connector JX3. Due to this limitation, USB1 peripheral cannot be implemented on an end user carrier card.

2.5.2 Available PL IO User Pins

PicoZed 7015/7030 provides 50 user PL IO pins from bank 34, 50 user PL IO pins from bank 35 of the Zynq-7000 AP SoC. Additionally, the PicoZed 7015/7030 provides access to 35 more user PL IO pins from bank 13. The PL IO pins are connected to the Zynq Programmable Logic Sub-System for user implementation of any feasible interface.

The PL IO pins were routed with matched lengths to each of the JX connectors. The matched pairs, noted by "LVDS" in the net name of Tables 9, 10 AND 11 may be used as either single ended I/O or differential pairs depending on the end users design requirements.

Use of these signals for various interfaces depends on the bank voltages assigned. The end user carrier card is responsible for providing VCCO for bank 34, bank 35, and bank 13 depending on what it being implemented and whether you are using PicoZed 7015 or PicoZed 7030.

The PicoZed 7030 Banks 34 and 35 operate at 1.8V ONLY as they are high performance banks, while the PicoZed 7015 banks 34 and 35 can operate at 1.8V, 2.5V or 3.3V.

It is recommended that any custom interface to be implemented be run through the Vivado tool suite for a sanity check on place and route and timing closure in advance of end user carrier card manufacturing.

Pin out details of the available PL IO are included in section 2.8: Expansion Headers.

2.6 Clock source

The PicoZed 7015/7030 connects a dedicated 33.3333 MHz clock source to the Zynq-7000 AP SoC's PS. An ABRACON ASDMB-33.333MHZ-LC-T with 40-ohm series termination is used. The PS infrastructure can generate up to four PLL-based clocks for the PL system.

2.7 Reset Sources

2.7.1 Power-on Reset (PS_POR_B)

The Zynq PS supports an external power-on reset signal. The power-on reset is the master reset of the entire chip. This signal resets every register in the device capable of being reset. On PicoZed 7015/7030 this signal is labeled PG_MODULE and it is connected to the power good output of the final stage of the power regulation circuitry. These power supplies have open drain outputs that pull this signal low until the output voltage is valid. If an carrier card is connected to PicoZed 7015/7030, the carrier card should also wire-OR to this net and not release it until the carrier card power is also good. Review the PicoZed 7015/7030 schematic for other devices that are reset by the PG_MODULE open-drain signal.

To stall Zynq boot-up, this signal should be held low. No other signal (SRST, PROGRAM_B, INIT_B) is capable of doing this as in other FPGA architectures.

2.7.2 PROGRAM_B, DONE, PUDC_B, INIT_B Pins

INIT_B, PROGRAM_B and PUDC_B all have pull-up resistors to 3.3V. The INIT_B, PUDC_B and DONE signals are routed to the carrier card via the Micro Headers, JX1 and JX2.

There is not a DONE LED indicator on the PicoZed 7015/7030 System-On-Module. When PL configuration is complete DONE will go high. It is recommended that the DONE signal be connected to an LED on the carrier card to indicate when the FPGA configuration is complete.

When mating to the Avnet PicoZed Carrier Card a blue LED labeled DONE will illuminate.

2.7.3 Processor Subsystem Reset

System reset, labeled PS_SRST_B, resets the processor as well as erases all debug configurations. The external system reset allows the user to reset all of the functional logic within the device without disturbing the debug environment. For example, the previous break points set by the user remain valid after system reset. Due to security concerns, system reset erases all memory content within the PS, including the OCM. The PL is also reset in system reset. System reset does not re-sample the boot mode strapping pins.

This active-low signal can be asserted via the carrier card through the Micro Header interface.

Note: This signal cannot be asserted while the boot ROM is executing following a POR reset. If PS_SRST_B is asserted while the boot ROM is running through a POR reset sequence it will trigger a lock-down event preventing the boot ROM from completing. To recover from lockdown the device either needs to be power cycled or PS_POR_B needs to be asserted.

2.8 Expansion Headers

2.8.1 Micro Headers

PicoZed 7015/7030 features three 100-pin Micro Headers (FCI, 61082-103400LF) for connection to carrier cards.

The JX1 and JX2 connectors interface PL, PS I/O to the carrier card as well as two dedicated analog inputs, the four dedicated JTAG signals, power and control signals.

The JX3 connector interfaces to peripheral interfaces such as Ethernet, microSD Card, UART, Gigabit transceivers (GTP/GTX), USB 2.0 and Bank 13 PL I/O.

The connectors are FCI 0.8mm Bergstak®, 100 Position, Dual Row, BTB Vertical Receptacles. These have variable stack heights from 5mm to 16mm, making it easy to connect to a variety of carrier or system boards. Each pin can carry 500mA of current and support I/O speeds in excess of what Zynq can achieve.

PicoZed 7015/7030 does not power the PL VCCIO banks. This is required to be provided by the carrier card. This gives the carrier card the flexibility to control the I/O bank voltages. Separate routes/planes are used for VCCO_34 and VCCO_35 such that the carrier card could potentially power these independently. The PicoZed 7015/7030 has three PL I/O banks. Banks 34 and 35 each contain 50 I/O. Bank 13 is partially connected (33 I/O) on the PicoZed 7015/7030. Bank 13's power has an independent rail, VCCO_13, which is powered from the carrier card as well.

Within a PL I/O bank, there are 50 I/O capable of up to 24 differential pairs. Differential LVDS pairs on a -1 speed grade device are capable of 950Mbps of DDR data. Each differential pair from Bank 34 and 35 is isolated by a power or ground pin. Additionally, eight of these I/O can be connected as clock inputs (four MRCC and four SRCC inputs). Each PL bank can also be configured to be a memory interface with up to four dedicated DQS data strobes and data byte

groups. Bank 35 adds the capability to use the I/O to interface up to 16 differential analog inputs. One of the differential pairs (JX1_LVDS_2) in Bank 34 is shared with PUDC_B.

The diagram below illustrates the connections on the Micro Headers.

Table 7 – Micro Header JX1 and JX2 Pin-out

Micro Header #1 (JX1)				Micro Header #2 (JX2)			
Signal Name		**Source**	**Pins**	**Signal Name**		**Source**	**Pins**
PL	Bank 35 I/Os	Zynq Bank 35	50	PL	Bank 34 I/Os (except for PUDC_B)	Zynq Bank 34	49
	Bank 13 pins	Bank 13	8		Bank 13 pins	Bank 13	7
JTAG	TMS_0	Zynq Bank 0	5	PS	PS Pmod MIO[0,9-15]	Zynq Bank 500	8
	TDI_0	Zynq Bank 0		C	Init_B_0	Zynq Bank 0	2
	TCK_0	Zynq Bank 0			PUDC_B / IO	Zynq Bank 34	
	TDO_0	Zynq Bank 0		Power	PG_1V8	Module/Carrier	1
	Carrier_SRST#	Carrier			PG_MODULE	Module/Carrier	1
Analog	VP_0	Zynq Bank 0	4		Vin	Carrier	5
	VN_0	Zynq Bank 0			GND	Carrier	23
	DXP_0	Zynq Bank 0			VCCO_35	Carrier	3
	DXN_0	Zynq Bank 0			VCCO_13	Carrier	1
C	FPGA_DONE	Zynq Bank 0	1	**Total**			100
	PWR_Enable	Carrier	1				
	Vin	Carrier	4				
	GND	Carrier	23				
	VCCO_34	Carrier	3				
	VBATT	Carrier	1				
TOTAL			100				

Table 8 – Micro Header JX3 Pin-out

Micro Header #3 (JX3)			
Signal Name		**Source**	**Pins**
PL	Bank 13 I/Os	Zynq Bank 13	20
PS	Ethernet I/O	501	10
	USB I/O	501	4
	PS MIO[40-51]	Zynq Bank 501	12
MGT	MGTREFCLK_P/N[1:0]	Zynq Bank 112	20
	MGTTX_P/N[3:0]		
	MGTRX_P/N[3:0]		
Power	MGTAVCC	Carrier	4
	MGTAVTT	Carrier	2
	VCCO_13	Carrier	2
	GND	Carrier	25
	USB_VBUS_OTG	Carrier	1
Total			100

Table 9 – JX1 Connections

SoC Pin #	PicoZed 7015/7030 Net	JX1 Pin #	JX1 Pin #	PicoZed 7015/7030 Net	SoC Pin #
Bank 0, H11	JTAG_TCK	1	2	JTAG_TMS	Bank 0, H10
Bank 0, G9	JTAG_TDO	3	4	JTAG_TDI	Bank 0, H9
N/A	PWR_ENABLE	5	6	CARRIER_SRST#	N/A
N/A	FPGA_VBATT	7	8	FPGA_DONE	Bank 500, T10
Bank 35, H6	JX1_SE_0	9	10	JX1_SE_1	Bank 35, H5
Bank 35, H4	JX1_LVDS_0_P	11	12	JX1_LVDS_1_P	Bank 35, F5
Bank 35, H3	JX1_LVDS_0_N	13	14	JX1_LVDS_1_N	Bank 35, E5
N/A	**GND**	15	16	**GND**	N/A
Bank 35, G3	JX1_LVDS_2_P	17	18	JX1_LVDS_3_P	Bank 35, F2
Bank 35, G2	JX1_LVDS_2_N	19	20	JX1_LVDS_3_N	Bank 35, F1
N/A	**GND**	21	22	**GND**	N/A
Bank 35, G4	JX1_LVDS_4_P	23	24	JX1_LVDS_5_P	Bank 35, E4
Bank 35, F4	JX1_LVDS_4_N	25	26	JX1_LVDS_5_N	Bank 35, E3
N/A	**GND**	27	28	**GND**	N/A
Bank 35, G6	JX1_LVDS_6_P	29	30	JX1_LVDS_7_P	Bank 35, B2
Bank 35, F6	JX1_LVDS_6_N	31	32	JX1_LVDS_7_N	Bank 35, B1
N/A	**GND**	33	34	**GND**	N/A
Bank 35, E8	JX1_LVDS_8_P	35	36	JX1_LVDS_9_P	Bank 35, H1
Bank 35, D8	JX1_LVDS_8_N	37	38	JX1_LVDS_9_N	Bank 35, G1
N/A	**GND**	39	40	**GND**	N/A
Bank 35, C6	JX1_LVDS_10_P	41	42	JX1_LVDS_11_P	Bank 35, D5
Bank 35, C5	JX1_LVDS_10_N	43	44	JX1_LVDS_11_N	Bank 35, C4
N/A	**GND**	45	46	**GND**	N/A
Bank 35, B4	JX1_LVDS_12_P	47	48	JX1_LVDS_13_P	Bank 35, D3
Bank 35, B3	JX1_LVDS_12_N	49	50	JX1_LVDS_13_N	Bank 35, C3

N/A	**GND**	51	52	**GND**	N/A
Bank 35, D1	JX1_LVDS_14_P	53	54	JX1_LVDS_15_P	Bank 35, A2
Bank 35, C1	JX1_LVDS_14_N	55	56	JX1_LVDS_15_N	Bank 35, A1
N/A	**VIN**	57	58	**VIN**	N/A
N/A	**VIN**	59	60	**VIN**	N/A
Bank 35, E2	JX1_LVDS_16_P	61	62	JX1_LVDS_17_P	Bank 35, D7
Bank 35, D2	JX1_LVDS_16_N	63	64	JX1_LVDS_17_N	Bank 35, D6
N/A	**GND**	65	66	**GND**	N/A
Bank 35, F7	JX1_LVDS_18_P	67	68	JX1_LVDS_19_P	Bank 35, A5
Bank 35,E7	JX1_LVDS_18_N	69	70	JX1_LVDS_19_N	Bank 35, A4
N/A	**GND**	71	72	**GND**	N/A
Bank 35, G8	JX1_LVDS_20_P	73	74	JX1_LVDS_21_P	Bank 35, A7
Bank 35, G7	JX1_LVDS_20_N	75	76	JX1_LVDS_21_N	Bank 35, A6
N/A	**GND**	77	78	**VCCO_34**	N/A
N/A	**VCCO_34**	79	80	**VCCO_34**	N/A
Bank 35, B7	JX1_LVDS_22_P	81	82	JX1_LVDS_23_P	Bank 35, C8
Bank 35, B6	JX1_LVDS_22_N	83	84	JX1_LVDS_23_N	Bank 35, B8
N/A	**GND**	85	86	**GND**	N/A
Bank 13, AA14	BANK13_LVDS_0_P	87	88	BANK13_LVDS_1_P	Bank 13, Y14
Bank 13, AA15	BANK13_LVDS_0_N	89	90	BANK13_LVDS_1_N	Bank 13, Y15
Bank 13, U19	BANK13_LVDS_2_P	91	92	BANK13_LVDS_3_P	Bank 13, V18
Bank 13, V19	BANK13_LVDS_2_N	93	94	BANK13_LVDS_3_N	Bank 13, W18
N/A	**GND**	95	96	**GND**	N/A
Bank 0, L12	VP_0_P	97	98	DXP_0_P	Bank 0, N12
Bank 0, M11	VN_0_N	99	100	DXN_0_N	Bank 0, N11

Table 10 – JX2 Connections

SoC Pin #	PicoZed 7015/7030 Net	JX2 Pin #	JX2 Pin #	PicoZed 7015/7030 Net	SoC Pin #
Bank 500, G16	MIO10	1	2	MIO13	Bank 500, A17
Bank 500, B17	MIO14	3	4	MIO15	Bank 500, E17
Bank 500, C18	MIO12	5	6	MIO11	Bank 500, B19
Bank 500, G17	MIO0	7	8	MIO9	Bank 500, C19
Bank 0, T8	INIT#	9	10	PG_1V8	N/A
N/A	PG_MODULE	11	12	**VIN**	N/A
Bank 34, H8	JX2_SE_0	13	14	JX2_SE_1	Bank 34, R8
N/A	**GND**	15	16	**GND**	N/A
Bank 34, M4	JX2_LVDS_0_P	17	18	JX2_LVDS_1_P	Bank 34, J2
Bank 34, M3	JX2_LVDS_0_N	19	20	JX2_LVDS_1_N	Bank 34, J1
N/A	**GND**	21	22	**GND**	N/A
Bank 34, K7	JX2_LVDS_2_P	23	24	JX2_LVDS_3_P	Bank 34, J3
Bank 34, L7	JX2_LVDS_2_N	25	26	JX2_LVDS_3_N	Bank 34, K2
N/A	**GND**	27	28	**GND**	N/A
Bank 34, P7	JX2_LVDS_4_P	29	30	JX2_LVDS_5_P	Bank 34, L2
Bank 34, R7	JX2_LVDS_4_N	31	32	JX2_LVDS_5_N	Bank 34, L1
N/A	**GND**	33	34	**GND**	N/A
Bank 34, N4	JX2_LVDS_6_P	35	36	JX2_LVDS_7_P	Bank 34, P3
Bank 34, N3	JX2_LVDS_6_N	37	38	JX2_LVDS_7_N	Bank 34, P2
N/A	**GND**	39	40	**GND**	N/A
Bank 34, M2	JX2_LVDS_8_P	41	42	JX2_LVDS_9_P	Bank 34, N1
Bank 34, M1	JX2_LVDS_8_N	43	44	JX2_LVDS_9_N	Bank 34, P1
N/A	**GND**	45	46	**GND**	N/A
Bank 34, K4	JX2_LVDS_10_P	47	48	JX2_LVDS_11_P	Bank 34, L5
Bank 34, K3	JX2_LVDS_10_N	49	50	JX2_LVDS_11_N	Bank 34, L4

N/A	**GND**	51	52	**GND**	N/A
Bank 34, T2	JX2_LVDS_12_P	53	54	JX2_LVDS_13_P	Bank 34, U2
Bank 34, T1	JX2_LVDS_12_N	55	56	JX2_LVDS_13_N	Bank 34, U1
N/A	**VIN**	57	58	**VIN**	N/A
N/A	**VIN**	59	60	**VIN**	N/A
Bank 34, R3	JX2_LVDS_14_P	61	62	JX2_LVDS_15_P	Bank 34, L6
Bank 34, R2	JX2_LVDS_14_N	63	64	JX2_LVDS_15_N	Bank 34, M6
N/A	**GND**	65	66	**GND**	N/A
Bank 34, J5	JX2_LVDS_16_P	67	68	JX2_LVDS_17_P	Bank 34, R5
Bank 34, K5	JX2_LVDS_16_N	69	70	JX2_LVDS_17_N	Bank 34, R4
N/A	**GND**	71	72	**GND**	N/A
Bank 34, J7	JX2_LVDS_18_P	73	74	JX2_LVDS_19_P	Bank 34, P6
Bank 34, J6	JX2_LVDS_18_N	75	76	JX2_LVDS_19_N	Bank 34, P5
N/A	**GND**	77	78	**VCCO_35**	N/A
N/A	**VCCO_35**	79	80	**VCCO_35**	N/A
Bank 34, J8	JX2_LVDS_20_P	81	82	JX2_LVDS_21_P	Bank 34,N6
Bank 34, K8	JX2_LVDS_20_N	83	84	JX2_LVDS_21_N	Bank 34,N5
N/A	**GND**	85	86	**GND**	N/A
Bank 34, M8	JX2_LVDS_22_P	87	88	JX2_LVDS_23_P	Bank 34, N8
Bank 34, M7	JX2_LVDS_22_N	89	90	JX2_LVDS_23_N	Bank 34, P8
N/A	**GND**	91	92	**GND**	N/A
Bank 13, AB21	BANK13_LVDS_4_P	93	94	BANK13_LVDS_5_P	Bank 13, AB18
Bank 13, AB22	BANK13_LVDS_4_N	95	96	BANK13_LVDS_5_N	Bank 13, AB19
Bank 13, AA19	BANK13_LVDS_6_P	97	98	**VCCO_13**	N/A
Bank 13, AA20	BANK13_LVDS_6_N	99	100	BANK13_SE_0	Bank 13, T16

Table 11 – JX3 Connections

SoC Pin #	PicoZed 7015/7030 Net	JX3 Pin #	JX3 Pin #	PicoZed 7015/7030 Net	SoC Pin #
Bank 112, U9	MGTREFCLK0_P	1	2	MGTREFCLK1_P	Bank 112, U5
Bank 112, V9	MGTREFCLK0_N	3	4	MGTREFCLK1_N	Bank 112, V5
N/A	**MGTAVCC**	5	6	**GND**	N/A
N/A	**MGTAVCC**	7	8	MGTRX0_P	Bank 112, AA7
N/A	**MGTAVCC**	9	10	MGTRX0_N	Bank 112, AB7
N/A	**MGTAVCC**	11	12	**GND**	N/A
Bank 112, AA3	MGTTX0_P	13	14	MGTRX1_P	Bank 112, W8
Bank 112, AB3	MGTTX0_N	15	16	MGTRX1_N	Bank 112, Y8
N/A	**GND**	17	18	**GND**	N/A
Bank 112, W4	MGTTX1_P	19	20	MGTRX2_P	Bank 112, AA9
Bank 112, Y4	MGTTX1_N	21	22	MGTRX2_N	Bank 112, AB9
N/A	**GND**	23	24	**GND**	N/A
Bank 112, AA5	MGTTX2_P	25	26	MGTRX3_P	Bank 112, W6
Bank 112, AB5	MGTTX2_N	27	28	MGTRX3_N	Bank 112, Y6
N/A	**GND**	29	30	**MGTAVTT**	N/A
Bank 112, W2	MGTTX3_P	31	32	**MGTAVTT**	N/A
Bank 112, Y2	MGTTX3_N	33	34	PS_MIO41	Bank 501, C15
N/A	**GND**	35	36	PS_MIO43	Bank 501, B12
Bank 501, D15	PS_MIO42	37	38	PS_MIO45	Bank 501, B14
Bank 501, E10	PS_MIO44	39	40	**GND**	N/A
Bank 501, D11	PS_MIO46	41	42	PS_MIO48	Bank 501, D12
Bank 501, E9	PS_MIO40	43	44	PS_MIO49	Bank 501, C9

N/A	**VCCO_13**	45	46	**VCCO_13**	N/A
N/A	ETH_PHY_LED0	47	48	EETH_PHY_LED1	N/A
N/A	**GND**	49	50	**GND**	N/A
N/A	ETH_MD1_P	51	52	ETH_MD2_P	N/A
N/A	ETH_MD1_N	53	54	ETH_MD2_N	N/A
N/A	**GND**	55	56	**GND**	N/A
N/A	ETH_MD3_P	57	58	ETH_MD4_P	N/A
N/A	ETH_MD3_N	59	60	ETH_MD4_N	N/A
N/A	**GND**	61	62	**GND**	N/A
N/A	USB_ID	63	64	PS_MIO51	Bank 501, C13
N/A	**GND**	65	66	PS_MIO50	Bank 501, D10
N/A	USB_OTG_P	67	68	**USB_VBUS_OTG**	N/A
N/A	USB_OTG_N	69	70	USB_OTG_CPEN	N/A
N/A	**GND**	71	72	**GND**	N/A
Bank 13, Y18	BANK13_LVDS_7_P	73	74	BANK13_LVDS_8_P	Bank 13, AA16
Bank 13, Y19	BANK13_LVDS_7_N	75	76	BANK13_LVDS_8_N	Bank 13, AA17
N/A	**GND**	77	78	**GND**	N/A
Bank 13, AA11	BANK13_LVDS_9_P	79	80	BANK13_LVDS_10_P	Bank 13, Y12
Bank 13, AB11	BANK13_LVDS_9_N	81	82	BANK13_LVDS_10_N	Bank 13, Y13
N/A	**GND**	83	84	**GND**	N/A
Bank 13, V11	BANK13_LVDS_11_P	85	86	BANK13_LVDS_12_P	Bank 13, V13
Bank 13, W11	BANK13_LVDS_11_N	87	88	BANK13_LVDS_12_N	Bank 13, V14
N/A	**GND**	89	90	**GND**	N/A
Bank 13, W12	BANK13_LVDS_13_P	91	92	BANK13_LVDS_14_P	Bank 13, R17
Bank 13, W13	BANK13_LVDS_13_N	93	94	BANK13_LVDS_14_N	Bank 13, T17
N/A	**GND**	95	96	**GND**	N/A
Bank 13, V15	BANK13_LVDS_15_P	97	98	BANK13_LVDS_16_P	Bank 13, V16
Bank 13, W15	BANK13_LVDS_15_N	99	100	BANK13_LVDS_16_N	Bank 13, W16

2.9 Multi-Gigabit Transceivers (MGTs)

PicoZed 7015/7030 has four gigabit full-duplex transceiver lanes that reside on Bank 112 of the Zynq device. These high speed transceivers can be used to interface to multiple high speed interface protocols such as PCI Express, Ethernet, Serial ATA and more.

The XC7Z015-1CLG484 is enabled with GTP transceivers which are capable of a transceiver data rate up to 3.75Gb/s. Speed grade devices of -2 or -3 are capable of data transceiver rates up to 6.25Gb/s.

The Xilinx XC7Z030-1SBG485 is enabled with GTX transceivers which are capable of a transceiver data rate up to 6.6Gb/s. Speed grade devices of -2 or -3 are also capable of data transceiver rates up to 6.6Gb/s in the SB package.

Two differential MGT reference clock inputs are available for use with the GTP/GTX lanes. Either clock input can be used as the clock reference for any one or more of the GT lanes in bank 112. This allows the user to implement various protocols requiring different line rates.

Gigabit transceiver lanes and their associated reference clocks are connected to the carrier board via the JX3 Micro Header. The table below shows the connections between the Zynq device and the JX Micro Header.

Table 12 – MGT Pin Assignments

GTP/GTX	Net Name	Zynq Pin	JX3 Pin
MGT0	MGTTX0_P	AA3	JX3.13
	MGTTX0_N	AB3	JX3.15
	MGTRX0_P	AA7	JX3.8
	MGTRX0_N	AB7	JX3.10
MGT1	MGTTX1_P	W4	JX3.19
	MGTTX1_N	Y4	JX3.21
	MGTRX1_P	W8	JX3.14
	MGTRX1_N	Y8	JX3.16
MGT2	MGTTX2_P	AA5	JX3.25
	MGTTX2_N	AB5	JX3.27
	MGTRX2_P	AA9	JX3.20
	MGTRX2_N	AB9	JX3.22
MGT3	MGTTX3_P	W2	JX3.31
	MGTTX3_N	Y2	JX3.33
	MGTRX3_P	W6	JX3.26
	MGTRX3_N	Y6	JX3.28
MGT_REFCLK0	MGTREFCLK0_P	U9	JX3.1
	MGTREFCLK0_N	V9	JX3.3
MGT_REFCLK1	MGTREFCLK1_P	U5	JX3.2
	MGTREFCLK1_N	V5	JX3.4

2.10 Configuration Modes

Zynq-7000 AP SoC devices use a multi-stage boot process that supports both non-secure and secure boot. The PS is the master of the boot and configuration process. Upon reset, the device mode pins are read to determine the primary boot device to be used: NOR, NAND, Quad-SPI, SD Card or JTAG. PicoZed 7015/7030 allows 3 of those boot devices: QSPI is the default, while SD Card and JTAG boot are easily accessible by changing switch settings.

Note: SD Card and JTAG interfaces should be implemented on the end user carrier card.

Zynq has Voltage Mode pins, which are fixed on PicoZed 7015/7030

The boot mode pins are shared with MIO[8:2]. The usage of these mode pins can be and are used as follows:

- MIO[2] / Boot_Mode[3]
  - sets the JTAG mode
- MIO[5:3] / Boot_Mode[2:0]
  - select the boot mode
  - Boot_Mode[1] is fixed since it is only required for NOR boot, which is not supported on PicoZed 7015/7030
- MIO[6] / Boot_Mode[4]
  - enables the internal PLL
  - fixed to ‘enabled’ on PicoZed 7015/7030
- MIO[8:7] / Vmode[1:0]

- configures the I/O bank voltages
- fixed on PicoZed 7015/7030
- MIO Bank 0 / 500 (MIO[7] / Vmode[0]) set to '0' for 3.3V
- MIO Bank 1 / 501 (MIO[8] / Vmode[1]) set to '1' for 1.8V

All mode pins are pulled either high or low through a 20 KΩ resistor that is either hard wired or connected to a switch or resistor jumper. By default, four mode signals are not jumper-adjustable and are populated as follows:

- MIO[3] / Boot_Mode[1] is pulled low via 20 KΩ resistor.
- MIO[6] / Boot_Mode[4] is pulled low via 20 KΩ resistor.
- MIO[7] / Vmode[0] is pulled low via 20 KΩ resistor.
- MIO[8] / Vmode[1] is pulled high via 20 KΩ resistor.

The other three mode signals, MIO[2], MIO[4] and MIO[5], are configurable via a jumper resistor or switch setting.

MIO[2] is pulled either high or low via a 0 ohm resistor jumper JT4. Default setting from the factory it is pulled low (position 1-2) and puts the Zynq in Cascade JTAG mode.

MIO[5:4] is pulled high or low via a two channel dip switch SW1. Setting the switch positions will determine whether the Zynq boots from QSPI or from the microSD card.

The table below shows the available boot mode configuration setting using JT4 and SW1.

Table 13 – PicoZed 7015/7030 Configuration Modes

BOOT MODE	JT4	SW1 (1-3)	SW1 (4-6)
QSPI	X	LOW (2-3)	HIGH (4-5)
SD CARD	X	HIGH (1-2)	HIGH (4-5)
JTAG	X	LOW (2-3)	LOW (5-6)
IND JTAG	HIGH (2-3)	LOW (2-3)	LOW (5-6)
CASCADE JTAG	LOW (1-2)	LOW (2-3)	LOW (5-6)

SD CARD BOOT MODE

QSPI BOOT MODE

Zynq has many other configuration options, PicoZed 7015/7030 uses this configuration:

- V_{CCO_0} is tied to 3.3V on PicoZed 7015/7030.
- PUDC_B can be pulled high or low on PicoZed 7015/7030 via a resistor (JT2). This active-low input enables internal pull-ups during configuration on all SelectIO pins. By default, JT2 is populated with a 1K resistor in the 1-2 position, which pulls down PUDC_B and enables the pull-ups during configuration. PUDC_B is shared with Bank 34 I/O IO_L3P and is connected to the Micro Header.
- Init_B is pulled high via a 4.7KΩ resistor (RP2.2), but also connected to the Micro Header.

- Program_B is pulled high via a 4.7KΩ resistor (RP2.4).
- CFGBVS is pulled high via a 4.7KΩ resistor (RP2.1).

The PS is responsible for reconfiguring the PL. Zynq will not automatically reconfigure the PL as in standard FPGAs by toggling PROG. Likewise, it is not possible to hold off Zynq boot up with INIT_B as this is now done with POR. If the application needs to reconfigure the PL, the software design must do this, or you can toggle POR to restart everything. When PL configuration is complete and the end user is using the Avnet PicoZed FMC Carrier Card, a blue LED will illuminate.

2.10.1 JTAG Connections

PicoZed 7015/7030 requires an external JTAG cable connector populated on the carrier card for JTAG operations. JTAG signals are routed from Bank 0 of the Zynq to the Micro Header JX1. The following table shows the JTAG signal connections between the Zynq and the Micro Header.

The Zynq Bank 0 reference voltage, Vcco_0, is connected to 3.3V. The JTAG Vref on the End User Carrier Card should be connected to 3.3V to ensure compatibility between the interfaces. For reference, see the PicoZed FMC Carrier Card schematics.

Table 14 – JTAG Pin Connections

SoC Pin #	PicoZed 7015/7030 Net	JX1 Pin #
H11	JTAG_TCK	1
H10	JTAG_TMS	2
G9	JTAG_TDO	3
H9	JTAG_TDI	4

2.11 Power Supplies

2.11.1 Voltage Rails and Sources

PicoZed 7015/7030 is powered through the Micro Header connection between itself and the carrier card.

Four regulators reside on the PicoZed 7015/7030 SOM that provide 1.0V, 1.35V, 1.8V, 3.3V and 0.75V. These voltages are used to power the peripheral devices on the PicoZed System-On-Module. These regulators are powered from the end user carrier card via the VIN pins on the Micro Headers and are expected to carry 5V to the PicoZed System-On-Module for the input to the regulators.

There are there also three bank voltages that are supplied form the carrier card to the PicoZed System-On-Module. Bank 34 (VCCO_34), Bank 35 (VCCO_35) and Bank 13 (VCCO_13) are generated on the carrier card and connected to the 7015/7030 System-On-Module via the Micro Headers. The voltage at which these banks operate is up to the carrier card design as all I/O that connect to these banks is exclusive to the Micro Headers (no on-board device is connected to these banks).

Additionally, two of the voltages for the gigabit transceivers are also supplied from the carrier card: MGTAVCC (1.0V) and MGTAVTT (1.2V). The MGT rails are filtered with 220 ohm inductors prior to connecting to the MGTAVTT and MGTAVCC power pins to reduce noise coupling into the transceivers.

The diagram below shows a high level depiction of the power scheme for PicoZed 7015/7030 System-On-Module.

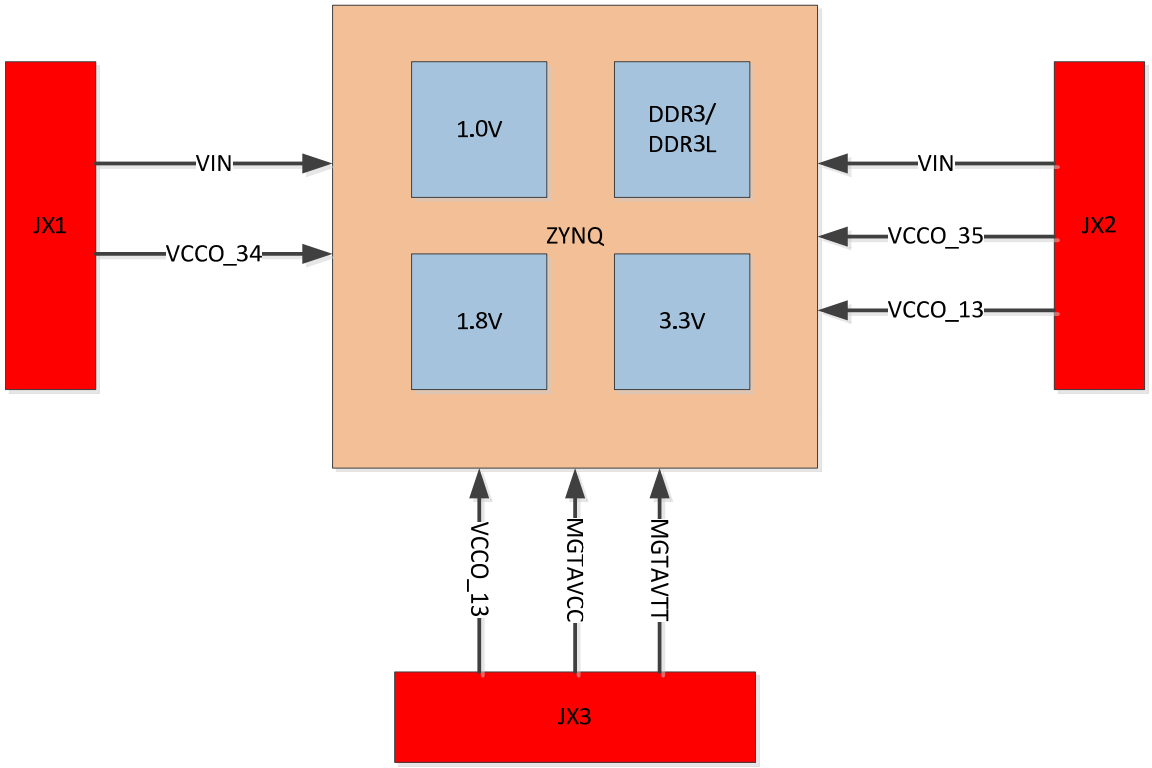

Figure 4 - PicoZed 7015/7030 Power Scheme

The table below shows the various voltage rail names on the schematic, the associated voltage for each rail and where they are connected on the Zynq 7015/7030, and where the voltage originates from.

Table 15 - PicoZed 7015/7030 Voltage Rails

Schematic Voltage Name	Voltage Level	Zynq Connection	Voltage Origination
1.0V	1.0V	VCCINT	SOM
		VCCBRAM	
		VCCPINT	
VCCO_DDR3	1.35V	VCCO_DDR_502 (Bank 502)	
VTTREF	0.675V	PS_DDR_VREF0 (Bank 502)	
		PS_DDR_VREF1 (Bank 502)	
1.8V	1.8V	VCCO_MIO1_501 (Bank 501)	
		MGTVCCAUX	
		VCCAUX	
		VCCPAUX	
3.3V	3.3V	VCCO_0 (Bank 0)	
		VCC_MIO0_500 (Bank 500)	
VCCO_34	1.8V/2.5V/3.3V **	VCCO_34 (Bank 34)	JX1
VCCO_35	1.8V/2.5V/3.3V **	VCCO_35 (Bank 35)	JX2
VCCO_13	1.8V/2.5V/3.3V	VCCO_13 (Bank 13)	JX2/JX3
MGTAVTT	1.2V	MGTAVTT	JX3
MGTAVCC	1.0V	MGTAVCC	JX3

2.11.2 Voltage Regulators

The following power solution provides the power rails of the PicoZed 7015/7030. Sequencing of the supplies is implemented by cascading the POWER GOOD outputs of each supply to the ENABLE input for the next supply in the sequence. 3.3V is the last supply to come up, therefore the PG for the 3.3V supply is used to drive the PG_MODULE net and is used as the power-on reset control for Zynq (U1.pin B18), Ethernet PHY (U5.pin 16), and USB-Host PHY (U7.pin 27).

This net is also connected to the Micro Headers so power supplies on the carrier card can also control this signal.

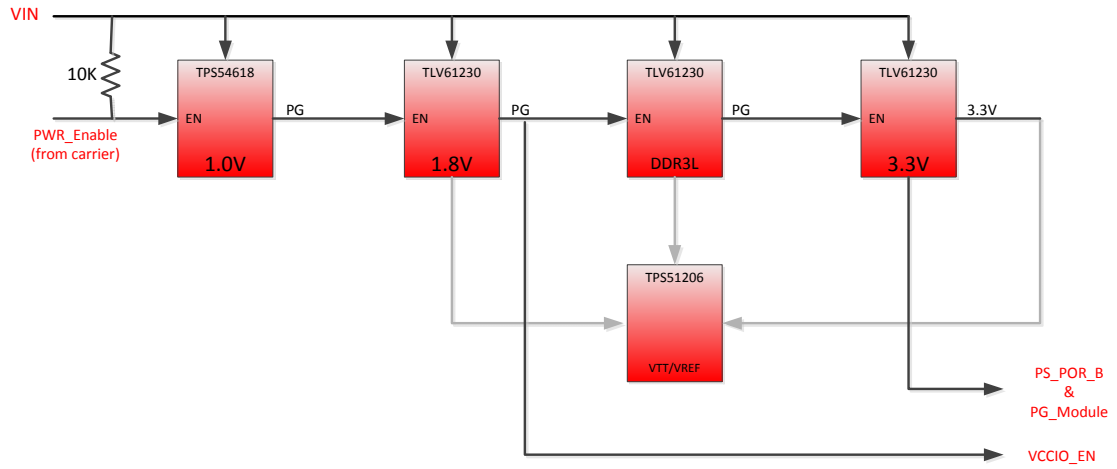

Figure 5 - Regulation Circuitry (VCCIO_EN is PG_1V8)

This circuit sequences power-up of PicoZed 7015/7030. 1.0V comes up first, then 1.8V, then VCCO_DDR3 and then 3.3V. PG_MODULE is connected to PS_POR_B on Zynq, thus when the power supplies are valid, PS_POR_B is released.

When the PicoZed 7015/7030 is mated to a carrier card, the power good outputs of the carrier card should also be tied to the PG_MODULE net on JX1.pin 8. If the carrier card power supplies do not have power good outputs, a voltage supervisor or open-drain buffer should be used to complement this circuit.

PicoZed 7015/7030 also provides an Enable signal to the carrier card to signal that Vccint and Vccaux are both up and the carrier card is free to bring up the Vcco supplies. This signal is called VCCIO_EN (PG_1V8) and is tied to JX2.pin 10.

NOTE: VCCIO_EN is provided by the power good output of the 1.8V regulator.

The table below shows the maximum output current for each regulator on the PicoZed 7015/7030 SOM.

Table 16 – Voltage Rails w/ Max Output Current

TI Part Number	Voltage (V)	Max Current (A)
TPS54618	1.0	6
TLV62130	1.8	3
TLV62130	1.35	3
TLV62130	3.3	3
TPS51206	0.675	2

2.11.3 Power Supply Sequencing

When attached to a carrier card, the carrier card must provide an active-high, power enable signal, PWR_ENABLE. This controls the first PicoZed 7015/7030 regulator (U17, 1.0V) turning on. This should be an open drain design such that when PicoZed 7015/7030 is in standalone mode, this signal will float high (pulled high to 5V on PicoZed 7015/7030 via R99). This may allow for the special circumstance of the carrier card controlling the powering of the PicoZed 7015/7030 for low power applications.

Sequencing for the power supplies follows the recommendations for the Zynq device. PS and PL INT and AUX supplies are tied together on the PicoZed 7015/7030 platform to create a low cost design. The following diagram illustrates the supply sequencing:

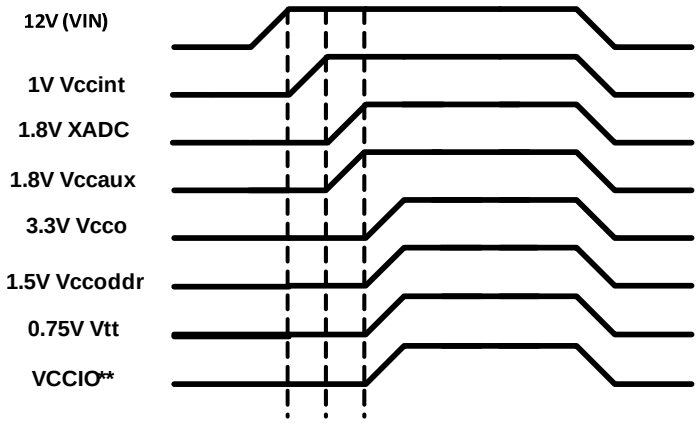

Figure 6 - Power Sequencing

** VCCIO driven from carrier card.

As noted above, if connected to a carrier card, the 1.8V power supply's power good output should be used to enable the VCCIO regulators via the PG_1V8 (VCCIO_EN) signal on the Micro Headers.

The following diagram illustrates sequencing with a carrier card:

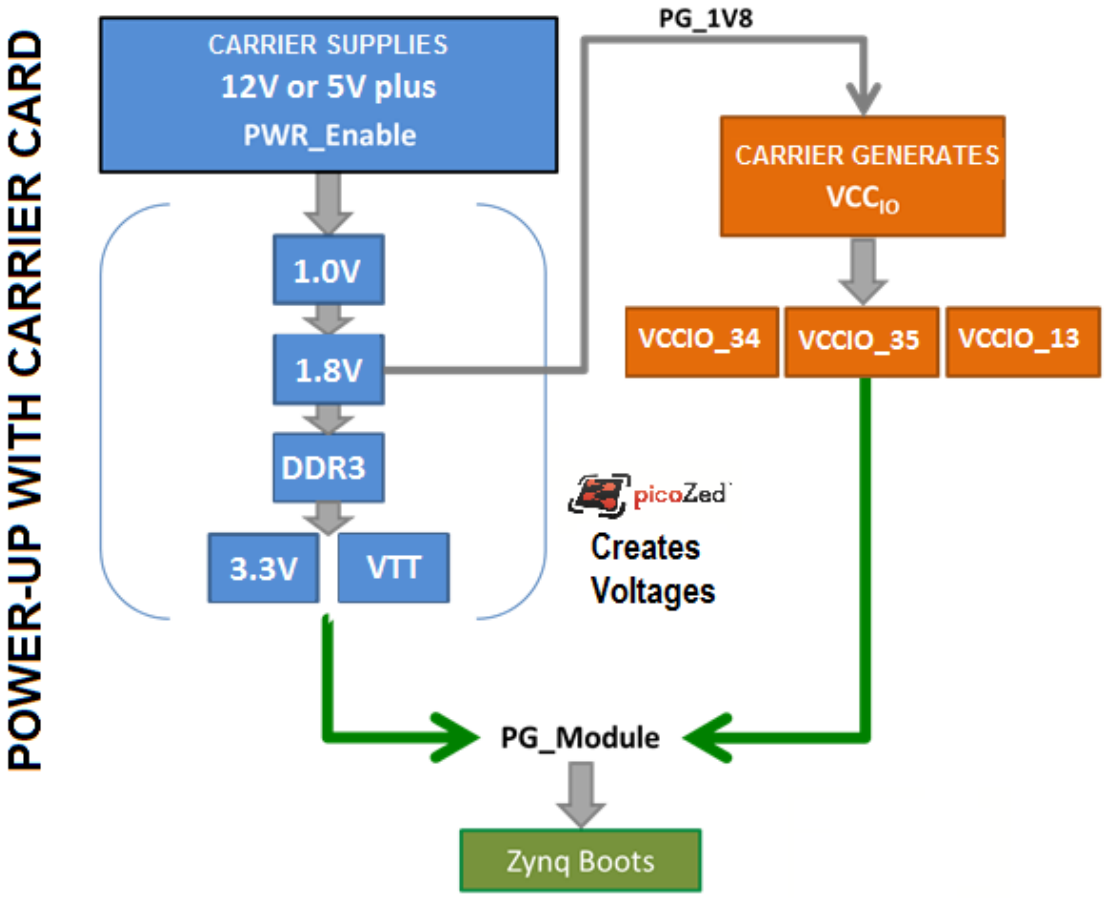

Figure 7 - Power Sequencing with Carrier Card

2.11.4 Bypassing/Decoupling

The PicoZed 7015/7030 design follows the PCB decoupling strategy as outlined in UG933. The 7015 version comes in a CLG485 package and the 7030 a SBG485 package. Since the two packages have varying requirements for the number of some of the decoupling capacitors, the PicoZed 7015/7030 was designed to have the minimum number of required capacitors for either package.

Package	Device	V_{CCINT}[3]					V_{CCBRAM}				V_{CCAUX}			V_{CCAUX_IO}			V_{CCO} per Bank[4][5]			Bank 0
		680 µF	330 µF	100 µF	4.7 µF	0.47 µF	100 µF	47 µF	4.7 µF	0.47 µF	47 µF	4.7 µF	0.47 µF	47 µF	4.7 µF	0.47 µF	100 µF	4.7 µF	0.47 µF	47 µF
CLG485	Z-7015	0	1	0	2	4	1	0	1	1	1	1	2	NA	NA	NA	1	2	4	1
SBG485	Z-7030	0	1	0	1	0	1	0	1	2	1	0	0	NA	NA	NA	1	0	0	1

Figure 8 - CLG4485/SBG485 PL Decoupling

Package	Device	V_{CCPINT}			V_{CCPAUX}[2]			V_{CCO_DDR}			V_{CCO_MIO0}			V_{CCO_MIO1}			V_{CCPLL}[1][3]	
		100 µF	4.7 µF	0.47 µF	100 µF	4.7 µF	0.47 µF	100 µF	4.7 µF	0.47 µF	100 µF	4.7 µF	0.47 µF	100 µF	4.7 µF	0.47 µF	10 µF	0.47 µF
CLG485	Z-7015	1	1	3	1	1	1	1	1	4	1	1	1	1	1	1	1	1
SBG485	Z-7030	1	0	0	1	1	1	1	0	0	1	1	1	1	1	1	1	1

Figure 9 - CLG4485/SBG485 PS Decoupling

2.11.5 Power Good LED

A green status LED, D3, illuminates with the U13 3.3V power rail. Since this regulator is the last one in the sequence to come up, it is an effective indication that all regulators are on.

2.11.6 Power Estimation

Since the total power consumption of the system heavily depends on many factors with regard to the configuration/utilization of the Zynq device, it is highly recommended that the end user perform some power estimation and analysis using the Xilinx Power Estimator (XPE). This tool is very useful for plugging in various parameters and getting an estimated power consumption estimate for the system.

The XPE tool can be downloaded from the following link:

http://www.xilinx.com/products/design_tools/logic_design/xpe.htm

When designing the PicoZed 7015/7030 power system, this tool was used to insure that the SOM system could supply enough power to the Zynq and its on-board peripherals using worst case parameters including logic utilization, operating frequency and temperature.

Since the power supply for the VCCIO rails for banks 34, 35, 13 and the MGT Bank 112 are supplied from the carrier card, it is important to make sure the carrier card power supplies are adequate to power these rails over the desired and/or estimated operating scenario.

NOTE: When designing a custom PicoZed Carrier Board, be sure to use XPE (Xilinx Power Estimator) to estimate the power needed by the FPGA. The designer will need this figure in sizing the input supply to the SOM. In addition to the XPE results for the core power supplies, Vccint/Vccpint (1V) and Vccaux/Vccpaux/Vccpll (1.8V), you will need to add an additional 3.0W to your power estimate to compensate for the additional power that is needed for the peripherals on the PicoZed System-On-Modules such as memory and USB and Ethernet PHY devices.

2.11.7 XADC Power Configuration

The XADC component is powered from the filtered 1.8V VCCaux supply utilizing the on-chip reference as shown below.

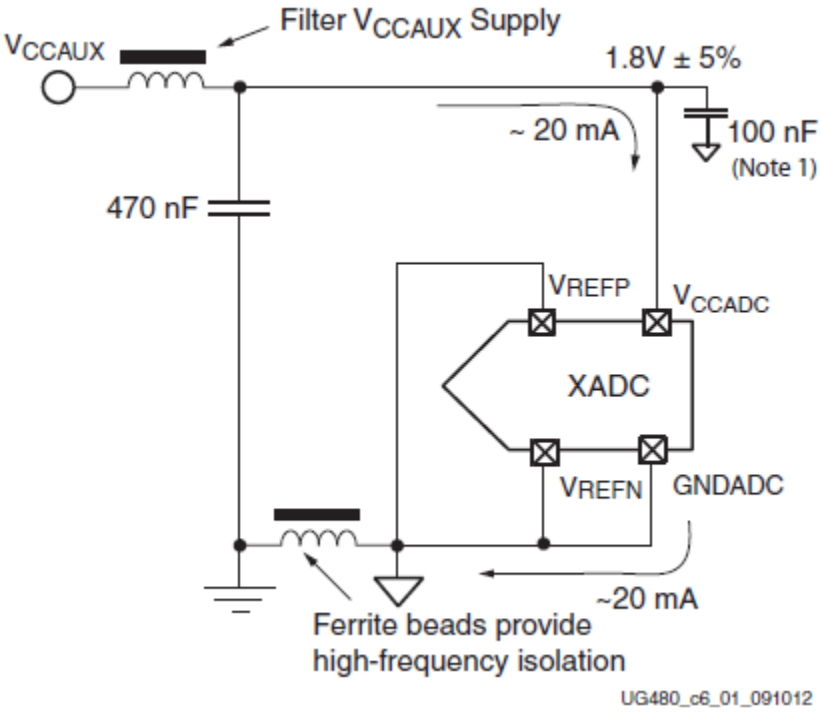

Figure 10 - XADC Power Configuration

2.11.8 Battery Backup for Device Secure Boot Encryption Key

Zynq power rail V_{CCBATT} is a 1.0V to 1.89V voltage typically supplied by a battery. This supply is used to maintain an encryption key in battery-backed RAM for device secure boot. The encryption key can alternatively be stored in eFuse which does not require a battery.

As specified in the Zynq TRM, if the battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX}. On PicoZed, V_{CCBATT} is connected to net FPGA_VBATT and is tied through a 0 Ω resistor (R51) to the PicoZed V_{CCAUX} supply, which is 1.8V. However, FPGA_VBATT is also extended to the carrier card. To apply an external battery to Zynq from the end user carrier card, remove R51 from the PicoZed System-On-Module.

2.11.9 Cooling Fan

An unpopulated-header JP1, labeled FAN, is available in the event a fan is needed for high performance designs. This header provides two ground connections and one connection to the Vin voltage, which is 12V by default (VIN). PicoZed 7015/7030 also provides a resistor option for a 3.3V fan via JT3. Thermal adhesive tape should be used to attach the chosen sink and/or fan sink to the Zynq device.

3 Zynq-7000 AP SoC I/O Bank Allocation

3.1 PS MIO Allocation

There are 54 I/O available in the PS MIO. The table below lists the number of required I/O per peripheral and the MIO locations where the interface exists.

Table 17 – PS MIO Interface Requirements

Interface	I/O Required	MIO
QSPI FLASH	7	1-6, 8
USB Host	13	7, 28-39
ETHERNET	15	16-27, 47, 52-53
eMMC / Micro Header General Purpose	6	10-15
Micro Header General Purpose	13	0, 9, 40-46, 48-51
TOTAL	**54**	

The Micro Header GPIO assignments aren't specifically defined interfaces such as those that are defined in Table 17. The table below provides the MIO locations of the PS MIO general purpose pins and the functions that they are intended to support. The end user is encouraged to utilize the Zynq TRM in defining the MIO peripheral mappings that they would like to utilize on a custom PicoZed carrier card.

Table 18 – PS GPIO Assignments

MIO	Voltage	Function
7	3.3V	USB RESET
8	3.3V	QSPI FB CLK
0, 9	3.3V	PS GPIO
10-15	3.3V	eMMC or PS GPIO
40-46, 48-51	1.8V	PS GPIO
47	1.8V	PS GPIO or ETHERNET RESET

3.2 Zynq-7000 AP SoC Bank Voltages

The I/O bank voltage assignments are shown in the table below.

Table 19 – Zynq Bank Voltage Assignments

PS-Side	
Bank	**Voltage (default)**
MIO Bank 0/500	3.3V
MIO Bank 1/501	1.8V
DDR3L	1.35V
PL-Side	
Bank0	3.3V
Bank 34	Carrier card – Vcco_34
Bank 35	Carrier card – Vcco_35
Bank 13	Carrier card – Vcco_13

NOTE: If using a PicoZed 7030 Bank 34 and Bank 35 voltage MUST BE 1.8V ONLY!!!

PL I/O Banks 34, 35, and 13 are powered from the end user carrier card. These bank supplies are designed to be independent on the PicoZed 7010/7020. Maximum flexibility is allowed to the designer for these banks as the voltage level and standards are left to the end user carrier card design. The designer of the end user carrier card VCCO supplies is provided the choice of whether the IO banks use a shared voltage supply or independent voltage supplies.

4 Mechanical

PicoZed 7015/7030 measures 2.25” x 4.00” (57.15 mm x 101.6 mm)

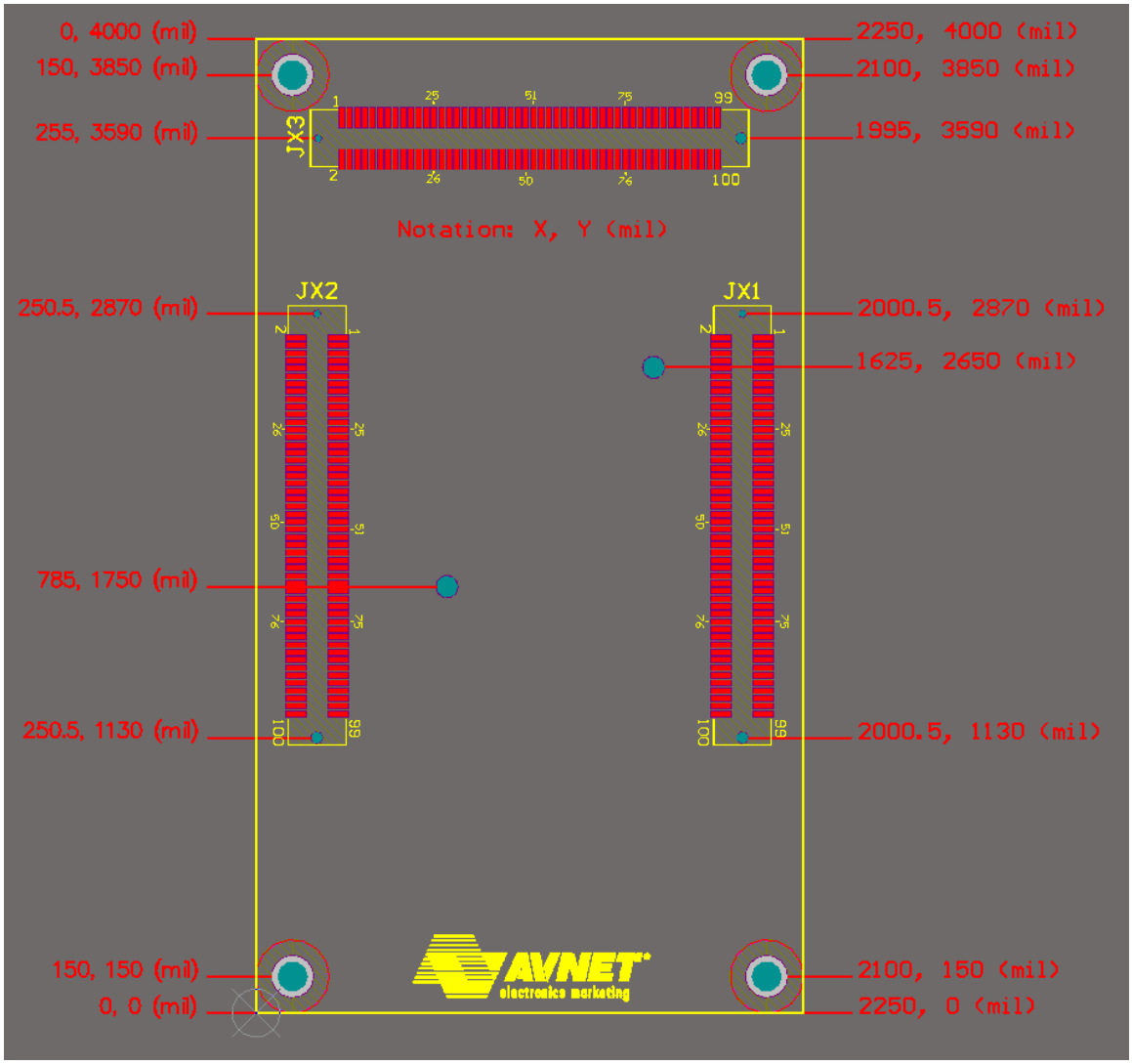

Figure 11 - PicoZed 7015/7030 Mechanical

PicoZed 7015/7030 has a maximum vertical dimension of 0.366” (9.3mm).

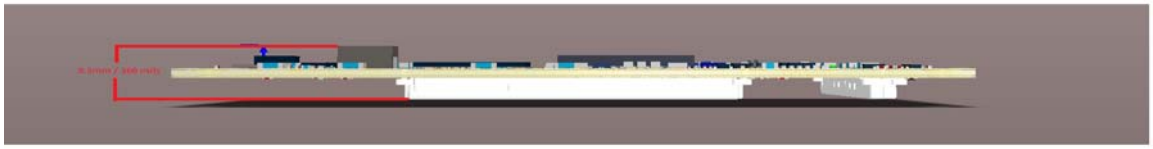

Figure 12 - PicoZed 7015/7030 Side Vertical Dimensions

5 Revision History

Rev date	Rev #	Reason for change
16 Oct 14	1.0	Initial PicoZed 7015/7030 Hardware User Guide
12/3/14	1.1	Updated Tables 9, 10, 11. Updated for DDR3L (text, tables, figures)