Getting Started Guide

Version 2.0

Xilinx® Spartan®-6 FPGA Industrial Video Processing Kit

AVNET® electronics marketing

REVISION HISTORY

DATE	VERSION	REVISION
7/8/2010	1.0	Initial Release
11/18/2010	2.0	Update for ISE 12.2

AVNET DESIGN KIT TECHNICAL SUPPORT FILES AND DOWNLOADS WEB ACCESS INSTRUCTIONS

Thank you for purchasing an Avnet design kit. The technical support documents associated with this kit, including the User Guide, Bill of Materials, Schematics, Source Code and Application Notes, are available online. You, the Customer, can access these documents at any time by visiting Avnet's Design Resource Center ("DRC") at: www.em.avnet.com/drc/support

On your first visit to the DRC, you will be required to site register before you can download the documents. To get started, select the name of the manufacturer associated with your design kit from the drop down menu. A complete listing of available design kits will appear. Select the kit you purchased. Scroll to the bottom of the design kit page to access the support files. Before you download a file, you will be prompted to login. If you are an existing user, please login. If you are a new user, click on the "Need to sign-up?" text. Please complete the short registration form. Upon completion, be sure to retain your login and password information for future visits to Avnet's DRC. Logging in once, gives you unlimited access to all technical support files and downloads. You will also have the chance to request e-mail notifications whenever there are updates to your design kit.

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ABOUT THIS GUIDE

This guide provides information for getting started with the Avnet Spartan®-6 Industrial Video Processing Kit (IVK).

This guide provides steps to setup the IVK hardware and run a demonstration that exercises an HD image sensor, as well as video IP cores. This guide also provides steps for installing the Xilinx® ISE® Design Suite: System Edition software, obtaining updates, and generating a license.

See the product web site at www.em.avnet.com/spartan6video.

Additional Documentation

The following documents are available for download at www.xilinx.com/products/spartan6/.

- **Spartan-6 Family Overview**
  This overview outlines the features and product selection of the Spartan-6 family
- **Spartan-6 FPGA Data Sheet: DC and Switching Characteristics**
  This data sheet contains the DC and switching characteristic specifications for the Spartan-6 family.
- **Spartan-6 FPGA Packaging and Pinout Specifications**
  This specification includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications.
- **Spartan-6 FPGA Configuration User Guide**
  This all-encompassing configuration guide includes chapters on configuration interfaces (serial and parallel), multi-bitstream management, bitstream encryption, boundary-scan and JTAG configuration, and reconfiguration techniques.
- **Spartan-6 FPGA SelectIO Resources User Guide**
  This guide describes the SelectIO™ resources available in all Spartan-6 devices.
- **Spartan-6 FPGA Clocking Resources User Guide**
  This guide describes the clocking resources available in all Spartan-6 devices, including the DCMs and PLLs.
- **Spartan-6 FPGA Block RAM Resources User Guide**
  This guide describes the Spartan-6 device block RAM capabilities.
- **Spartan-6 FPGA GTP Transceivers User Guide**
  This guide describes the GTP transceivers available in the Spartan-6 LXT FPGAs.
- **Spartan-6 FPGA DSP48A1 Slice User Guide**
  This guide describes the architecture of the DSP48A1 slice in Spartan-6 FPGAs and provides configuration examples.
- **Spartan-6 FPGA Memory Controller User Guide**
  This guide describes the Spartan-6 FPGA memory controller block, a dedicated embedded multi-port memory controller that greatly simplifies interfacing Spartan-6 FPGAs to the most popular memory standards
- **Spartan-6 FPGA PCB Designer's Guide**
  This guide provides information on PCB design for Spartan-6 devices, with a focus on strategies for making design decisions at the PCB and interface level.

Additional Support Resources

To access the most current collateral for the Avnet Spartan®-6 Industrial Video Processing Kit please visit the product website at: www.em.avnet.com/spartan6video

Once on the IVK product website:

To access the latest IVK documentation and designs, click on the following link:

To access technical support for the IVK, click on the following link:

To access the technical forums, click on the following icon:

To search the database of silicon and software questions and answers or to create a technical support case in WebCase, see the Xilinx website at: www.xilinx.com/support

GETTING STARTED WITH THE SPARTAN-6 INDUSTRIAL VIDEO PROCESSING KIT

Introduction

The Xilinx® Spartan®-6 FPGA Industrial Video Processing Kit (IVK) is a Targeted Design Platform (TDP) consisting of the Spartan-6 LX150T FPGA development board with two daughter cards based on the industry-standard FPGA Mezzanine Card (FMC) specification, ISE® Design Suite System Edition software, and four Reference Designs.

The addition of the FMC-DVI and FMC-IMAGEOV daughter cards provide the video interfaces necessary for the development of video applications. The IVK supports the following video interfaces:

- 2 HD image sensor inputs
- 1 DVI-D input
- 2 DVI-D outputs
- DisplayPort output
- Avnet LCD Panel interface (ALI)

It also features the OmniVision image sensor which provides direct support for real-time high-definition (HD) video streaming. The IVK provides a development environment that allows the user to accelerate development of high-performance video processing applications for low-cost, low-power industrial imaging systems. Industrial equipment OEMs can now rapidly build and evaluate reprogrammable imaging solutions with high-definition image resolutions, specialized image sensor interfaces, and intelligent video and advanced image processing algorithms.

Video Kit Contents

Figure 1 – Spartan-6 Industrial Video Processing Kit

The IVK contains the following components:

What's Inside the Box:

- Hardware
  - 1 – Xilinx Spartan®-6 LX150T system board
  - 1 – Dual Image Sensor with DVI Output FMC Module (FMC-IMAGEOV)
  - 1 – DVI Input/Output FMC Module (FMC-DVI)
  - 1 – OmniVision OV9715 image sensor module
  - 1 – Plexiglas mounting base-plate and image sensor mounting assembly
- Documentation
  - Welcome Letter
  - Spartan-6 FPGA Industrial Video Processing Kit Getting Started Guide
- Cables
  - 1 – USB-A to USB-B Cable
  - 2 – HDMI-DVI Cables
  - 1 – Ethernet Cable
  - Universal 12 V power supply
  - Xilinx Platform Cable USB-II JTAG programming cable
- Out of Box Demo (firmware)
  - Camera Video Processing and Video Frame Buffer demonstration
- Software
  - ISE Design Suite System Edition license voucher: (device-locked) for Spartan-6 LX150T FPGA

What's Available Online:

- Development Kit home page with Documentation and Reference Designs
  - www.em.avnet.com/spartan6video
- Schematics and PCB files
- Reference Designs and Demonstrations
  - HDL demonstrations
    - DVI Pass-through demonstration
  - EDK demonstrations
    - DVI Video Processing demonstration
    - DVI Video Frame Buffer demonstration
    - Camera Video Processing and Video Frame Buffer demonstration
  - System Generator demonstrations
    - Validating a 5x5 Video Filter Kernel with Hardware Co-Simulation
- License for ISE Design Suite System Edition
  - www.xilinx.com/getproduct
  - www.xilinx.com/tools/faq.htm

Key Features

Xilinx Spartan®-6 LX150T Development Base Kit

- Spartan-6 LX150T-3FGG676 FPGA
- Avnet LCD interface connector
- PCI Express® x1 and x4 support
- SFP and SATA connectors
- Dual LPC FMC slot
- 128 MB DDR3 SDRAM
- 32 MB Parallel Flash
- 10/100/1000 Ethernet PHY
- USB 2.0 PHY
- USB-UART bridge
- LVDS clock generator
- Temperature sensor and RTC
- Platform Flash
- Voltage regulators

DVI Input/Output FMC Module (FMC-DVI)

- DVI-D input
- DVI-D output
- Video clock synthesizer
- DisplayPort output
- Low jitter clock generator

Dual Image Sensor with DVI Output FMC Module (FMC-IMAGEOV)

- Image sensor module support
- DVI transmitter
- Video clock synthesizer

Omnivision OV9715 Image Sensor Module

- High definition video
  - 1280x800 @ 30 frames per sec
  - 640x400 @ 60 frames per sec
- Zero degree microlens shift : extreme wide angle field of view
- Low light performance : 3300 mB/(lux-sec)

Key Features Illustrated

The following image illustrates the location and various features on the IVK.

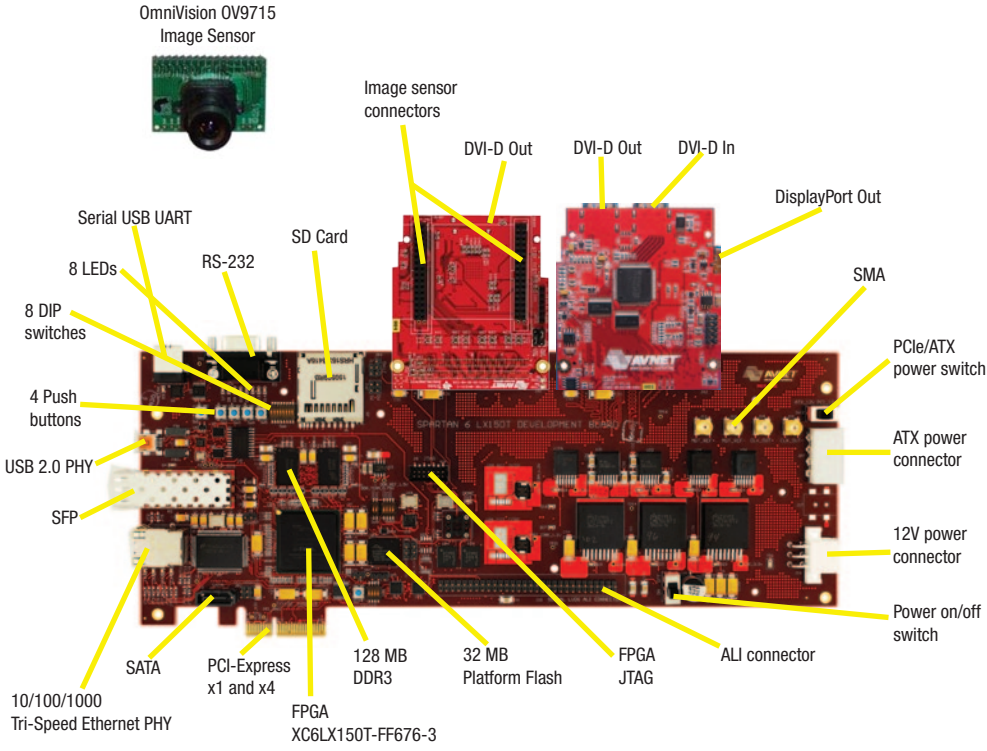
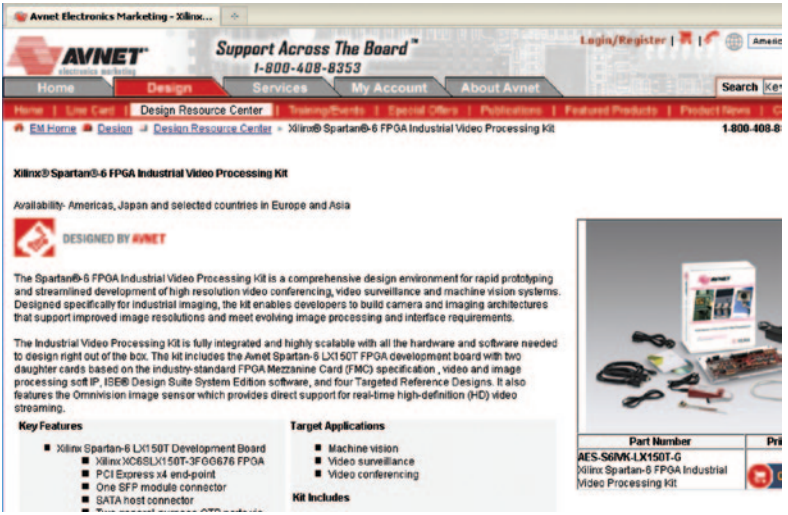


Figure 2 – Spartan-6 Industrial Video Processing Kit – Key Features

IVK on the Avnet Design Resource Center (DRC)

To access the most current collateral for the Avnet Spartan®-6 Industrial Video Processing Kit please visit the product website at: www.em.avnet.com/spartan6video



To access the technical forums, click on the following icon:

To access technical support for the IVK, click on the following link:

To access the latest IVK documentation and reference designs, click on the following link:

Access to the Avnet DRC requires registration. If you are a returning user you can enter your login credentials here. If you are new to the DRC you can create a new account for yourself.

Once logged-in, you will see a web page with content similar to the following excerpt. This web page contains links to:

- The Getting Started User Guide
- The Reference Designs (including design files and documentation)
- Links to the hardware boards
- Links to optional LCD panel kits

Xilinx® Spartan®-6 FPGA Industrial Video Processing Kit

App Notes/Ref Designs

ISE Design Suite 12.2

> HDL Designs – Avnet LCD Interface (ALI) Reference Design Tutorial
> HDL Designs – DVI Pass-Through Reference Design Tutorial
> EDK Designs – DVI/Camera Video Processing and Frame Buffer Reference Design Tutorial
> System Generator Designs – Hardware Co-Simulation Reference Design Tutorial

Other

> Avnet LCD Interface (ALI) Specification
> CP2102 USB Drivers

IVK Hardware Components

The S6-IVK is composed of the following Avnet hardware components:

Xilinx® Spartan®-6 LX150T Development Kit

- Hardware guide, schematic, and BOM are available at the following product page:
  - www.em.avnet.com/spartan6lx150t-dev
- This base board can be used independently from the IVK, and has its own set of documentation and reference designs.

Dual Image Sensor FMC Module

- Hardware guide, schematic, and BOM are available at the following product page:
  - www.em.avnet.com/fmc-image

DVI I/O FMC Module

- Hardware guide, schematic, and BOM are available at the following product page:
  - www.em.avnet.com/fmc-dvi

The S6-IVK also contains an OmniVision OV9715 image sensor module.

OmniVision OV9715 Image Sensor Module

- The datasheet for the OV9715 image sensor must be requested at:
  - www.ovt.com/support/datasheet.php
- The schematics for the OV9715 image sensor module must also be requested directly from OmniVision.

XILINX VIDEO SOLUTION OVERVIEW

This section gives an overview of the Xilinx video solution. This includes software tools and intellectual property (IP) cores.

Choosing your Design Suite

The Spartan-6 Industrial Video Processing Kit gives entitlement to one seat of ISE Design Suite – System Edition. The System Edition is the most complete design suite available from Xilinx, as shown in the following table:

	ISE Design Suite			
Features	**Logic Edition**	**Embedded Edition**	**DSP Edition**	**System Edition**
ISE Foundation with ISE Simulator	▲	▲	▲	▲
PlanAhead Design and Analysis Tool	▲	▲	▲	▲
ChipScope Pro	▲	▲	▲	▲
ChipScope Pro Serial I/O Toolkit	▲	▲	▲	▲
Embedded Development Kit (EDK)		▲		▲
Software Development Kit (SDK)		▲		▲
System Generator for DSP			▲	▲

Table 1 – Xilinx Design Suite Overview

The following table describes three design suites, which have been color-coded as a visual cue throughout this document.

Design Suite	Description
Logic Edition	ISE is used for HDL development
Embedded Edition	EDK is used for embedded development
System Edition	EDK is used for embedded development System Generator for DSP is used for: – validating DSP designs using hardware co-simulation – creating pcores which can be assembled into a system in EDK

The recommended design suite for the IVK is the System Edition. System Generator for DSP is used to create PCOREs which can then be assembled into an embedded processor system with EDK.

IVK Reference Design Overview

There are three sets of reference designs provided for the Spartan-6 Industrial Video Processing Kit. The following table identifies which design suite is required for each of the reference designs.

	Design Suite		
Reference Design	**Logic Edition**	**Embedded Edition**	**System Edition**
HDL Demonstrations			
DVI Pass-Through Demo	▲	▲	▲
Avnet LCD Interface (ALI) Demo	▲	▲	▲
EDK Demonstrations			
DVI Video Processing Demo		▲[1]	▲
DVI Video Frame Buffer Demo		▲	▲
Camera Video Processing with External Frame Buffer Demo		▲[1]	▲
System Generator for DSP Demonstrations			
Hardware Co-Simulation Demo			▲

Table 2 – Reference Design Overview with respect to Design Suite

As described in section **IVK on the Avnet Design Resource Center (DRC)**, each of these reference designs can be downloaded from the Avnet DRC:

www.em.avnet.com/spartan6video ➔ SUPPORT FILES & DOWNLOADS

[1] These EDK projects use pcores which were created with System Generator. Although System Generator for DSP is not required to build the EDK projects which instantiates SysGen pcores, it is required to rebuild or to modify these pcores.

The Xilinx Streaming Video Interface

The Xilinx Streaming Video Interface (XSVI) is a standard streaming video interface used to connect video modules in all design suites.

The XSVI is similar to the DVI interface, but adds additional VBLANK/HBLANK signals. These differ from the DVI's VSYNC/HSYNC signals and are shown in the following illustration.

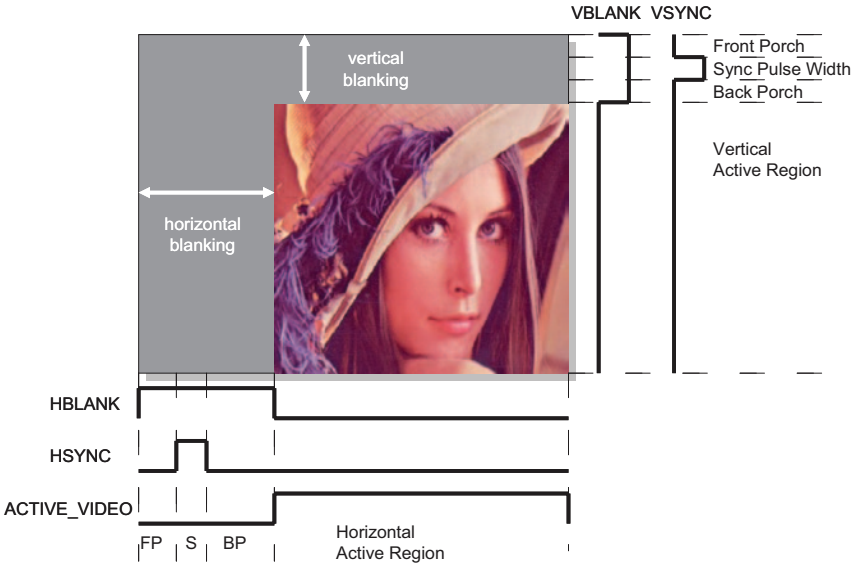


Figure 3 – Xilinx Streaming Video Interface (XSVI)

All of the Xilinx Video IP, as well as most of the IVK reference designs, use the XSVI interface.

For more information on the XSVI interface, as well as detailed timing diagrams, refer to the Xilinx Video Communications Interface White Paper [Ref 8]. This white paper also described FIFO and host processor interfaces.

Xilinx Video IP Overview

Another important point to consider when choosing a design suite is which Video IP are supported by each of the design suites. The following table provides a list of the Xilinx Video IP and their dependency of the three design suites.

	Design Suite		
Video IP Core	**Logic Edition**	**Embedded Edition**	**System Edition[2]**
Core Generator Video IP			
Color Filter Array Interpolation	▲	▲	▲
Color Correction Matrix	▲	▲	▲
Defective Pixel Correction	▲	▲	▲
Gamma Correction	▲	▲	▲
Image Edge Enhancement	▲	▲	▲
Image Noise Reduction	▲	▲	▲
Image Statistics	▲	▲	▲
Motion Adaptive Noise Reduction	▲	▲	▲
RGB to YCrBCb Color-Space Conversion YCrCb to RGB Color-Space Conversion	▲ ▲	▲ ▲	▲ ▲
Video Direct Memory Access	▲	▲	▲
Video On Screen Display	▲	▲	▲
Video Scaler	▲	▲	▲
Video Timing Controller	▲	▲	▲
MPMC related Video IP			
Video Frame Buffer Controller (VFBC)		▲	▲[3]

Table 3 – Video IP Overview with respect to Design Suite

[2] All of the Core Generator Video IP can be instantiated in System Generator using the Black Box functionality.

[3] For information on how to integrate the Video Frame Buffer Controller (VFBC) in System Generator, refer to XAPP1136 [Ref 47]

SETTING UP THE HARDWARE

The Spartan®-6 FPGA Industrial Video Processing Kit will need to be assembled once it is received. The following steps will provide the steps necessary to complete this setup for initial use. These steps will need to be completed only once before using your newly purchased IVK.

Remove the pre-assembled plexiglas assembly from the IVK box

Remove the following pre-assembled plexiglas assembly from the IVK box.

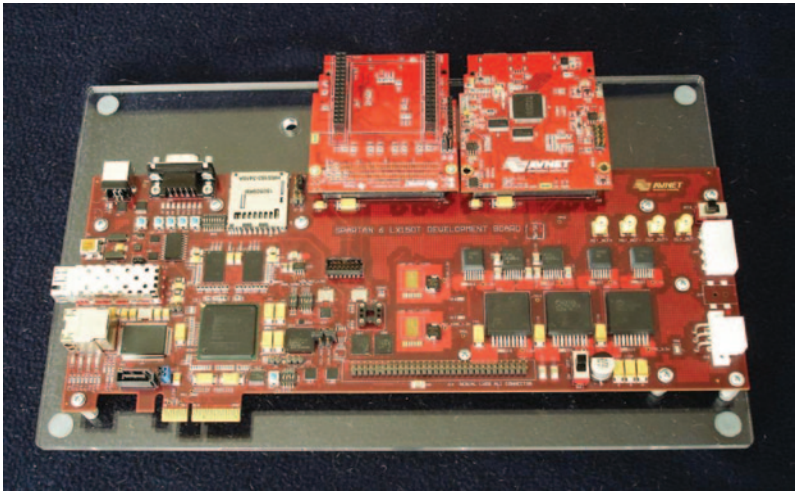


Figure 4 – Pre-assembled plexiglas assembly

Configuring the jumpers

Ensure that the jumpers on the FMC-IMAGEOV module are configured as shown in Figure 5.

- Jumper J302 should be installed on pins 1-2 (VCAM = 3V3)
- Jumper J500 should be installed on pins 2-3 (VGPIO = 5V)

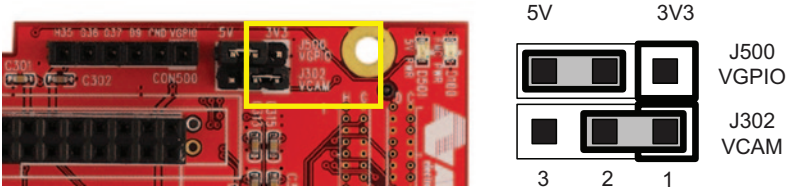


Figure 5 – FMC-IMAGEOV jumper configuration

Mounting the Image Sensor

Remove the following components from the IVK box:

1. OV9715 image sensor module
2. Flat cable
3. Camera mounting bracket (plexiglass)
4. Flexible mounting post
5. 1/4" – 20 screw

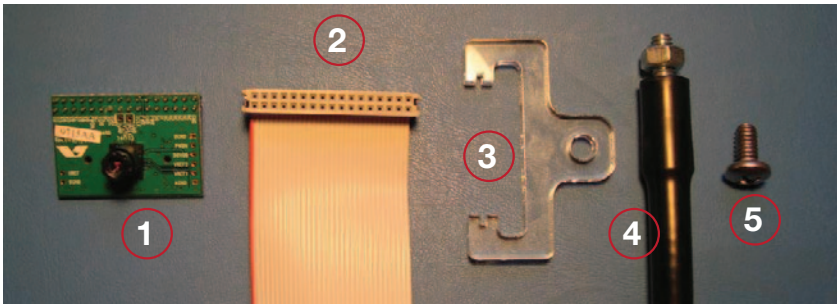


Figure 6 – Image sensor assembly – components

Attach the OV9715 image sensor module to the flat cable as shown in Figure 7. It is important to align pin 1 of the image sensor module to pin 1 of the flat cable. Notice that the flat cable is wider than the image sensor header. There should be two extra holes on the right.

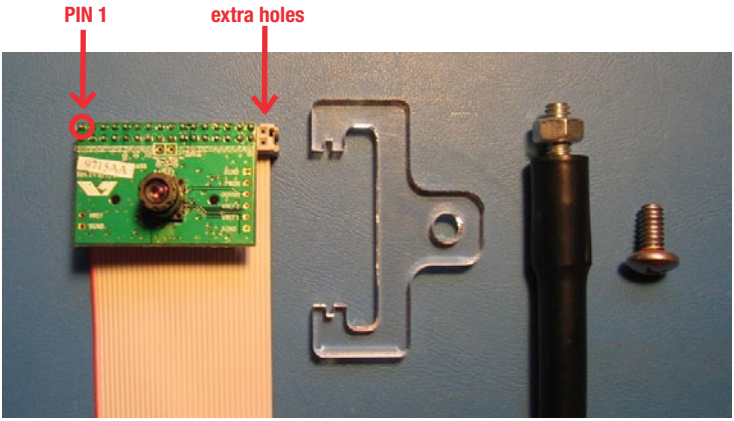


Figure 7 – Image sensor assembly – step 1

Insert the image sensor module into the small slits of the camera mounting bracket as shown in Figure 8. The flat cable will hang in the large opening behind the image sensor module.

Figure 8 – Image sensor assembly – step 2

Attach the camera mounting bracket on the flexible mounting post using the nut as shown in Figure 9.

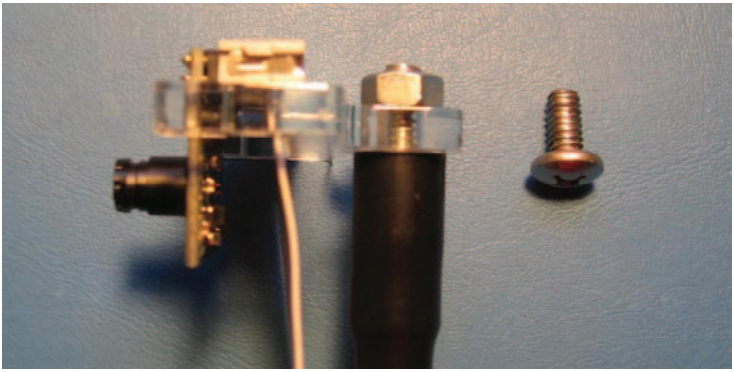


Figure 9 – Image sensor assembly – step 3

The image sensor assembly should look like the following:

Figure 10 – image sensor assembly — complete

The flexible mounting post needs to be mounted on the plexiglas base-plate. Using the screw provided, screw the Image Sensor Assembly onto the IVK assembly at the location shown in Figure 11.

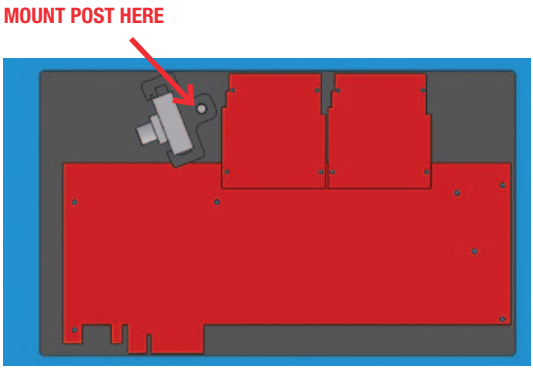


Figure 11 – Mounting location of image sensor assembly

Connecting the Image Sensor Input Source

Now connect the flat cable onto the FMC-IMAGEOV module's CON301 header. The ribbon cable should be connected so that Pin 1 (identified with a red strip on the flat cable) aligns with Pin 1 on the header (identified with a 1 on the PCB).

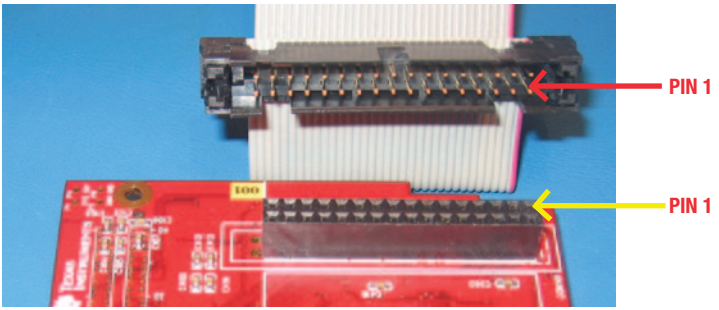


Figure 12 – Connecting the image sensor's flat cable (1 of 2)

Note : The flat cable's connector (2x34) is wider than the header (2x32).

Once the flat cable is in place, the connector should be centered on the white box drawn on the PCB, as shown in the following figure.

Figure 13 – Connecting the image sensor's flat cable (2 of 2)

In order to focus the image sensor, the lens can be turned clockwise or counter-clockwise, as shown in the following image.

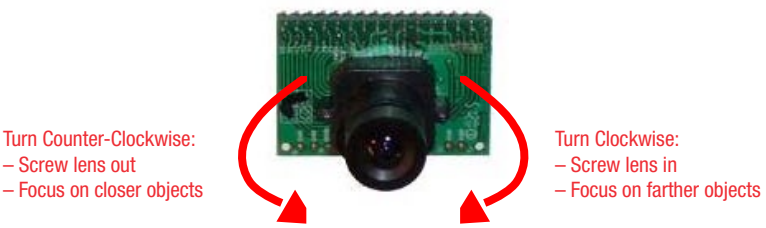


Figure 14 – Focusing the image sensor lens

The completely assembled Spartan-6 Industrial Video Processing Kit should look like the following figure.

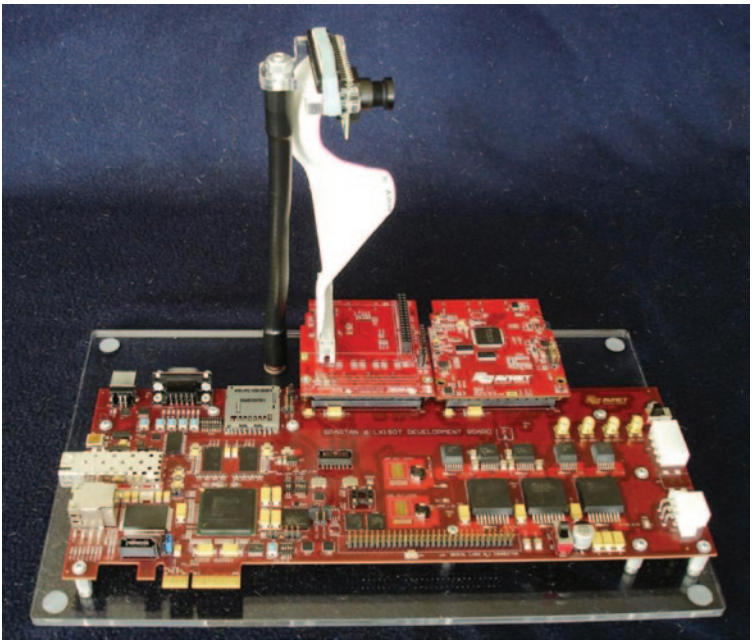


Figure 15 – Fully assembled IVK

Note: The fully assembled IVK shown in Figure 15 has an elastic which holds the image sensor module firmly to the camera mounting bracket. If the image sensor module does not sit firmly in place, an elastic can be added as seen in Figure 15. An elastic has not been provided with the IVK.

Connecting a DVI Monitor

Remove the HDMI-DVI cable from the IVK box, and connect the HDMI end of the cable to one of the DVI-D outputs depending on the desired reference design described in Table 4 and shown in Figure 16.

Reference Design	FMC Module	DVI-D Output Connector
Camera Demonstration	FMC-IMAGEOV	CON400
DVI Demonstrations	FMC-DVI	J3

Table 4 – IVK – Video Output Interfaces

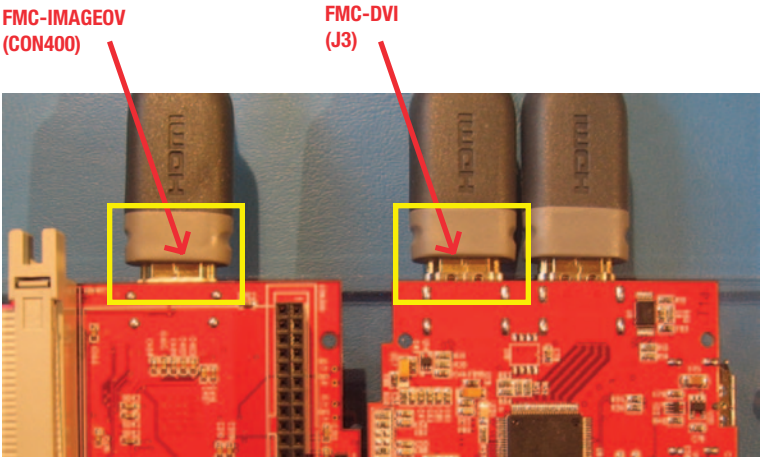


Figure 16 – Connecting a DVI monitor

For the Camera Demonstration, connect the HDMI end of the cable to the CON400 connector.

Connect the DVI end of the cable to a DVI monitor.

Connecting a DVI-D Video Source

Remove the second HDMI-DVI cable from the IVK box, and connect the HDMI end of the cable to the DVI-D input shown in the following figure:

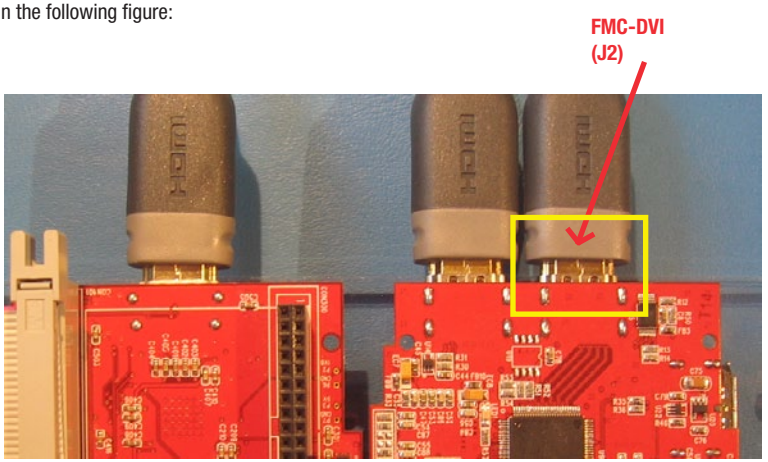


Figure 17 – Connecting a DVI-D monitor

Connect the DVI end of the cable to a DVI-D video input source.

Note: This video source cannot originate from an analog VGA connector since only the digital portion (DVI-D) of the DVI connector is connected to the FMC-DVI module.

Connecting the USB/UART

Remove the USB-A to USB-B cable from the IVK box, and connect the USB-B end of the cable to the Spartan-6 LX150T development board's JR1 connector.

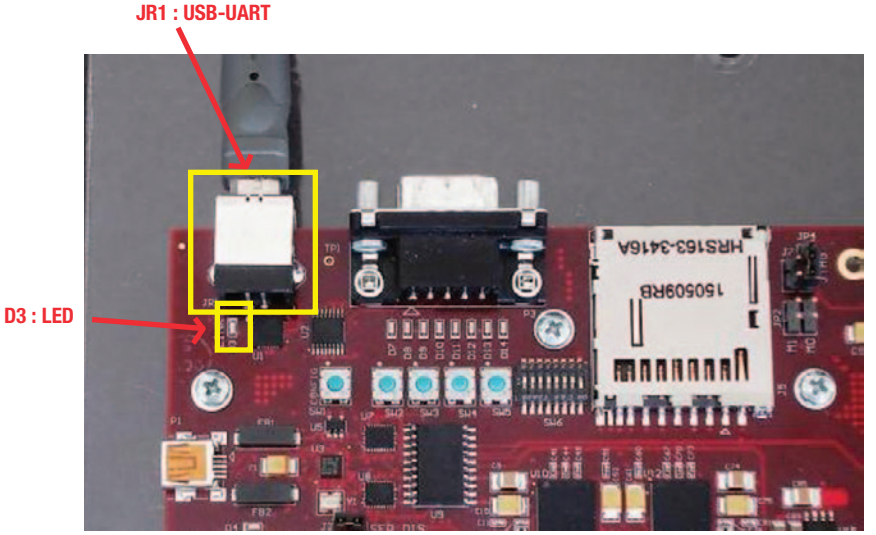


Figure 18 – Connecting the USB-UART

Connect the USB A end of the cable to your PC.

When the serial link between the IVK and the PC is active, the D3 LED close to the connector will light up. This will occur after the board has been powered on, and once the USB UART device drivers are installed, as described in the next sections.

Connecting the 12 V Power Supply

Remove the 12 V Power Block from the IVK box. Plug in the power adapter to the local AC power. Ensure that the IVK power switch SW11 is in the off position. Plug the 12 V power jack into the Spartan-6 LX150T carrier board's J16 connector. Turn on the power by switching the SW11 to the "ON" position.

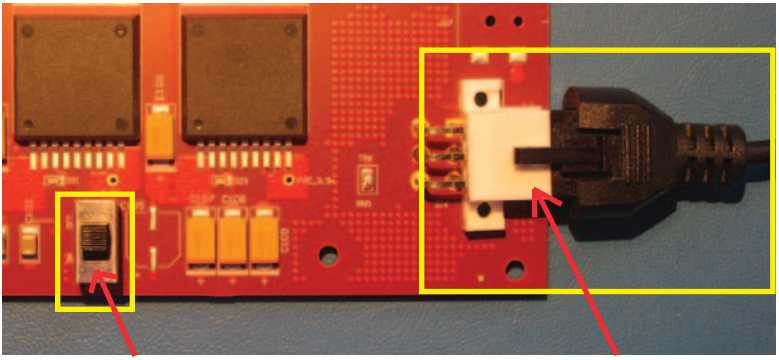


Figure 19 – IVK – Connecting the 12 V power supply

When the power is turned on, the PC will detect the presence of a new USB device. If the PC does not recognize the USB UART as a COM port, the Found New Hardware Wizard will start, prompting you to specify the location of the software driver to install. If this occurs, leave the wizard window open and follow these steps in section **Setting up the Host PC** to download and install the USB UART device driver.

SETTING UP THE HOST PC

This section describes how to install the USB drivers on the host PC for the USB-UART connection to the IVK.

Install the USB/UART software drivers

The Spartan-6 LX150T Development Board has a USB-UART based on the CP2102 chipset. Use of this feature requires that a USB driver be installed on your Host PC.

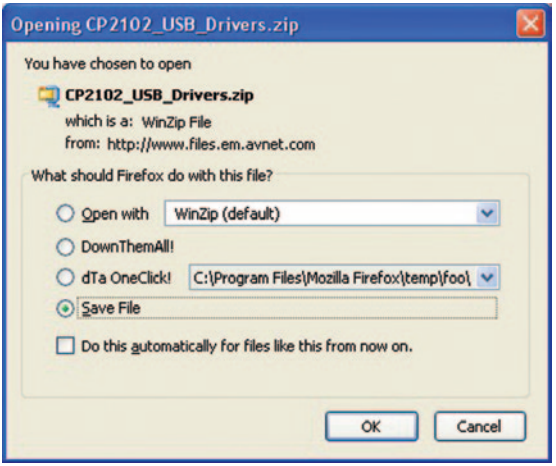
If Windows recognizes the USB UART and loads the software driver please skip ahead to the **Configuring the USB/UART** section. However, if the PC does not recognize the USB UART as a COM port the Found New Hardware Wizard will start, prompting you to specify the location of the software driver to install. Leave the wizard window open and follow these steps to download and install the device driver.

As described in section **IVK on the Avnet Design Resource Center (DRC)**, use your web browser to navigate to the IVK's product page on the Avnet DRC:

www.em.avnet.com/spartan6video ➔ 

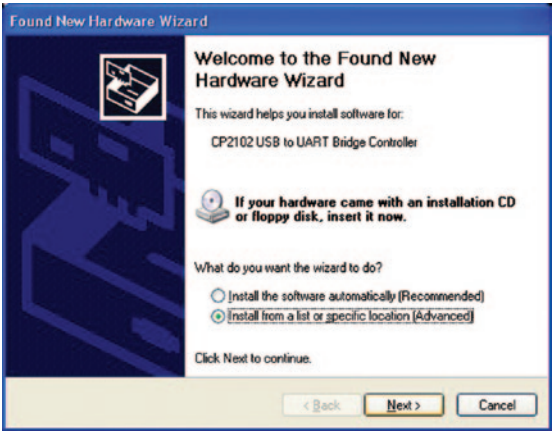
On the IVK's "Support Files and Downloads" page, double-click on the "**CP2102 USB Drivers**" link to download Windows software drivers for the SiLabs CP2102 USB to RS232 serial bridge chip.

When prompted, click the Save button and download the driver zip file to a folder of your choice.

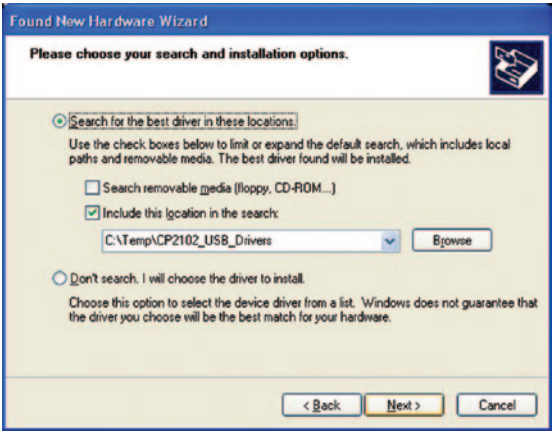


Once downloaded, extract the **CP2102_USB_Drivers.zip** file. The extracted driver files will be in a folder named **<download_folder>\ CP2102_USB_Drivers**.

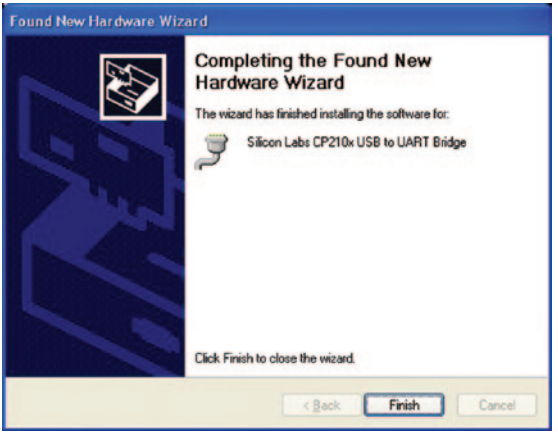
Go to the **Found New Hardware Wizard** window and select ***Install from a list or specific location*** and click **Next:**



Select **Search for the best driver in these locations** and **Include this location in the search**, then click **Browse** and navigate to the folder where the driver zip file was extracted. Click **Next** when ready:



Windows will copy the appropriate driver files and the following screen will be seen. Click **Finish** to complete the driver installation. Windows will then load the software driver and the USB UART will be ready to use.



Configuring the USB/UART

Check the Device Manager on the host PC to verify the Com port used, as the HyperTerminal settings may need to be modified to match this host specific value. Follow these steps:

- In Windows Explorer, right-click on My Computer and select Manage.
- Select Device Manager in the left panel
- Select Ports (Com & LPT) in the right panel. The CP210x USB to UART bridge should indicate the Com port selected. In the case of this example, it is COM6. Write this down for future reference, and keep in mind that it might change if the computer reboots.

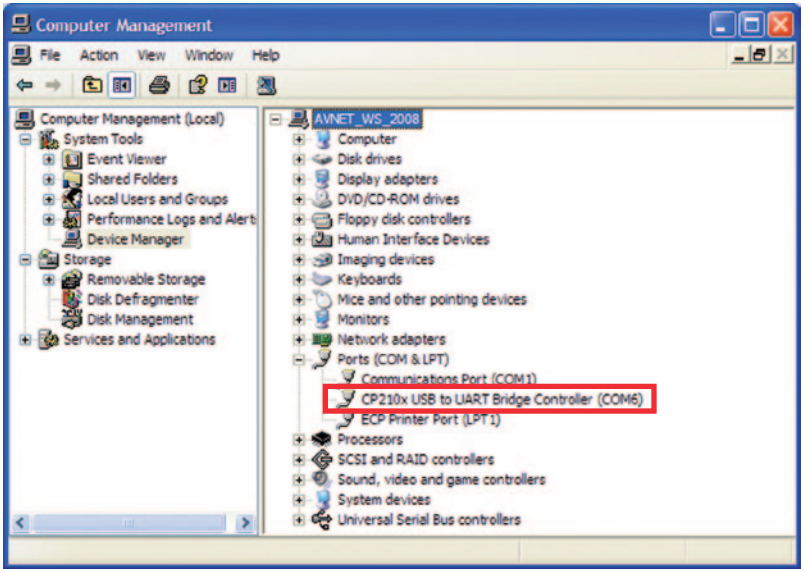


Figure 20 – USB-UART – Verifying COM port in Device Manager

- If you don't have Device Manager available in the Computer Management panel, you can also access this from the Windows start menu:

  Start ➔ My Computer ➔ View System Information ➔ Hardware tab ➔ Device Manager

- Close the Computer Management Window.

Open a Terminal Program

On the PC, open a serial terminal program. By default, Windows comes with HyperTerminal which can be accessed from the start menu:

Select Start ➔ Programs ➔ Accessories ➔ Communications ➔ HyperTerminal

Figure 21 – HyperTerminal – Setup Screen 1 of 3

Specify something like "IVK" for the name of the terminal session, then click **OK**.

Figure 22 – HyperTerminal – Setup Screen 2 of 3

Select the COM port corresponding to the previous installation step, then click **OK**.

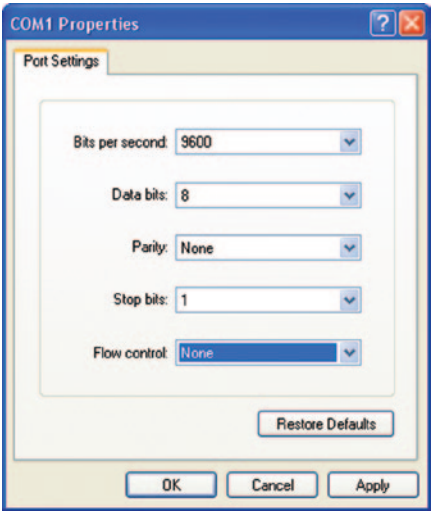


Figure 23 – HyperTerminal – Setup Screen 3 of 3

Specify the settings of the serial connection:

- Bits per second = 9600
- Data bits = 8
- Parity = None
- Stop bits = 1
- Flow control = None

Then click **OK**.

In the serial console, press the '?' key to display the menu as shown in Figure 24.

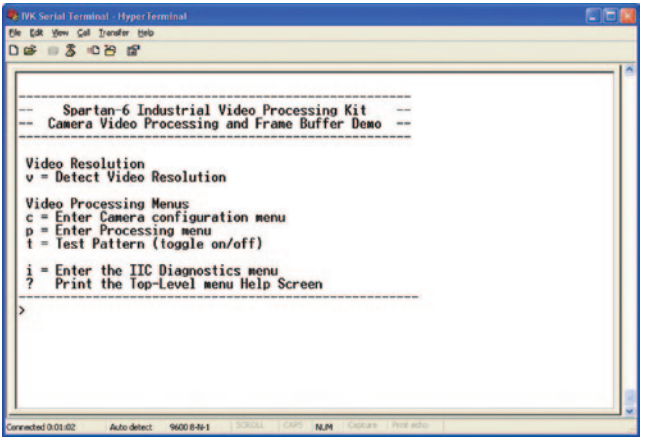


Figure 24 – HyperTerminal – IVK Power-On Display

This menu is described in detail in the following section.

GETTING STARTED WITH THE CAMERA DEMONSTRATION

Now that the IVK hardware is setup, the Camera demonstration is ready to use!

The following hardware setup is required to run this demonstration:

- Image Sensor connected to the FMC-IMAGEOV's CON301 header
- DVI Monitor connected to the FMC-IMAGEOV's CON400 connector.
- USB connected to the S6-LX150T carrier's JR1 connector

Refer to section **Setting up the Hardware** for more information of setting up the IVK hardware.

Overview

The following block diagram illustrates the video pipeline in the camera demonstration.

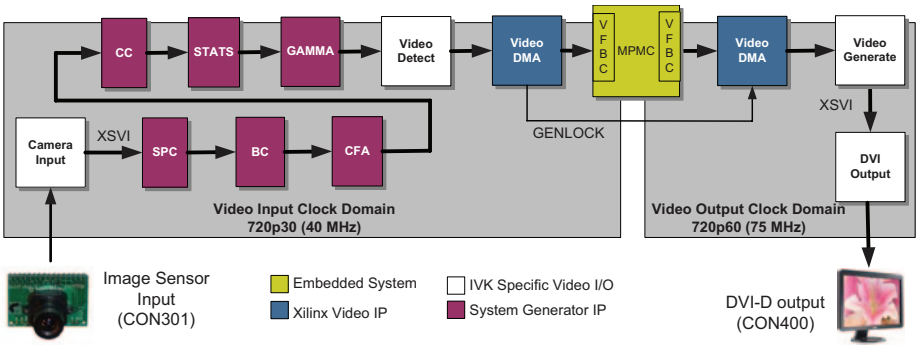


Figure 25 – Camera Demonstration – Video Pipeline

The video pipeline consists of the following components:

- SPC : Stuck Pixel Correction
- BC : Brightness and Contrast
- CFA : Color Filter Array Interpolation
- CC : Color Correction
- STATS : Image Statistics
- GAMMA : Gamma Correction

This demonstration supports video capture at 1280x720P @ 30 Hz and video playback at 1280x720P @ 60 Hz. These resolutions are configured by the embedded processor (MicroBlaze) and can be modified to support other resolutions (limited by the image sensor used).

Loading the Demonstration

The IVK is shipped with a "**Camera Video Processing with Video Frame Buffer**" demonstration programmed into its Xilinx Platform Flash. In order to load this design, simply power-on the IVK.

Using the Application

The lens on the camera can be screwed in and out to adjust the focus if needed. All other aspects of the Camera Demo are controlled with the Serial Terminal program.

In the serial console, press the '?' key to display the menu as shown in Figure 26.

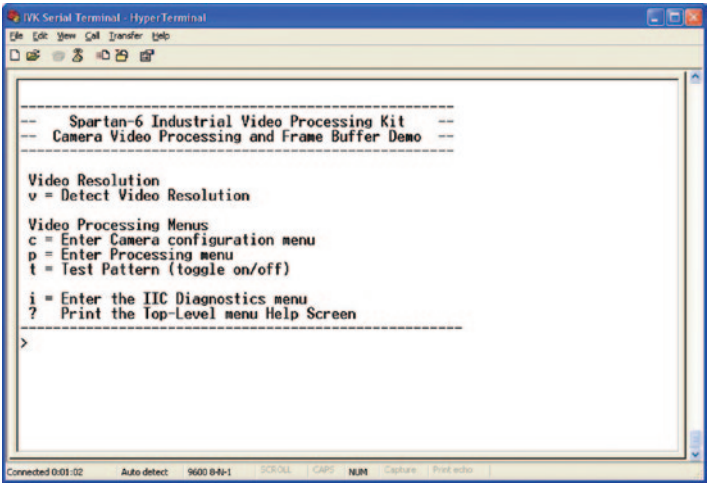


Figure 26 – Camera Demonstration – Top Level Menu

The live video stream from the image sensor on the DVI monitor should be seen. If nothing appears on the DVI monitor, refer to the Troubleshooting section in the **IVK EDK Reference Design Tutorial** [Ref 2].

Notice the brightness of the image being displayed on the DVI monitor.

Press '**p**' to access the Processing Menu. Then press '**o**' to apply gamma correction of the input video as shown in Figure 27.

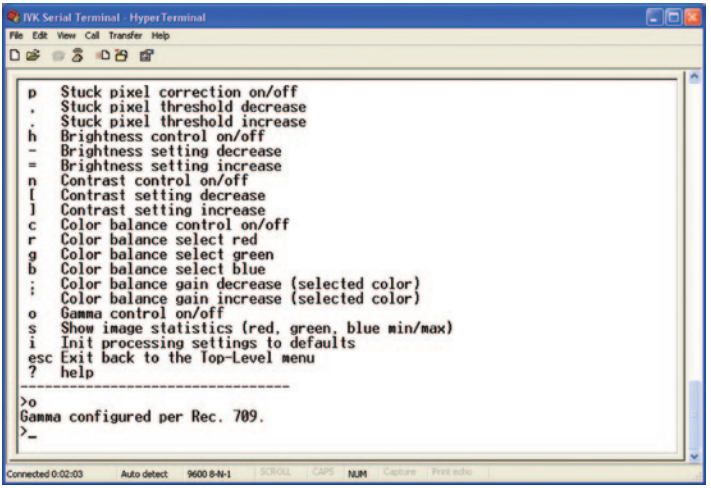


Figure 27 – Camera Demonstration – Processing Menu

This will enable gamma correction on the video input. Notice how the image changed to become brighter. Pressing '**o**' again will enable and disable the gamma correction.

In a similar fashion, you can adjust the following parameters in the camera processing menu:

- Stuck Pixel Correction
- Brightness
- Contrast
- Color Balance
- Gamma Correction
- Image Statistics

This concludes the camera demonstration!

For more information on gamma correction, and on the other processing features available in the camera demonstration, refer to the **IVK EDK Reference Design Tutorial** [Ref 2]

Recommended Next Steps

The recommended next steps, after going through this **Getting Started Guide**, are:

- Getting familiar with the **EDK Concepts, Tools, and Techniques** [Ref 48]
- Licensing the Video DMA core
- Rebuilding the Camera Frame Buffer demonstration
- Modify the demonstration to meet your needs:
  - Adding custom image processing IP cores
  - Adding Xilinx Image Processing IP cores — for a complete list, please go to: www.xilinx.com/esp/ind_sci_med/ism_avail_ip.htm

For detailed information on rebuilding the project and adding IP to the video processing pipeline, please refer to the **IVK EDK Reference Design Tutorial** [Ref 2].

INSTALLING THE XILINX TOOLS

Installing and Licensing the ISE Design Suite Software

This IVK comes with entitlement to a full seat of the ISE Design Suite: System Edition that is device locked to a Spartan-6 LX150T. This software can be installed from the DVD, which is included in the kit, or the latest version can be downloaded from

www.xilinx.com/support/download/index.htm

For detailed instructions on installing and licensing the Xilinx tools, please refer to the ISE Design Suite 12: Installation, Licensing, and Release Notes, available from the Xilinx website:

www.xilinx.com/support/documentation/sw_manuals/xilinx12_2/irn.pdf

Connecting the Xilinx Platform Cable USB-II JTAG programming cable

Now that the Xilinx software is installed, including the JTAG drivers, connect the Xilinx Platform Cable USB-II JTAG programming cable.

Remove the Xilinx Platform Cable USB-II from the IVK box, connect the USB-B end of the cable to the Xilinx Platform Cable USB-II (ie. red box). Connect the flat cable to the Spartan-6 LX150T development board's J9 connector as shown in Figure 28.

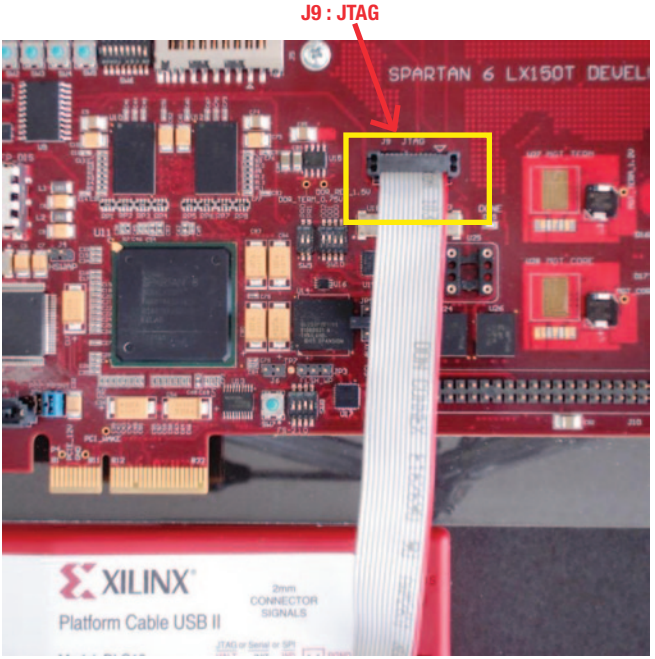


Figure 28 – Connecting the Xilinx Platform Cable USB-II

Connect the USB A end of the cable to the PC. If this is the first time the Xilinx Platform Cable USB-II has been connected to the PC, the USB drivers will need to be configured. This is described in the following section.

Configuring the Xilinx USB JTAG drivers

If this is the first time the Xilinx Platform Cable USB-II has been connected to the PC, the Xilinx USB JTAG drivers will need to be installed.

To obtain the current version of the USB Cable Installation Guide, see the Xilinx website at:
www.xilinx.com/support/documentation/user_guides/ug344.pdf

GETTING STARTED WITH THE DVI VIDEO PROCESSING DEMONSTRATION

Now that the Xilinx tools are installed, the DVI Video Processing demonstration is ready to use!

The following hardware setup is required to run this demonstration:

- DVI Source connected to the FMC-DVI's J2 connector
- DVI Monitor connected to the FMC-DVI's J3 connector
- USB connected to the S6-LX150T carrier's JR1 connector
- JTAG connected to the S6-LX150T carrier's J9 connector

Refer to section **Setting up the Hardware** for more information of setting up the IVK hardware. Refer to section **Connecting the Xilinx Platform Cable USB-II JTAG programming cable** for more information on setting up the JTAG connection.

The DVI-D video source must be configured to one of the following supported video resolutions:

Resolution	Pixel Rate (MHz)	Frame Dimensions
VGA	25.125	640 x 480
SVGA	27.000	800 x 600
XGA	40.000	1024 x 768
720P	74.250	1280 x 720

Table 5 – DVI Video Processing Demo – Supported Video Resolutions

Overview

The following block diagram illustrates the video pipeline in the camera demonstration.

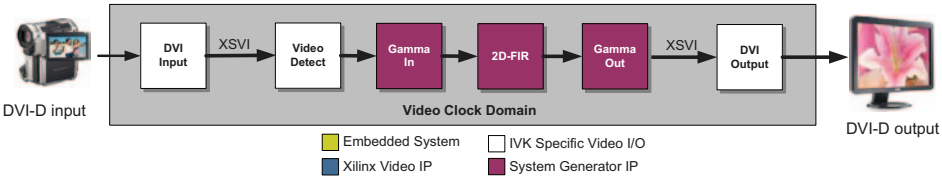


Figure 29 – DVI Video Processing Demonstration – Video Pipeline

The video pipeline consists of the following components:

- GAMMA : Gamma Correction
- 2D-FIR : Spatial Filtering (edge detect, smoothing, sharpening, …)

Obtaining the Demonstration from the Avnet DRC

As described in section **IVK on the Avnet Design Resource Center (DRC)**, the web browser can be used to navigate to the IVK's product page on the Avnet DRC:

www.em.avnet.com/spartan6video ➔ SUPPORT FILES & DOWNLOADS

On the IVK's "Support Files and Downloads" page, double-click on the "**DVI/Camera Video Processing and Frame Buffer Demos**" link to download the project files. When prompted, click the Save button and download the project zip file to a folder of choice.

Once downloaded, extract the **IVK_EDK_Demonstrations_{date}.zip** file to **C:**. The extracted design files will be in a folder named **C:\IVK_EDK_Demonstrations_{date}**.

Loading the Demonstration

The demonstration can be loaded using the following batch file:

\IVK_EDK_Demonstrations\IVK_DVI_Video_Processing_Demo\ready_for_download**run_demo.bat**

Double-clicking on this batch file will perform the following operations:

- Download the FPGA bitstream (download.bit) to the hardware via JTAG
- Load the application software (executable.elf) to external memory
- Start executing the application software

The following boot display on the serial terminal will be seen:

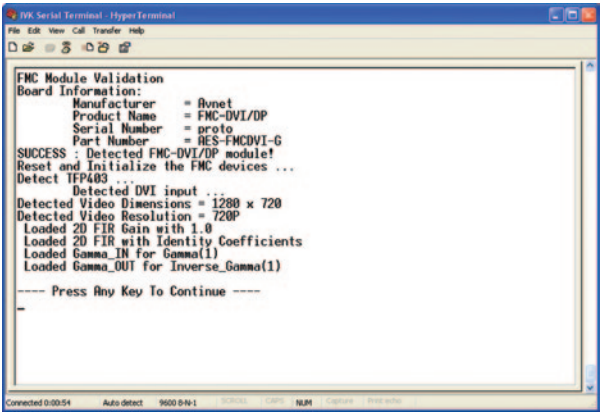


Figure 30 – DVI Video Processing Demonstration – Boot Display

Using the Application

The DVI Video Processing demonstration is controlled with the Serial Terminal program.

After loading the demonstration, the boot display shown in Figure 31 will be seen.

In the serial terminal, press any key to access the demonstration's top level menu.

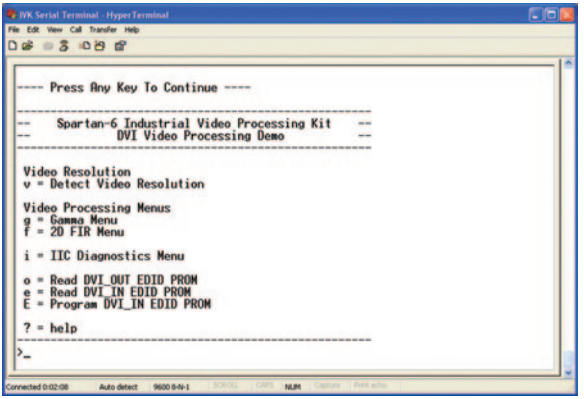


Figure 31 – DVI Video Processing Demonstration – Top Level Menu

The live video stream from the DVI-D input source should be seen being driven on the DVI monitor. If nothing is seen on the DVI monitor, refer to the Troubleshooting section in the **IVK EDK Reference Design Tutorial** [Ref 2]**.**

Notice the brightness of the image being displayed on the DVI monitor.

Press '**g**' to access the Gamma Menu.

Then press '**i**' to enable/disable gamma correction at the input and '**o**' to enable/disable gamma correction at the output as shown in Figure 32.

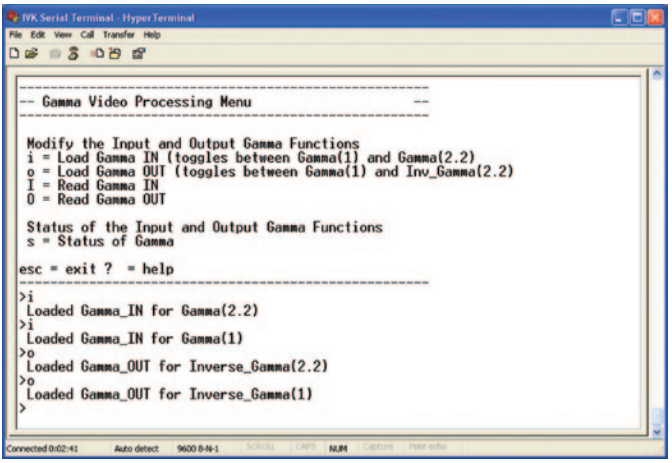


Figure 32 – DVI Video Processing Demonstration – Gamma Menu

Notice how both types of gamma correction affect the video:

- Input Gamma (when enabled)
  - gamma = 2.2
  - performs gamma expansion
  - makes the image darker
- Output Gamma (when enabled)
  - gamma = 1/2.2
  - performs gamma compression
  - makes the image lighter

When both gamma corrections are enabled, they cancel each other out.

Press '**ESC**' to return to the top level menu.

Press '**f**' to access the 2D FIR Menu.

Then press '**5**' to load the coefficients for an edge detection filter as shown in Figure 33.

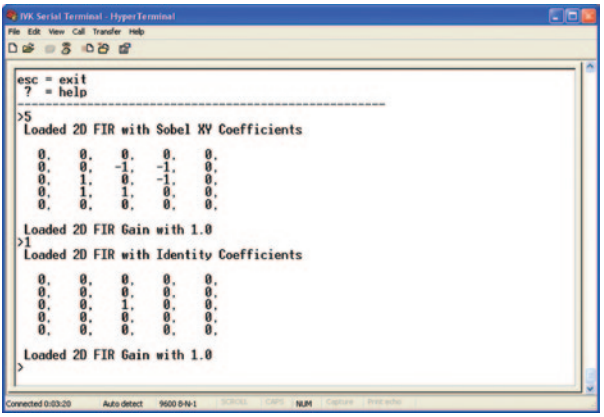


Figure 33 – DVI Video Processing Demonstration – 2D FIR Menu

Experiment with the various filter coefficients by pressing '**1**' through '**9**'.

Press '**1**' to return to a "pass-through" filter

Press '**ESC**' to return to the top level menu.

This concludes the DVI Video Processing demonstration!

For more information on gamma correction, 2D FIR filtering, and on the other processing features available in the DVI video processing demonstration, refer to the **IVK EDK Reference Design Tutorial** [Ref 2].

Recommended Next Steps

The recommended next steps, after going through this Getting Started Guide, are:

- Getting familiar with the **EDK Concepts, Tools, and Techniques** [Ref 48]
- Licensing the Video DMA core
- Rebuilding the DVI Video Processing and DVI Frame Buffer demonstrations
- Modify the demonstrations to meet your needs:
  - Adding custom image processing IP cores
  - Adding Xilinx Image Processing IP cores - for a complete list, please go to: www.xilinx.com/esp/ind_sci_med/ism_avail_ip.htm

For detailed information on licensing the Video DMA core and rebuilding the project and adding IP to the video processing pipeline, please refer to the **IVK EDK Reference Design Tutorial** [Ref 2].

INSTALLING AND LICENSING MATLAB AND SIMULINK

The ISE Design Suite: System Edition includes System Generator for DSP that enables the use of Simulink for FPGA design. Customers who wish to use or evaluate this design flow and don't already have MathWorks tools can download evaluation software per the instructions below:

Download a 30-day trial of MATLAB and Simulink for FPGA design
www.mathworks.com/xilinx_dspkits

The trial request form will automatically populate with the required and recommended MathWorks product mix for System Generator. The MathWorks software Release 2009b is compatible with Xilinx® ISE® Design Suite 11.4.

E-mail: fpga_expert@mathworks.com with questions.

GETTING ADDITIONAL HELP AND SUPPORT

Avnet Support

For questions regarding the Avnet Spartan-6 Industrial Video Processing Kit, please visit the product website at:

www.em.avnet.com/spartan6video

Once on the IVK product website:

To access the latest IVK documentation and designs, click on the following link:

To access technical support for the IVK, click on the following link:

To access the technical forums, clock on the following icon:

Xilinx Support

For questions regarding products within your Product Entitlement Account or if you feel you have received this notification in error, send an e-mail message to your regional Customer Service Representative:

Canada, USA and South America - isscs_cases@xilinx.com

Europe, Middle East, and Africa - eucases@xilinx.com

Asia Pacific including Japan - apaccase@xilinx.com

For technical support including the installation and use of your product license file you may contact Xilinx Online Technical Support at www.support.xilinx.com. On this site you will also find the following resources for assistance:

Software, IP and Documentation Updates

Access to Technical Support Web Tools

Searchable Answer Database with Over 4,000 Solutions

User Forums

REFERENCES

All documentation supporting the Spartan-6 Industrial Video Processing Kit is available on the Avnet Design Resource Center (DRC): www.em.avnet.com/spartan6video

1. Getting Started with the Spartan-6 Industrial Video Processing Kit
   www.em.avnet.com/spartan6video ➔ Support Files & Downloads
2. Spartan-6 Industrial Video Processing Kit – Reference Designs User Guide
   www.em.avnet.com/spartan6video ➔ Support Files & Downloads
3. Avnet Spartan-6 LX150T Development Kit – Hardware User Guide
   www.em.avnet.com/spartan6lx150t-dev ➔ Support Files & Downloads
4. Avnet FMC-IMAGEOV – Hardware User Guide
   www.em.avnet.com/fmc-image ➔ Support Files & Downloads
5. Avnet FMC-DVI – Hardware User Guide
   www.em.avnet.com/fmc-dvi ➔ Support Files & Downloads
6. Avnet LCD Interface (ALI) Specification, Version 1.00
   www.em.avnet.com/spartan6video ➔ Support Files & Downloads

The OmniVision OV9715 image sensor datasheet can be obtained from the OmniVision web site.

7. OmniVision OV9715 Image Sensor – datasheet request form
   www.ovt.com/support/datasheet.php

The following reference provides links to documentation supporting video interfaces (XSVI) and video intellectual property (IP).

8. WP### Xilinx Video Communication Interfaces White Paper
   www.xilinx.com ➔ search for XSVI on the Xilinx web site
9. Color Filter Array Interpolation
   www.xilinx.com/products/ipcenter/EF-DI-CFA.htm
10. Color Correction Matrix
    www.xilinx.com/products/ipcenter/EF-DI-CCM.htm
11. Defective Pixel Correction
    www.xilinx.com/products/ipcenter/EF-DI-DEF-PIX-CORR.htm
12. Gamma Correction
    www.xilinx.com/products/ipcenter/EF-DI-GAMMA.htm
13. Image Edge Enhancement
    www.xilinx.com/products/ipcenter/EF-DI-IMG-ENHANCE.htm
14. Image Noise Reduction
    www.xilinx.com/products/ipcenter/EF-DI-IMG-NOISE.htm
15. Image Statistics Engine
    www.xilinx.com/products/ipcenter/EF-DI-IMG-STATS.htm
16. Motion Adaptive Noise Reduction
    www.xilinx.com/products/ipcenter/EF-DI-IMG-MA-NOISE.htm

17. RGB to YCrCb Color-Space Converter
    www.xilinx.com/products/ipcenter/RGB_to_YCrCb.htm
18. YCrCb to RGB Color-Space Converter
    www.xilinx.com/products/ipcenter/YCrCb_to_RGB.htm
19. Video Direct Memory Access (DMA)
    www.xilinx.com/products/ipcenter/EF-DI-VID-DMA.htm
20. Video On Screen Display (OSD)
    www.xilinx.com/products/ipcenter/EF-DI-OSD.htm
21. Video Scaler
    www.xilinx.com/products/ipcenter/EF-DI-VID-SCALER.htm
22. Video Timing Controller
    www.xilinx.com/products/ipcenter/EF-DI-VID-TIMING.htm

The following references provides links to documentation supporting Spartan-6 FPGAs, tools, and IP. For additional information, see www.xilinx.com/support/documentation/index.htm.

23. DS160 Spartan-6 Family Overview
    www.xilinx.com/support/documentation/data_sheets/ds160.pdf
24. DS162 Spartan-6 FPGA Data Sheet: DC and Switching Characteristics
    www.xilinx.com/support/documentation/data_sheets/ds162.pdf
25. UG380 Spartan-6 FPGA Configuration User Guide
    www.xilinx.com/support/documentation/user_guides/ug380.pdf
26. UG381 Spartan-6 FPGA SelectIO Resources User Guide
    www.xilinx.com/support/documentation/user_guides/ug381.pdf
27. UG382 Spartan-6 FPGA User Guide: Clocking Resources
    www.xilinx.com/support/documentation/user_guides/ug382.pdf
28. UG383 Spartan-6 FPGA Block RAM Resources User Guide
    www.xilinx.com/support/documentation/user_guides/ug383.pdf
29. UG384 Spartan-6 FPGA Configurable Logic Block User Guide
    www.xilinx.com/support/documentation/user_guides/ug384.pdf
30. UG385 Spartan-6 FPGA Packaging and Pinouts
    www.xilinx.com/support/documentation/user_guides/ug385.pdf
31. UG386 Spartan-6 FPGA GTP Transceivers User Guide
    www.xilinx.com/support/documentation/user_guides/ug386.pdf
32. UG388 Spartan-6 FPGA Memory Controller User Guide
    www.xilinx.com/support/documentation/user_guides/ug388.pdf
33. UG389 Spartan-6 FPGA DSP48A1 Slice User Guide
    www.xilinx.com/support/documentation/user_guides/ug389.pdf
34. UG029 ChipScope Pro Software and Cores User Guide
    www.xilinx.com/tools/cspro.htm
35. DS614 Clock Generator Data Sheet
    www.xilinx.com/support/documentation/ip_documentation/clock_generator.pdf
36. DS643 Multi-Port Memory Controller (MPMC) Data Sheet
    www.xilinx.com/support/documentation/ip_documentation/mpmc.pdf
37. UG138 LogiCORE™ IP Tri-Mode Ethernet MAC User Guide
    www.xilinx.com/support/documentation/ip_documentation/tri_mode_eth_mac_ug138.pdf

Documents supporting the Spartan-3ADSP Video Starter Kit:

38. XtremeDSP Video Starter Kit — Spartan-3A DSP Edition
    www.xilinx.com/support/documentation/do-s3adsp-video-sk-uni-g.htm
39. XtremeDSP Video Starter Kit — Spartan-3A DSP Edition
    www.xilinx.com/support/documentation/do-s3adsp-video-sk-uni-g.htm
40. UG456 Spartan-3A DSP FPGA Video Starter Kit User Guide
    www.xilinx.com/support/documentation/boards_and_kits/ug456.pdf
41. UG514 Spartan-3A DSP FPGA Video Starter Kit Software User Guide
    www.xilinx.com/support/documentation/boards_and_kits/ug514.pdf

Various video related reference designs:

42. XAPP1064 Source-Synchronous Serialization and Deserialization (up to 1050 Mbps)
    www.xilinx.com/support/documentation/application_notes/xapp1064.pdf
43. XAPP460 Video Connectivity Using TMDS I/O in Spartan-3A FPGAs
    www.xilinx.com/support/documentation/application_notes/xapp460.pdf
44. XAPP930 Color-Space Converter: RGB to YCrCb
    www.xilinx.com/support/documentation/application_notes/xapp930.pdf
45. XAPP931 Color-Space Converter: YCrCb to RGB
    www.xilinx.com/support/documentation/application_notes/xapp931.pdf
46. XAPP932 Chroma Resampler
    www.xilinx.com/support/documentation/application_notes/xapp932.pdf
47. XAPP1136 Integrating a Video Frame Buffer Controller (VFBC) in System Generator
    www.xilinx.com/support/documentation/application_notes/xapp1136.pdf

Xilinx provides an excellent document that provides a more in depth description of how to work in the EDK development environment:

48. UG683 EDK Concepts, Tools, and Techniques
    www.xilinx.com/support/documentation/sw_manuals/xilinx12_2/edk_ctt.pdf

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