## Configuring the Xilinx Spartan-6 LX9 MicroBoard



Version 1.3

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## **Revision History**

Version	Description	Date
1.1	Initial release for ISE 13.1 and 12.x	3/7/11
1.2	Eliminated redundant step in Appendix A	3/22/11
1.3	Added steps to open Windows Device Manager. Added link for MCS creation instructions, Tested fully against Windows7,64-bit.	4/18/11



### Overview

The Spartan-6 LX9 MicroBoard has two external interfaces for configuring the FPGA. There is a traditional Platform Cable JTAG header on the bottom of the board (J6) and a new on-board USB-to-JTAG circuit. Both interfaces offer the ability to configure the FPGA and program the on-board serial flash, as well as other Xilinx JTAG functions like Chipscope and SDK Debugger..

The FPGA is pre-set to Master Serial Mode, which means it initiates configuration upon power-up and generates a configuration clock. It reads configuration data from an on-board <u>Micron 128Mb</u> <u>Serial Flash memory</u>. This flash can be programmed through either of the two aforementioned interfaces. This document will illustrate how to use these interfaces to configure the FPGA and program the on-board serial flash.

**Note**: Throughout this document, the word '**configuration**' applies to downloading a bitstream to the FPGA whereas the word '**programming**' applies to downloading a flash image to the onboard serial flash.

This board provides three ways to program the serial flash:

- 1. iMPACT Indirect SPI Programming via on-board USB-to-JTAG (Procedure #1)
- 2. SFUTIL Direct SPI Programming via on-board USB-to-SPI (Procedure #2)
- 3. iMPACT Indirect SPI Programming via external JTAG cable (Procedure #3)



Figure 1 – Spartan-6 LX9 MicroBoard Configuration Interfaces



## Configuration and Programming via the on-board USB-JTAG Circuitry

This board incorporates an on-board USB-JTAG access circuit that eliminates the need for an external Xilinx JTAG cable. The on-board JTAG is compatible with all Xilinx tools, including iMPACT, ChipScope, and SDK Debugger. This circuit can be utilized in your design if you would like JTAG access and Xilinx tool support in your product. Digilent sells this solution to customers who wish to have this capability on their own designs.

A note about using this on-board USB programming circuit is that it interfaces to a PC via an Atmel <u>AT90USB162</u> Full-Speed USB microcontroller. This microcontroller is pre-programmed by Digilent to translate USB-to-JTAG and thus providing access to the on-board JTAG chain. Since this is a Full-Speed USB interface, it will not perform as fast as Hi-Speed USB interfaces. So if faster performance is required for programming or debugging, the Xilinx Platform Cables or a High-Speed Digilent USB cable can be used.

There are two methods of using this on-board USB-JTAG circuitry. One uses iMPACT software that is included with Xilinx ISE design tools. This method gives you all the access to the FPGA that the Platform Cable solution provides. The other method uses a Digilent programming utility called SFUTIL.exe, which is run via a command line batch file. This utility only programs the attached serial flash and is much faster than using the iMPACT GUI.

Finally, this programming method is only available in ISE 12.x and ISE 11.x. ISE 13.x will be available soon.

#### **Download and Install the Digilent Drivers**

To use the Digilent USB-JTAG FPGA configuration circuitry you will first need to download and install the required Digilent software. The steps below will guide you through this process.

- 1. Open a web browser and navigate to <u>www.digilentinc.com</u>
- 2. Click on Software on the left-side of the webpage
- 3. Click on Digilent Plug-in for Xilinx Tools

First, download the plug-in.

- 4. Select Download for the appropriate version of your O/S. For this document, Windows XP Service Pack 3, 32-bit was tested as well as Windows 7, 64-bit.
- 5. Once downloaded, unzip the archive.



The archive contains both ISE11x, 12x and 13x folders. This example uses ISE 12.4, browse into the ISE12x folder.



Figure 2 – Digilent Plug-in Archive

6. Open the Digilent\_Plug-in\_Xilinx\_v12.pdf document for reference only; we will execute these instructions later in this guide.

The document states:

To begin, ensure that the Xilinx ISE Suite (12.x only) and Digilent Adept System 2.4 (or greater) is installed on the host computer.

7. If not previously completed, please install Xilinx ISE ver.12.4. Instructions for installing and licensing ISE v12.4 are available at:

http://www.xilinx.com/support/documentation/sw manuals/xilinx12 4/irn.pdf

As stated in the Digilent document, Digilent Adept must also be installed. The following steps will guide you through this.

- 8. In a web browser navigate to <u>www.digilentinc.com</u>
- 9. Click on Software
- 10. Click on Digilent Adept
- Select Download for the appropriate version of your O/S. For this document, Adept 2.6.1 System, 32/64-bit Windows was downloaded – digilent.adept.system\_v2.6.1.exe, (7.2MB file, dated November 22, 2010).



12. Once downloaded, launch the executable. The Digilent Adept Setup Wizard will launch, Click **Next >**.



Figure 3 – Digilent Adept Setup Wizard

13. Read the license agreement and then click I Agree.



Figure 4 – Adept License Agreement



14. Make sure all boxes are checked then click **Next >**.

🛆 Digilent Adept Setup		. 🗆 🗙
Choose Components Choose which features of Digilen	t Adept you want to install.	
Check the components you want install. Click Next to continue.	to install and uncheck the components you don't want to	
Select components to install:	<ul> <li>Required</li> <li>✓ Adept Runtime (install 2.5.2)</li> <li>✓ Adept Application (install 2.5.1)</li> </ul>	
Space required: 23,9MB		
	< Back Next > Cano	:el

Figure 5 – Adept Choose Components

15. Select the appropriate options then select Next >.

🛕 Digilent Adept Setup	- IX
Shortcut options Choose for which users you want to create shortcuts.	
Select whether you want to create shortcuts for yourself only or for all users of this computer. Click Next to continue.	
Create Shortcuts	_
For anyone using this computer	
C Just for me	
Create Quick Launch shortcuts?	
< Back Next >	Cancel

Figure 6 – Adept Shortcuts



16. Browse to the preferred Destination Folder then click **Install**.

🛕 Digilent Adept Setup	
<b>Choose Install Location</b> Choose the folder in which to install Digilent Adept.	
Setup will install Digilent Adept in the following folder. To Browse and select another folder. Click Install to start the	install in a different folder, click e installation.
Destination Folder	Browse
Space required: 23.9MB Space available: 20.4GB	
< Bac	k Install Cancel

Figure 7 – Adept Choose Install Location

17. Click Continue Anyway.



Figure 8 – Windows Logo Testing



18. Uncheck both boxes, and then click **Finish**.



Figure 9 – Complete Adept Setup



Now we will complete the installation of the Plug-in.

- 19. Browse to the unzipped libCseDigilent\_2.0.3-x86-x64-Windows archive, then into the ISE12x\plugin\nt\plugins directory.
- Copy the Digilent folder to the Xilinx ISE 12.4 installation at C:\Xilinx\12.4\ISE\_DS\ISE\Iib\nt\plugins. This is how your Xilinx ISE plugins directory should look after completing this:



Figure 10 – Digilent Plug-ins Copied to ISE 12.4 Installation

**NOTE**: The directory structure is the same for ISE 13.x with the only thing changing is the address path. It changes from 12.4 to 13.1 (for ISE 13.1).



- 21. Plug in the Spartan-6 LX9 MicroBoard into the PC's USB port. The included USB extension cable can be used if USB access is not convenient.
- 22. The Found New Hardware Wizard will pop up. Select **No, not this time** then **Next >**. **NOTE:** Windows 7 may complete the following steps automatically. If so, that completes this section.

Found New Hardware Wizard	
	Welcome to the Found New Hardware Wizard Windows will search for current and updated software by looking on your computer, on the hardware installation CD, or on the Windows Update Web site (with your permission). Read our privacy policy
	Can Windows connect to Windows Update to search for software? O Yes, this time only O Yes, now and every time I connect a device O No, not this time Click Next to continue.
	< Back Next > Cancel

Figure 11 – Found Digilent JTAG USB Hardware

23. Select Install the software automatically then click Next >.





#### Figure 12 – Install Software Automatically

24. A warning will appear about Windows Logo testing, see the figure below. Press the **Continue Anyway** button.

Hardware	: Installation
<u>.</u>	The software you are installing for this hardware: Digilent USB Device has not passed Windows Logo testing to verify its compatibility with Windows XP. (Tell me why this testing is important.) Continuing your installation of this software may impair or destabilize the correct operation of your system either immediately or in the future. Microsoft strongly recommends that you stop this installation now and contact the hardware vendor for software that has passed Windows Logo testing.
	Continue Anyway STOP Installation

Figure 13 – Warning: Not passed Windows Logo testing

25. Press the **Finish** button to complete the process. This will complete installation of the Digilent USB drivers.





#### Figure 14 – Digilent USB Device driver installed

# Procedure 1: Configuration and Programming using iMPACT with the on-board USB-JTAG Circuitry

Once the Digilent driver is installed, you can continue with configuration and programming using the on-board USB-JTAG Circuitry. Follow the steps for programming and configuring using this method.

- 1. Make sure no Xilinx or Digilent programming cable is attached to the PC.
- If not done so already, connect the Spartan-6 LX9 MicroBoard to the host PC by plugging it into an open USB port or by using the USB extension cable (Type A Male to Type A Female) as show here:



Figure 15 – Connect USB-JTAG programming interface to host PC



3. Check in the Windows Device Manager to ensure the Digilent USB Driver is available. To open Windows Device Manager, select Start → Control Panel → System (System and Security for Windows 7). For WinXP, In the System Properties window, select the Hardware tab then click on Device Manager. For Windows 7, just click on Device Manager. Expand Universal Serial Bus Controllers, if the Digilent USB device is not listed, please follow the steps in the section, Download and Install the Digilent Drivers:

🖳 Device Manager	<u> </u>
File Action View Help	
🗄 🗳 Universal Serial Bus controllers	
🛛 🕰 Digilent USB Device	
Generic USB Hub	
Generic USB Hub	
🖌 😋 Intel(R) 82801G (ICH7 Family) USB Universal Host Controller - 27C8	
- 🚓 Intel(R) 82801G (ICH7 Family) USB Universal Host Controller - 27C9	
🛛 🚔 Intel(R) 82801G (ICH7 Family) USB Universal Host Controller - 27CA	
🖌 😋 Intel(R) 82801G (ICH7 Family) USB Universal Host Controller - 27CB	
🛶 🙀 Intel(R) 82801G (ICH7 Family) USB2 Enhanced Host Controller - 27CC	
USB Composite Device	
· 즉 육 USB Mass Storage Device	
USB Printing Support	
USB Root Hub	
USB Root Hub	
USB Root Hub	
Sector State	
USB Root Hub	_

Figure 16 – Windows Device Manager

- 4. Launch iMPACT 12.4 by selecting Start → Programs → Xilinx ISE Design Suite 12.4 → ISE Design Tools → Tools → iMPACT.
- 5. Select create a new project (.ipf) at the New iMPACT Project Wizard and click OK.



New iMPACT Project		×
I want to		
C load most recent project	▼ Browse,	
	$\square$ Load most recent project file when iMPACT starts	
• create a new project (.ipf) test.ipf	Browse	
ОК	Cancel	

Figure 17 – New iMPACT Project Wizard

6. Select the option to **Configure devices using Boundary-Scan (JTAG)** then click **OK**.

🐉 Welcome to iMPACT	×
Please select an action from the list below	
Configure devices using Boundary-Scan (JTAG)	
Automatically connect to a cable and identify Boundary-Scan chain	
C Prepare a PROM File	
C Prepare a System ACE File	
C Prepare a Boundary-Scan File	
SVF	
OK Carcel	

Figure 18 – Configure Devices



7. A warning is issued that a cable cannot be found. This is expected and normal since we have not configured iMPACT to use the Digilent Cable. Click **OK** to close the warning.



Figure 19 – Can Not Find Cable

- 8. In iMPACT, select **Output**  $\rightarrow$  **Cable Setup**.
- 9. Click **OK** to clear the error.

💳 Error	Message X
8	ERROR: iMPACT - This function requires that a target is opened first.
	ОК

Figure 20 – iMPACT Error

10. Check the box to **Open Cable Plug-in**. In the dialog box, type "digilent\_plugin" as shown below. Note that "digilent\_plugin" will not show up in the drop-down box even after you have installed the plug-in correctly. Click **OK**.



Cable Communication Setup	X
Communication Mode	
C Parallel Cable III	C Platform Cable USB/II
C Parallel Cable IV	
	Advanced USB Cable Setup
TCK Speed/Baud Rate:	Port:
Default Speed	<b></b>
Cable Location	
C Remote	
Cable Plug-in	
🔽 Open Cable Plug-in. Select or enter	a Plug-in from the list below:
digilent_plugin	
OK Ca	ncel Help

Figure 21 – Cable Communication Setup



11. In the Boundary Scan area, right-click and select **Initialize Chain**.

r			
1111111111		Add Xilinx Device Add Non-Xilinx Device	Ctrl+D Ctrl+K
	Right click to Add Device or Initialize JTAG chain	Initialize Chain	Ctrl+I
		Cable Auto Connect Cable Setup	
1111		Output File Type	+
	Boundary Scan		

Figure 22 – Initialize Chain

12. Follow the pop-up dialog window to select a .BIT file by clicking **Yes**. Selecting a .BIT file will directly configure the FPGA. The FPGA is non-volatile however and thus a power-cycle or pressing the PROG pushbutton, SW4, will cause the FPGA to lose this configuration.





Figure 23 – JTAG Chain Identified



13. To program the attached SPI Flash, either continue with the Configuration File Assignment or right-click on the SPI/BPI link above the FPGA and select 'Add SPI/BPI Flash'. This will require a .MCS file which can be generated from a .BIT file in the iMPACT software. To create a .MCS file, see <u>Appendix A</u> or consult iMPACT help or the <u>Xilinx Spartan-6 FPGA</u> <u>Configuration Guide</u>.

**NOTE**: programming an uncompressed LX9 bitstream to the Flash using the iMPACT GUI takes approximately 17 minutes. The command-line mode detailed in <u>Procedure 2</u> is much faster as it bypasses the JTAG protocol.

🐉 ISE iMPACT (M.81d) - [Boundary Scan]		
🛞 File Edit View Operations Output Debug	Window Help	
] 🗋 ờ 🖬 🛛 🔏 🗅 🔓 🗙 🏭 🖽 🗉	🚡 🗉 🛛 🎤 K?	
MPACT Flows ↔ □		
<ul> <li>         ⊕ ■ Boundary Scan         <ul> <li>SystemACE</li> <li>Create PROM File (PROM File Formatter)</li> <li> <ul> <li>WebTalk Data</li> </ul> </li> </ul></li></ul>	TDI Get Exam Add xc6s byps TDO Set I Set I	Device ID Device Signature/Usercode SPI/BPI Flash gn New Configuration File Programming Properties Erase Properties
IMPACT Processes ↔	Laur	nch File Assignment Wizard
Available Operations are: Get Device ID Get Device Signature/Usercode Read Device Status		

Figure 24 – Selecting SPI Flash



14. Select SPI PROM, N25Q128 and change the Data Width to 4. Setting the Data Width to four bits wide requires that the bitstream and MCS files were created to support this width. It is acceptable to use x1 and x2 data widths as well. See <u>Appendix A</u> for details on how to create bitstreams that support wider data widths. Note: ISE 12.x may not show the voltages (1.8V/3.3V) after N25Q128.

Select Attached SPI/BPI	2
Select the PROM attached to FPGA:	
SPI PROM	N25Q128 1.8/3.3V
Data Width:	4
OK	Cancel

Figure 25 – Select N25Q128 PROM



15. The Flash above the FPGA will now look like an IC labeled 'FLASH'. Right-click on this and select Program:



Figure 26 – Right-click on FLASH and select Program

16. Device Programming Properties will appear. Click OK.

Value		
Value V		
V		
operties		
auton	natically load FPGA v	
	Apply	Apply Help

Figure 27 – Device Programming Properties



17. iMPACT will begin programming the Flash, depending on the size of the MCS file, this could take several minutes. Once completed, assuming no errors are encountered, the Flash is programmed and the FPGA will now have its configuration data stored in non-volatile memory. The FPGA will automatically reconfigure with this new image upon pressing the PROG\_B pushbutton, SW4, or power cycling the board.

🐉 ISE iMPACT (M.81d) - [Boundary Scan]		
🐼 File Edit View Operations Output Debug Win	ndow Help	_ 8 ×
🗋 ờ 🔒   器 器 🛷   😤 🗉   🔑 🌾		
iMPACT Flows ↔ □ 문 × Right	ht click device to select operations	
	xc6six9 bypass TDO	
MPACT Processes ↔		
5	Configuration Operation Status	
	Execution command	
	2%	
	Abort	
2	· · · · ·	
	Boundary Scan	
Console		+□ & ×
INFO: iMPACT - 0011 1100 1110 1100	)	
INFO: iMPACT: 2492 - '1': Completed	d downloading core to device.	
'1': IDCODE is '20ba18' (in hex).		
'1': ID Check passed.		
'1': IDCODE 13 '200818' (in nex)		
'1': Erasing Device.		
'1': Using Sector Erase.		
'1': Programming Flash.		
		<u> </u>
Console 💟 Errors 🔔 Warnings		
		Configuration Avnet On-Board Programmer 4000000

Figure 28 – Device Programming

Note: See <u>Appendix B</u> for improved programming performance.

This concludes this section. Programming of the serial flash and configuration of the FPGA are completed.



#### Procedure 2: Programming via on-board USB-JTAG Circuitry and Digilent's Serial Flash Utility

The Digilent SFUTIL.exe utility provides a fast programming interface to the on-board serial flash. The utility must be downloaded from Digilent's website. Once downloaded, this utility can be run from Windows command line or a batch file. Additionally this utility is customizable to perform a number of functions. To use this utility, follow the below instructions:

1. Open a Web Browser and navigate to Digilent's website:

http://www.digilentinc.com/

2. Click on **Software** link under Products:



Figure 29 – Select Software on Digilent's Webpage

3. Scroll down to Serial Flash Utility and click Download!



Figure 30 – Download Serial Flash Utility

4. Save the attached zip file and extract it to a known place on your PC.



5. In this same directory create a batch file. Open a text editor, such as Notepad, and copy the following commands:

- The 'sfutil' executable is called with options to program this S6LX9 MicroBoard's on-board serial flash. This serial flash utility accepts MCS format files. These files can be created with ISE iMPACT software from a FPGA's bitstream file. The placeholder, 'PROGRAMMING\_IMAGE.mcs', must be replaced with your MCS file.
- 7. Save this batch file, for example S6\_LX9\_EraseProgram.bat, and close the editor.
- 8. Connect the S6LX9 MicroBoard to the host PC as shown in Figure 15.
- 9. Double-click the batch file created above to execute it. Programming will ensue. **Note:** Programming times will vary based on FPGA Utilization as well as USB port speed.



Figure 31 – SFUTIL Programming

Note: See <u>Appendix B</u> for improved programming performance.

This concludes this section, to learn more about SFUTIL, type 'sfutil ?' at a DOS prompt or visit Digilent's Website.



# Configuration and Programming using Xilinx iMPACT and Platform Cable USB

Using a <u>Xilinx USB JTAG Platform Cable</u> and Xilinx's iMPACT programming tool, the FPGA can be configured directly, as well as program the attached flash device. The iMPACT programming tool is a subset of the Xilinx ISE WebPACK or ISE Design Suites which can be downloaded from here:

http://www.xilinx.com/tools/designtools.htm

#### Procedure 3: iMPACT using a Platform Cable USB

To configure the Spartan-6 LX9 FPGA and program the attached serial flash using this method, follow the steps outlined below:

- Power must be applied to the MicroBoard. This is done by connecting the board to the host PC via the MicroUSB cable. Alternatively, the board can be connected via the Type-A USB connector as shown in <u>Figure 15</u>.
- 19. Connect the Xilinx Platform Cable to the host PC and S6LX9 MicroBoard's JTAG port, J6.
- 20. When completed, the S6LX9 MicroBoard should be connected to the host PC as shown in the figure below:



Figure 32 – Configuration Setup with Xilinx Platform Cable USB



- 21. Launch iMPACT 12.4 or 13.1 by selecting Start → Programs → Xilinx ISE Design Suite 13.1 → ISE Design Tools → Tools → iMPACT.
- 22. Select **No** when asked to automatically load the last project and when asked to create and save a project.



Figure 33 – Automatic iMPACT Project Wizard

23. Select create a new project (.ipf) at the New iMPACT Project Wizard and click OK.

🐉 New iMPACT Project	×
I want to	
C load most recent project top.ipf	Browse
	$\square$ Load most recent project file when iMPACT starts
• create a new project (.ipf) default.ipf	Browse
ОК	Cancel

Figure 34 – New iMPACT Project Wizard



24. Select the option to Configure devices using Boundary-Scan (JTAG) then click OK.

🐉 Welcome to iMPACT	×	
Please select an action from the list below		
Configure devices using Boundary-Scan (JTAG)		
Automatically connect to a cable and identify Boundary-Scan chain		
Prepare a PROM File		
C Prepare a System ACE File		
🔿 Prepare a Boundary-Scan File		
SVF _		
OK Cancel		
Prepare a PROM File Prepare a System ACE File Prepare a Boundary-Scan File   SVF     OK   Cancel		

Figure 35 – Configure Devices



25. Follow the pop-up dialog window to select a .BIT file by clicking **Yes**. Selecting a .BIT file will directly configure the FPGA. The FPGA is non-volatile however and thus a power cycle or pressing the PROG pushbutton, SW4, will cause the FPGA to lose this configuration.



Figure 36 – JTAG Chain Identified

26. The next pop-up dialog window asks if you want to attach a PROM device. It is OK to say YES and continue with the Configuration File Assignment Wizard, however for this example, click **No**.



Figure 37 – Attach PROM



27. Finally, Click **OK** to accept default programming properties.

Device Programming Properties - Devic	e 1 Programming Properties	×
Category Boundary-Scan Device 1 (FPGA xc6slx9)	Property Name Value Verify	
c	Cancel Apply Help	

Figure 38 – Accept Default Programming Properties

 To program the attached SPI Flash, right-click on the SPI FPGA and select 'Add SPI/BPI Flash'. This will require a .MCS file which can be generated from a .BIT file in the iMPACT software.

**NOTE**: programming the Flash using the iMPACT GUI can take as much, or more, than 5 times the programming time. It is recommended using command line mode, as detailed in <u>Procedure 2</u>, as it is much faster.



Figure 39 – Selecting SPI Flash



- 29. When asked, select the desired .MCS file to program the serial flash.
- 30. Select SPI PROM, N25Q128 and change the Data Width to 4. Setting the Data Width to four bits wide requires that the bitstream and MCS files were created to support this width. It is acceptable to use x1 and x2 data widths as well. See <u>Appendix A</u> for details on how to create bitstreams that support wider data widths. Note: ISE 12.x may not show the voltages (1.8V/3.3V) after N25Q128.

Select Attached SPI/BPI	X
Select the PROM attached to FPGA:	
SPI PROM	N25Q128 1.8/3.3V
Data Width:	4
ОК	Cancel

Figure 40 – Select N25Q128 PROM and Data Width

31. The Flash above the FPGA will now look like an IC labeled 'FLASH'. Right-click on this and select **Program**:



Figure 41 – Right-click on FLASH and select Program



32. Device Programming Properties will appear. Click **OK**. Note, properties are shown for the Attached Flash in the window below. Leave all settings as default.

j,	Device Programming Properties - Dev	/ice	e 1 Programming Properties		×
1	Category				
	Boundary-Scan → Device 1 ( FPGA xc6slx9 )		Property Name	Value	1
	Device 1 ( Attached FLASH, N250		Verify	<b>v</b>	
			General CPLD And PROM Properties		
			Erase Before Programming	V	
			FPGA Device Specific Programming Properties		
			After programming Flash	automatically load FPGA v	
				Þ	
			OK Cancel	Apply Help	

Figure 42 – Device Programming Properties



33. iMPACT will begin programming the Flash, depending on the size of the MCS file, this could take several minutes. Once completed, assuming no errors are encountered, the Flash is programmed and FPGA will now have its configuration data stored in non-volatile memory. The FPGA will automatically reconfigure with this new image upon pressing the PROG\_B pushbutton, SW4, or power cycling the board.

🐉 ISE iMPACT (M.81d) - [Boundary Scan]		
😵 File Edit View Operations Output Debug	Window Help	_ <del>_</del> # ×
🗋 ờ 🔒   器 器 🛷    🐂 🗉    🎤	k?	
iMPACT Flows ↔ □ ♂ ×	Right click device to select operations	
<ul> <li>⊕ ■ Boundary Scan</li> <li>B SystemACE</li> <li>Create PROM File (PROM File Formatter)</li> <li>⊕ ■ WebTalk Data</li> </ul>	TDIEXILIAR xc6stx9 TDO	
MPACT Processes ↔ □ -		
	Configuration Operation Status  Executing command  2%  Abort	
	Boundary Scan	
Console		+□ ⊡ ×
<pre>INFO: iMPACT - 0011 1100 1110 1 INFO: iMPACT: 2492 - '1': Comple '1': IDCODE is '20ba18' (in he '1': ID Check passed. '1': IDCODE is '20ba18' (in h '1': IDCODE is '20ba18' (in he '1': IDCODE is '20ba18' (in he) '1': IDCODE is '20ba18' (</pre>	100 ted downloading core to device. xx). mex).	×
📋 Console 🔞 Errors 🔬 Warnings		
		Configuration Avnet On-Board Programmer 4000000

Figure 43 – Device Programming



34. If no errors are encountered, programming will succeed.

🐉 ISE iMPACT (M.81d) - [Boundary Scan]		-민즈
👺 File Edit View Operations Output Debug	Window Help	<u>– 8 ×</u>
🗋 ờ 🗐    🐰 🔓 🗙 🏭 🔅	# # # 🖉 ] 🚡 🗖 ] 🌶 K?	
iMPACT Flows ↔ □ ₽ ×	Right click device to select operations	
<ul> <li>⊕ ■ Boundary Scan</li> <li>■ SystemACE</li> <li>■ Create PROM File (PROM File Formatter)</li> <li>⊕ ■ WebTalk Data</li> </ul>	TDIXC6stx9	
	TDO	
MPACT Processes ↔ □		
Available Operations are:		
Program		
In the second se		
👄 Erase		
Blank Check	Program Succeeded	
Readback	i logram Succeeded	
Get Device Checksum		
Read Device Status		
	😵 Boundary Scan 🛛 😵 PROM File Formatter: SPI Flash Single FPGA 🛛	
Console	+	• 🗆 🗗 🗙
11:Programming in x4 mode		
'1': Programmed successfully.		
() INFO: iMPACT - '1': Flash was n	programmed successfully.	
LCK cvcle = NoWait.		
LCK cycle: NoWait		
3 INFO: iMPACT - '1': Checking do	ne pindone.	
'1': Programmed successfully.	-	
PROGRESS END - End Operation.		
Elapsed time = 63 sec.		
		•
📋 Console 🙆 Errors 🔔 Warnings		
	Configuration Platform Cable USB 6 MHz u	isb-hs

Figure 44 – Programming Succeeded Window

35. This concludes this section. Programming of the serial flash and configuration of the FPGA are completed. For more on configuration using this method, please read the Spartan-6 FPGA Configuration User Guide:

http://www.xilinx.com/support/documentation/user\_guides/ug380.pdf

## Conclusion

That completes this guide. As shown in the three procedures above, there are several ways to configure the FPGA and program the attached serial flash on the S6LX9 MicroBoard. For more information please visit the <u>Avnet Design Resource Center</u> or visit <u>Xilinx's Support Website</u>. Additionally, the <u>Xilinx Spartan-6 FPGA Configuration User Guide</u> provides complete documentation for all configuration methods.



### Appendix A: Creating a SPI x4 Bitstream and MCS file

This section will show how to create a bitstream and MCS file that supports 4-bit wide SPI configuration. This must be initiated during bitstream creation. The purpose of this is to increase the configuration rate of the FPGA. The steps below guide you through this process.

1. In ISE Project Navigator, assuming the design has been fully implemented without errors, right-click on Generate Programming File and select **Process Properties**.

No Processes Running	e aspectation de la parte de la		
Processes: PB_IO_Top - Behavioral			
User Constraints User Constraints Synthesize - XST View RTL Schematic View Technology Schematic Check Syntax Generate Post-Synthesis Sir	nulation Model		
Generate Programming File     Generate Programming File	Run ReRun		
🗾 Start 🔍 Design 🚺 Files 🚺 L	Rerun All		
Warnings	View Text Report		
	Force Process Up-to-Date  Implement Top Module Design Goals & Strategies  Implement Top Module		
	Process Properties		

Figure 45 – Select Process Properties under Generate Programming File



2. In the Process Properties – Configuration Options window, select Configuration Options and set SPI Configuration Bus Width to 4. Then Click OK. (Note: you must have the Property Display Level set to Advanced to see these options.) For increased performance, the configuration rate can be increased. Moreover, the external Master CCLK (40MHz) can be used for maximum performance. Be aware this only applies to the FPGA loading the bitstream from the serial flash.

#\$Process Properties - Configuration Options					
Category	Switch Name	Property Name	Value		
General Options	-g ConfigRate:	Configuration Rate	2		
Configuration Options     Startup Options	-g ProgPin:	Configuration Pin Program	Pull Up		
- Readback Options	-g DonePin:	Configuration Pin Done	Pull Up 🔹		
Suspend/Wake Options	-g TckPin:	JTAG Pin TCK	Pull Up 🗾		
	-g TdiPin:	JTAG Pin TDI	Pull Up 🗾		
	-g TdoPin:	JTAG Pin TDO	Pull Up 🗾		
	-g TmsPin:	JTAG Pin TMS	Pull Up 🗾		
	-g UnusedPin:	Unused IOB Pins	Pull Down		
	-g UserID:	UserID Code (8 Digit Hexadecimal)	0×FFFFFFFF		
	-g ExtMasterCclk_en:	Enable External Master Clock			
	-o ExtMasterCclk_divide:	Setun External Master Clock Division	1		
	-g SPI_buswidth:	Set SPI Configuration Bus Width	4		
	granek_ere.	watchaog nimer valae	0XIIII		
		Place MultiBoot Settings into Bitstream			
	-g next_config_addr:	MultiBoot: Starting Address for Next Configuration	0x0000000		
	-g next_config_new_mode:	MultiBoot: Use New Mode for Next Configuration	M		
	-g next_config_boot_mode:	MultiBoot: Next Configuration Mode	001		
	-g golden_config_addr:	MultiBoot: Starting Address for Golden Configuration	0×00000000		
	-g failsafe_user:	MultiBoot: User-Defined Register for Failsafe Scheme 0x0000			
	· · · · · · · · · · · · · · · · · · ·				
		Property display level: Advanced 🗾 🔽 Display	switch names Default		
		OK Cancel	Apply Help		

Figure 46 – Configuration Options



3. The dialog box should close and return to ISE Project Navigator. Right-click on **Generate Programming File** and select **Run**.

Ø	No Processes Running				
Proc	tesses:	PB_IO_Top - Behavioral	Sinu	2000 - Carlo Ca	
	$\Sigma$	Design Summary/Reports			
÷	2	Design Utilities			
÷	2	User Constraints			
<u> </u>	₹ <u>2</u>	Synthesize - XST			
	<b>X</b>	View RTL Schematic			
	3	View Technology Schematic			
	-0	Check Syntax			
	<b>C</b>	Generate Post-Synthesis Sim	nulati	on Model	
<u> </u>	₹ <u>2</u>	Implement Design			
	Ē. 🚺	<u>4</u> Translate			
	Ē 🖸	🧭 Map			
	🖻 ·· 🔁	🥑 Place & Route			
····	<u>0</u>	Generate Programming File		Rup	
÷	2	Configure Target Device	+++	i sun	
·	6т	Analyze Design Using ChipScope		ReRun	
				Rerun All	
			맛	Stop	
				View Text Report	
				Force Process Up-to-Date	

Figure 47 – Generate Programming File

4. Watch the Console window to validate the programming file is created.

Console					
ſ		WebTalk report has been successfully sent to Xilinx. For additional details			
I		about this file, please refer to the WebTalk log file at			
	C:/Work/Avnet/S6LX9/PB_IO_Ports/webtalk.log				
		WebTalk is complete.			
	Process "Generate Programming File" completed successfully				
l	•				

Figure 48 – Bitstream Generation Successful



5. This process only creates a bitstream, .BIT, file used for configuring the FPGA. A .MCS file must be created for programming the attached serial flash. Expand **Configure Target Device** and select **Generate Target PROM/ACE File**. A warning window may pop up, click OK.

	No Processes Running		3	1	
91	Processes: PB_IO_Top - Behavioral		4	)x	
Byt	🔤 🗠 🗵 Design Summary/Reports				
×4	🕀 🎾 Design Utilities				
91	🕀 🎾 User Constraints				
	🖻 🏹 🦺 Synthesize - XST		5		
	🔲 🛛 🖂 View RTL Schematic				
	🛛 🚽 📝 View Technology Schematic				
	🛶 🍋 Generate Post-Synthesis Simulation Model				
	🗄 🔁 🚹 Implement Design				
🕀 🔂 Translate					
	🕀 🕀 🔁 🖉 Map				
	🗄 💽 🕗 Place & Route				
	🖻 😼 Configure Target Device				
	Generate Target PROM/ACE File	œ۳	Due	1	
	Manage Configuration Project (iMPA	11,	Run		
	Analyze Design Using ChipScope		Rerun All		
Charles Daniers Die Citers Dithursuing		煛	Stop		
			Run With Current Data		
Errors			Implement Top Module	1	
			Desire Geele (Charles)		
			Design Goals & Strategies		
		<b>9</b> 0	Process Properties		

Figure 49 – Generate PROM File



6. Double-click on Create PROM File (PROM File Formatter).



Figure 50 – Select Create PROM File



- 7. Step through the File Formatter Wizard:
  - 1. Under SPI Flash, select Configure Single FPGA
  - 2. Click left most green arrow box to continue.
  - 3. In the Storage Device (bits) pull-down, select 128M.
  - 4. Click Add Storage Device button.
  - 5. Click right most green arrow box to continue.
  - 6. Enter Output File Name and Location
  - 7. Click OK



Figure 51 – PROM File Formatter

- 8. Add Device window will appear, click **OK**. Select the .BIT file created in step 3. This .BIT file will be located in your project directory, unless specified otherwise in the ISE project.
- 9. When asked to add another device file, click **No**. A pop-up window will appear noting device entry is complete, click **OK**.



10. When returned to the iMPACT window, double-click **Generate File**. A pop-up window will appear stating Generate Succeeded.



Figure 52 – Successful PROM File Generation

- 11. This concludes generating a x4 bitstream and MCS programming file.
- 12. When exiting you will be asked to save your iMPACT project file, you may do so to prevent going through all of these steps again for future builds.



# Appendix B: Increasing USB-JTAG Circuitry Performance

# Adding a Hi-Speed USB hub to increase USB scheduling rates equals faster downloads

The Spartan-6 LX9 MicroBoard uses an Atmel <u>AT90USB162</u> full-speed USB microcontroller that is programmed to translate USB commands to JTAG commands. Most computers recognize the S6LX9 MicroBoard as a full-speed device and thus default it to a full-speed USB root hub. This can be seen in Windows Device Manager. When detected as a full-speed device, the Windows host controller enumerates the device into a full-speed scheduler. The full-speed scheduler uses a frame period of one millisecond. Hi-speed devices divide a frame into 8 micro-frames of 125 microseconds.

A trick can be applied to make the Windows PC put the S6LX9 MicroBoard into a hi-speed scheduling mode. When a hi-speed hub is plugged into a USB port, the host controller driver schedules transactions to it using the hi-speed scheduling rules. Thus when data packets are sent to the S6LX9 MicroBoard, they are done on a faster schedule. This results in faster download times. For example, the factory test code that ships with board is a large flash image and when directly plugged into a PC's USB port, download times can take nearly 7 minutes\*. However, simply inserting a hi-speed USB hub between the PC and the S6LX9 MicroBoard will reduce this time down to nearly two minutes!

This was tested on a number of hi-speed USB hubs and all had the same performance improvements.

\*Procedure 2 was used for this programming test.

#### **Upcoming Hi-Speed JTAG Interface Cable**

Avnet is pursuing a JTAG cable solution similar to Xilinx's Platform Cable series. This new cable will offer faster JTAG communication and will be offered at a much lower cost. Xilinx has full integration plans for this cable in a future ISE release. The cable will start selling in the second quarter of 2011.



## **Getting Help and Support**

Evaluation Kit home page with Documentation and Reference Designs

http://em.avnet.com/s6microboard

Avnet Spartan-6 LX9 MicroBoard forum:

http://community.em.avnet.com/t5/Spartan-6-LX9-MicroBoard/bd-p/Spartan-6LX9MicroBoard

Xilinx Spartan-6 FPGA Configuration User Guide:

http://www.xilinx.com/support/documentation/user\_guides/ug380.pdf

For Xilinx technical support, you may contact your local Avnet/Silica FAE or Xilinx Online Technical Support at www.support.xilinx.com. On this site you will also find the following resources for assistance:

- Software, IP, and Documentation Updates
- Access to Technical Support Web Tools
- Searchable Answer Database with Over 4,000 Solutions
- User Forums
- Training Select instructor-led classes and recorded e-learning options

Contact Avnet Support for any questions regarding the Spartan-6 LX9 MicroBoard reference designs, kit hardware, or if you are interested in designing any of the kit devices into your next design.

<u>http://www.em.avnet.com/techsupport</u>

You can also contact your local Avnet/Silica FAE.

