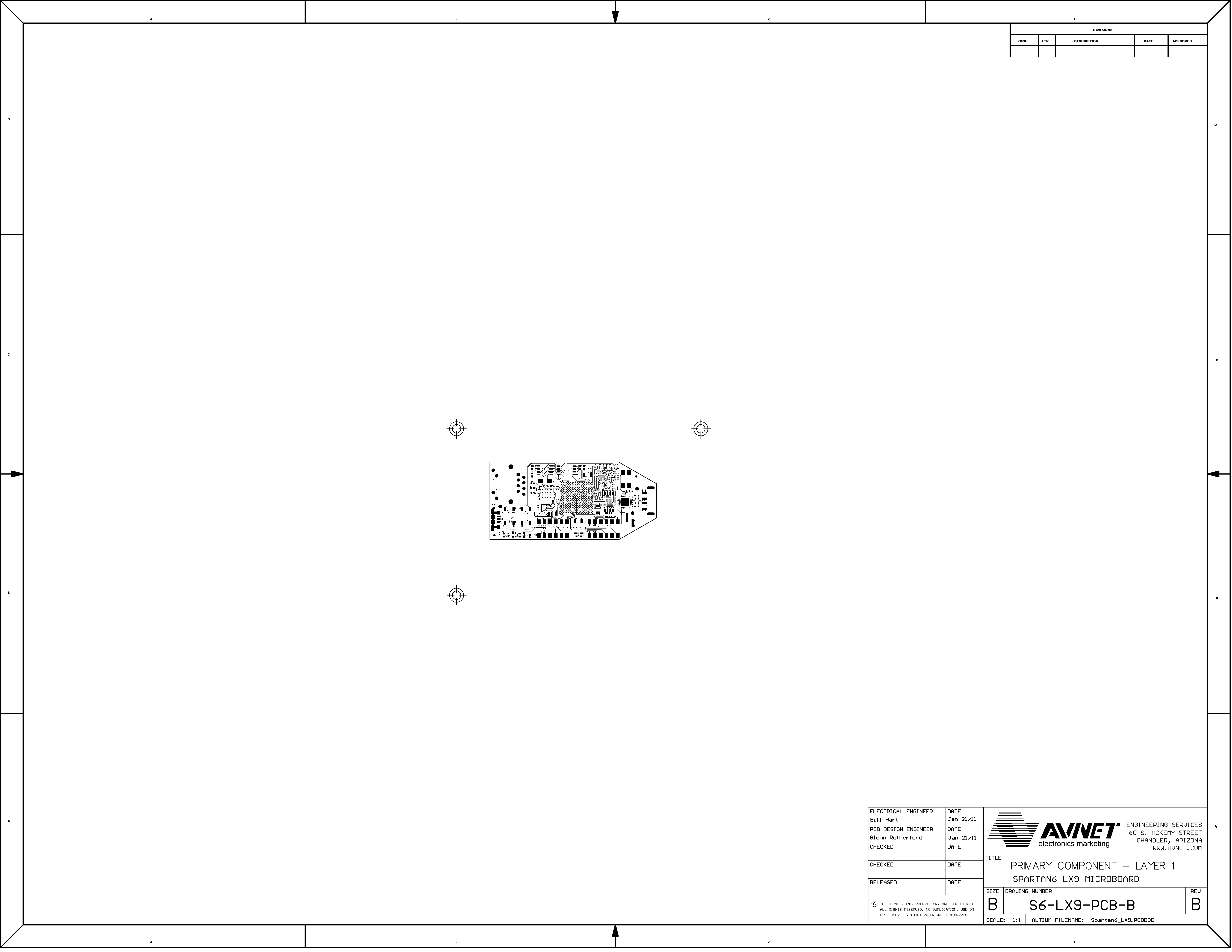
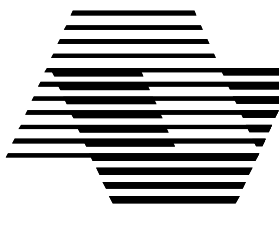




REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

ELECTRICAL ENGINEER	DATE
Bill Hart	Jan 21/11
PCB DESIGN ENGINEER	DATE
Glenn Rutherford	Jan 21/11
CHECKED	DATE
CHECKED	DATE
RELEASED	DATE

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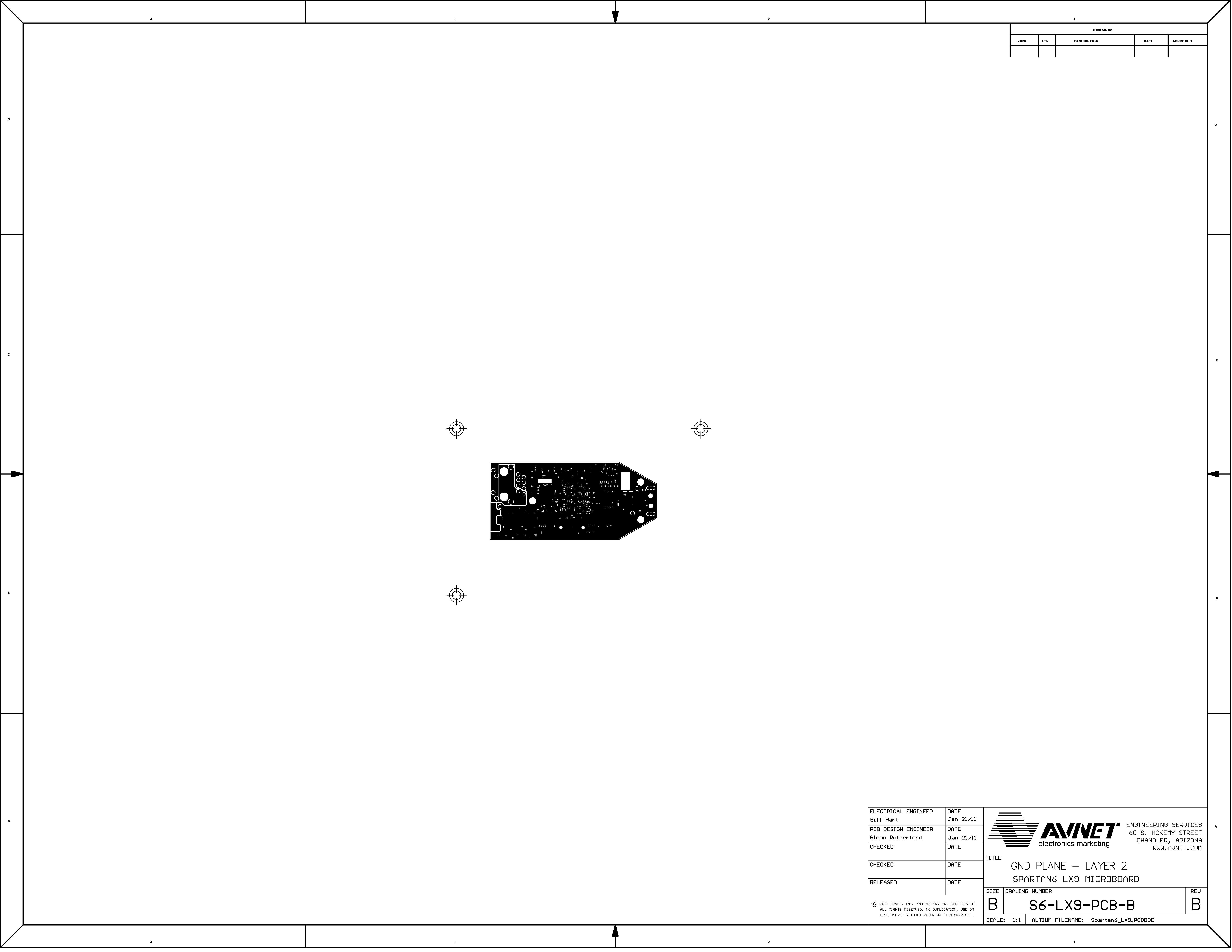
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CHANDLER, ARIZONA
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TITLE
PRIMARY COMPONENT – LAYER 1
SPARTAN6 LX9 MICROBOARD

SIZE	DRAWING NUMBER	REV
B	S6-LX9-PCB-B	B

SCALE: 1:1 ALTIUM FILENAME: Spartan6_LX9.PCBDOC



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

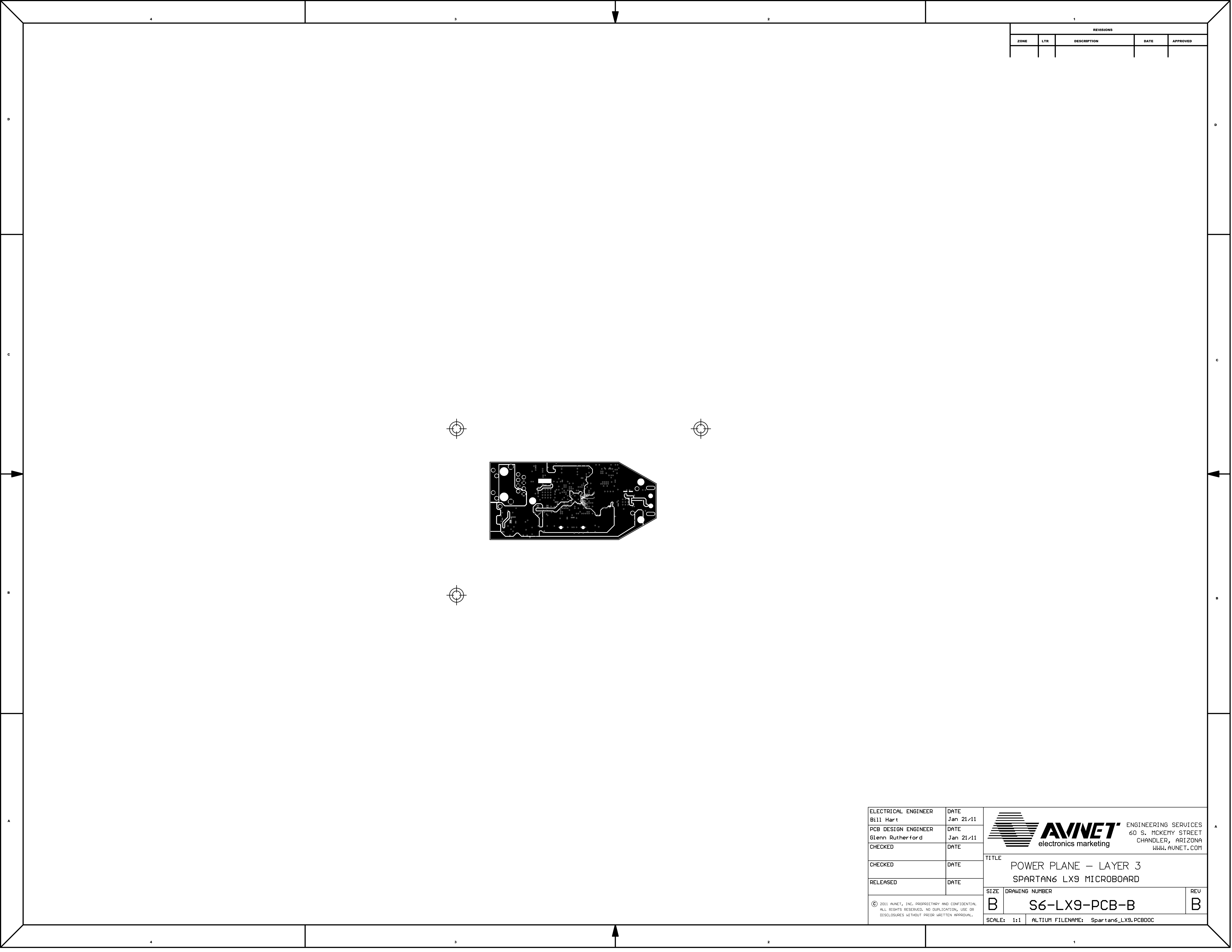
ELECTRICAL ENGINEER	DATE
Bill Hart	Jan 21/11
PCB DESIGN ENGINEER	DATE
Glenn Rutherford	Jan 21/11
CHECKED	DATE
CHECKED	DATE
RELEASED	DATE
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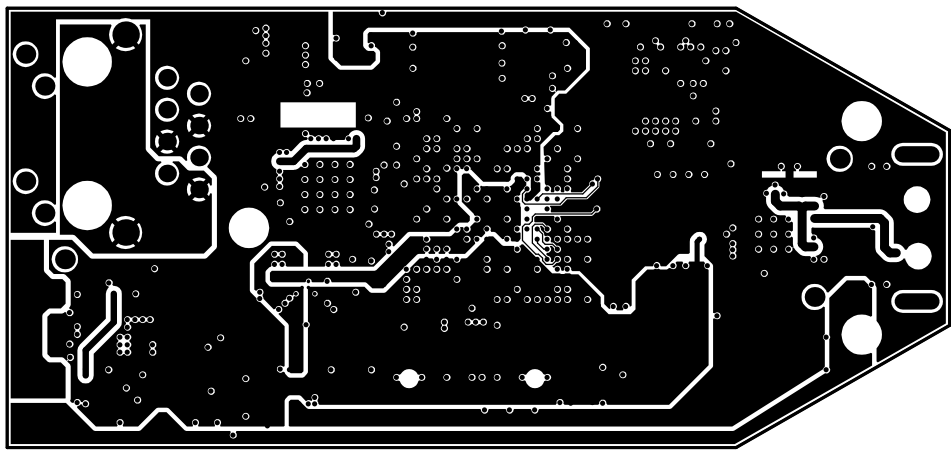
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TITLE
GND PLANE – LAYER 2
SPARTAN6 LX9 MICROBOARD

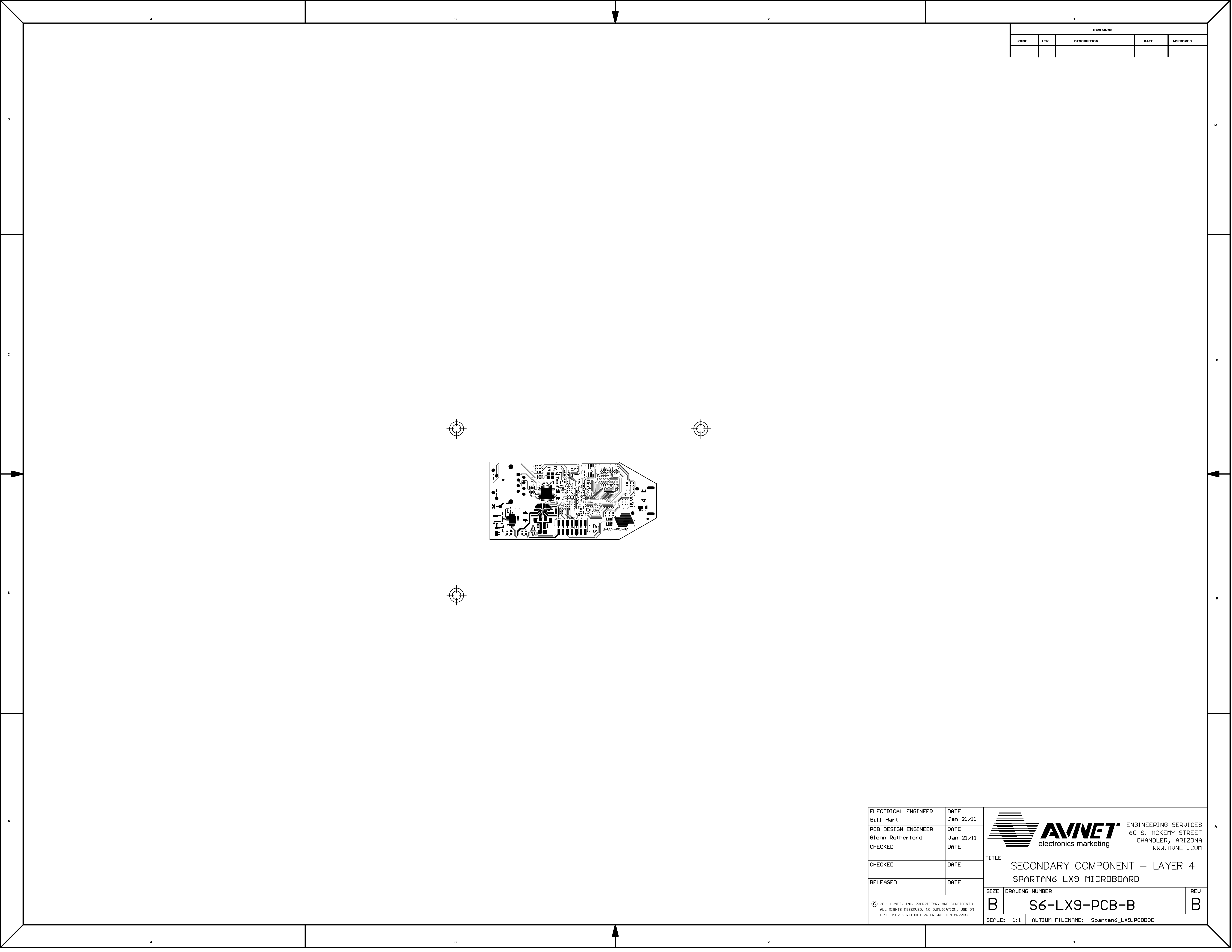
SIZE B	DRAWING NUMBER S6-LX9-PCB-B	REV B
SCALE: 1:1	ALTIUM FILENAME: Spartan6_LX9.PCBDOC	



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ELECTRICAL ENGINEER	DATE	 ENGINEERING SERVICES 60 S. MCKENY STREET CHANDLER, ARIZONA WWW.AUNET.COM		
Bill Hart	Jan 21/11			
PCB DESIGN ENGINEER	DATE			
Glenn Rutherford	Jan 21/11			
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CHECKED	DATE	TITLE POWER PLANE – LAYER 3 SPARTAN6 LX9 MICROBOARD		
RELEASED	DATE			
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SCALE: 1:1		ALTIUM FILENAME: Spartan6_LX9.PCBDOC		



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ELECTRICAL ENGINEER	DATE
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PCB DESIGN ENGINEER	DATE
Glenn Rutherford	Jan 21/11
CHECKED	DATE
CHECKED	DATE
RELEASED	DATE

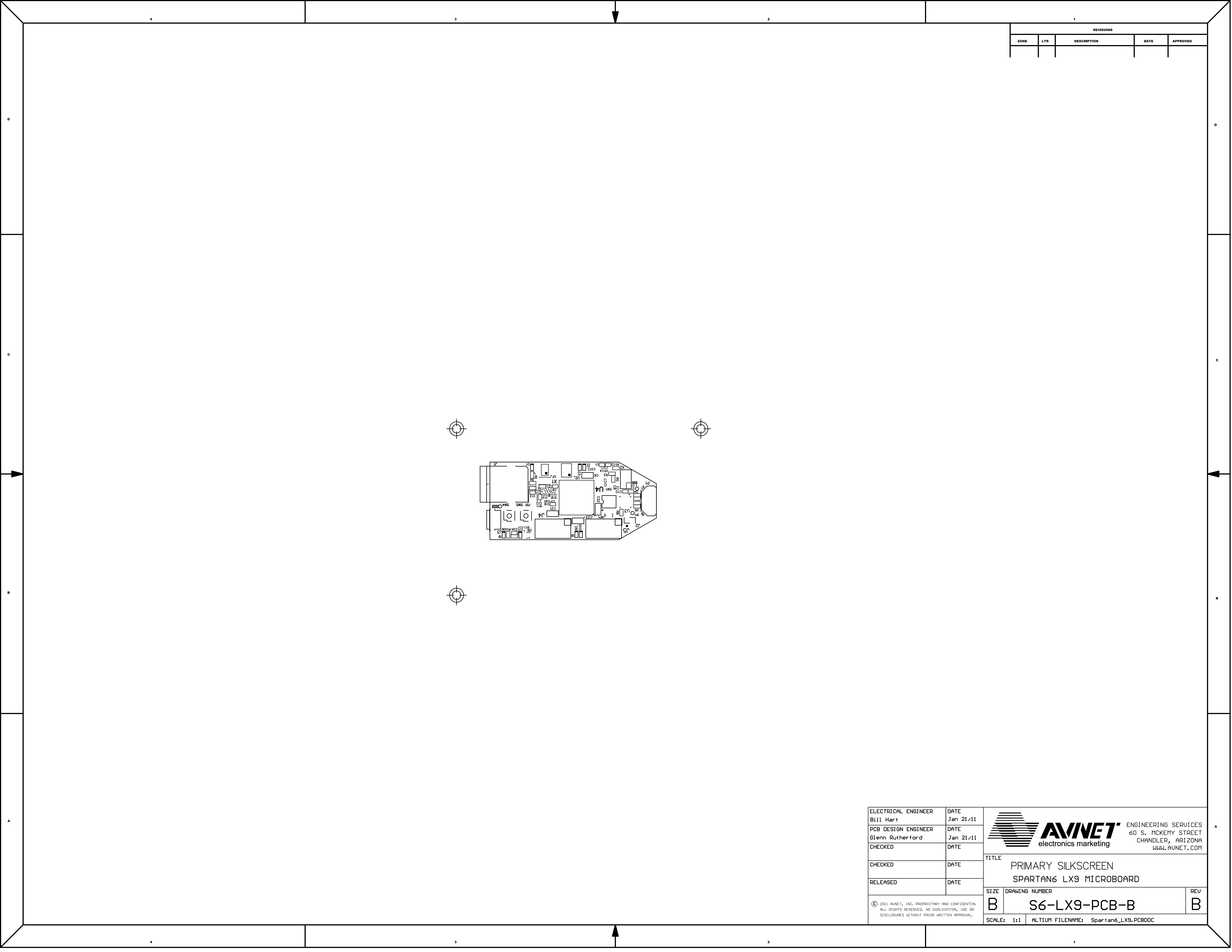
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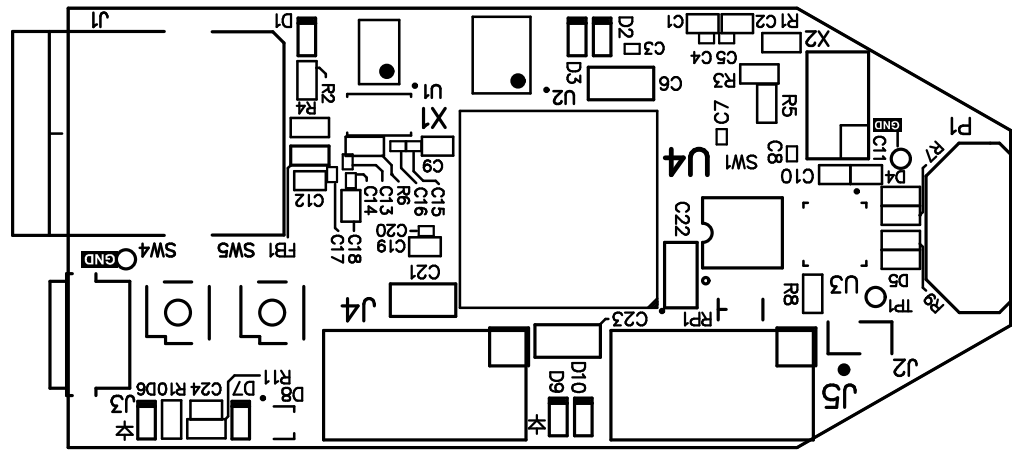
TITLE
SECONDARY COMPONENT – LAYER 4
SPARTAN6 LX9 MICROBOARD

SIZE	DRAWING NUMBER	REV
B	S6-LX9-PCB-B	B

SCALE: 1:1 ALTIUM FILENAME: Spartan6_LX9.PCBDOC



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



ELECTRICAL ENGINEER	DATE
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PCB DESIGN ENGINEER	DATE
Glenn Rutherford	Jan 21/11
CHECKED	DATE
CHECKED	DATE
RELEASED	DATE

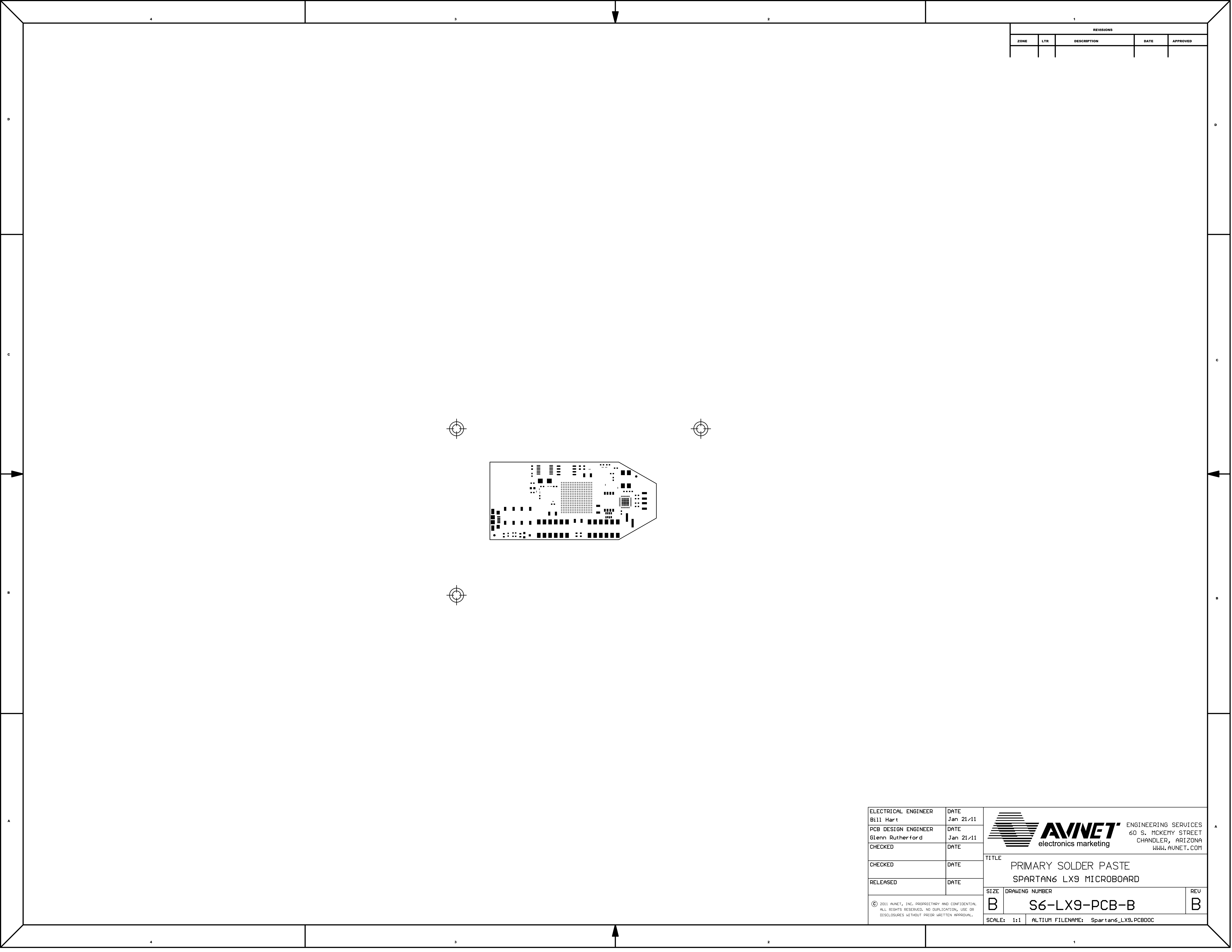
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TITLE	
PRIMARY SILKSCREEN	
SPARTAN6 LX9 MICROBOARD	

SIZE	DRAWING NUMBER	REV
B	S6-LX9-PCB-B	B

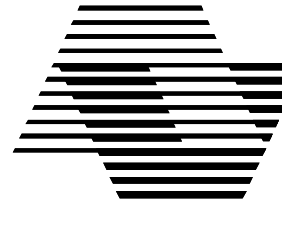
SCALE: 1:1 ALTIUM FILENAME: Spartan6_LX9.PCBDOC



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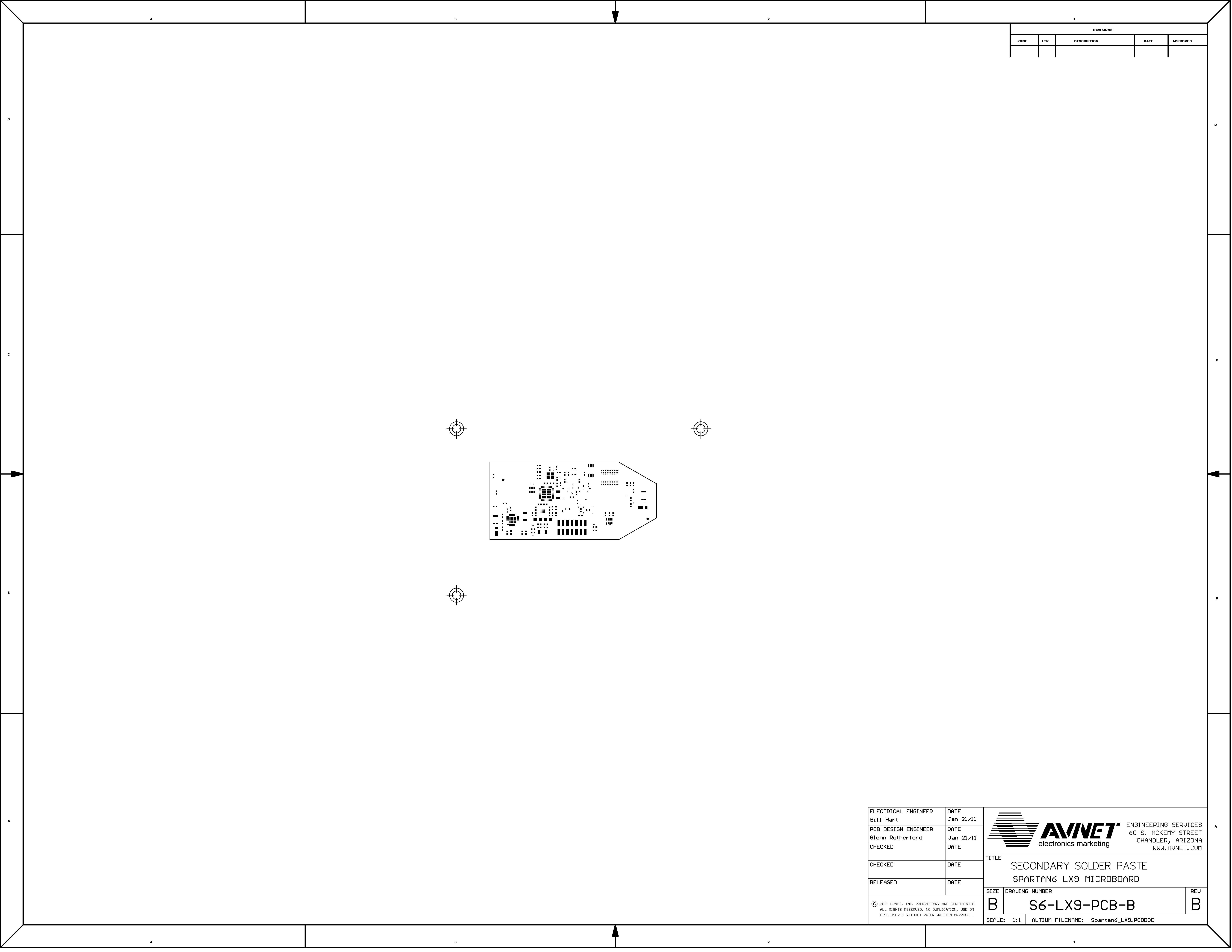
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TITLE	PRIMARY SOLDER PASTE SPARTAN6 LX9 MICROBOARD
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SIZE	DRAWING NUMBER	REV
B	S6-LX9-PCB-B	B

SCALE: 1:1 ALTIUM FILENAME: Spartan6_LX9.PCBDOC



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

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Glenn Rutherford	Jan 21/11
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RELEASED	DATE

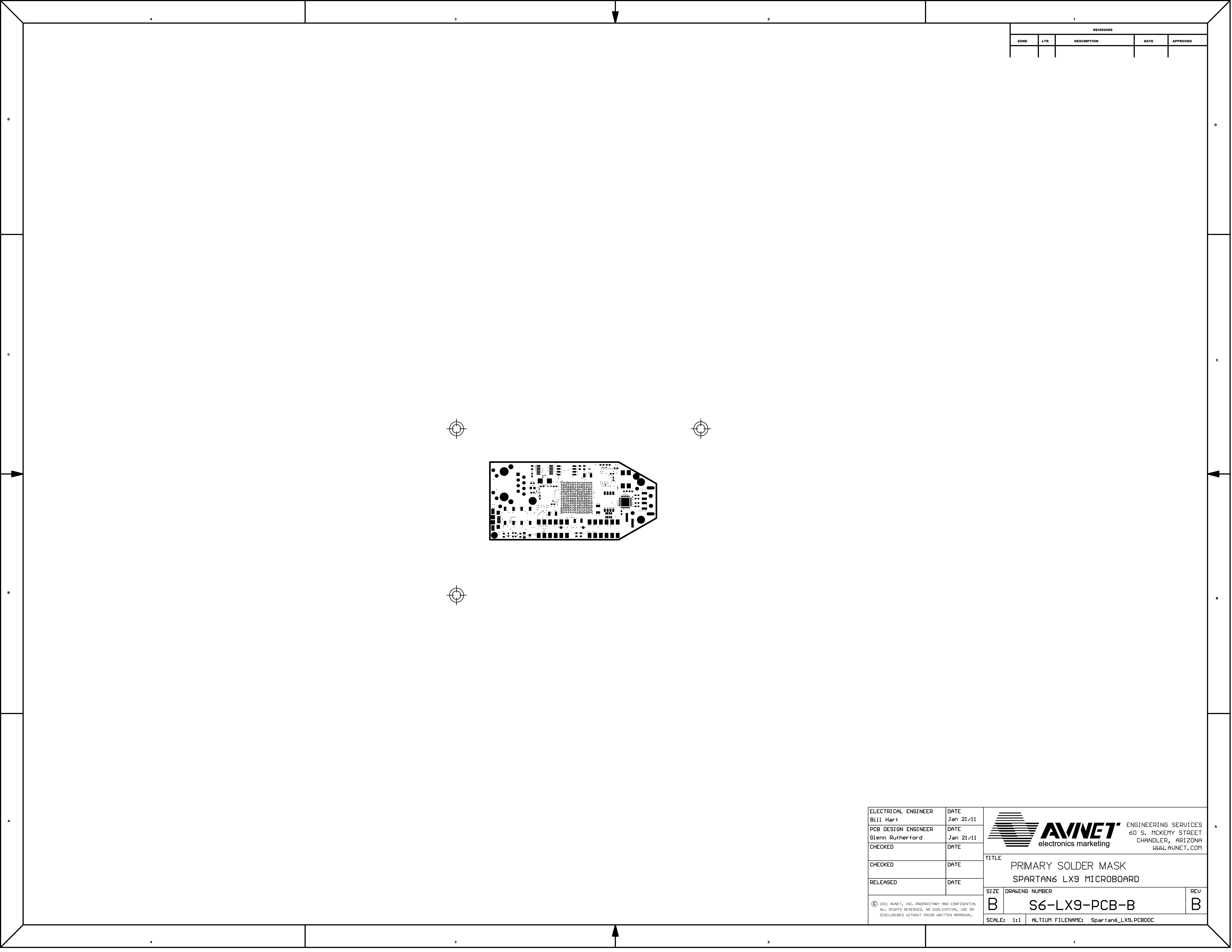
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TITLE
SECONDARY SOLDER PASTE
SPARTAN6 LX9 MICROBOARD

SIZE	DRAWING NUMBER	REV
B	S6-LX9-PCB-B	B

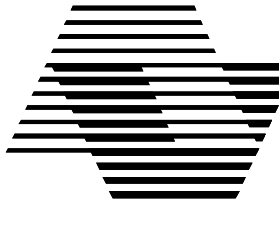
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REVISIONS				
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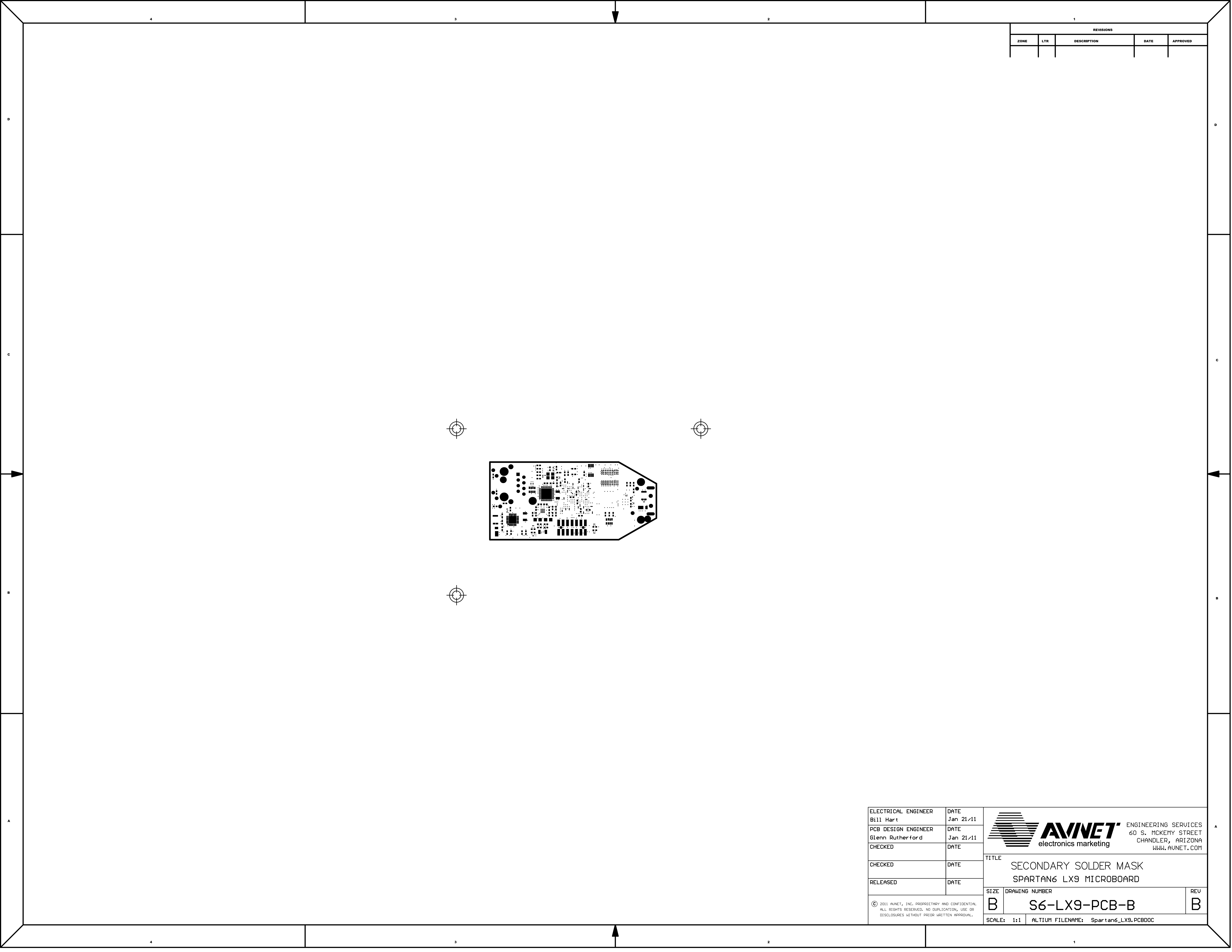
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TITLE	
PRIMARY SOLDER MASK SPARTAN6 LX9 MICROBOARD	

SIZE	DRAWING NUMBER	REV
B	S6-LX9-PCB-B	B

SCALE: 1:1 ALTIUM FILENAME: Spartan6_LX9.PCBDOC



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

ELECTRICAL ENGINEER	DATE
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TITLE
SECONDARY SOLDER MASK
SPARTAN6 LX9 MICROBOARD

SIZE	DRAWING NUMBER	REV
B	S6-LX9-PCB-B	B

SCALE: 1:1 ALTIUM FILENAME: Spartan6_LX9.PCBDOC

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

NOTES: UNLESS OTHERWISE SPECIFIED

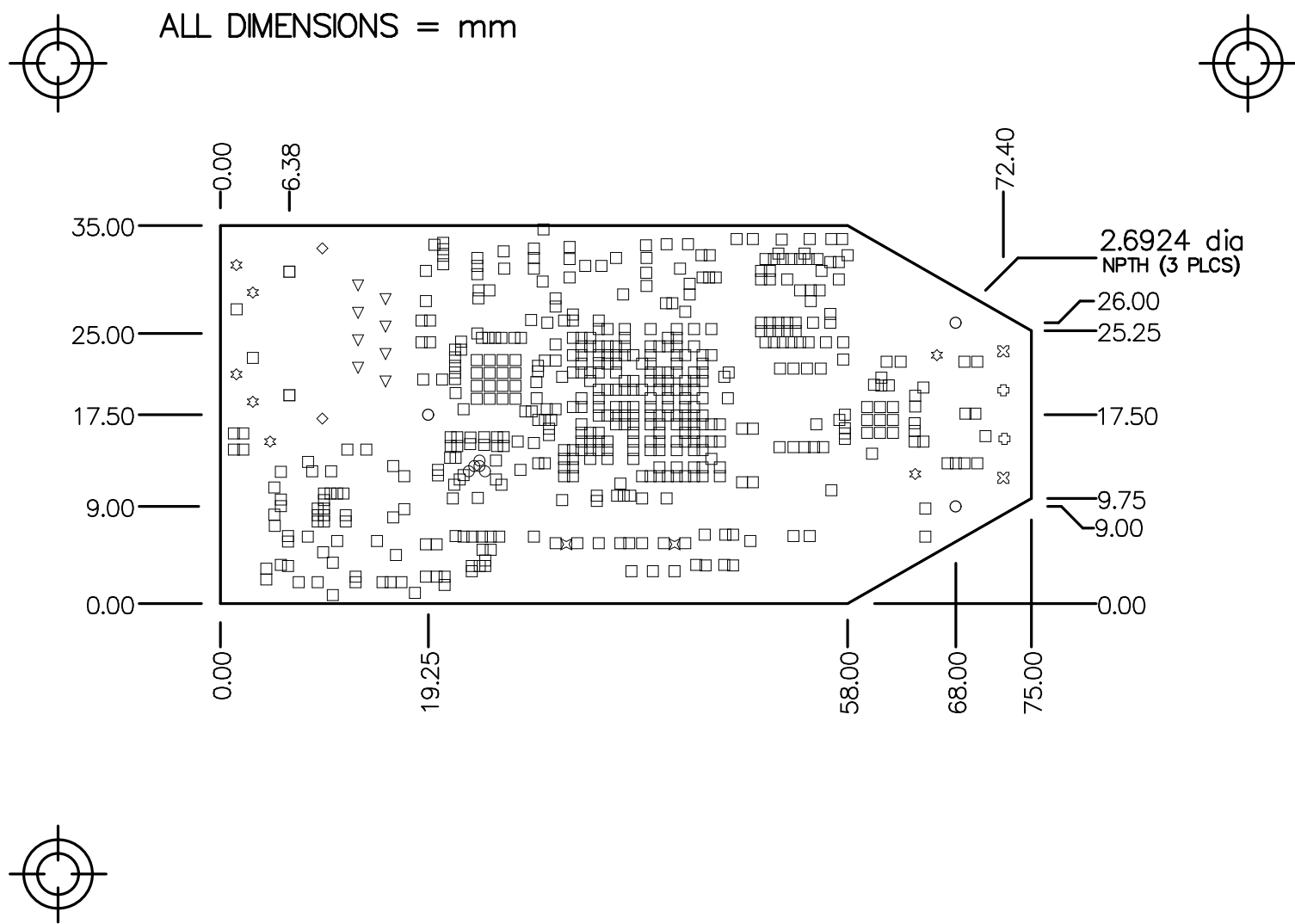
- BOARD SHALL BE FABRICATED – PERFORMANCE CLASS II AS PER IPC-6011 AND IPC-6012
- VENDOR IDENTIFICATION AND DATE CODE OF MANUFACTURING SHALL BE ETCHED ON THE SOLDER SIDE OF BOARD
- FABRICATE USING FILM "FAB/DRILL IDENT" FOR REFERENCE
- PERMANENTLY MARK BARE BOARD WITH TEST STAMP USING NON-CONDUCTIVE, RoHS COMPLIANT INK
- SILKSCREEN BOTH SIDES WITH NON-CONDUCTIVE, RoHS COMPLIANT INK, NOT ALLOWED ON COMPONENT PADS, COMPONENT MOUNTING HOLES, OR VIAS (COLOR = WHITE)
- MATERIAL: PER IPC-4101A/24/26/29/99, COPPER CLAD, HIGH TEMPERATURE FR4 CLASS EPOXY GLASS RATED UL94V-0, 0.5 OZ COPPER FOR EXTERNAL LAYERS AND 0.5 OZ COPPER FOR INTERNAL LAYERS. MUST BE RoHS COMPLIANT AND SURVIVE A LEAD-FREE ASSEMBLY MAX REFLOW OF 260 DEG C (6 PASSES)
 - Td RATING: > 340 DEG C
 - Z AXIS CTE < 3.5%
 - Tg > 170 DEG C (MIN)
- SOLDER MASK: SMOBC PER IPC-SM-840C, CLASS T, MUST BE RoHS COMPLIANT, TYPE LPI, 0.0002" MIN TO 0.0008" MAX MEASURED OVER COPPER PLATING, MUST CLEAR ALL LANDS AS INDICATED ON GERBER SOLDER MASK LAYERS, (COLOR = RED)
- FINISH: ELECTRO-LESS NICKEL IMMERSION GOLD (ENIG), 2-8 MICRO INCHES GOLD OVER 150-250 MICRO INCHES NICKEL
- SOLDERABILITY TEST: CATEGORY 2 OF J-STD-003
- ALL TEST POINTS SHALL BE FREE OF SOLDERMASK AND SILKSCREEN
- ALL HOLE SIZES ARE AFTER PLATING
- VENDOR MAY USE TEAR DROPS TO IMPROVE ANNULAR RINGS AS LONG AS DRC RULES ARE FOLLOWED
- FINISHED BOARDS SHALL NOT HAVE NICKS, SCRATCHES, VOIDS, EXPOSED COPPER, POOR PLATING OR MISDRILLED HOLES
- TIE-BARS ON THERMAL PADS SHOULD BE 15 MILS MINIMUM WIDTH
- MAKE ALL VIA CONNECTIONS TO POWER AND GROUND PLANES SOLID (E: THERMALS WITH 25 MIL O.D. OR 45 MIL O.D. SHOULD BE REMOVED FROM INNER PLANE LAYERS)
- VENDOR MAY ADD COPPER THEIVING AS NEEDED TO IMPROVE MANUFACTURABILITY, THEIVING TO BE 0.030" ROUND PADS AT 0.050" SPACING. THEIVING WILL HAVE A MINIMUM OF 0.100" CLEARANCE FROM EXISTING COPPER AND SHOULD NOT BE PLACED UNDER SURFACE MOUNT DEVICES
- ALL UNCONNECTED PADS ON INNER SIGNAL LAYERS MUST BE REMOVED
- ALL FINISHED BOARDS TO BE 100% ELECTRICALLY TESTED
- UNLESS OTHERWISE INDICATED, ALL LINEAR TOLERANCES SHALL BE XX +/- .010 AND XXX +/- .005

ADDITIONAL NOTES:

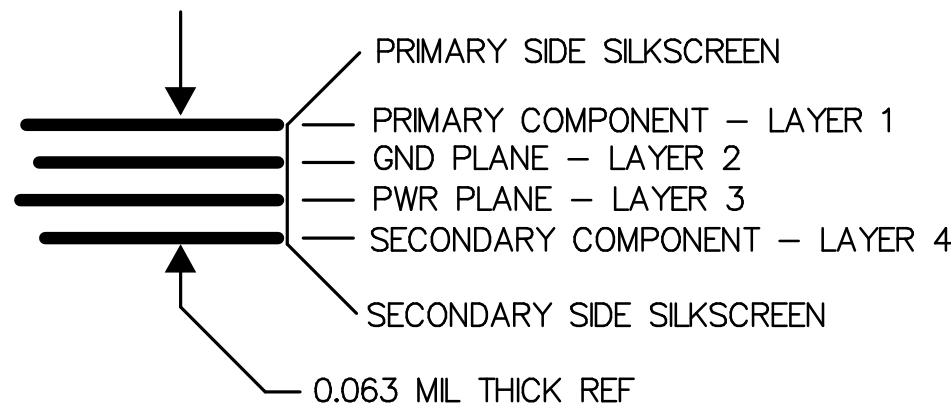
- FINISHED BOARD THICKNESS = 0.063" (+/- 0.007")
- CONTROL DIFFERENTIAL IMPEDANCE TO 100 OHMS +/- 10% ON ALL EXTERNAL SIGNALS OF WIDTH 4 MILS
- CONTROL SINGLE-ENDED IMPEDANCE TO 50 OHMS +/- 10% ON ALL INTERNAL AND EXTERNAL SIGNALS OF WIDTH 4 MILS
- ALL VIAS ON PRIMARY COMPONENT SIDE (LAYER 1) ARE TO BE TENTED WITH APPROPRIATE, RoHS COMPLIANT, SOLDER MASK (SECONDARY OPERATION)
- VIA-IN-PAD TO BE PLUGGED WITH SOLDER ON SECONDARY COMPONENT SIDE FINISHED DRILL SIZE = 6 MIL, 5 PLACES
- TO IMPROVE SILKSCREEN LEGIBILITY, USE #300 MESH
- NO PARTS CONTAINING LEAD, OR ANY OTHER NON-RoHS COMPLIANT MATERIAL MAY BE INSTALLED ON THE ASSEMBLY WITHOUT PRIOR WRITTEN APPROVAL FROM AVNET ENGINEERING
- ALL SOLDERING AND CLEANING PROCESSES FOR THIS ASSEMBLY MUST BE LEAD-FREE AND RoHS COMPLIANT
- ALL ASSEMBLY AND RE-WORK MUST USE LEAD-FREE SOLDER AND FOLLOW RoHS PROCEDURES
- THIS ASSEMBLY SHALL BE RoHS COMPLIANT. VENDOR SHALL DELIVER ASSEMBLY WITH ACCOMPANYING CERTIFICATE OF COMPLIANCE

Symbol	Hit Count	Tool Size	Physical Length	Rout Path Length	Plated	Hole Type
○	5	0.1524mm (6mil)			PTH	Round
□	520	0.2032mm (8mil)			PTH	Round
▽	8	0.889mm (35mil)			PTH	Round
⌘	2	1.016mm (40mil)			NPTH	Round
☆	7	1.016mm (40mil)			PTH	Round
◇	2	1.6mm (62.992mil)			NPTH	Round
◇	2	1.6002mm (63mil)			PTH	Round
◇	3	2.6924mm (106mil)			NPTH	Round
□	2	3.4mm (133.858mil)			NPTH	Round
⌘	2	0.7mm (27.559mil)	2.3mm (90.551mil)	1.6mm (62.992mil)	PTH	Slot
553 Total						

Slot definitions : Rout Path Length = Calculated from tool start centre position to tool end centre position.
Physical Length = Rout Path Length + Tool Size = Slot length as defined in the PCB layout



MINIMUM HOLE SIZE = 6 MIL
MINIMUM CONDUCTOR SPACING = 3 MIL
MINIMUM ANNULAR RING WIDTH = 2.7 MIL



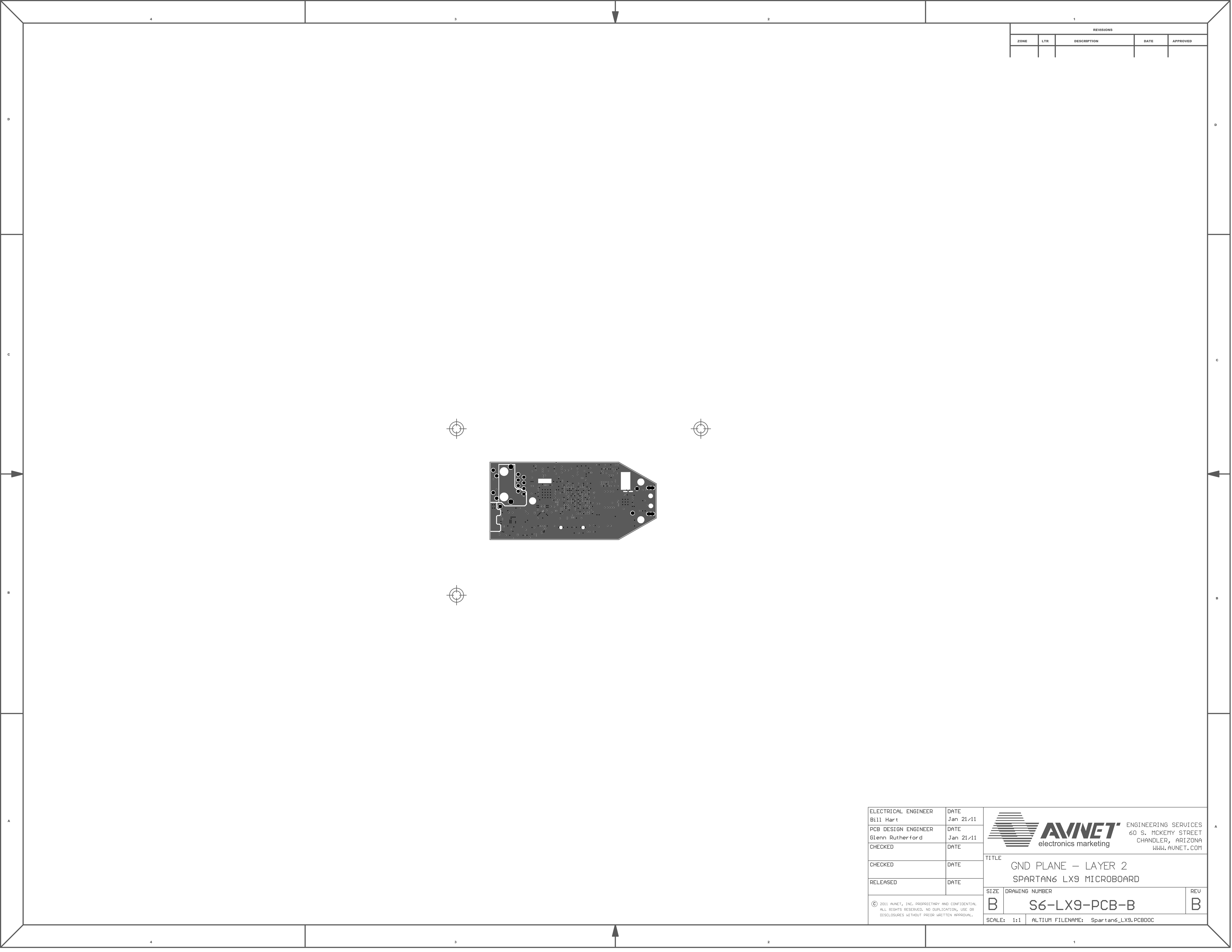
ELECTRICAL ENGINEER	DATE
Bill Hart	Jan 21/11
PCB DESIGN ENGINEER	DATE
Glenn Rutherford	Jan 21/11
CHECKED	DATE
CHECKED	DATE
RELEASED	DATE

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TITLE
FAB / DRILL ID
SPARTAN6 LX9 MICROBOARD

SIZE	DRAWING NUMBER	REV
B	S6-LX9-PCB-B	B
SCALE: 1:1	ALTIIUM FILENAME: Spartan6_LX9.PCBDOC	



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

ELECTRICAL ENGINEER	DATE
Bill Hart	Jan 21/11
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Glenn Rutherford	Jan 21/11
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CHECKED	DATE
RELEASED	DATE

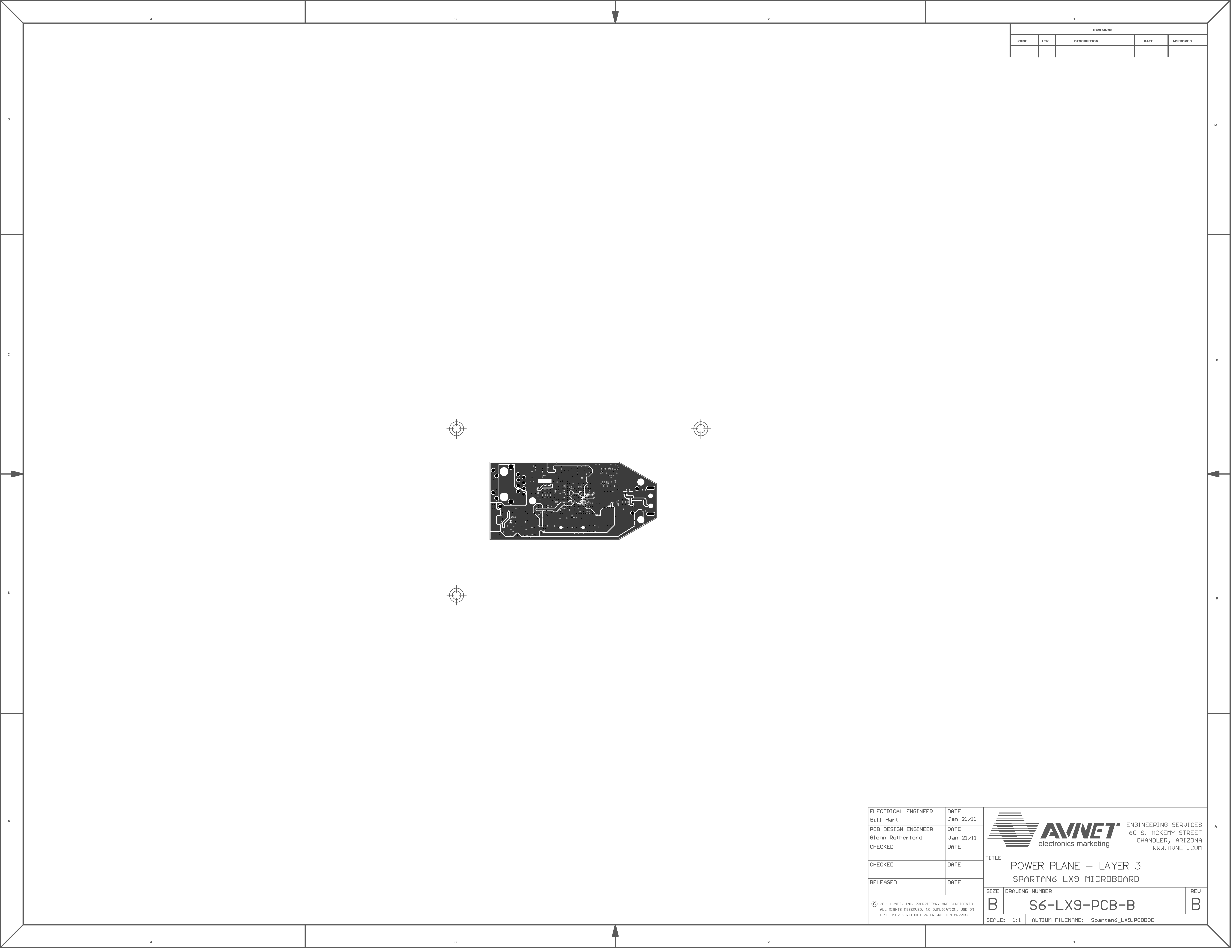


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TITLE
GND PLANE – LAYER 2
SPARTAN6 LX9 MICROBOARD

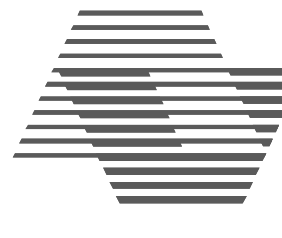
SIZE B	DRAWING NUMBER S6-LX9-PCB-B	REV B
SCALE: 1:1 ALTIUM FILENAME: Spartan6_LX9.PCBD0C		

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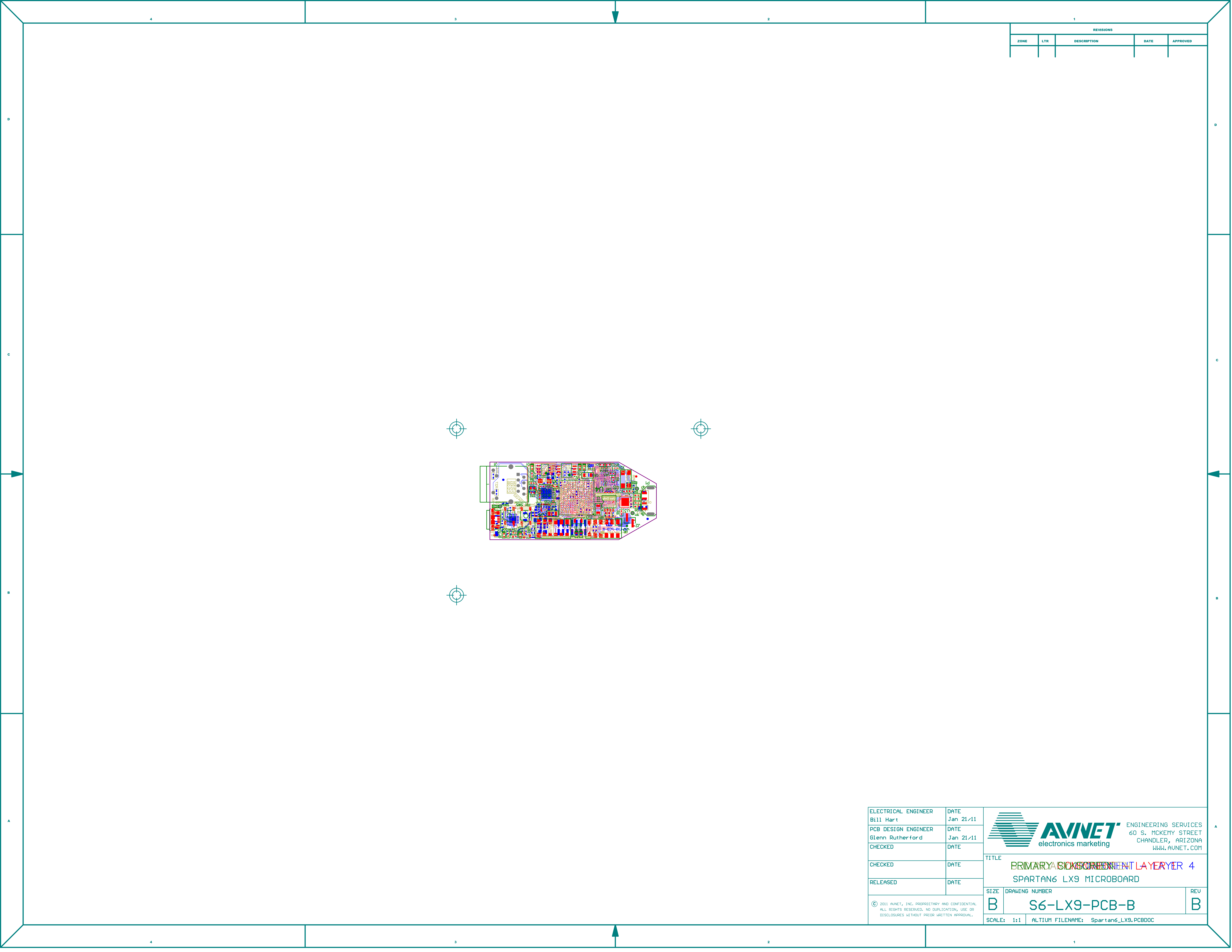
ELECTRICAL ENGINEER	DATE
Bill Hart	Jan 21/11
PCB DESIGN ENGINEER	DATE
Glenn Rutherford	Jan 21/11
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CHECKED	DATE
RELEASED	DATE

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TITLE		
POWER PLANE – LAYER 3 SPARTAN6 LX9 MICROBOARD		
SIZE	DRAWING NUMBER	REV
B	S6-LX9-PCB-B	B
SCALE: 1:1 ALTIUM FILENAME: Spartan6_LX9.PCBD0C		

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PCB DESIGN ENGINEER	DATE		
Glenn Rutherford	Jan 21/11		
CHECKED	DATE		
CHECKED	DATE	TITLE PRIMARY SCREEN LAYER 4 SPARTAN6 LX9 MICROBOARD	
RELEASED	DATE		
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		DRAWING NUMBER S6-LX9-PCB-B	ALTIIUM FILENAME: Spartan6_LX9.PCBD0C

