Getting Started Guide

Version 1.0

Xilinx® Zynq® 7Z045 Mini-Module Plus Development Kit

AVNET® electronics marketing

REVISION HISTORY

DATE	VERSION	REVISION
8/28/2013	1.0	Initial release for production board (AES-MMP-7Z045-G Revision B)

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1.0 INTRODUCTION

The purpose of this manual is to describe the functionality and contents of the Zynq 7Z045 Mini-Module Plus Development Kit from Avnet Electronics Marketing. This document includes instructions for operating the board, descriptions of the hardware features and explains out-of-the-box design code programmed in the on-board QSPI flash.

1.1 Description

The Zynq Z7045 Mini-Module Plus Development Kit provides a complete hardware environment for designers to accelerate their time to market. The kit delivers a stable platform to develop and test designs targeted to the advanced Xilinx Zynq AP PSoC family. The installed Zynq Z7045 device offers a prototyping environment to effectively demonstrate the enhanced benefits of leading edge Xilinx AP PSoC solutions. Reference designs are included with the kit to exercise standard peripherals on the evaluation board for a quick start to device familiarization.

The Zynq Z7045 Mini-Module Plus Development Board is a SOM (System on a Module) that requires mating it to a baseboard for access non-local peripherals and power. Currently the Zynq Z7045 Mini-Module Plus is compatible with one Avnet designed baseboard.

AVNET DESIGNED BASEBOARD	AVNET ORDERABLE PART NUMBER
Mini-Module Plus Baseboard 2	AES-MMP-BB2-G

1.2 Board Features

- Zynq AP PSoC
  - Xilinx XC7Z045-1FFG900
- I/O Connectors
  - Two (2) Mictor style connectors providing 132 user I/O signals and 8 Giga-bit transceivers to the baseboard.
- Multi-gigabit Serial transceivers (GTX)
  - Eight (8) GTX ports
- Memory
  - 1 GB DDR3 SDRAM components (2 banks of 256 MB x 16)
  - 128 MB Parallel Flash (x16)
  - 32 MB QSPI Flash
  - 8 KB I²C EEPROM
  - Micro SD Card
- Communication
  - USB-UART
  - USB 2.0
  - 10/100/1000 Ethernet
- Configuration
  - 32 MB QSPI Flash
  - Micro SD Card
  - JTAG via baseboard
- Other
  - Programmable LVDS clock source
  - Processor PJTAG port
  - XADC header.
  - Real-time clock (I²C)

1.3 Reference Designs

Reference designs that demonstrate some of the potential applications of the Zynq Z7045 Mini-Module Plus Development Kit can be downloaded from the Avnet Design Resource Center (www.em.avnet.com/MMP-7Z045-G). The reference designs include all of the source code and project files necessary to implement the designs. See the PDF document included with each reference design for a complete description of the design and detailed instructions for running a demonstration on the development board. Check the DRC periodically for updates and new designs.

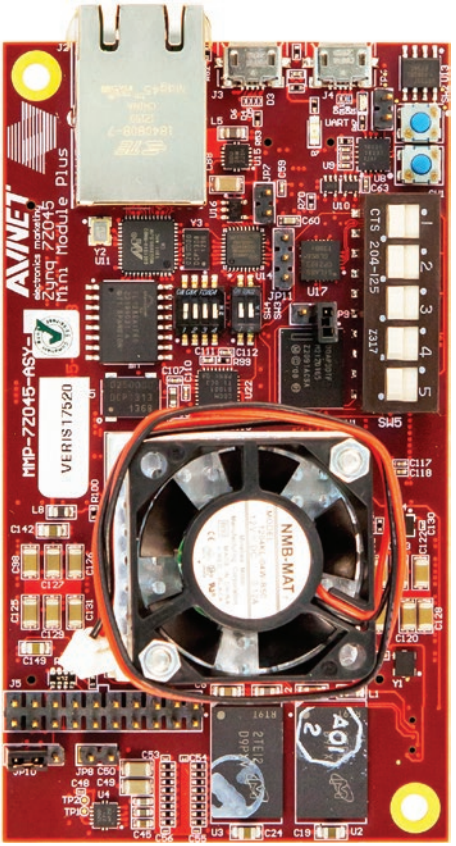

Figure 1 – Zynq 7Z045 Mini-Module Plus Development Board Picture

1.4 Ordering Information

The following table lists the development kit part number. Internet link at www.em.avnet.com/MMP-7Z045-G.

PART NUMBER	HARDWARE
AES-MMP-7Z045-G	Xilinx Zynq 7Z045 Mini-Module Plus Development Kit populated with an XC7Z045 FFG900 -1 speed grade device

Table 1 - Ordering Information

2.0 FUNCTIONAL DESCRIPTION

A high-level block diagram of the Zynq 7Z045 Mini-Module Plus development board is shown below followed by a brief description of each sub-section.

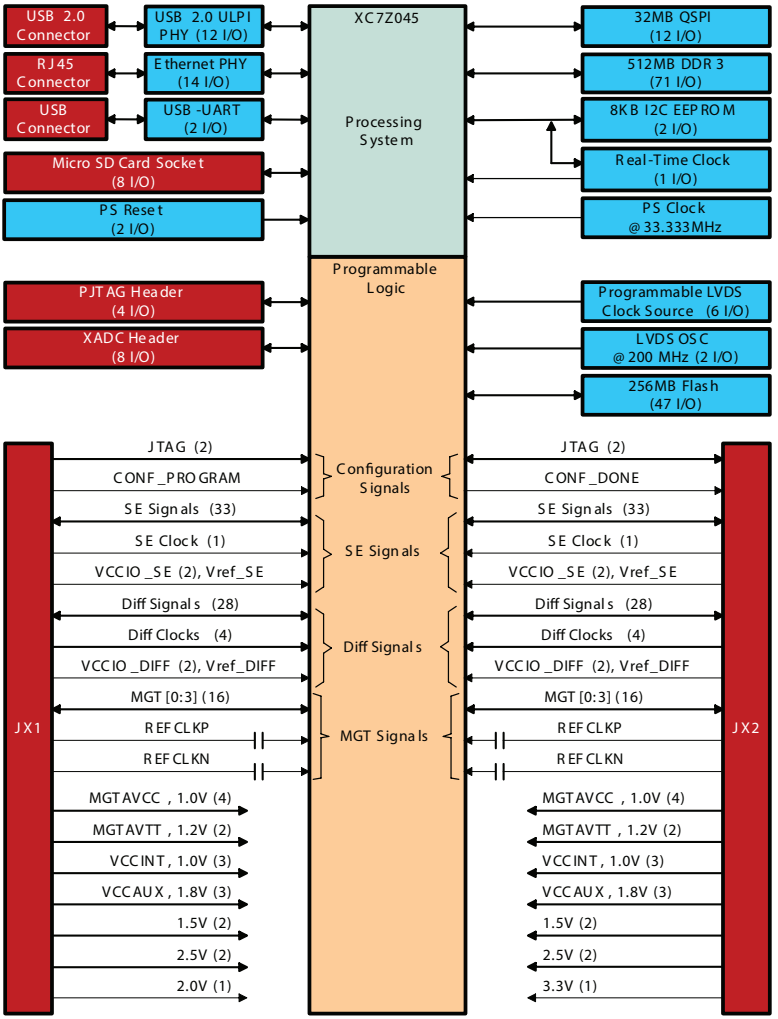

Figure 2 – Zynq 7Z045 Mini-Module Plus Development Board Block Diagram

2.1 Xilinx Zynq 7Z045 AP SoC

The Zynq 7Z045 AP SoC device available in the FFG900 package has an impressive list of features. The device is made up of two main systems one of which is the Processing System (PS) and the other Programmable Logic (PL). The table below lists some of the 7Z045 features.

PROCESSING SYSTEM	
Processor Core	Dual ARM Cortex-A9 MPCore
Processor Extensions	NEON and Single/Double Precision Floating Point for each processor
Max Frequency	667 MHz (-1)
L1 cache	32 KB Instruction, 32 KB Data per processor
L2 cache	512 KB
On-Chip Memory	256 KB
External Memory Controllers	DDR3, DDR3L, DDR2, LPDDR2
External Static Memory Controllers	2X Quad SPI, NAND, NOR
DMA Channels	8 (4 dedicated to PL)
Peripherals	2x UART, 2x CAN, 2x SPI, 2x I^2C, 4x 32b GPIO
Security	RSA, AES, SHA 256b
PROGRAMMABLE LOGIC	
Programmable Logic Cells	350 K
LUTs	218,600
Flip-Flops	437,200
Block RAM	2,180 KB
DSP Slices	900
PCI Express (Root Complex or Endpoint)	Gen2 x8
Analog Mixed Signal	2x 12-bit, MSPS ADCs with up to 17 differential inputs
Security	AES, SHA 256b

Table 2 – Zynq 7Z045 AP SoC Features

2.2 GTX Interface

The GTX transceiver is a full-duplex serial transceiver for point-to-point transmission applications. Up to 16 transceivers are available on a single 7Z045 FFG900 device. The transceiver block is designed to operate at up to 12.5 Gb/s per channel, including the specific bit rates used by the communications standards listed in the following table. Only the -3 speed grade part is capable of 12.5 Gb/s. The -1 speed grade part is capable of 8.0 Gb/s in the FF package.

The Zynq 7Z045 GTX transceivers are grouped into four transceivers per bank. Banks 109, 110, 111, and 112 are the GTX banks. Each GTX bank has two inputs for reference clocks. The Zynq Mini-Module Plus Development Board only uses Bank 109 and 112. GTX banks 110 and 11 are left unconnected.

When mated with a Mini-Module Plus Baseboard 2, bank 112 interfaces to a PCI Express x4 connector while Bank 109 interfaces to a FMC serial gigabit lane, and SFP module, a Display Port connector (TX Only), and one lane of SMA connectors.

GTX BANK	GTP INTERFACE	LANES	NUMBER 7Z045	
109	FMC	1	GTX0_109	GTX_X0Y3
109	SFP	1	GTX1_109	GTX_X0Y2
109	Display Port	1/2	GTX2_109	GTX_X0Y1
109	SMA	1	GTX3_109	GTX_X0Y0
112	PCI Express x4	0	GTX3_112	GTX_X0Y15
112		1	GTX2_112	GTX_X0Y14
112		2	GTX1_112	GTX_X0Y13
112		3	GTX0_112	GTX_X0Y12

Table 3 - GTX Interface Pin Assignments

2.2.1 GTX Reference Clock Inputs

Each GTX bank has reference clock inputs. One of these reference clock inputs are supplied by on-board clock sources while two others are supplied from the baseboard. A single programmable LVDS synthesizer is used to provide variable frequency clock sources to GTX bank 109. This synthesizer provides reference clock frequencies that support the full range of line rates. The following figure shows the clock sources provided to the dedicated GTX clock inputs from the baseboard and the on-board synthesizer.

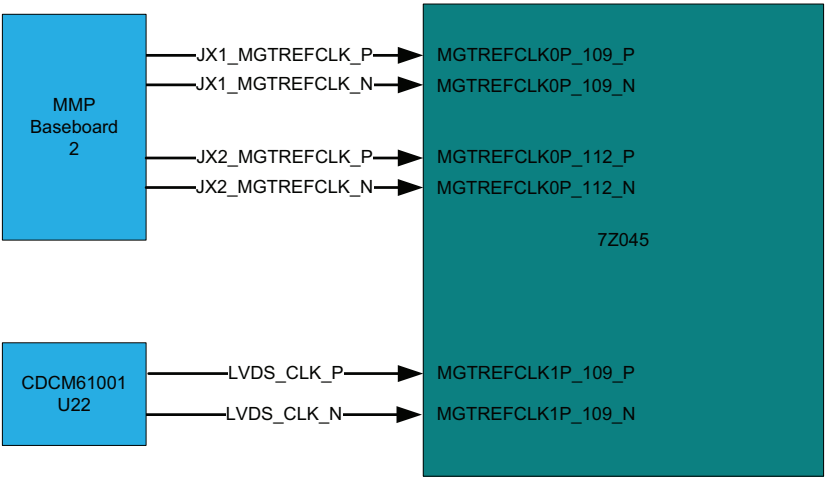

Figure 3 - GTX Clock Sources on the Zynq 7Z045 Mini-Module Plus Development Board

2.2.2 PCI Express x4 Interface

One of the GTX transceiver banks is connected to the PCI Express x4 card edge interface on the Mini-Module Plus Baseboard 2. PCI Express is an enhancement to the PCI architecture where the parallel bus has been replaced with a scalable, fully serial interface. The differences in the electrical interface are transparent to the software so existing PCI software implementations are compatible. Use of the Zynq 7Z045 Mini-Module Plus Development Board in a PCI Express application requires the implementation of the PCI Express protocol in the ZYNQ PL. The PCI Express Endpoint Block embedded in the Zynq 7Z045 implements the PCI Express protocol and the physical layer interface to the GTX ports. This block must be instantiated in the user design. Refer to UG963 documentation on the Xilinx website for more details.

The PCI Express electrical interface on the Zynq 7Z045 Mini-Module Plus Development Board consists of 4 lanes, having unidirectional transmit and receive differential pairs. It supports second generation PCI Express data rates of 5.0 Gbps. In addition to the data lanes there is a 100 MHz reference clock that is provided from the system slot. In

order to work in open systems, add-in cards must use the reference clock provided over the PCI Express card edge to be frequency locked with the host system. The 100 MHz clock is sourced from the baseboard edge connector and forwarded to a jitter attenuator prior to being forwarded to the Zynq Mini-Module Plus via the JX2 connector.

There is also a side band signal from the PCI Express card edge that connects to a standard I/O pin on the Zynq 7Z045. The "PERST#" signal is an active low reset signal provided by the host PCI Express slot. The following figure shows the PCI Express interface to the Zynq 7Z045.

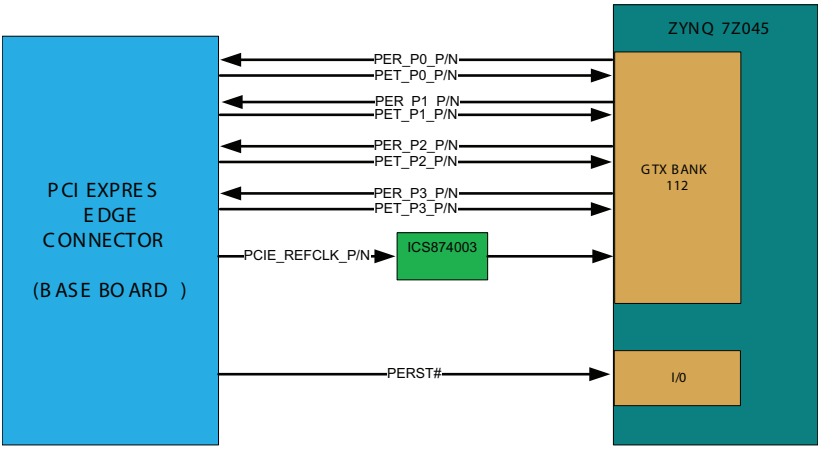

Figure 4 - PCI Express x4 Interface

The PCI Express transmit lanes are AC coupled (DC blocking capacitors are included in the signal path) on the baseboard as required by the PCI Express specification.

BANK 112 GTX INSTANCE	NET NAME	7Z045 PIN #
GTX_X0Y15 (PCIE LANE 0)	JX2_MGTTX2_P	N4
	JX2_MGTTX2_N	N3
	JX2_MGTRX2_P	P6
	JX2_MGTRX2_N	P5
GTX_X0Y14 (PCIE LANE 1)	JX2_MGTTX3_P	P2
	JX2_MGTTX3_N	P1
	JX2_MGTRX3_P	T6
	JX2_MGTRX3_N	T5
GTX_X0Y13 (PCIE LANE 2)	JX2_MGTTX0_P	R4
	JX2_MGTTX0_N	R3
	JX2_MGTRX0_P	U4
	JX2_MGTRX0_N	U3
GTX_X0Y12 (PCIE LANE 3)	JX2_MGTTX1_P	T2
	JX2_MGTTX1_N	T1
	JX2_MGTRX1_P	V6
	JX2_MGTRX1_N	V5
PERST#	JX1_SE_IO_32	AC14

Table 4 - GTX Pin Assignments for PCI Express

2.2.2.1 PCI Express Configuration Timing

The Zynq 7Z045 Mini-Module Plus Development Board meets the 200 ms configuration time requirement for ATX based PC systems when configuring from the QSPI interface.

2.2.3 GTX for FMC Expansion Connector, SFP, Display Port and SMA (Baseboard)

Four other high-speed gigabit interfaces from the Mini-Module Plus Baseboard 2 are connected to the 7Z045 via the JX1 connector. Each interface is one lane wide and all reside on bank 109 of the 7Z045.

One GTX transceiver port is connected to the baseboard's FMC LPC connector. The FMC LPC connector has one gigabit lane dedicated to it for use with FMC daughter cards.
One GTX transceiver port is connected to the baseboard's SFP interface.
One GTX transceiver port is connected to the baseboard's SMA interface.
One GTX transceiver port is connected to the baseboard's Display Port interface (TX only).

BANK 109 GTX INSTANCE	NET NAME	7Z045 PIN #
GTX_X0Y0 (SMA)	JX1_MGTTX3_P	AK2
	JX1_MGTTX3_N	AK1
	JX1_MGTRX3_P	AE8
	JX1_MGTRX3_N	AE7
GTX_X0Y1 (Display Port)	JX1_MGTTX2_P	AJ4
	JX1_MGTTX2_N	AJ3
	JX1_MGTRX2_P	AG8
	JX1_MGTRX2_N	AG7
GTX_X0Y2 (SFP)	JX1_MGTTX1_P	AK6
	JX1_MGTTX1_N	AK5
	JX1_MGTRX1_P	AJ8
	JX1_MGTRX1_N	AJ7
GTX_X0Y3 (FMC)	JX1_MGTTX0_P	AK10
	JX1_MGTTX0_N	AK9
	JX1_MGTRX0_P	AH10
	JX1_MGTRX0_N	AH9

Table 5 - GTX Pin Assignments for Baseboard FMC, SFP, DP and SMA Connectors

2.3 Memory

The Zynq 7Z045 Mini-Module Plus Development Board is populated with both high-speed RAM and non-volatile ROM to support various types of applications. Each development board has five memory interfaces:

1. DDR3: 1GB x32 DDR3 SDRAM
2. 32 MB QSPI Flash
3. 256 MB Parallel Flash x16
4. 8 KB I²C EEPROM
5. SD Micro Card

2.3.1 DDR3 SDRAM Interface

Two **Micron** DDR3 SDRAM devices, part number **MT41K256M16HA-125E:E**, make up the 1 GB x32 SDRAM memory interface. Each device provides 512 MB of memory on a single IC and is organized as 32 Megabits x 16 x 8 banks. The device has an operating voltage of 1.5 V and the interface is JEDEC Standard SSTL_15 (Class I for unidirectional signals, Class II for bidirectional signals). The -125E speed grade supports 1.25 ns cycle times with 11 clock read latency (DDR3-1600). The following figures show a high-level block diagram of the DDR3 SDRAM interface on the development board.

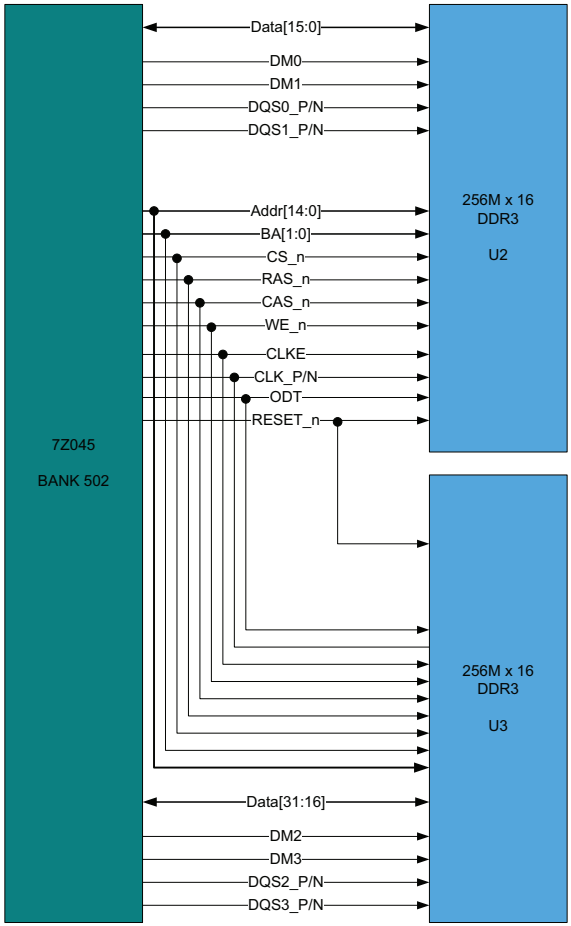

Figure 5 - DDR3 SDRAM Interface

The DDR3 signals are connected to bank 502 of the 7Z045. The 7Z045 VCCO pins for the bank 502 are connected to 1.5 V. This supply rail can be measured at the test point labeled 1.5_1.35 V On the Mini-Module Plus Baseboard 2. The reference voltage pins (VREF) for the DDR3 bank are connected to the reference output of the Texas Instruments TPS51200. This device provides the termination voltage and reference voltage necessary for the DDR3 and 7Z045 devices. The termination and reference voltage is 0.75 V.

The following guidelines were used in the design of the DDR3 interface to the 7Z045. These guidelines are based on Micron recommendations and board level simulation.

- DDR3 devices routed with daisy-chain topology for shared signals of the two devices (clock, address, control).
- 40 ohm* controlled trace impedance for single ended signals. 80 ohm* differential impedance for differential signals.
- Dedicated data bus with matched trace lengths (+/- 50 mils).
- Memory clocks and data strobes routed differentially.
- Series termination following the memory device connection on shared signals (control, address).
- Termination supply that can both source and sink current.

* Ideal impedance values. Actual may vary.

All DDR3 signals are compliant to the Xilinx recommended and MIG generated pin out. The following table contains the ZYNQ PL pin assignments used for the DDR3 SDRAM interface.

NET NAME	7Z045 PIN
DDR3_A0	L25
DDR3_A1	K26
DDR3_A2	L27
DDR3_A3	G25
DDR3_A4	J26
DDR3_A5	G24
DDR3_A6	H26
DDR3_A7	K22
DDR3_A8	F27
DDR3_A9	J23
DDR3_A10	G26
DDR3_A11	H24
DDR3_A12	K23
DDR3_A13	H23
DDR3_A14	J24
DDR3_BA0	M27
DDR3_BA1	M26
DDR3_BA2	M25
DDR3_WE#	N23
DDR3_RAS#	N24
DDR3_CAS#	M24
DDR3_RST#	F25
DDR3_ODT	L23
DDR3_CKE	M22
DDR3_CK0_P	K25
DDR3_CK0_N	J25
DDR3_DQS0_P	C26
DDR3_DQS0_N	B26
DDR3_DQS1_P	C29
DDR3_DQS1_N	B29
DDR3_DQS2_P	G29
DDR3_DQS2_N	F29
DDR3_DQS3_P	L28
DDR3_DQS3_N	L29

NET NAME	7Z045 PIN
DDR3_D0	A25
DDR3_D1	E25
DDR3_D2	B27
DDR3_D3	D25
DDR3_D4	B25
DDR3_D5	E26
DDR3_D6	D26
DDR3_D7	E27
DDR3_D8	A29
DDR3_D9	A27
DDR3_D10	A30
DDR3_D11	A28
DDR3_D12	C28
DDR3_D13	D30
DDR3_D14	D28
DDR3_D15	D29
DDR3_D16	H27
DDR3_D17	G27
DDR3_D18	H28
DDR3_D19	E28
DDR3_D20	E30
DDR3_D21	F28
DDR3_D22	G30
DDR3_D23	F30
DDR3_D24	J29
DDR3_D25	K27
DDR3_D26	J30
DDR3_D27	J28
DDR3_D28	K30
DDR3_D29	M29
DDR3_D30	L30
DDR3_D31	M30
DDR3_DM0	C27
DDR3_DM1	B30
DDR3_DM2	H29
DDR3_DM3	K28
DDR3_CS#	N22

Table 6 – 7Z045 Pin Assignments for DDR3

2.3.2 Parallel Flash Interface

The parallel flash memory consists of a single 128 MB Micron device in a 64-ball BGA package, part number **PC28F00AP30TFA**. The PC28F device is an asynchronous memory that also supports a synchronous-burst read mode for high-performance applications. The PC28F device has a 100 nanosecond access time. The PC28F flash connects to Bank 34 of the 7Z045. The Flash I/O voltage is 1.8 V. The following figure shows the PC28F flash interface on the development board.

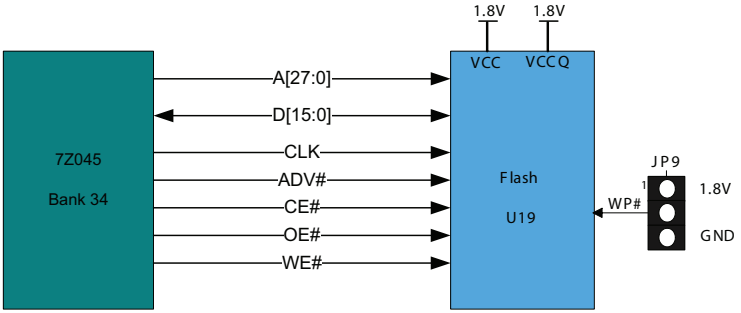

Figure 6 – Parallel Flash Interface

The following table contains the ZYNQ PL pin number assignments for the Flash interface.

NET NAME	7Z045 PIN #
PFLASH_A1	A9
PFLASH_A2	D10
PFLASH_A3	D6
PFLASH_A4	F7
PFLASH_A5	F8
PFLASH_A6	A10
PFLASH_A7	G11
PFLASH_A8	B9
PFLASH_A9	D11
PFLASH_A10	F10
PFLASH_A11	F9
PFLASH_A12	E11
PFLASH_A13	A8
PFLASH_A14	C7
PFLASH_A15	D8
PFLASH_A16	E8
PFLASH_A17	E10
PFLASH_A18	A7
PFLASH_A19	C9
PFLASH_A20	C6
PFLASH_A21	D9
PFLASH_A22	B7
PFLASH_A23	M10
PFLASH_A24	K8
PFLASH_A25	B6
PFLASH_A26	C8
PFLASH_A27	M12

NET NAME	7Z045 PIN #
PFLASH_D0	L12
PFLASH_D1	H12
PFLASH_D2	L10
PFLASH_D3	K12
PFLASH_D4	J11
PFLASH_D5	K10
PFLASH_D6	J10
PFLASH_D7	K7
PFLASH_D8	G10
PFLASH_D9	H11
PFLASH_D10	L9
PFLASH_D11	L8
PFLASH_D12	H7
PFLASH_D13	L7
PFLASH_D14	J8
PFLASH_D15	G9
PFLASH_CE#	B10
PFLASH_WE#	J9
PFLASH_OE#	H8
PFLASH_RST#	E7
PFLASH_ADV#	G7
PFLASH_WAIT	H9
PFLASH_CLK	K11

Table 7 – Parallel Flash Pin Assignments

2.3.3 QSPI Flash Interface

The Zynq 7Z045 Mini-Module Plus Development Board utilizes two on-board Spansion multi-bit (x4) SPI flash devices, part number **S25FL128SAGMFIR0**, to configure the Zynq PL quickly using the QSPI configuration mode. The QSPI devices are connected to bank 500 of the 7Z045. For PCI Express applications the QSPI interface must be used to configure the 7Z045 to insure meeting the 200 ms PCI Express configuration time requirement.

The figure below shows the interface between the SPI flash and the 7Z045 AP PSoC.

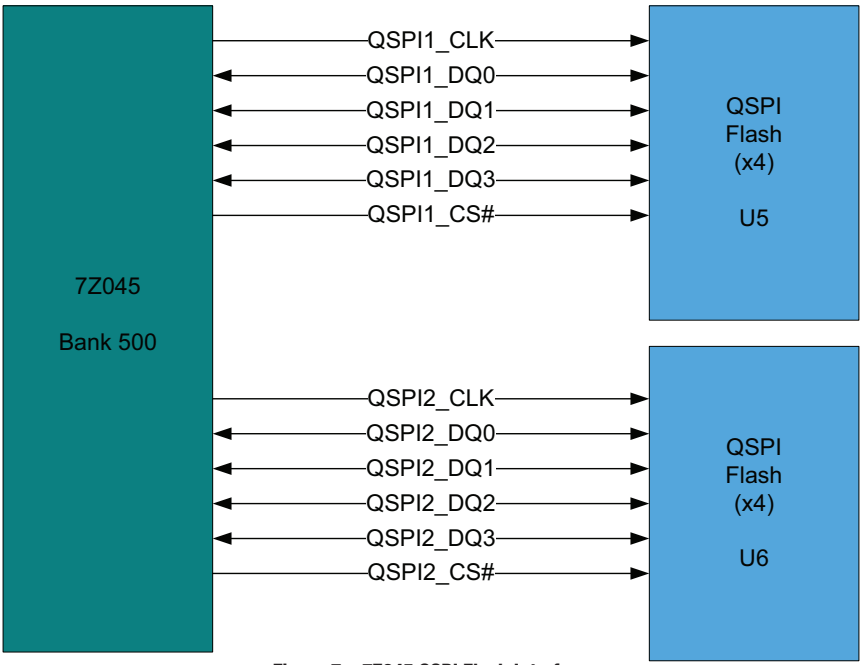

Figure 7 – 7Z045 QSPI Flash Interface

To configure the 7Z045 using the QSPI flash interface the configuration mode for the 7Z045 must be set to QSPI mode. This is accomplished by setting the configuration mode switches to the proper setting. The configuration mode switch is SW5 on the Mini-Module. It is a five position slide switch. **Setting SW5 to SW[5:0] = x001x** will put the 7Z045 in QSPI configuration mode at power-on. See Section 2.8.1 for more details on the various 7Z045 configuration modes.

2.3.4 I²C EEPROM Interface

The Zynq 7Z045 Mini-Module Plus Development Board has an on-board 8 KB I²C EEPROM for additional data storage. A Micron M24C08-R is the device used. The I²C EEPROM is on the shared I²C bus with the I²C real time clock (RTC). The table below shows the pin connections to the 7Z045.

NET NAME	7Z045 PIN #
I²C_SDA	F19
I²C_SCL	A19

Table 8 – I²C EEPROM Pin Assignments

2.3.5 Micro SD Card Interface

The Zynq 7Z045 Mini-Module Plus Development Board implements a micro SD card interface that can be used for boot configuration as well as additional data storage. The module ships with a 4 GB micro SD card installed into the card slot at J1 on the bottom side of the board.

When boot code is stored on the micro SD card, configuration of the PS can be done by setting the configuration mode switch SW5 to the proper setting. The proper setting for configuring from the micro SD card is **SW[5:0]=x011x**. See Section 2.8.1 for more details on the various 7Z045 configuration modes.

2.4 Clock Sources

The Zynq 7Z045 Mini-Module Plus Development Board used in conjunction with the Mini-Module Plus Baseboard 2 includes all of the necessary clocks to implement high-speed logic and GTX transceiver designs. Most of these master clocks are sourced from the baseboard's FMC connector and the on-board LVDS clock synthesizer. All of these clocks are tied to the Z7045 MRCC pins giving access to the 7Z045's global clock tree. The clock sources described in this section are used to derive the required clocks for the memory and communications devices, and the general system clocks for the logic design. For a description of the GTX reference clock sources, see Section 2.2.1.

The following figure shows the clock nets connected to the I/O banks of the 7Z045

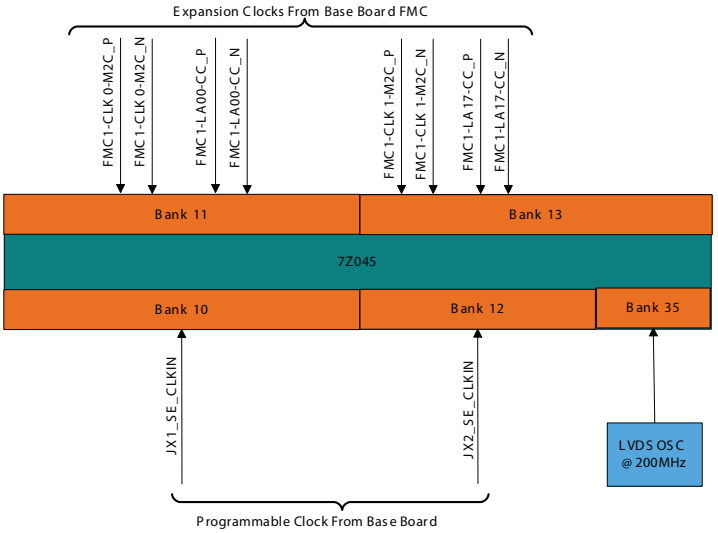

Figure 8 - Clock Nets Connected to Global Clock Inputs

The on-board 200 MHz LVDS oscillator provides the system clock input to the global clock tree. This 200 MHz clock can be used in conjunction with the 7Z045's internal clock generators to generate the various logic clocks and the clocks forwarded to the DDR3 SDRAM devices.

Additionally, there is an on-board 33 MHz LVTTL clock source connected to bank 500 and serves as the PS system clock.

2.4.1 CDCM61001 Programmable LVDS Clock Synthesizer

The Zynq 7Z045 Mini-Module Plus Development Board design uses the TI CDCM61001 LVDS frequency synthesizer for generating various clock frequencies as an input reference clock for GTX bank 109. A list of features included in the CDCM61001 device is shown below.

- Output frequency range: 43.75 MHz to 683.264 MHz
- RMS period jitter: 0.509 ps @ 625 MHz
- Output rise and fall time: 255 ps (maximum)
- Output duty cycle: varies dependent on output frequency

The following figure shows a high-level block diagram of the CDCM61001 programmable clock synthesizer. Inputs OS0 and OS1 are hard wired to use the LVDS mode of the CDCM61001 device.

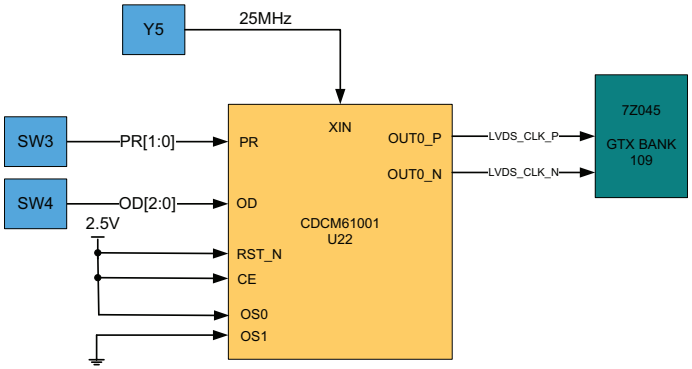

Figure 9 - CDCM61001 Clock Synthesizer

SIGNAL NAME	DIRECTION	PULL UP/PULL DOWN	DESCRIPTION
PR[1:0]	Input	Pull up	Prescaler and Feedback divider control pins.
OD[2:0]	Input	Pull up	Output divider control pins.
OS[1:0]	Input	Pull up	Output type select control pins.
CE	Input	Pull up	Chip enable.
RST_N	Input	Pull up	Device reset (active low).
XIN	Input	Pull up	Parallel resonant crystal/LVCMOS input.
OUT0 P/N	Input		Differential output pair.

Table 9 - CDCM61001 Clock Synthesizer Pin Description

2.4.1.1 CDCM61001 Clock Generation

The CDCM61001 output clocks are generated based on the following formula (assuming the crystal clock input is 25 MHz):

FOUT = (FIN) (FD) / OD

Equation Variables:
FOUT = Output Frequency
FIN = Clock Input Frequency
FD = Feedback Divider Value
OD = Output Divider Value

Please refer to the CDCM61001 datasheet for detailed tables regarding the Feedback Divider and Output Divider values. The CDCM61001 FD and OD values are programmed via dipswitches **SW3** and **SW4**. These dipswitches should be configured prior to powering up the board.

The following table shows how to set the dipswitches for a common application. All the values are based on a 25 MHz crystal clock input to the CDCM61001 device.

INTERCONNECT TECHNOLOGY	OUT0 AND OUT1 (MHZ)	PR1	PR0	OD2	OD1	OD0
SATA	150	0	0	0	1	1
GigE	125	1	1	0	1	1
10 GigE	156.25	1	0	0	1	1
12 GigE	187.5	0	1	0	0	1

Table 10 - CDCM61001 Common Application Settings

2.4.1.2 CDCM61001 Programming Mode

The Zynq 7Z045 Mini-Module Plus Development Board allows programming of the PR and OD values in parallel mode. This is the only mode supported by the device. In parallel mode, PR and OD values are programmed into the device upon the release of the master reset signal (rising edge of the MR_N signal). The switches should be set into the correct position prior to turning on power to the board. Should the switch settings change after power up the board will have to be power cycled to reset the device.

2.5 Communication

The Zynq 7Z045 Mini-Module Plus Development Board utilizes Ethernet, USB 2.0 (Host mode or Endpoint) and USB UART physical layer transceivers for communication purposes. Network access is provided by a single 10/100/1000 Mb/s Ethernet PHY device, which is connected to 7Z045 via a standard RGMII interface. The PHY device connects to the outside world with a standard RJ45 connector.

Serial port communication to the embedded ARM processor or ZYNQ PL fabric is provided through a Cypress USB-RS232 transceiver.

2.5.1 10/100/1000 Ethernet PHY

The PHY device is a **Marvel 88E1518**. The PHY is connected to a Tyco Electronics RJ-45 jack with integrated magnetics (part number: **1840808-7**. The jack also integrates two LEDs that indicate a valid link and traffic over the interface. The PHY clock is generated from a 25 MHz crystal. The following figure shows a high-level block diagram of the interface to the Ethernet PHY.

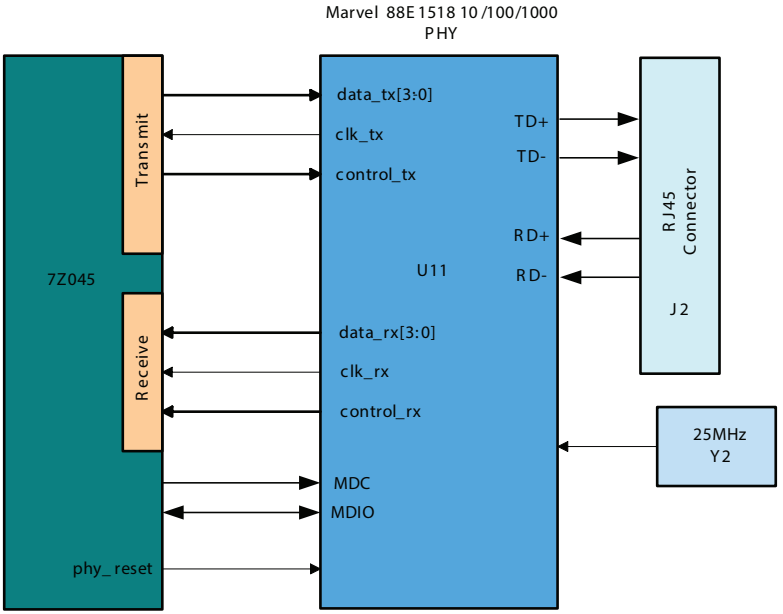

Figure 10 - 10/100/1000 Ethernet Interface

The PHY has two methods that can be used to reset the device. The PHY reset signal is ORed (active low) with the on-board power-on reset circuit and one of the I/O pins in bank 500. If having the 7Z045 reset the device is desired toggle pin B24 LOW. To manually reset the PHY SW1 can be pressed. See section 2.7 for details about the power-on reset circuit.

The following tables provide the 7Z045 pin assignments for the Ethernet PHY interface.

NET NAME	7Z045 PIN #
ETH_MDC	D19
ETH _MDIO	C18
ETH _TX_CTRL	
ETH_TX_CLK	L19
ETH _TX_D0	K21
ETH _TX_D1	K20
ETH _TX_D2	J20
ETH _TX_D3	M20

NET NAME	7Z045 PIN #
ETH _RST#	B24 or SW1
ETH _RX_CTRL	G20
ETH_RX_CLK	L20
ETH _RX_D0	J21
ETH _RX_D1	M19
ETH _RX_D2	G19
ETH _RX_D3	M17

Table 11 - Ethernet PHY Pin Assignments

2.5.2 USB UART

The Zynq 7Z045 Mini-Module Plus Development Board implements a Silicon Labs CP2103 device that provides a USB-to-RS232 bridge. The USB physical interface is brought out on a USB Micro-AB connector labeled "J4".

The USB UART interface connects to the 7Z045 at the following pins:

NET NAME	7Z045 PIN #
USB_UART_RXD	C19
USB_UART_TXD	D18

Table 12 – USB UART Pin Assignments

2.5.3 USB 2.0 On-the-Go (OTG)

The Zynq 7Z045 Mini-Module Plus Development Board implements a **SMSC USB3320** USB 2.0 PHY that has the ability to operate in host mode (OTG) or as an endpoint device. The USB3320 device is interfaced to the outside world via the USB Micro-A-B connector "J3" on the board. In addition to the built-in ESD protection the USB3320 offers there are added ESD protection diodes on-board to protect against electrostatic discharge when plugging in a USB cable.

Two jumpers allow the switching of device modes from OTG (Host) mode or endpoint mode. The USB 2.0 circuit ships in endpoint mode by default. To switch the device into OTG mode JP11 must be moved to the 2-3 position and JP7 must be placed.

The USB3320 device also offers over current detection/protection when in OTG mode. "U16" provide the 7Z045 with an OC signal that asserts LOW when an over-current condition exists.

The USB3320 device is powered from 1.8 V and is clocked at 26 MHz via "Y3".

Resetting the USB 2.0 PHY can be done two ways. The USB_RESET# signal is wire ORed (active low) by an I/O pin on the 7Z045 and the power-on reset circuit. To reset the USB PHY via the 7Z045 I/O pin toggle pin A18 LOW. To reset the USB PHY via the power-on reset circuit press SW2. See section 2.7 for details about the power-on reset circuit.

The table below shows the pin assignments of the USB 2.0 PHY to the 7Z045

NET NAME	7Z045 PIN #
USB_D0	K17
USB_D1	G22
USB_D2	K18
USB_D3	G21
USB_D4	L17
USB_D5	B21

NET NAME	7Z045 PIN #
USB_D6	A20
USB_D7	F18
USB_STP	L18
USB_NXT	H21
USB_DIR	H22
USB_CLK	H17
USB_RESET#	A18 or SW2

Table 13 – USB 2.0 Pin Assignments

When operating in host mode, the Zynq Mini-Module must supply 5 V to the endpoint devices. The Zynq Mini-Module Plus does not have a 5 V power source that is supplied from the baseboard. To accommodate this requirement the Zynq Mini-Module implements a highly efficient TI TPS61027 synchronous boost converter. The TPS61027 has the ability to source up to 1.5A at 3.3 V for the VBUS voltage rail at the USB connector J3.

2.6 Real-Time Clock (RTC)

The Zynq 7Z045 Mini-Module Plus Development Board has a real-time clock circuit that can be accessed via the I²C interface. The **Maxim DS1337** device is used for this purpose. The DS1337 can count seconds, minutes, hours, days, date, month and year with leap year compensation up to the year 2100.

The table below show the I²C signals and their connection to the 7Z045.

NET NAME	7Z045 PIN #
I²C_SDA	F19
I²C_SCL	A19

Table 14 – RTC Pin Assignments

2.7 Power-on Reset

The Zynq 7Z045 Mini-Module Plus Development Board utilizes a power-on reset IC and circuit to insure the 7Z045 PS_POR# and PS_SRST# signals de-assert in the correct sequence at power-up. To accomplish this, the **Maxim MAX16025TE** device is used and is referenced on the board as "U8". As shipped, the delay sequence is programmed to release the PS_SRST# signal before the PS_POR# signal. The delay for PS_POR# Is adjustable and set by C66, which as shipped is a 3300pf capacitor.

Please also note that the PS_POR# signal also gates the reset signal of the Ethernet and USB 2.0 PHY devices.

The power-on reset circuit also allows for the reset outputs of the MAX16025TE device to be controlled manually by way of two push button switches. SW1 when depressed will assert the PS_POR# signal which will completely reset the processor and all of the 7Z045 PS registers. Depressing SW2 will assert the PS_SRST# signal which will send a soft reset to the 7Z045 PS block. This reset signal will reset the processor but retain register data.

Both reset outputs can be asserted low together by placing a jumper on JP6 which is a master reset for the MAX16025TE device.

2.8 Configuration

The Zynq 7Z045 Mini-Module Plus Development Board supports several methods of configuring the 7Z045 PSoC. The possible configuration sources include Boundary-scan (JTAG cable), QSPI and Micro SD card. The blue LED D1 labeled "DONE" on the baseboard illuminates to indicate when the 7Z045 has been successfully configured.

2.8.1 Configuration Modes and Boot Settings

Upon power-up the 7Z045 will be enabled in a configuration mode defined by the position of the switches on the five position slide switch "SW5". JTAG device configuration can occur at any time regardless of the configuration switch setting after power-on.

SW5 also controls the JTAG mode and whether the PS PLL is enabled or disabled.

SW5 position 0 controls the JTAG mode. The JTAG mode options are "cascaded" and "independent". In cascaded mode, the PS and the PL systems of the 7Z045 are included in the JTAG chain while in independent mode only the PL system is included. While in independent mode the ARM DAP is accessible but the user must use a separate JTAG cable via the 20-pin PJTAG connector J5.

SW5 position 4 controls the PLL.

The following table shows the two configuration modes and settings and the proper SW5 position settings:

CONFIG MODE/SETTING	SW5[0]	SW5[1]	SW5[2]	SW5[3]	SW5[4]
JTAG Cascaded	0	x	x	x	x
JTAG Independent	1	x	x	x	x
JTAG Config Mode	x	0	0	0	x
QSPI Config Mode	x	0	0	1	x
SD Card Config Mode	x	0	1	1	x
Disable PLL	x	x	x	x	0
Enable PLL	x	x	x	x	1

Table 15 - Setting the Configuration Mode "SW5"

2.8.2 JTAG Interface (PL TAP and ARM DAP)

The Zynq 7Z045 Mini-Module Plus Development Board's JTAG interface originates at the baseboard and is routed to the 7Z045 via the JX1 and JX2 connectors. A Xilinx parallel or USB cable is required to configure the 7Z045 in JTAG mode. The JTAG connector is located on the Mini-Module Plus Baseboard 2 and is referenced on the baseboard as J1. The 7Z045 PROGRAM_B signal is also sourced from the baseboard via push button SW4. The following figure shows a block diagram of the JTAG interface.

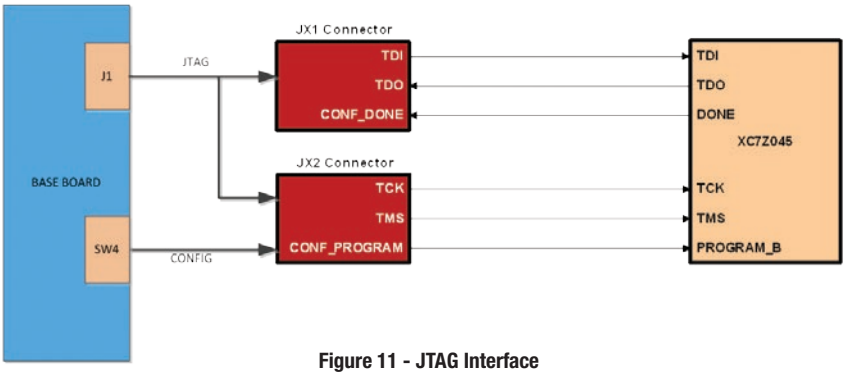

Figure 11 - JTAG Interface

Programming the 7Z045 via Boundary-scan mode requires a JTAG download cable. For more information about JTAG download cables, perform a search on the Xilinx web page www.xilinx.com using the key words "Programming Cables".

JP10 can be used to allow the JTAG programmer's reset pin to assert the 7Z045 PS_SRST# signal.

If using the Xilinx PC4 JTAG module (14-pin connector) the reset output on the cable is pin 14.

If using the JTAG-SMT2 module pin 7 is the reset output.

Since the Mini-Module Plus Baseboard 2 does not give access to these signals via the JX1 and JX2 connectors the reset signal from either or both sources can be connected to the ZMMP with wire jumpers.

NOTE: JP10 must be placed in either position to allow the 7Z045 PS Block to come out of reset. If no jumper is placed the 7Z045 will be non-functional. By default this jumper is populated in position 2-3.

2.8.3 PJTAG Interface (ARM DAP)

The Zynq 7Z045 Mini-Module Plus Development Board has a dedicated JTAG connector that can be used to debug/trace the PS ARM processor via third party debugger/trace modules. This 20-pin connector is referenced on the board as J5. This JTAG connector cannot be used for 7Z045 configuration. The PJTAG signals are connected to pins on the 7Z045 at bank 9. The table below shows the connections between J5 and the 7Z045.

J5 PIN	SIGNAL NAME	7Z045 PIN
5	PJTAG_TDI	Y20
7	PJTAG_TMS	AA20
9	PJTAG_TCK	AB19
13	PJTAG_TDO	AB20

Table 16 – PJTAG Pin Assignments

JP8 gives the user an option to provide a reference voltage to the third party debugger module if required.

2.9 Expansion Connectors

The Zynq 7Z045 Mini-Module Plus Development Board connects to the Mini-Module Plus Baseboard 2 via two 120 pin connectors referenced on the board as JX1 and JX2. These two connectors provide all of the power required to operate the module as well as provide I/O to the baseboard's peripheral interfaces. The baseboard peripheral interfaces the module has access to are the high speed gigabit transceiver channels such as PCI Express x4, SFP, SMA, and Display port. Additionally the baseboard's FMC low pin count (LPC) Mezzanine Card expansion connector, dual PMOD, USB-UART, SD card, clock generators, user LEDs, user dip switches and configuration JTAG are mapped to these connectors and connected to the 7Z045 AP SoC. Refer to the Mini-Module Plus Baseboard 2 User's Guide for detailed information about these interfaces.

Together the two connectors provide 132 I/O and 8 Giga-bit transceiver lanes to the baseboard.

Below are tables that describe the signals on the JX1 and JX2 connectors, 7Z045 pin assignments, and the signal mapping to the baseboard.

BB2 CONNECTOR SIGNAL NAME	I/O CONNECTOR SIGNAL NAME	JX1 PIN #	7Z045 PIN #	7Z045 PIN #	JX1 PIN #	I/O CONNECTOR SIGNAL NAME	BB2 CONNECTOR SIGNAL NAME
JTAG_TDI	MMP_JTAG_TDI	1	P10	Y10	2	MMP_JTAG_TDO	MMP_TDO
FMC1-LA29_P	JX1_SE_IO_0_P	3	AF18	AF17	4	JX1_SE_IO_0_N	FMC1-LA29_N
FMC1-LA31_P	JX1_SE_IO_2_P	5	AH18	AJ18	6	JX1_SE_IO_2_N	FMC1-LA31_N
FMC1-LA30_P	JX1_SE_IO_4_P	7	AG17	AG16	8	JX1_SE_IO_4_N	FMC1-LA30_N
FMC1-LA33_P	JX1_SE_IO_6_P	9	AE12	AF12	10	JX1_SE_IO_6_N	FMC1-LA33_N
FMC1-LA32_P	JX1_SE_IO_8_P	11	AE16	AE15	12	JX1_SE_IO_8_N	FMC1-LA32_N
SDA_0_VT	JX1_SE_IO_10_P	13	AE13	AF13	14	JX1_SE_IO_10_N	SCL_0
FMC_TRST_L	JX1_SE_IO_12_P	15	AE18	AE17	16	JX1_SE_IO_12_N	FMC1-PRSNT-M2C_L_VT
SW0	JX1_SE_IO_14_P	17	AG12	AH12	18	JX1_SE_IO_14_N	SW1
SW2	JX1_SE_IO_16_P	19	AF15	AG15	20	JX1_SE_IO_16_N	SW3
FMC_VADJ	JX1_VCCIO_SE	21	-	-	22	JX1_VCCIO_SE	FMC_VADJ
SW4	JX1_SE_IO_18_P	23	AJ16	AK16	24	JX1_SE_IO_18_N	SW5
SW6	JX1_SE_IO_20_P	25	AK13	AK12	26	JX1_SE_IO_20_N	SW7
LED0	JX1_SE_IO_22_P	27	AH14	AH13	28	JX1_SE_IO_22_N	LED1
LED2	JX1_SE_IO_24_P	29	AD16	AD15	30	JX1_SE_IO_24_N	LED3
LED4	JX1_SE_IO_26_P	31	AD14	AD13	32	JX1_SE_IO_26_N	DP_HPD
CDCE_SDA_VT	JX1_SE_IO_28_P	33	AJ15	AK15	34	JX1_SE_IO_28_N	CDCE_SCL
UART_RX_VT	JX1_SE_IO_30_P	35	AJ14	AJ13	36	JX1_SE_IO_30_N	UART_TX

BB2 CONNECTOR SIGNAL NAME	I/O CONNECTOR SIGNAL NAME	JX1 PIN #	7Z045 PIN #	7Z045 PIN #	JX1 PIN #	I/O CONNECTOR SIGNAL NAME	BB2 CONNECTOR SIGNAL NAME
PCIe_PERST#_VT	JX1_SE_IO_32_P	37	AC14	AA9	38	MMP_CONF_DONE	FPGA_DONE
CDCE_Y1_OUT	JX1_SE_CLKIN	39	AF14	-	40	JX1_VREF_SE	NC
GND	GND	41	-	-	42	GND	GND
FMC1-DP0-M2C_p	JX1_MGTRX0_P	43	AH10	AK10	44	JX1_MGTTX0_P	FMC1-DP0-C2M_p
FMC1-DP0-M2C_n	JX1_MGTRX0_N	45	AH9	AK9	46	JX1_MGTTX0_N	FMC1-DP0-C2M_n
GND	GND	47	-	-	48	GND	GND
SFP0-RX_p	JX1_MGTRX1_P	49	AJ8	AK6	50	JX1_MGTTX1_P	SFP0-TX_p
SFP0-RX_n	JX1_MGTRX1_N	51	AJ17	AK5	52	JX1_MGTTX1_N	SFP0-TX_n
GND	GND	53	-	-	54	GND	GND
NC	JX1_MGTRX2_P	55	AG8	AJ4	56	JX1_MGTTX2_P	DP_ML_L0_P
NC	JX1_MGTRX2_N	57	AG7	AJ3	58	JX1_MGTTX2_N	DP_ML_L0_N
GND	GND	59	-	-	60	GND	GND
SMA_RX_P	JX1_MGTRX3_P	61	AE8	AK2	62	JX1_MGTTX3_P	SMA_TX_P
SMA_RX_N	JX1_MGTRX3_N	63	AE7	AK1	64	JX1_MGTTX3_N	SMA_TX_N
GND	GND	65	-	-	66	GND	GND
CLK_MUX_OUT_P	JX1_MGTREFCLK_P	67	AD10	-	68	MGTAVTT (1.2V)	1V2
CLK_MUX_OUT_N	JX1_MGTREFCLK_N	69	AD9	-	70	MGTAVTT (1.2V)	1V2
1V0	MGTAVCC (1.0V)	71	-	-	72	MGTAVCC (1.0V)	1V0
1V0	MGTAVCC (1.0V)	73	-	-	74	MGTAVCC (1.0V)	1V0
FMC1-LA01-CC_P	JX1_DIFF_IO_0_P	75	AH19	AK17	76	JX1_DIFF_IO_1_P	FMC1-LA02_P
FMC1-LA01-CC_N	JX1_DIFF_IO_0_N	77	AJ19	AK18	78	JX1_DIFF_IO_1_N	FMC1-LA02_N
1V8	VCCAUX	79	-	-	80	VCCAUX	1V8
FMC1-LA04_P	JX1_DIFF_IO_2_P	81	AF20	AK22	82	JX1_DIFF_IO_3_P	FMC1-LA03_P
FMC1-LA04_N	JX1_DIFF_IO_2_N	83	AG20	AK23	84	JX1_DIFF_IO_3_N	FMC1-LA03_N
1V8	VCCAUX	85	-	-	86	2.5 V	2V5
FMC1-LA05_P	JX1_DIFF_IO_4_P	87	AJ20	AJ23	88	JX1_DIFF_IO_5_P	FMC1-LA06_P
FMC1-LA05_N	JX1_DIFF_IO_4_N	89	AK20	AJ24	90	JX1_DIFF_IO_5_N	FMC1-LA06_N
1V5	1.5V	91	-	-	92	1.5 V	1V5
FMC1-LA07_P	JX1_DIFF_IO_6_P	93	AJ21	AH23	94	JX1_DIFF_IO_7_P	FMC1-LA08_P
FMC1-LA07_N	JX1_DIFF_IO_6_N	95	AK21	AH24	96	JX1_DIFF_IO_7_N	FMC1-LA08_N
1V0	VCCINT	97	-	-	98	VCCINT	1V0
FMC1-LA11_P	JX1_DIFF_IO_8_P	99	AD21	AJ25	100	JX1_DIFF_IO_9_P	FMC1-LA12_P
FMC1-LA11_N	JX1_DIFF_IO_8_N	101	AE21	AK25	102	JX1_DIFF_IO_9_N	FMC1-LA12_N
1V0	VCCINT	103	-	-	104	2.5 V	2V5
FMC1-LA10_P	JX1_DIFF_IO_10_P	105	AD23	AC24	106	JX1_DIFF_IO_11_P	FMC1-LA09_P
FMC1-LA10_N	JX1_DIFF_IO_10_N	107	AE23	AD24	108	JX1_DIFF_IO_11_N	FMC1-LA09_N
FMC_Vadj	JX1_VCCIO_DIFF	109	-	-	110	JX1_VCCIO_DIFF	FMC_Vadj
FMC1-LA14_P	JX1_DIFF_IO_12_P	111	AF23	AG24	112	JX1_DIFF_IO_13_P	FMC1-LA13_P
FMC1-LA14_N	JX1_DIFF_IO_12_N	113	AF24	AG25	114	JX1_DIFF_IO_13_N	FMC1-LA13_N
NC	JX1_Vref_DIFF	115		-	116	2.0 V	2V0
FMC1-LA00-CC_P	JX1_DIFF_RCLKIN_P	117	AG21	AE22	118	JX1_DIFF_CLKIN_P	FMC1-CLK0-M2C_P
FMC1-LA00-CC_N	JX1_DIFF_ RCLKIN_N	119	AH21	AF22	120	JX1_DIFF_CLKIN_N	FMC1-CLK0-M2C_N

Table 17 – JX1 Pin Assignments and Baseboard Signal Mapping

BB2 CONNECTOR SIGNAL NAME	I/O CONNECTOR SIGNAL NAME	JX2 PIN #	7Z045 PIN #	7Z045 PIN #	JX2 PIN #	I/O CONNECTOR SIGNAL NAME	BB2 CONNECTOR SIGNAL NAME
JTAG_TCK	MMP_JTAG_TCK	1	Y12	V10	2	MMP_JTAG_TMS	JTAG_TMS
PB0	JX2_SE_IO_0_P	3	Y30	AA30	4	JX2_SE_IO_0_N	PB1
PB2	JX2_SE_IO_2_P	5	Y28	AA29	6	JX2_SE_IO_2_N	PB3
SFP0_TX_FAULT_VT	JX2_SE_IO_4_P	7	AG26	AG27	8	JX2_SE_IO_4_N	SFP0_TX_DISABLE
SFP0_MOD2_VT	JX2_SE_IO_6_P	9	AF29	AG29	10	JX2_SE_IO_6_N	SFP0_MOD1
SFP0_MOD0_VT	JX2_SE_IO_8_P	11	Y26	Y27	12	JX2_SE_IO_8_N	SFP0_RSEL
SFP0_LOS_VT	JX2_SE_IO_10_P	13	AE25	AF25	14	JX2_SE_IO_10_N	PMOD1_P1_VT
PMOD1_P2_VT	JX2_SE_IO_12_P	15	AA27	AA28	16	JX2_SE_IO_12_N	PMOD1_P3_VT
PMOD1_P4_VT	JX2_SE_IO_14_P	17	AC26	AD26	18	JX2_SE_IO_14_N	PMOD1_P7_VT
PMOD1_P8_VT	JX2_SE_IO_16_P	19	AD30	AE30	20	JX2_SE_IO_16_N	PMOD1_P9_VT
FMC_VADJ	JX2_VCCIO_SE	21	-	-	22	JX2_VCCIO_SE	FMC_VADJ
PMOD1_P10_VT	JX2_SE_IO_18_P	23	AC29	AD29	24	JX2_SE_IO_18_N	PMOD2_P1_VT
PMOD2_P2_VT	JX2_SE_IO_20_P	25	AF30	AG30	26	JX2_SE_IO_20_N	PMOD2_P3_VT
PMOD2_P4_VT	JX2_SE_IO_22_P	27	AE28	AF28	28	JX2_SE_IO_22_N	PMOD2_P7_VT
PMOD2_P8_VT	JX2_SE_IO_24_P	29	AB27	AC27	30	JX2_SE_IO_24_N	PMOD2_P9_VT
PMOD2_P10_VT	JX2_SE_IO_26_P	31	AE27	AF27	32	JX2_SE_IO_26_N	SD1_D0_VT
SD1_D1_VT	JX2_SE_IO_28_P	33	AB29	AB30	34	JX2_SE_IO_28_N	SD1_D2_VT
SD1_D3_VT	JX2_SE_IO_30_P	35	AD25	AE26	36	JX2_SE_IO_30_N	SD1_CMD
SD1_CLK	JX2_SE_IO_32_P	37	AH28	Y9	38	MMP_CONF_ PROGRAM	FPGA_PROG#
CDCE_Y2_OUT	JX2_SE_CLK	39	AC28	-	40	JX2_Vref_SE	NC
GND	GND	41	-	-	42	GND	GND
PCIe-RX2_P	JX2_MGTRX0_P	43	U4	R4	44	JX2_MGTTX0_P	PCIe-TX2_P
PCIe-RX2_N	JX2_MGTRX0_N	45	U3	R3	46	JX2_MGTTX0_N	PCIe-TX2_N
GND	GND	47	-	-	48	GND	GND
PCIe-RX3_P	JX2_MGTRX1_P	49	V6	T2	50	JX2_MGTTX1_P	PCIe-TX3_P
PCIe-RX3_N	JX2_MGTRX1_N	51	V5	T1	52	JX2_MGTTX1_N	PCIe-TX3_N
GND	GND	53	-	-	54	GND	GND
PCIe-RX0_P	JX2_MGTRX2_P	55	P6	N4	56	JX2_MGTTX2_P	PCIe-TX0_P
PCIe-RX0_N	JX2_MGTRX2_N	57	P5	N3	58	JX2_MGTTX2_N	PCIe-TX0_N
GND	GND	59	-	-	60	GND	GND
PCIe-RX1_P	JX2_MGTRX3_P	61	T6	P2	62	JX2_MGTTX3_P	PCIe-TX1_P
PCIe-RX1_N	JX2_MGTRX3_N	63	T5	P1	64	JX2_MGTTX3_N	PCIe-TX1_N
GND	GND	65	-	-	66	GND	GND
LJ-PCIe-REFCLK0_P	JX2_MGTREFCLK_P	67	N8	-	68	MGTAVTT (1.2 V)	1V2
LJ-PCIe-REFCLK0_N	JX2_MGTREFCLK_N	69	N7	-	70	MGTAVTT (1.2 V)	1V2
1V0	MGTAVCC (1.0V)	71	-	-	72	MGTAVCC (1.0 V)	1V0
1V0	MGTAVCC (1.0V)	73	-	-	74	MGTAVCC (1.0 V)	1V0
FMC1-LA15_P	JX2_DIFF_IO_0_P	75	V28	U25	76	JX2_DIFF_IO_1_P	FMC1-LA16_P
FMC1-LA15_N	JX2_DIFF_IO_0_N	77	V29	V26	78	JX2_DIFF_IO_1_N	FMC1-LA16_N
1V8	VCCAUX	79	-	-	80	VCCAUX	1V8
FMC1-LA18-CC_P	JX2_DIFF_IO_2_P	81	W29	P30	82	JX2_DIFF_IO_3_P	FMC1-LA20_P
FMC1-LA18-CC_N	JX2_DIFF_IO_2_N	83	W30	R30	84	JX2_DIFF_IO_3_N	FMC1-LA20_N
1V8	VCCAUX	85	-	-	86	2.5 V	2V5
FMC1-LA23_P	JX2_DIFF_IO_4_P	87	T29	W25	88	JX2_DIFF_IO_5_P	FMC1-LA19_P
FMC1-LA23_N	JX2_DIFF_IO_4_N	89	U29	W26	90	JX2_DIFF_IO_5_N	FMC1-LA19_N
1V5	1.5V	91	-	-	92	1.5 V	1V5
FMC1-LA21_P	JX2_DIFF_IO_6_P	93	T30	R27	94	JX2_DIFF_IO_7_P	FMC1-LA22_P
FMC1-LA21_N	JX2_DIFF_IO_6_N	95	U30	T27	96	JX2_DIFF_IO_7_N	FMC1-LA22_N

BB2 CONNECTOR SIGNAL NAME	I/O CONNECTOR SIGNAL NAME	JX2 PIN #	7Z045 PIN #	7Z045 PIN #	JX2 PIN #	I/O CONNECTOR SIGNAL NAME	BB2 CONNECTOR SIGNAL NAME
1V0	VCCINT	97	-	-	98	VCCINT	1V0
FMC1-LA24_P	JX2_DIFF_IO_8_P	99	N26	P25	100	JX2_DIFF_IO_9_P	FMC1-LA25_P
FMC1-LA24_N	JX2_DIFF_IO_8_N	101	N27	P26	102	JX2_DIFF_IO_9_N	FMC1-LA25_N
1V0	VCCINT	103	-	-	104	2.5V	2V5
FMC1-LA28_P	JX2_DIFF_IO_10_P	105	N28	T24	106	JX2_DIFF_ IO_11_P	FMC1-LA27_P
FMC1-LA28_N	JX2_DIFF_IO_10_N	107	P28	T25	108	JX2_DIFF_ IO_11_N	FMC1-LA27_N
FMC_Vadj	JX2_VCCIO_DIFF	109	-	-	110	JX2_VCCIO_DIFF	FMC_Vadj
FMC1-LA26_P	JX2_DIFF_IO_12_P	111	N29	V27	112	JX2_DIFF_ IO_13_P	DP_AUX_CH_P
FMC1-LA26_N	JX2_DIFF_IO_12_N	113	P29	W28	114	JX2_DIFF_ IO_13_N	DP_AUX_CH_N
NC	JX2_Vref_DIFF	115	-	-	116	3.3V	3V3
FMC1-LA17-CC_P	JX2_DIFF_ RCLKIN_P	117	R25	U26	118	JX2_DIFF_ CLKIN_P	FMC1-CLK1-M2C_P
FMC1-LA17-CC_N	JX2_DIFF_ RCLKIN_N	119	R26	U27	120	JX2_DIFF_ CLKIN_N	FMC1-CLK1-M2C_N

Table 18 – JX2 Pin Assignments and Baseboard Signal Mapping

2.10 Power

The Zynq 7Z045 Mini-Module Plus Development Board's power is sourced from the Mini-Module Plus baseboard 2 via the JX1 and JX2 connectors. Below is a diagram that illustrates the voltage rails sourced by the baseboard.

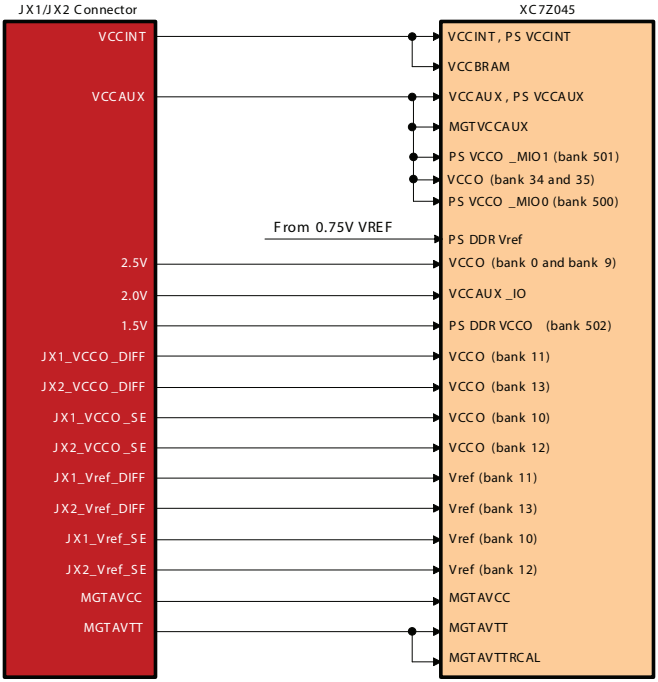

Figure 12 - Power Supply Diagram

FMC_VADJ, VCC_AUX and the 1.5 V voltage rails are selectable from the baseboard. Early versions (Rev B) of the Mini-Module Plus Baseboard 2 have three slide switches SW13, SW14 and SW15 to select these voltages.

Baseboard SW13 selects the DDR voltage that is supplied to the DDR3 devices. Since the Mini-Module Plus Baseboard 2 supports the Virtex-5 Mini-Module Plus the DDR voltage is selectable between 1.8 V (DDR2) and 1.5 V/1.35 V (DDR3). Since the Zynq utilizes DDR3 devices it is important to always have SW13 in the UP position (marked "K7" on the baseboard) to insure the proper 1.5 V voltage is being supplied to the Zynq Mini-Module's DDR3 memory.

Baseboard SW14 selects the VCC_AUX voltage that is supplied to the 7Z045 AP SoC. Placing the switch in the UP position (marked "K7" on the baseboard) supplies the correct voltage of 1.8 V to the 7Z045. If the switch is put in the DOWN position this will select 2.5V and cause damage to the 7Z045.

SW15 selects the FMC_ADJ voltage rail to be 2.5 V or 3.3 V . The FMC_VADJ rail powers the 7Z045 VCCO pins for the banks that the baseboard's FMC LPC interface is connected to, banks 10, 11, 12 and 13. The 2.5 V or 3.3 V selection depends on what hardware or application is connected to the baseboard's FMC LPC connector.

NOTICE!

It is VERY IMPORTANT to insure SW13 and SW14 on the Mini-Module Plus Baseboard 2 are in the UP (K7) position while operating the Zynq 7Z045 Mini-Module Plus!!! Failure to insure the correct switch positions prior to powering up the system can cause damage to the module.

All versions of the Mini-module Plus Baseboard 2 ship with SW13 and SW14 in the UP position to support K7 and Zynq series Mini-Modules. SW15 is placed in the DOWN position to select 2.5 V for the FMC_VADJ rail.

Later versions (Rev C and later) only have SW15 (FMC_VADJ) populated. SW13 (DDR Voltage) and SW14 (VCC_AUX) voltage rails are hard wired to support DDR3 memory and K7 and Zynq series devices. These voltage settings can be modified by changing the position of the 0-ohm resistor(s) on the back side of the baseboard.

Refer the Mini-Module plus Baseboard 2 User's Guide on the DRC for more detailed information about the baseboard power system.

www.em.avnet.com/en-us/design/drc/Pages/Mini-Module-Plus-Baseboard-2.aspx

2.11 Thermal Management

An active heat sink is used to dissipate heat from the 7Z045. A Cool Innovations heat sink (PN: **3-121204UBFA**) and an NMB 12 V fan (PN: **1204KL-04W-B50-B00**) are assembled together and shipped with the Zynq 7Z045 Mini-Module Plus. The active heat sink is powered by connecting the three position connector (TE PN: 173977-3) to the mating connector on the Mini-Module Plus Baseboard 2. Earlier versions (Rev B) of the baseboard will not have a mating connector but will have a pigtail provided with the board to connect to the fan connector.

For aggressive applications that utilize large amounts of ZYNQ PL resources it is recommended that an accurate worst-case power analysis be performed to avoid the pitfalls of overdesigning or under designing your product's power or cooling system, using the Xilinx Power Estimator (XPE).

3.0 PRE-PROGRAMMED MEMORY

This section describes the factory programmed applications that reside on the Zynq 7Z045 Mini-Module Plus upon shipment. Other test and reference designs are posted on the Zynq 7Z045 Mini-Module Plus DRC page under the "Support and Downloads" link.

www.em.avnet.com/en-us/design/drc/Pages/Xilinx-Zynq-7000-SoC-Mini-Module-Plus-Development-Kit.aspx

Both the QSPI and the included micro SD card included with the Zynq 7Z045 Mini-Module Plus board are pre-programed with applications that allow the user to quickly power on the board and utilize some of the board peripherals.

3.1 QSPI - PCI Express Endpoint

The QSPI devices on the Zynq 7Z045 Mini-Module Plus are programmed with the Xilinx PCI Express 2.0 Endpoint design that is created from CoreGen. This application allows the Zynq 7Z045 Mini-Module Plus system to be enumerated on a PCI Express bus and simple bus transactions be made.

The Zynq 7Z045 Mini-Module Plus is shipped with the configuration SW5 set to configure from the QSPI interface. SW5 should be set to **SW5[0:4] = x0010**. The user can install the Zynq 7Z045 Mini-Module Plus system into a PCI Express slot and power up the system and see the Zynq 7Z045 Mini-Module Plus system enumerated on the PCI Express bus using a PCI Express bus analyzer/viewer such as PCI Tree.

NOTE: The Mini-Module Plus Baseboard does not get power from the PCI Express slot. The external power supply shipped with the baseboard must be used to power the Zynq 7Z045 Mini-Module Plus system.

3.2 Micro SD Card - Linux

The supplied micro SD card shipped with the Zynq 7Z045 Mini-Module Plus is pre-programmed with a Linux image that will boot upon power-up when the configuration switch SW5 is set to the proper mode. To configure from the micro SD card and boot Linux set S**W5[0:4] = x011x**.

Prior to power-on the user will need to attach a USB cable between the Zynq 7Z045 Mini-Module Plus USB UART connector J4 and a PC or laptop. Open a terminal session and set it for the correct COM port (shown in the device manager as CP210x) with the following settings: 115200-8-N-1.

Once the terminal shell is open turn on power to the system and the user will see Linux booting on the terminal screen. After boot is complete a Linux command line will be present and commands can be entered.

NOTE: The PC or laptop will require the Silicon Labs CP210x driver be installed in order to use the USB UART interface. These drivers can be found at the Silicon Labs website or on the Avnet Zynq 7Z045 Mini-Module Plus DRC site under the "Support and Downloads" link.

www.em.avnet.com/en-us/design/drc/Pages/Xilinx-Zynq-7000-SoC-Mini-Module-Plus-Development-Kit.aspx

APPENDIX A – ASSEMBLY DRAWING AND JUMPER DEFINITIONS

This section provides a description of the jumper settings for the Zynq 7Z045 Mini-Module Plus Development Board. The board is ready to use out of the box with the default jumper settings. The following assembly drawing of the component side of the board shows the location of the jumpers followed by a brief description of the jumper functions.

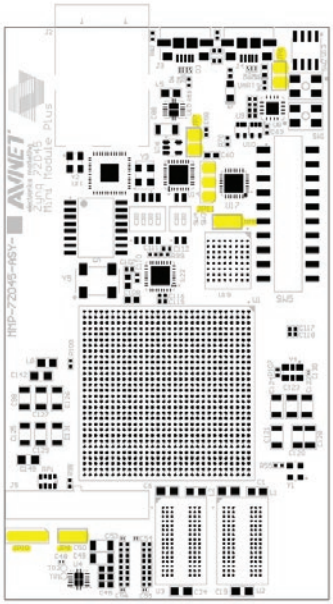

Figure 13 - Board Jumpers

JP6 – MASTER RESET: When a jumper is placed JP6 will assert both the PS_POR# and PS_SRST# signals LOW to reset the 7Z045. Default: DNP

JP7 – USB 2.0 VBUS SELECT: Place this jumper when the USB 2.0 interface is to be used as the Host (OTG). This will provide VBUS with 5.0V to the endpoint device. Default: DNP

JP8 – PJTAG VREF: Place this jumper to provide a 2.5 V reference voltage to a third party debugger. Default: DNP

JP9 – PFLASH WP#: Place this jumper to enable the Write Protect function for the parallel flash device U19. Default: DNP

JP10 – JTAG RESET: This jumper is populated to allow the user to hard wire the baseboard's JTAG reset signal to the 7Z045's PS_SRST# signal. Default: 2-3.

JP11 – USB 2.0 MODE: When USB is operating in Device Mode this jumper must be placed in position 1-2. When operating in Host/OTG Mode this jumper must be placed in position 2-3. Default: DNP

GS-AES-7Z7045-G-01-v1