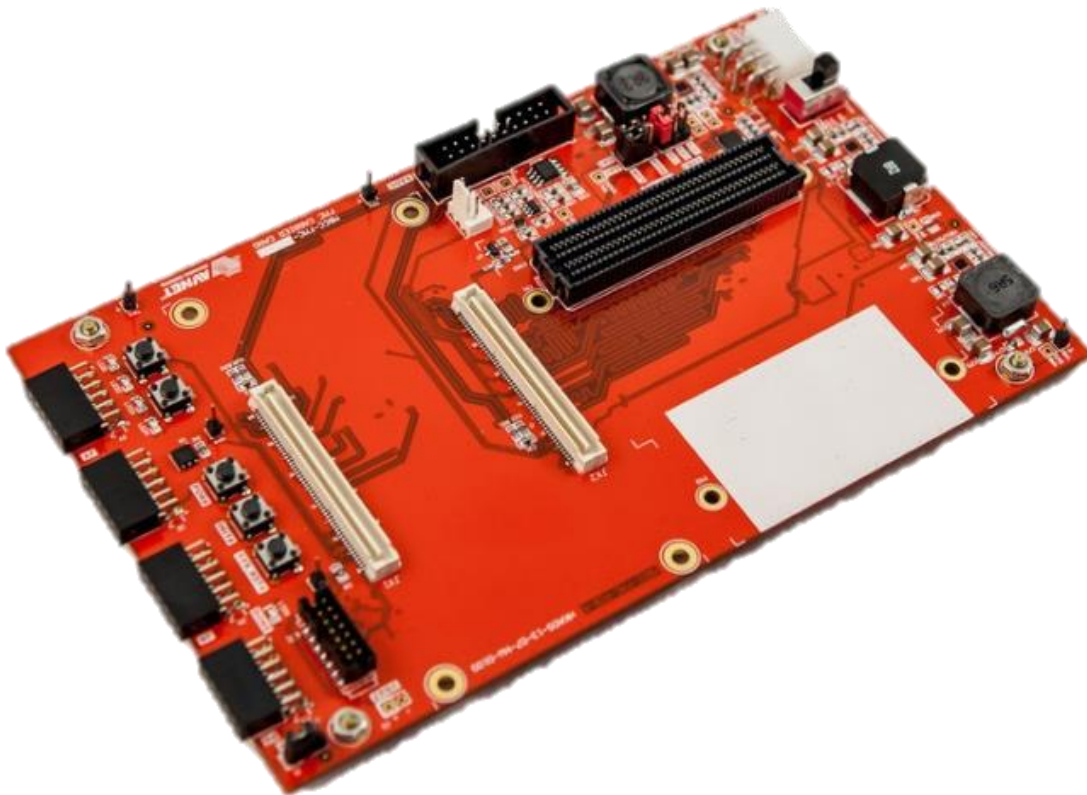

MicroZed FMC Carrier Card

Zynq™ System On Module
Hardware User Guide



Revision 1.1
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1 Introduction

The MicroZed FMC Carrier Card (FMC-CC) is a low cost evaluation board for the MicroZed series System On Module (SOM) boards. The function of this board is to provide SoC I/O pin accessibility to the MicroZed SOM board through the low-pin-count FPGA Mezzanine Card (FMC) connector. In addition to SoC I/O pin access through the FMC-CC interface, the FMC-CC also provides SOM board power via the JX MicroHeaders. Please refer to the MicroZed Hardware User's guide for the MicroZed's feature set. The features provided by the FMC-CC are:

- Interfaces
 - FMC LPC (72 differential, 4 SE)
 - Xilinx PC4 Header for programming
 - Accesses PL JTAG
 - 5 Digilent Pmod™ compatible interfaces
 - One connected to PS MIO
 - Two connected to Bank 13 PL (7Z020 only)
 - One connected to Bank 34 PL
 - One connected to Bank 35 PL
 - Two 100-pin MicroHeaders for MicroZed insertion
 - Reset Push Button (SYS_RST#)
 - 2 User Push Buttons
 - 2 Configuration Push Buttons (POR# & INIT#)
 - 4 User LEDs
 - 2 Status LEDs (DONE & PWR)
 - 1 slide switch for main power
- On-board Memory:
 - 2 Kbit EUI-48 MAC ID EEPROM
 - 1Kbit 1-wire SHA EEPROM (optional – default not populated)
- Power
 - On Board
 - High-efficiency regulator for 5.0V @ 3A
 - For MicroZed SOM module
 - High-efficiency regulator for 3.3V @ 3A
 - For FMC connection
 - High-efficiency regulator Vadj for 1.8V/2.5V/3.3V @ 4A
 - For MicroZed SOM VCC_{IO} Bank_34, Bank_35, and Bank_13 and also FMC VADJ
 - Wall Adapter
 - Primary 12V ≥ 5.0A, 2x3 connector
 - NOTE: not an ATX compatible power supply.
 - <http://www.em.avnet.com/12Vpower>
 - [AES-SLP-12V5A-G](#)

1.1 Zynq Bank Pin Assignments

The following figure shows the Zynq bank pin assignments on the MicroZed. When paired with the FMC-CC, the board pair includes all the features shown below, as well as all the FMC-CC features that interface to the MicroZed through MicroHeaders 1 and 2.

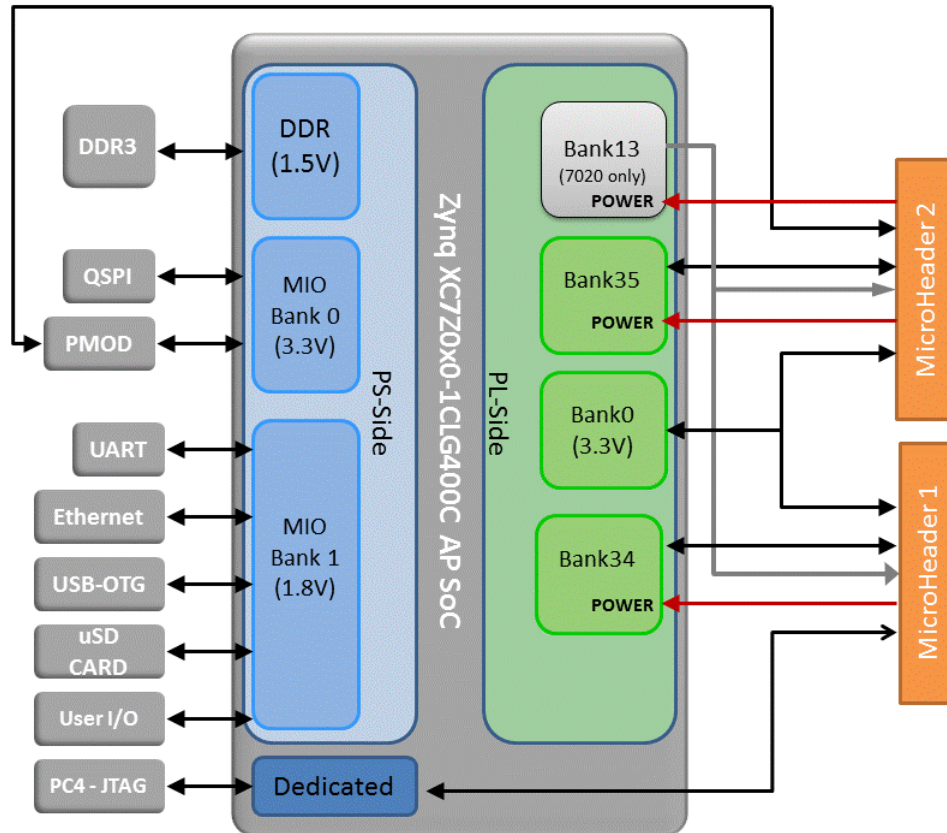


Figure 1 – MicroZed Zynq 7010/20 CLG400 Bank Assignments

1.2 MicroZed FMC-CC Block Diagram

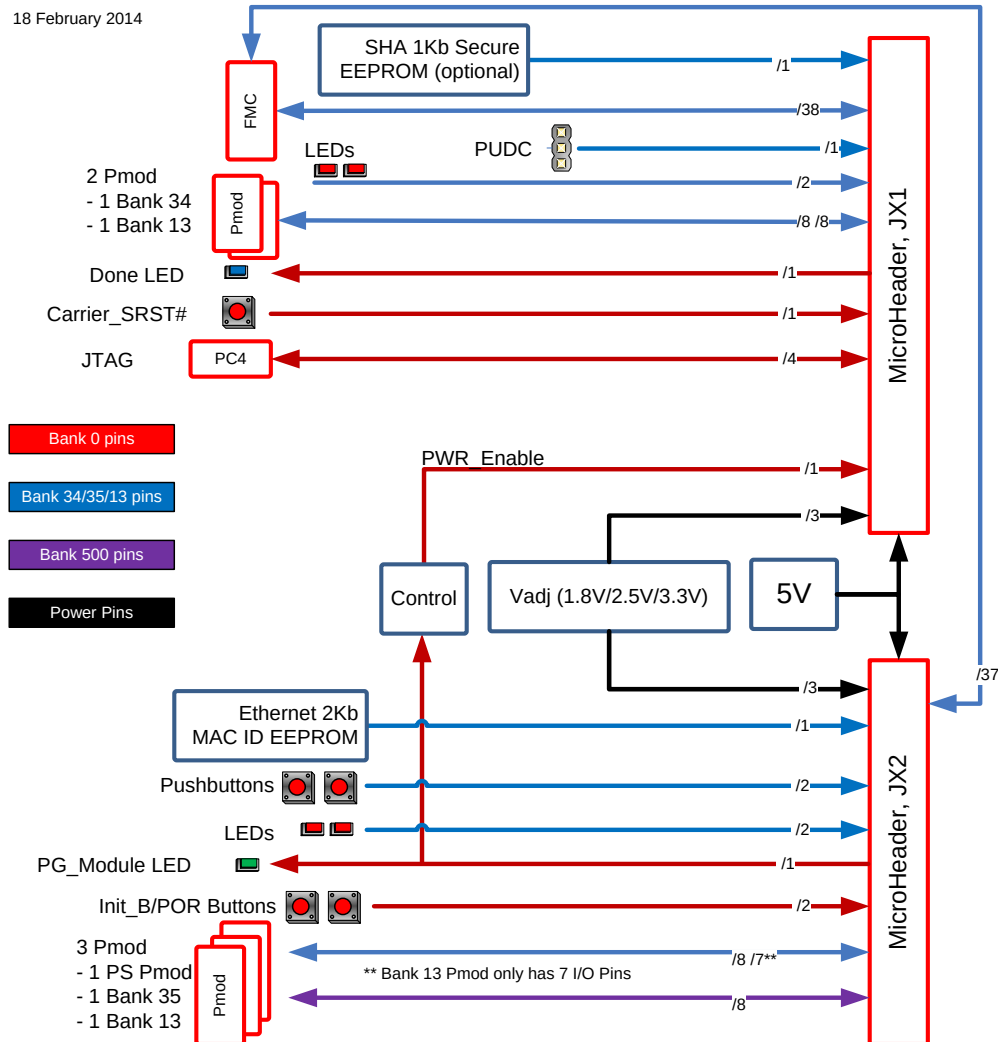


Figure 2 – MicroZed FMC-CC Block Diagram

1.3 FMC-CC Circuit Identification

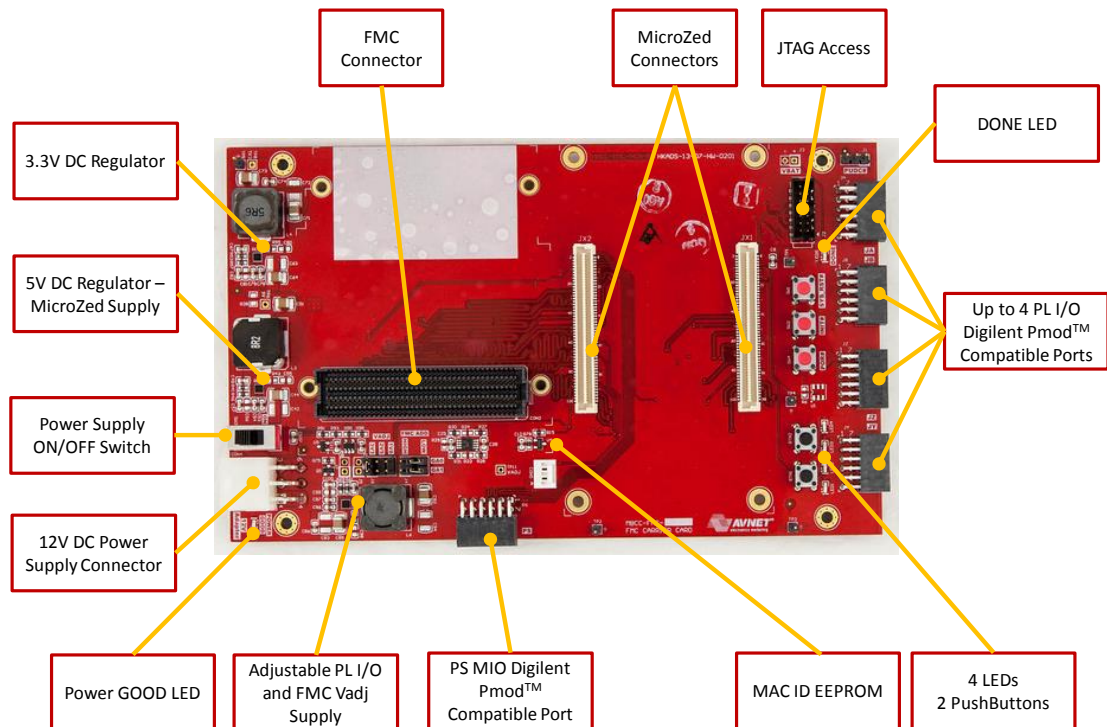


Figure 3: FMC-CC Topology

2 Functional Description

The FMC-CC is an expansion board for MicroZed. It is very similar to the I/O Carrier Card with the exception the FMC-LPC is the primary means of exposing the additional I/O rather than Pmod connections. The FMC-CC bridges Avnet's MicroZed 7Z010 or 7Z020 System On Module (SOM) product to application specific FMC modules. In addition to the LPC FMC connector, the FMC-CC also adds up to 5 Digilent Pmod™ compatible Interfaces, 4 User LEDs, 2 User Pushbuttons, and an Ethernet MAC ID EEPROM.

2.1 Memory Sources

2.1.1 SHA EEPROM

The FMC-CC provides an optional footprint for a SHA-1 Security 1 Kbit EEPROM for FPGA authentication using the Maxim DS28E02P+ device. This interface requires 1 SOC I/O and one pull-up resistor. Refer to Maxim's website for further use information.

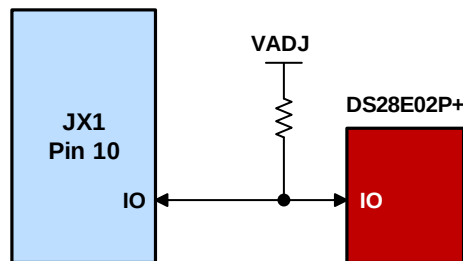


Figure 4 – SHA EEPROM 1-wire Interface

Table 1 – Push Button Connections

Carrier Net Name	MicroHeader Connection	Zynq AP SoC Connection	Zynq AP SoC pin name
EEPROM	JX1, pin 10	Bank 34, T19	IO_25_34

2.1.2 MAC ID EEPROM

The FMC-CC provides a 2 Kbit EEPROM with a pre-programmed EUI-48 48-bit Node address using a Microchip 11AA02E48 device. This device may be used for a unique MAC ID for the Ethernet circuit on the MicroZed SOM. This interface requires 1 SoC I/O and one pull-up resistor. Refer to Microchip's website for further use information.

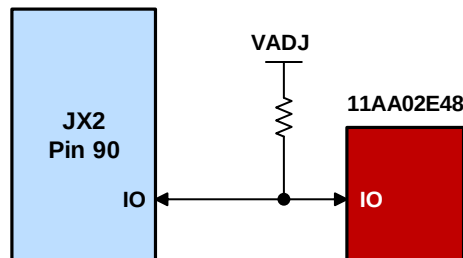


Figure 5 – MAC ID EEPROM 1-wire Interface

Table 2 – Push Button Connections

Carrier Net Name	MicroHeader Connection	Zynq AP SoC Connection	Zynq AP SoC pin name
MAC_ID	JX2, pin 90	Bank 35, J16	IO_L24N_T3_AD15N_35

2.2 Reset sources

2.2.1 INIT# button – SW2

The INIT# button provides an active low input signal to the SoC. It is used to stall the power-on configuration sequence at the end of the initialization process of the SOC. This signal is rarely used.

Table 3 – INIT# Connection

Carrier Net Name	MicroHeader Connection	Zynq AP SoC Connection
INIT#	JX2, pin 9	INIT#

2.2.2 Power On Reset – POR# button – SW4

The POR# button provides an active low signal to the PG_CARRIER net on the JX2 MicroHeader pin 11 and to the LPC FMC connector, pin D1. When asserted, this signal resets the MicroZed's USB UART, USB OTG circuit and turns off the FMC-CC VCCIO_34/35 power supplies. It is used to invoke an FMC-CC and MicroZed total system power reset. The PS and PL are reset to power on default settings and the selected boot process is initiated.

Table 4 – POR Connection

Carrier Net Name	MicroHeader Connection	Zynq AP SoC Connection
PG_CARRIER	JX2, pin 11	PG_MODULE

2.2.3 Processor Subsystem Reset: SYS_RST# button – SW1

The SYS_RST# button provides an active low signal to net CARRIER_SRST# which allows the user to reset all of the functional logic within the device without disturbing the debug environment. For example, the previous break points set by the user remain valid after system reset. Due to security concerns, system reset erases all memory content within the PS, including the OCM. The PL is also reset in system reset. System reset does not re-sample the boot mode strapping pins.

Table 5 – SYS_RST# Connection

Carrier Net Name	MicroHeader Connection	Zynq AP SoC Connection
CARRIER_SRST#	JX1, pin 6	CARRIER_SRST#

2.3 User I/O

2.3.1 User Push Buttons

The Carrier provides 2 user GPIO push buttons to the Zynq-7000 AP SoC. Pull-down resistors provide a known low default state. Pushing a button connects to VADJ to assert a logic high.

Table 6 – Push Button Connections

Carrier Net Name	MicroHeader Connection	Zynq AP SoC Connection	Zynq AP SoC pin name
PB0	JX2, pin 67	Bank 35, G19	IO_L18P_T2_AD13P_35
PB1	JX2, pin 69	Bank 35, G20	IO_L18N_T2_AD13N_35

2.3.2 User LEDs

The Carrier has 4 user LEDs. A logic high from the Zynq-7000 AP SoC I/O turns the LED on. LED's are sourced from 3.3V with current limiting resistors. The Bank 34 and 35 I/O control signals feed a BSS138

Table 7 – LED Connections

Carrier Net Name	MicroHeader Connection	Zynq AP SoC Connection	Zynq AP SoC pin name
LED0	JX1, pin 9	Bank 34, R19	IO_0_34
LED1	JX1, pin 19	Bank 34, V13	IO_L3N_T0_DQS_34
LED2	JX2, pin 88	Bank 35, K16	IO_L24P_T3_AD15P_35
LED3	JX2, pin 89	Bank 35, M15	IO_L24N_T3_AD15N_35

2.3.3 FMC GA [1:0] jumper header

The carrier allows the user to select the FMC board address via J4 and 2 jumper headers. The address range is from 0 to 3 via jumper headers. The jumpers force a high or a low on address bits 1 or 0. Default FMC address is 00 where the jumpers are placed at location 3-5 and 4-6 on J4. Refer to the schematic for further options.

Table 8 – FMC GA [1:0] address select

Carrier Net Name	FMC LPC CON2E connection
GA0	C34
GA1	D35

2.4 Interface Headers

2.4.1 FMC LPC Connector

A single FMC LPC slot is implemented on the FMC-CC to support plug-in modules. The block diagram shows the MicroHeader connections to the FMC LPC connectors.

There are four mounting holes in the FMC card area to facilitate secure FMC module mounting.

The following guidelines have been observed in the layout of the card:

- **CLK_#_M2C**
 - 50 ohm single-ended impedance
 - Less than 10mil skew in P/N pair
 - Connected to MRCC (Multi-Region)
 - No length matching to any other feature
- **LA bus**
 - 50 ohm single-ended impedance
 - Less than 10mil skew in P/N pair
 - Less than 100mil length skew across all bits in a bus
 - LA Bus 0:16 located in bank 34
 - LA Bus 17:33 located in bank 35
 - CC Pairs 0, 17 on MRCC pins
 - CC Pairs 1, 18 on SRCC pins
- To conserve SoC pins, GA[1:0] pins are connected jumpers

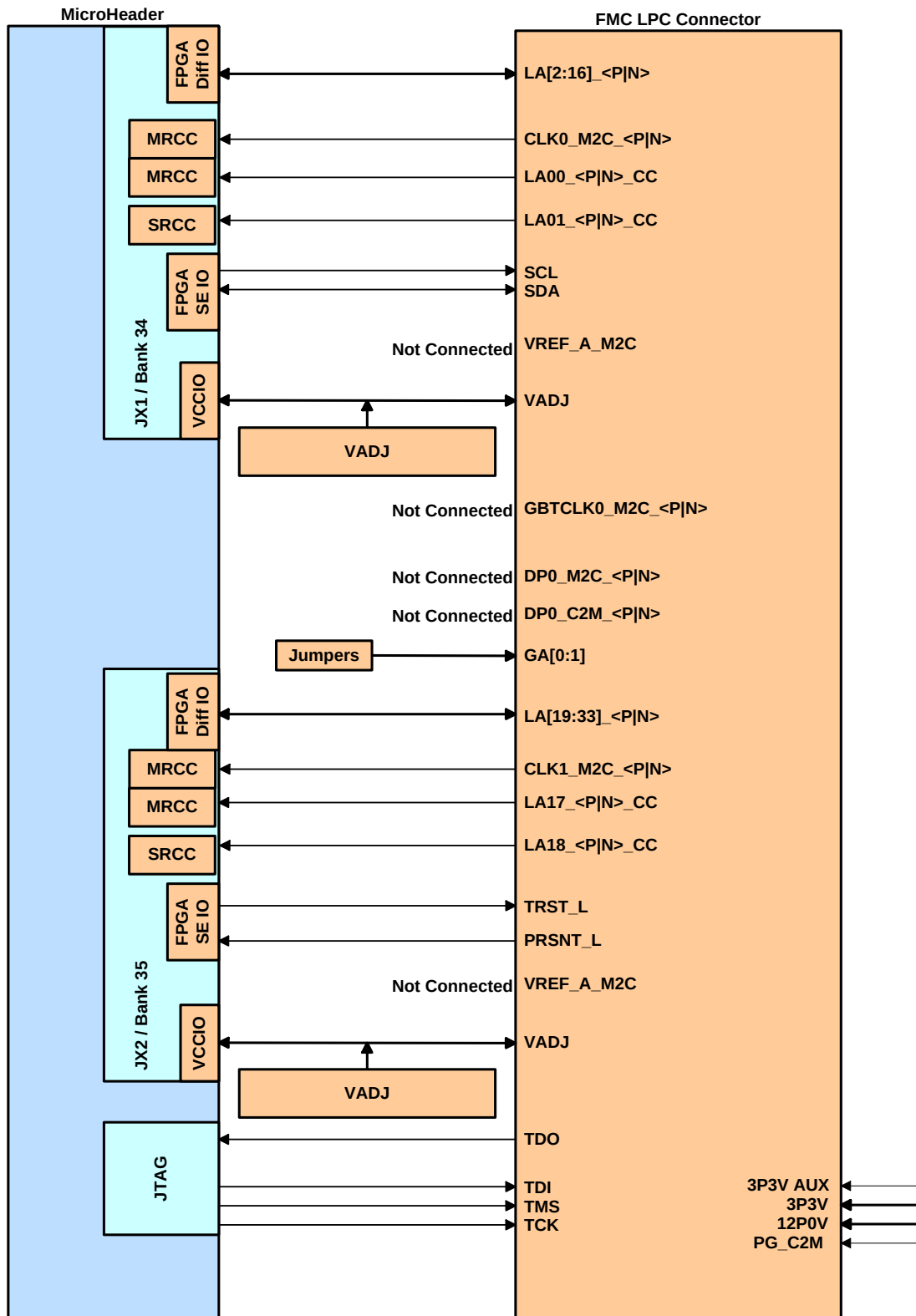


Figure 6 – FMC Connections

Note: The FMC slot SDA, SCL, PRSTN_M2C_L, and TRST_L signals are 3.3V levels, so a level translator (TCA9517A) is implemented to follow the VADJ level.

Table 9 – FMC JX1 (Bank 34) Connections

Carrier Net Name	MicroHeader Connection	Zynq AP SoC Connection	Zynq AP SoC Pin
CLK0_M2C_N	JX1, pin 44	Bank 34, U19	IO_L12N_T1_MRCC_34
CLK0_M2C_P	JX1, pin 42	Bank 34, U18	IO_L12P_T1_MRCC_34
FMC_SCL	JX1, pin 84	Bank 34, P16	IO_L24N_T3_34
FMC_SDA	JX1, pin 82	Bank 34, P15	IO_L24P_T3_34
LA00_N_CC	JX1, pin 49	Bank 34, P19	IO_L13N_T2_MRCC_34
LA00_P_CC	JX1, pin 47	Bank 34, N18	IO_L13P_T2_MRCC_34
LA01_N_CC	JX1, pin 50	Bank 34, P20	IO_L14N_T2_SRCC_34
LA01_P_CC	JX1, pin 48	Bank 34, N20	IO_L14P_T2_SRCC_34
LA02_N	JX1, pin 26	Bank 34, R14	IO_L6N_T0_VREF_34
LA02_P	JX1, pin 24	Bank 34, P14	IO_L6P_T0_34
LA03_N	JX1, pin 31	Bank 34, Y17	IO_L7N_T1_34
LA03_P	JX1, pin 29	Bank 34, Y16	IO_L7P_T1_34
LA04_N	JX1, pin 32	Bank 34, Y14	IO_L8N_T1_34
LA04_P	JX1, pin 30	Bank 34, W14	IO_L8P_T1_34
LA05_N	JX1, pin 37	Bank 34, U17	IO_L9N_T1_DQS_34
LA05_P	JX1, pin 35	Bank 34, T16	IO_L9P_T1_DQS_34
LA06_N	JX1, pin 38	Bank 34, W15	IO_L10N_T1_34
LA06_P	JX1, pin 36	Bank 34, V15	IO_L10P_T1_34
LA07_N	JX1, pin 43	Bank 34, U15	IO_L11N_T1_SRCC_34
LA07_P	JX1, pin 41	Bank 34, U14	IO_L11P_T1_SRCC_34
LA08_N	JX1, pin 55	Bank 34, U20	IO_L15N_T2_DQS_34
LA08_P	JX1, pin 53	Bank 34, T20	IO_L15P_T2_DQS_34
LA09_N	JX1, pin 56	Bank 34, W20	IO_L16N_T2_34
LA09_P	JX1, pin 54	Bank 34, V20	IO_L16P_T2_34
LA10_N	JX1, pin 63	Bank 34, Y19	IO_L17N_T2_34
LA10_P	JX1, pin 61	Bank 34, Y18	IO_L17P_T2_34
LA11_N	JX1, pin 64	Bank 34, W16	IO_L18N_T2_34
LA11_P	JX1, pin 62	Bank 34, V16	IO_L18P_T2_34
LA12_N	JX1, pin 69	Bank 34, R17	IO_L19N_T3_VREF_34
LA12_P	JX1, pin 67	Bank 34, R16	IO_L19P_T3_34
LA13_N	JX1, pin 70	Bank 34, R18	IO_L20N_T3_34
LA13_P	JX1, pin 68	Bank 34, T17	IO_L20P_T3_34
LA14_N	JX1, pin 75	Bank 34, V18	IO_L21N_T3_DQS_34
LA14_P	JX1, pin 73	Bank 34, V17	IO_L21P_T3_DQS_34
LA15_N	JX1, pin 76	Bank 34, W19	IO_L22N_T3_34
LA15_P	JX1, pin 74	Bank 34, W18	IO_L22P_T3_34
LA16_N	JX1, pin 83	Bank 34, P18	IO_L23N_T3_34
LA16_P	JX1, pin 81	Bank 34, N17	IO_L23P_T3_34

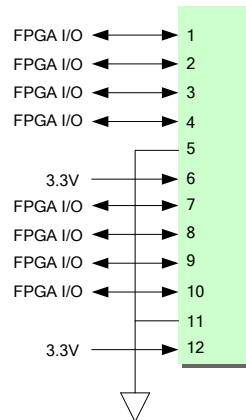
Table 10 – FMC JX2 (Bank 35) Connections

Carrier Net Name	MicroHeader Connection	Zynq AP SoC Connection	Zynq AP SoC Pin
CLK1_M2C_N	JX2, pin 50	Bank 35, K18	IO_L12N_T1_MRCC_35
CLK1_M2C_P	JX2, pin 48	Bank 35, K17	IO_L12P_T1_MRCC_35
FMC_PRSNT_L	JX2, pin 87	Bank 35, M14	IO_L23P_T3_35
LA17_N_CC	JX2, pin 55	Bank 35, H17	IO_L13N_T2_MRCC_35
LA17_P_CC	JX2, pin 53	Bank 35, H16	IO_L13P_T2_MRCC_35
LA18_N_CC	JX2, pin 56	Bank 35, H18	IO_L14N_T2_AD4N_SRCC_35
LA18_P_CC	JX2, pin 54	Bank 35, J18	IO_L14P_T2_AD4P_SRCC_35
LA19_N	JX2, pin 25	Bank 35, D18	IO_L3N_T0_DQS_AD1N_35
LA19_P	JX2, pin 23	Bank 35, E17	IO_L3P_T0_DQS_AD1P_35
LA20_N	JX2, pin 26	Bank 35, D20	IO_L4N_T0_35
LA20_P	JX2, pin 24	Bank 35, D19	IO_L4P_T0_35
LA21_N	JX2, pin 31	Bank 35, E19	IO_L5N_T0_AD9N_35
LA21_P	JX2, pin 29	Bank 35, E18	IO_L5P_T0_AD9P_35
LA22_N	JX2, pin 32	Bank 35, F17	IO_L6N_T0_VREF_35
LA22_P	JX2, pin 30	Bank 35, F16	IO_L6P_T0_35
LA23_N	JX2, pin 37	Bank 35, L20	IO_L7N_T1_AD2N_35
LA23_P	JX2, pin 35	Bank 35, L19	IO_L7P_T1_AD2P_35
LA24_N	JX2, pin 38	Bank 35, M20	IO_L8N_T1_AD10N_35
LA24_P	JX2, pin 36	Bank 35, M19	IO_L8P_T1_AD10P_35
LA25_N	JX2, pin 43	Bank 35, M18	IO_L9N_T1_DQS_AD3N_35
LA25_P	JX2, pin 41	Bank 35, M17	IO_L9P_T1_DQS_AD3P_35
LA26_N	JX2, pin 44	Bank 35, J19	IO_L10N_T1_AD11N_35
LA26_P	JX2, pin 42	Bank 35, K19	IO_L10P_T1_AD11P_35
LA27_N	JX2, pin 63	Bank 35, G18	IO_L16N_T2_35
LA27_P	JX2, pin 61	Bank 35, G17	IO_L16P_T2_35
LA28_N	JX2, pin 64	Bank 35, F20	IO_L15N_T2_DQS_AD12N_35
LA28_P	JX2, pin 62	Bank 35, F19	IO_L15P_T2_DQS_AD12P_35
LA29_N	JX2, pin 70	Bank 35, H20	IO_L17P_T2_AD5P_35
LA29_P	JX2, pin 68	Bank 35, J20	IO_L17N_T2_AD5N_35
LA30_N	JX2, pin 75	Bank 35, J14	IO_L20N_T3_AD6N_35
LA30_P	JX2, pin 73	Bank 35, K14	IO_L20P_T3_AD6P_35
LA31_N	JX2, pin 76	Bank 35, G15	IO_L19N_T3_VREF_35
LA31_P	JX2, pin 74	Bank 35, H15	IO_L19P_T3_35
LA32_N	JX2, pin 83	Bank 35, N16	IO_L21N_T3_DQS_AD14N_35
LA32_P	JX2, pin 81	Bank 35, N15	IO_L21P_T3_DQS_AD14P_35
LA33_N	JX2, pin 84	Bank 35, L15	IO_L22N_T3_AD7N_35
LA33_P	JX2, pin 82	Bank 35, L14	IO_L22P_T3_AD7P_35

2.4.2 Digilent Pmod™ Compatible Expansion Headers (2x6)

The Carrier has 5 Digilent Pmod™ right angle 0.1" female sockets (2x6). These connections include eight user I/O plus an adjustable voltage derived from the VADJ power supply. The VADJ power supply is jumper selectable to provide 1.8V, 2.5V or 3.3V. When 3.3V is selected, the electrical connection becomes Pmod™ compliant. All Pmod™ connections with the exception of the PS Pmod™ are matched differential Pmod™ connections and are routed differentially within the connector and with reference to one another to ensure high speed signal integrity.

- The Digilent Pmod™ compatible interface connects to Zynq banks 500, 34, 35 and 13. Bank 13 is only available on the 7Z020 version MicroZed.
- The PS Pmod attached to bank 500 can be used for PJTAG access (MIO[10-13]) as well as utilizing nine other hardened MIO peripherals (SPI, GPIO, CAN, I2C, UART, SD, QSPI, Trace, Watchdog). **NOTE:** The PS Pmod™ is also accessible on the MicroZed. Only one PS Pmod connection should be made at any given time.
- 7Z020 MicroZed only: Pmods™, JY and JZ, are sourced by Bank 13 and thus only available when MicroZed is populated with a 7Z020 device. Pmod™ JZ only has 7 pin connections, thus this Pmod™ interface cannot interface to QSPI or SD interface per the Digilent Pmod™ specification.



**Figure 7 – Digilent Pmod™ Compatible Interface Connections
when VCCIO_34/35 is set to 3.3V**

Table 11 – Digilent Pmod™ Compatible Interface Connections on PL I/Os

Pmod™	Carrier Net Name	Pmod Pin Number	MicroHeader Connection	Zynq AP SoC Connection
JA Pmod™	JA0-1 P	Pin 1	JX2, pin 47	Bank 35, L16
	JA0-1 N	Pin 2	JX2, pin 49	Bank 35, L17
	JA2-3 P	Pin 3	JX2, pin 13	Bank 35, G14
	JA2-3 N	Pin 4	JX2, pin 14	Bank 35, J15
	JA4-5 P	Pin 7	JX2, pin 18	Bank 35, B19
	JA4-5 N	Pin 8	JX2, pin 20	Bank 35, A20
	JA6-7 P	Pin 9	JX2, pin 17	Bank 35, C20
	JA6-7 N	Pin 10	JX2, pin 19	Bank 35, B20
JB Pmod™	JB0-1 P	Pin 1	JX1, pin 11	Bank 34, T11
	JB0-1 N	Pin 2	JX1, pin 13	Bank 34, T10
	JB2-3 P	Pin 3	JX1, pin 12	Bank 34, T12
	JB2-3 N	Pin 4	JX1, pin 14	Bank 34, U12
	JB4-5 P	Pin 7	JX1, pin 18	Bank 34, V12
	JB4-5 N	Pin 8	JX1, pin 20	Bank 34, W13
	JB6-7 P	Pin 9	JX1, pin 23	Bank 34, T14
	JB6-7 N	Pin 10	JX1, pin 25	Bank 34, T15
JY Pmod™ (7Z020 only)	JY0-1 P	Pin 1	JX1, pin 87	Bank 13, U7
	JY0-1 N	Pin 2	JX1, pin 89	Bank 13, V7
	JY2-3 P	Pin 3	JX1, pin 88	Bank 13, T9
	JY2-3 N	Pin 4	JX1, pin 90	Bank 13, U10
	JY4-5 P	Pin 7	JX1, pin 91	Bank 13, V8
	JY4-5 N	Pin 8	JX1, pin 93	Bank 13, W8
	JY6-7 P	Pin 9	JX1, pin 92	Bank 13, T5
	JY6-7 N	Pin 10	JX1, pin 94	Bank 13, U5
JZ Pmod™ (7Z020 only)	JZ0-1 P	Pin 1	JX2, pin 93	Bank 13, Y12
	JZ0-1 N	Pin 2	JX2, pin 95	Bank 13, Y13
	JZ2-3 P	Pin 3	JX2, pin 94	Bank 13, V11
	JZ2-3 N	Pin 4	JX2, pin 96	Bank 13, V10
	--	Pin 7	N/C	--
	JZ5	Pin 8	JX2, pin 100	Bank 13, V5
	JZ6-7 P	Pin 9	JX2, pin 97	Bank 13, V6
	JZ6-7 N	Pin 10	JX2, pin 99	Bank 13, W6

Table 12 – Digilent Pmod™ Compatible Interface Connections on PS I/Os

Pmod™	Carrier Net Name	Pmod Pin Number	MIO #	MicroHeader Connection	Zynq AP SoC Connection
PS Pmod™	PMOD_D0	Pin 1	MIO13	JX2, pin 1	Bank 500, E8
	PMOD_D1	Pin 2	MIO10	JX2, pin 2	Bank 500, E9
	PMOD_D2	Pin 3	MIO11	JX2, pin 3	Bank 500, C6
	PMOD_D3	Pin 4	MIO12	JX2, pin 4	Bank 500, D9
	PMOD_D4	Pin 7	MIO0	JX2, pin 5	Bank 500, E6
	PMOD_D5	Pin 8	MIO9	JX2, pin 6	Bank 500, B5
	PMOD_D6	Pin 9	MIO14	JX2, pin 7	Bank 500, C5
	PMOD_D7	Pin 10	MIO15	JX2, pin 8	Bank 500, C8

2.4.3 JX1 and JX2 MicroZed interface microheaders

The Carrier features two MicroHeaders, FCI PN: FCI_61083-101400LF Plugs for connection to MicroZed (which has the mating 61082 Receptacle). The total stack height for the mated pair is 5.00mm. For more information, see <http://www.em.avnet.com/avnetsomconnectors>

Each connector interfaces to Zynq PL I/O as well as eight PS- MIO, and four dedicated JTAG signals.

***NOTE:** the eight PS-MIO and four JTAG signals are shared on MicroZed, thus for each interface, it can only be used on either MicroZed or the Carrier, not simultaneously.

- The connectors are FCI BERGSTAK 0.8mm pitch Plugs. This family has variable stack heights from 5mm to 16mm, making it easy to connect to a variety of expansion or system boards. The default stack height for MicroZed (using the FCI 61082-101400LF Receptacle) and the MicroZed FMC Carrier (using the FCI 61083-101400LF Plug) results in a mated stack height of 5.00mm.
- Each connector has 100 pins which include I/O, analog signals, as well as power and ground. The Carrier powers the MicroZed as an alternative to the USB-UART. Each pin can carry 500mA of current and has been tested and certified against PCIe Gen2, thus sufficient bandwidth for this interface.
- MicroZed does not power the PL VCC_{IO} banks, this is required by the Carrier through the VADJ regulator. This gives the Carrier the flexibility to control the I/O bank voltages. The 7Z010 has two PL I/O banks, banks 34 and 35, each containing 50 I/O.
- The 7Z020 has a third I/O bank, bank 13, which is powered on the FMC-CC by VADJ.
- Within a PL I/O bank, there are 50 I/O capable of 24 differential pairs. Differential LVDS pairs on a -1 speed grade device are capable of 950Mbps of DDR data. Each differential pair is isolated by a power or ground pin. Additionally, eight of these I/O can be connected as clock inputs (four MRCC and four SRCC inputs).
- Each PL bank can also be configured to be a memory interface with up to four dedicated DQS data strobes and data byte groups. Bank 35 adds the capability to use the I/O to interface up to 16 differential analog inputs. One of the differential pairs in Bank 34 is not used as one of the pins is shared with PUDC_B.
- The MicroZed with the Zynq 7Z020 populated has bank 13. While the bank has 25 I/Os, only 15 of these signals are routed to the MicroHeader due to the header's pin limitations.

2.4.3.1 MicroHeader pinout assignments

Complete pin tables for JX1 and JX2 are contained in Appendix – JX1 Pin Table and Appendix – JX2 Pin Table.

Table 13 – MicroHeader Pinout

MicroHeader #1				MicroHeader #2					
Signal Name		Source	Pin Count	Signal Name		Source	Pin Count		
PL	All Bank 34 Pins except PUDC_B (below)	Zynq Bank 34	49	PL	All Bank 35 Pins	Zynq Bank 35	50		
JTAG	TMS_0	Zynq Bank 0	5	PS	PS Pmod MIO[0,9-15]	Zynq Bank 500	8		
	TDI_0	Zynq Bank 0			C	Init_B_0	Zynq Bank 0	2	
	TCK_0	Zynq Bank 0		Program_B_0		Zynq Bank 0			
	TDO_0	Zynq Bank 0		PG_Module	Module	1			
	Carrier_SRST#	Carrier		Power	5V	Carrier	28		
Analog	VP_0	Zynq Bank 0	4		GND	Carrier			
	VN_0	Zynq Bank 0			VCCO_35	Carrier	3		
	DXP_0	Zynq Bank 0			Bank 13 pins	Bank 13 **	8		
	DXN_0	Zynq Bank 0			Total		10		
C	PUDC_B	Zynq Bank 34	2						
	DONE	Zynq Bank 0							
Power	PWR_Enable	Carrier	1						
	Power	Carrier	28						
	GND	Carrier							
	VCCO_34	Carrier	3						
	Bank 13 pins	Bank 13 **	8						
TOTAL			100						

** 7020 device only

2.4.3.2 Layout Routing Guidelines

- The signals for each header follow FMC routing tolerances and guidelines. Each of the P/N pairs have 50Ω single-ended impedance (100Ω differential) with less than 10 mil skew between all P/N pairs on each header.
- There is less than 100 mil length skew across all bits in a bus or byte group, including DQ and DQS pins in each bank.

2.5 JTAG Configuration

The Carrier provides a traditional Platform Cable JTAG connector for use with Xilinx Platform Cables and Digilent JTAG HS1 or HS2 Programming Cables. When a MicroZed is plugged onto the Carrier, the Carrier's JTAG connector MUST be used. The JTAG connector on-board the MicroZed SOM will no longer function.

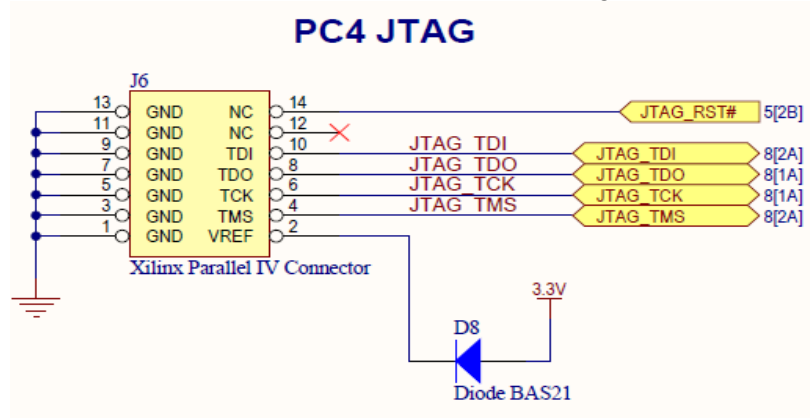


Figure 8 – JTAG Connections

The Carrier has a 3-pin jumper (J1) connected to PUDC. Default jumper placed at location 1-2, pulling the signal up to VADJ. At location 2-3, the signal is pulled low. PUDC may also be used as a User I/O, with caution regarding the pull-down.

Table 14 – PUDC B Connections

Carrier Net Name	MicroHeader Connection	Zynq AP SoC Connection	Zynq AP SoC Pin
PUDC#	JX1, pin 17	Bank 34, U13	IO_L3P_T0_DQS_PUDC_B_34

A blue DONE LED (LED5) is connected to Zynq through the MicroHeader. When the PL is properly configured, the DONE LED will light.

Table 15 – Done Connections

Carrier Net Name	MicroHeader Connection	Zynq AP SoC Connection	Zynq AP SoC Pin
FPGA_DONE	JX1, pin 8	Bank 0, R11	DONE_0

2.6 Power

2.6.1 Power Input

The board input voltage is through a 12V 2x3 6 pin connector. The current rating of the power supply is determined by the expected power requirements of the interfaced design.

The precise current demand is based on the end-use I/O requirements and therefore the application will determine the minimum current a power supply must source. As shipped from Avnet, a 12V, 5.0 Amp 2x3 power supply is provided in the kit. More information about this supply is available at the following links:

<http://www.em.avnet.com/12Vpower/AES-SLP-12V5A-G>

- Input Adapter:
 - Primary 12V 5A, 2x3 connector.
 - Note this connector is NOT ATX compatible.
- On Board:
 - High-efficiency regulator for 5.0V @ 3A
 - For MicroZed SOM module
 - High-efficiency regulator for 3.3V @ 3A
 - For FMC connection
 - High-efficiency regulator VADJ. for 1.8V/2.5V/3.3V @ 4A
 - For Module VCC_{IO} Bank_34, Bank_35, and Bank_13 and FMC

2.6.2 Voltage Regulators

The following table lists the power solution for the FMC Carrier Card. VADJ rail is independent and adjustable supplying power to the Zynq PL I/O banks and connected Pmods™. VADJ drives banks 34, 35 and 13 (if 7Z020 is populated on MicroZed) as well as the 5 Pmod™ connectors.

The table below shows the minimum required voltage rails, currents, and tolerances.

Table 16 – Voltage Rails w/ Current Estimates

Voltage (V)	7Z010 Current	7Z020 Current	Tolerance	IC	Notes
12V Input	N/A	N/A	10%	Wall adapter, NOT ATX compatible	5.0A
5V (Main)	N/A	N/A	5%	REG1, MAX15066	3A capable. JX.x uZ headers
VADJ (VCC _{IO} _13, 34,35) – 1.8V, 2.5V or 3.3V	<2.0A @ 3.3V	2.85A @ 3.3V	5%	REG3, MAX15066	4A capable
3.3V Main	N/A	N/A	5%	REG5, MAX15066	3A capable

2.6.3 Sequencing

- PWR_EN signal, active high, JX1.5, allows the carrier to turn on or off the MicroZed power supplies. R74 and C106 have been placed to adjust the timing of this signal during power off conditions. This signal should not be de-asserted until VCCIO_EN is de-asserted. In the carrier off condition (power plug removed or power switch turned off), this signal is driven low.
- VCCIO_EN signal, active high, JX2.10, originates on the microZed and is the output of the 1.8V regulator, PG_1V8. This signal enables the carrier's 3.3V supply, which in turn enables the VADJ regulator. When the carrier is turned off (power switch turned off or power plug removed) or the MicroZed's PG_1V8 signal is de-asserted VCCI_EN is driven low, which turns off the FMC-CC and the MicroZed.
- PG_CARRIER signal, active high, JX2.11, is pulled up by MicroZed's +3.3V PG_MODULE signal. This signal can be pulled low by the carrier board (SW4), the FMC board or the MicroZed when the board's power circuitry is not 'Good' yet.
- The following diagram illustrates the power supply sequencing on power up. Note Vin and PWR_Enable can come up simultaneously, but shown staggered as PWR_Enable can come up later.

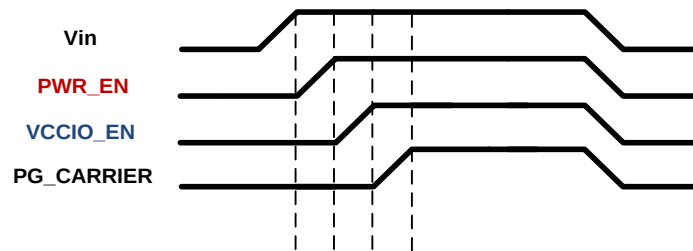


Figure 9 – Power Sequencing

The PG_CARRIER (on FMC-CC) and PG_MODULE (on MicroZed) signals are wired OR and tied to the Zynq Power On Reset signal. When the power supplies are valid on both the SOM and carrier, the PG signal de-asserts the Zynq POR signal.

2.6.4 Bypassing/Decoupling

The FMC-CC follows the recommended decoupling techniques per each manufacturer's datasheet.

2.6.5 System Power Good LED

A green status LED (LED6) indicates when PG_CARRIER signal is high (good).

2.7 Jumpers, configuration and test points:

The below table is a quick reference to all of the jumpers, configuration settings and test points on the FMC. For detailed information, refer to the appropriate sections in this document.

Table 17 – Jumpers, Switches, and Test Points

Reference Designator	Name	Default	Notes:
J1	PUDC#	Short 1-2 (disabled)	Power Up During Configuration when pulled low. Default is pulled high to VADJ.
J2	JTAG	Populated	Zynq JTAG interface.
J3	VBAT	Not Populated	JX1 pin 7. Zynq pin F11. +1.8V for SoC battery support. NOTE: If using VBAT, the SOM's VBAT resistor must be removed! Please see the MicroZed User Guide.
J4	FMC GA [1:0]	Set to 00	FMC address select. Use jumper headers for selection.
J5	PG_CARRIER	Not Populated	Used to test the on-board power supplies without a MicroZed inserted.
J6	VADJ Voltage Selection	1.8V Short 5-6	Jumper to set VADJ to 3.3V (1-2), 2.5V (3-4), or 1.8V (5-6). If not jumper is present, VADJ is set to 3.3V.
J7	VCCIO_EN	Not Populated	Used to test the on-board power supplies without a MicroZed inserted.
SW1	CARRIER_SRST#	Open	Active low SoC PS reset. Interfaced with JTAG J2.
SW2	INIT#	Open	Active low initialization signal. Rarely used.
SW3	PWR	Open	Applies 12V power to board. When off, disables PWR_EN & VCCIO_EN on MicroZed SOM.
SW4	PG_CARRIER	Open	Asserts open drain signal PG_CARRIER low, which initiates a Zynq POR# on MicroZed.
TP1	CARRIER_SRST#	N/A	Signal monitor test point
TP2-5	GND	N/A	Power supply ground
TP6	+5V	N/A	+5V test point
TP8	+3V3	N/A	+3.3V test point
TP11	+VADJ	N/A	+VADJ test point
CON4	+12Vin	N/A	+12V input
CON5	FAN Power	12V	Fan header connector. Selectable voltage via R39 or R42. Default is R39 placed (12V fan).
BTN1-2	PB0, PB1	Open	2 user input pushbuttons to the Zynq PL fabric. Pulled low, active high with VADJ voltage setting when pressed.

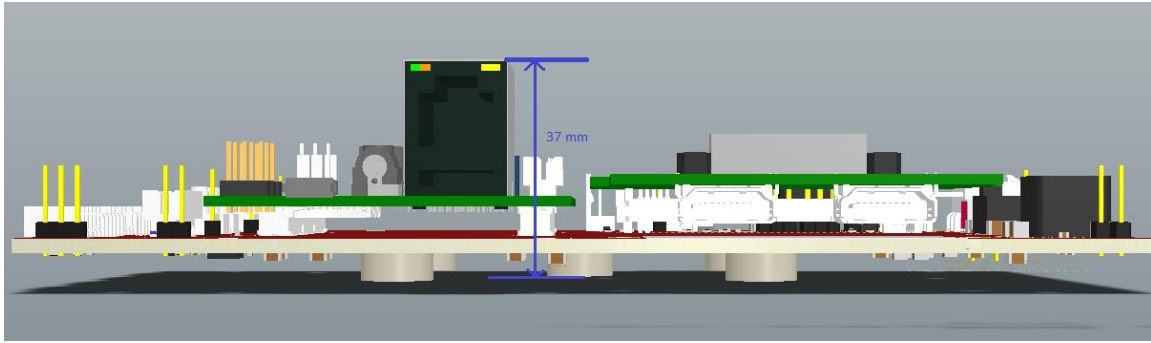


Figure 11: FMC+MicroZed Vertical Mechanical Dimensions 37.00 mm

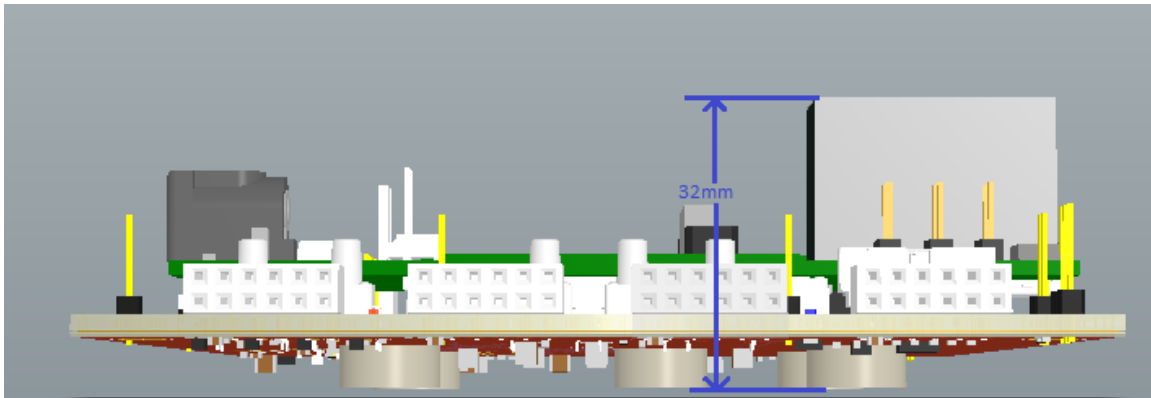


Figure 12 – MicroZed total height from bumper bottom to Ethernet top – 32.00 mm

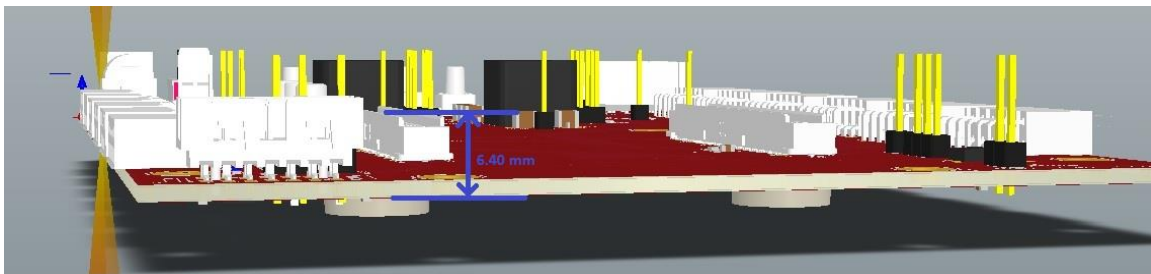


Figure 13 – FMC only bottom of PCB to top of JX.x connector – 6.40 mm

3.2 Weight:

The weight of the FMC-CC with rubber feet and all jumpers populated is 116 grams/ 4.01917 ounces.

4 Revision History

Rev date	Rev #	Reason for change
25 Feb 2014	1.0	Initial release
06 Nov 2015	1.1	Corrected pin errors in tables. Added JX pin tables to Appendix.

5 Appendix – JX1 Pin Table

Table 18 – JX1 Pin Table

JX1 Pin	MZCC-FMC Net Name	MicroZed Net Name	Zynq Pin	Zynq Name	VCCO Bank
1	JTAG_UZ_TCK	JTAG_TCK	F9	TCK_0	-1
2	JTAG_UZ_TMS	JTAG_TMS	J6	TMS_0	-1
3	JTAG_UZ_TDO	JTAG_TDO	F6	TDO_0	-1
4	JTAG_TDI	JTAG_TDI	G6	TDI_0	-1
5	PWR_EN	NetJX1_5	#N/A	#N/A	#N/A
6	CARRIER_SRST#	NetJX1_6	#N/A	#N/A	#N/A
7	VBAT	FPGA_VBATT	F11	VCCBATT_0	-1
8	FPGA_DONE	FPGA_DONE	R11	DONE_0	-1
9	LED0	JX1_SE_0	R19	IO_0_34	34
10	EEPROM	JX1_SE_1	T19	IO_25_34	34
11	JB0-1_P	JX1_LVDS_0_P	T11	IO_L1P_T0_34	34
12	JB2-3_P	JX1_LVDS_1_P	T12	IO_L2P_T0_34	34
13	JB0-1_N	JX1_LVDS_0_N	T10	IO_L1N_T0_34	34
14	JB2-3_N	JX1_LVDS_1_N	U12	IO_L2N_T0_34	34
15	GND	GND	A8	GND	-1
16	GND	GND	A8	GND	-1
17	PUDC#	JX1_LVDS_2_P	U13	IO_L3P_T0_DQS_PUDC_B_34	34
18	JB4-5_P	JX1_LVDS_3_P	V12	IO_L4P_T0_34	34
19	LED1	JX1_LVDS_2_N	V13	IO_L3N_T0_DQS_34	34
20	JB4-5_N	JX1_LVDS_3_N	W13	IO_L4N_T0_34	34
21	GND	GND	A8	GND	-1
22	GND	GND	A8	GND	-1
23	JB6-7_P	JX1_LVDS_4_P	T14	IO_L5P_T0_34	34
24	LA02_P	JX1_LVDS_5_P	P14	IO_L6P_T0_34	34
25	JB6-7_N	JX1_LVDS_4_N	T15	IO_L5N_T0_34	34
26	LA02_N	JX1_LVDS_5_N	R14	IO_L6N_T0_VREF_34	34
27	GND	GND	A8	GND	-1
28	GND	GND	A8	GND	-1
29	LA03_P	JX1_LVDS_6_P	Y16	IO_L7P_T1_34	34
30	LA04_P	JX1_LVDS_7_P	W14	IO_L8P_T1_34	34
31	LA03_N	JX1_LVDS_6_N	Y17	IO_L7N_T1_34	34
32	LA04_N	JX1_LVDS_7_N	Y14	IO_L8N_T1_34	34
33	GND	GND	A8	GND	-1
34	GND	GND	A8	GND	-1
35	LA05_P	JX1_LVDS_8_P	T16	IO_L9P_T1_DQS_34	34
36	LA06_P	JX1_LVDS_9_P	V15	IO_L10P_T1_34	34
37	LA05_N	JX1_LVDS_8_N	U17	IO_L9N_T1_DQS_34	34

38	LA06_N	JX1_LVDS_9_N	W15	IO_L10N_T1_34	34
39	GND	GND	A8	GND	-1
40	GND	GND	A8	GND	-1
41	LA07_P	JX1_LVDS_10_P	U14	IO_L11P_T1_SRCC_34	34
42	CLK0_M2C_P	JX1_LVDS_11_P	U18	IO_L12P_T1_MRCC_34	34
43	LA07_N	JX1_LVDS_10_N	U15	IO_L11N_T1_SRCC_34	34
44	CLK0_M2C_N	JX1_LVDS_11_N	U19	IO_L12N_T1_MRCC_34	34
45	GND	GND	A8	GND	-1
46	GND	GND	A8	GND	-1
47	LA00_CC_P	JX1_LVDS_12_P	N18	IO_L13P_T2_MRCC_34	34
48	LA01_CC_P	JX1_LVDS_13_P	N20	IO_L14P_T2_SRCC_34	34
49	LA00_CC_N	JX1_LVDS_12_N	P19	IO_L13N_T2_MRCC_34	34
50	LA01_CC_N	JX1_LVDS_13_N	P20	IO_L14N_T2_SRCC_34	34
51	GND	GND	A8	GND	-1
52	GND	GND	A8	GND	-1
53	LA08_P	JX1_LVDS_14_P	T20	IO_L15P_T2_DQS_34	34
54	LA09_P	JX1_LVDS_15_P	V20	IO_L16P_T2_34	34
55	LA08_N	JX1_LVDS_14_N	U20	IO_L15N_T2_DQS_34	34
56	LA09_N	JX1_LVDS_15_N	W20	IO_L16N_T2_34	34
57	5V	VIN_HDR	#N/A	#N/A	#N/A
58	5V	VIN_HDR	#N/A	#N/A	#N/A
59	5V	VIN_HDR	#N/A	#N/A	#N/A
60	5V	VIN_HDR	#N/A	#N/A	#N/A
61	LA10_P	JX1_LVDS_16_P	Y18	IO_L17P_T2_34	34
62	LA11_P	JX1_LVDS_17_P	V16	IO_L18P_T2_34	34
63	LA10_N	JX1_LVDS_16_N	Y19	IO_L17N_T2_34	34
64	LA11_N	JX1_LVDS_17_N	W16	IO_L18N_T2_34	34
65	GND	GND	A8	GND	-1
66	GND	GND	A8	GND	-1
67	LA12_P	JX1_LVDS_18_P	R16	IO_L19P_T3_34	34
68	LA13_P	JX1_LVDS_19_P	T17	IO_L20P_T3_34	34
69	LA12_N	JX1_LVDS_18_N	R17	IO_L19N_T3_VREF_34	34
70	LA13_N	JX1_LVDS_19_N	R18	IO_L20N_T3_34	34
71	GND	GND	A8	GND	-1
72	GND	GND	A8	GND	-1
73	LA14_P	JX1_LVDS_20_P	V17	IO_L21P_T3_DQS_34	34
74	LA15_P	JX1_LVDS_21_P	W18	IO_L22P_T3_34	34
75	LA14_N	JX1_LVDS_20_N	V18	IO_L21N_T3_DQS_34	34
76	LA15_N	JX1_LVDS_21_N	W19	IO_L22N_T3_34	34
77	GND	GND	A8	GND	-1
78	VADJ	VCCO_34	N19	VCCO_34	34
79	VADJ	VCCO_34	N19	VCCO_34	34

80	VADJ	VCCO_34	N19	VCCO_34	34
81	LA16_P	JX1_LVDS_22_P	N17	IO_L23P_T3_34	34
82	FMC_SDA	JX1_LVDS_23_P	P15	IO_L24P_T3_34	34
83	LA16_N	JX1_LVDS_22_N	P18	IO_L23N_T3_34	34
84	FMC_SCL	JX1_LVDS_23_N	P16	IO_L24N_T3_34	34
85	GND	GND	A8	GND	-1
86	GND	GND	A8	GND	-1
87	JY0-1_P	BANK13_LVDS_0_P	U7	IO_L11P_T1_SRCC_13	13
88	JY2-3_P	BANK13_LVDS_1_P	T9	IO_L12P_T1_MRCC_13	13
89	JY0-1_N	BANK13_LVDS_0_N	V7	IO_L11N_T1_SRCC_13	13
90	JY2-3_N	BANK13_LVDS_1_N	U10	IO_L12N_T1_MRCC_13	13
91	JY4-5_P	BANK13_LVDS_2_P	V8	IO_L15P_T2_DQS_13	13
92	JY6-7_P	BANK13_LVDS_3_P	T5	IO_L19P_T3_13	13
93	JY4-5_N	BANK13_LVDS_2_N	W8	IO_L15N_T2_DQS_13	13
94	JY6-7_N	BANK13_LVDS_3_N	U5	IO_L19N_T3_VREF_13	13
95	GND	GND	A8	GND	-1
96	GND	GND	A8	GND	-1
97	NetJX1_97	NetJX1_97	K9	VP_0	0
98	NetJX1_98	NetJX1_98	M9	DXP_0	-1
99	NetJX1_99	NetJX1_99	L10	VN_0	0
100	NetJX1_100	NetJX1_100	M10	DXN_0	-1

6 Appendix – JX2 Pin Table

Table 19 – JX2 Pin Table

JX2 Pin	MZCC-FMC Net Name	MicroZed Net Name	Zynq Pin	Zynq Name	VCCO Bank
1	PMOD_D0	PMOD_D0	E8	PS_MIO13_500	-1
2	PMOD_D1	PMOD_D1	E9	PS_MIO10_500	-1
3	PMOD_D2	PMOD_D2	C6	PS_MIO11_500	-1
4	PMOD_D3	PMOD_D3	D9	PS_MIO12_500	-1
5	PMOD_D4	PMOD_D4	E6	PS_MIO0_500	-1
6	PMOD_D5	PMOD_D5	B5	PS_MIO9_500	-1
7	PMOD_D6	PMOD_D6	C5	PS_MIO14_500	-1
8	PMOD_D7	PMOD_D7	C8	PS_MIO15_500	-1
9	INIT#	NetJX2_9	R10	INIT_B_0	-1
10	VCCIO_EN	NetJX2_10	L6	PROGRAM_B_0	-1
11	PG_CARRIER	PG_MODULE	C7	PS_POR_B_500	-1
12	5V	VIN_HDR	#N/A	#N/A	#N/A
13	JA2	JX2_SE_0	G14	IO_0_35	35
14	JA3	JX2_SE_1	J15	IO_25_35	35
15	GND	GND	A8	GND	-1
16	GND	GND	A8	GND	-1
17	JA6-7_P	JX2_LVDS_0_P	C20	IO_L1P_T0_AD0P_35	35
18	JA4-5_P	JX2_LVDS_1_P	B19	IO_L2P_T0_AD8P_35	35
19	JA6-7_N	JX2_LVDS_0_N	B20	IO_L1N_T0_AD0N_35	35
20	JA4-5_N	JX2_LVDS_1_N	A20	IO_L2N_T0_AD8N_35	35
21	GND	GND	A8	GND	-1
22	GND	GND	A8	GND	-1
23	LA19_P	JX2_LVDS_2_P	E17	IO_L3P_T0_DQS_AD1P_35	35
24	LA20_P	JX2_LVDS_3_P	D19	IO_L4P_T0_35	35
25	LA19_N	JX2_LVDS_2_N	D18	IO_L3N_T0_DQS_AD1N_35	35
26	LA20_N	JX2_LVDS_3_N	D20	IO_L4N_T0_35	35
27	GND	GND	A8	GND	-1
28	GND	GND	A8	GND	-1
29	LA21_P	JX2_LVDS_4_P	E18	IO_L5P_T0_AD9P_35	35
30	LA22_P	JX2_LVDS_5_P	F16	IO_L6P_T0_35	35
31	LA21_N	JX2_LVDS_4_N	E19	IO_L5N_T0_AD9N_35	35
32	LA22_N	JX2_LVDS_5_N	F17	IO_L6N_T0_VREF_35	35
33	GND	GND	A8	GND	-1
34	GND	GND	A8	GND	-1
35	LA23_P	JX2_LVDS_6_P	L19	IO_L9P_T1_DQS_AD3P_35	35
36	LA24_P	JX2_LVDS_7_P	M19	IO_L7P_T1_AD2P_35	35

37	LA23_N	JX2_LVDS_6_N	L20	IO_L9N_T1_DQS_AD3N_35	35
38	LA24_N	JX2_LVDS_7_N	M20	IO_L7N_T1_AD2N_35	35
39	GND	GND	A8	GND	-1
40	GND	GND	A8	GND	-1
41	LA25_P	JX2_LVDS_8_P	M17	IO_L8P_T1_AD10P_35	35
42	LA26_P	JX2_LVDS_9_P	K19	IO_L10P_T1_AD11P_35	35
43	LA25_N	JX2_LVDS_8_N	M18	IO_L8N_T1_AD10N_35	35
44	LA26_N	JX2_LVDS_9_N	J19	IO_L10N_T1_AD11N_35	35
45	GND	GND	A8	GND	-1
46	GND	GND	A8	GND	-1
47	JA0-1_P	JX2_LVDS_10_P	L16	IO_L11P_T1_SRCC_35	35
48	CLK1_M2C_P	JX2_LVDS_11_P	K17	IO_L12P_T1_MRCC_35	35
49	JA0-1_N	JX2_LVDS_10_N	L17	IO_L11N_T1_SRCC_35	35
50	CLK1_M2C_N	JX2_LVDS_11_N	K18	IO_L12N_T1_MRCC_35	35
51	GND	GND	A8	GND	-1
52	GND	GND	A8	GND	-1
53	LA17_CC_P	JX2_LVDS_12_P	H16	IO_L13P_T2_MRCC_35	35
54	LA18_CC_P	JX2_LVDS_13_P	J18	IO_L14P_T2_AD4P_SRCC_35	35
55	LA17_CC_N	JX2_LVDS_12_N	H17	IO_L13N_T2_MRCC_35	35
56	LA18_CC_N	JX2_LVDS_13_N	H18	IO_L14N_T2_AD4N_SRCC_35	35
57	5V	VIN_HDR	#N/A	#N/A	#N/A
58	5V	VIN_HDR	#N/A	#N/A	#N/A
59	5V	VIN_HDR	#N/A	#N/A	#N/A
60	5V	VIN_HDR	#N/A	#N/A	#N/A
61	LA27_P	JX2_LVDS_14_P	G17	IO_L16P_T2_35	35
62	LA28_P	JX2_LVDS_15_P	F19	IO_L15P_T2_DQS_AD12P_35	35
63	LA27_N	JX2_LVDS_14_N	G18	IO_L16N_T2_35	35
64	LA28_N	JX2_LVDS_15_N	F20	IO_L15N_T2_DQS_AD12N_35	35
65	GND	GND	A8	GND	-1
66	GND	GND	A8	GND	-1
67	PB0	JX2_LVDS_16_P	G19	IO_L18P_T2_AD13P_35	35
68	LA29_P	JX2_LVDS_17_P	J20	IO_L17P_T2_AD5P_35	35
69	PB1	JX2_LVDS_16_N	G20	IO_L18N_T2_AD13N_35	35
70	LA29_N	JX2_LVDS_17_N	H20	IO_L17N_T2_AD5N_35	35
71	GND	GND	A8	GND	-1
72	GND	GND	A8	GND	-1
73	LA30_P	JX2_LVDS_18_P	K14	IO_L20P_T3_AD6P_35	35
74	LA31_P	JX2_LVDS_19_P	H15	IO_L19P_T3_35	35
75	LA30_N	JX2_LVDS_18_N	J14	IO_L20N_T3_AD6N_35	35
76	LA31_N	JX2_LVDS_19_N	G15	IO_L19N_T3_VREF_35	35
77	GND	GND	A8	GND	-1
78	VADJ	VCCO_35	C19	VCCO_35	35

79	VADJ	VCCO_35	C19	VCCO_35	35
80	VADJ	VCCO_35	C19	VCCO_35	35
81	LA32_P	JX2_LVDS_20_P	N15	IO_L21P_T3_DQS_AD14P_35	35
82	LA33_P	JX2_LVDS_21_P	L14	IO_L22P_T3_AD7P_35	35
83	LA32_N	JX2_LVDS_20_N	N16	IO_L21N_T3_DQS_AD14N_35	35
84	LA33_N	JX2_LVDS_21_N	L15	IO_L22N_T3_AD7N_35	35
85	GND	GND	A8	GND	-1
86	GND	GND	A8	GND	-1
87	FMC_PRSENT_L	JX2_LVDS_22_P	M14	IO_L23P_T3_35	35
88	LED2	JX2_LVDS_23_P	K16	IO_L24P_T3_AD15P_35	35
89	LED3	JX2_LVDS_22_N	M15	IO_L23N_T3_35	35
90	MAC_ID	JX2_LVDS_23_N	J16	IO_L24N_T3_AD15N_35	35
91	GND	GND	A8	GND	-1
92	GND	GND	A8	GND	-1
93	JZ0-1_P	BANK13_LVDS_4_P	Y12	IO_L20P_T3_13	13
94	JZ2-3_P	BANK13_LVDS_5_P	V11	IO_L21P_T3_DQS_13	13
95	JZ0-1_N	BANK13_LVDS_4_N	Y13	IO_L20N_T3_13	13
96	JZ2-3_N	BANK13_LVDS_5_N	V10	IO_L21N_T3_DQS_13	13
97	JZ6-7_P	BANK13_LVDS_6_P	V6	IO_L22P_T3_13	13
98	VADJ	VCCO_13	T8	VCCO_13	13
99	JZ6-7_N	BANK13_LVDS_6_N	W6	IO_L22N_T3_13	13
100	JZ5	BANK13_SE_0	V5	IO_L6N_T0_VREF_13	13