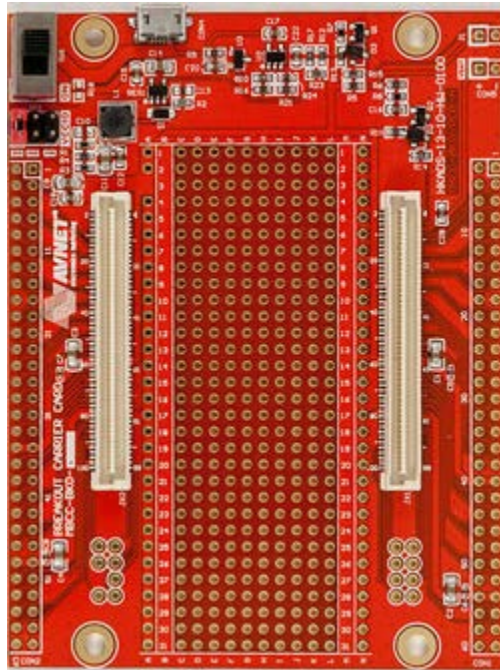


---

# MicroZed Breakout Carrier Card

Zynq™ System On Module  
Hardware User Guide



Revision 1.1  
15 May 2014

---

# Table of Contents

1	INTRODUCTION .....	2
1.1	ZYNQ BANK PIN ASSIGNMENTS.....	5
2	FUNCTIONAL DESCRIPTION.....	6
2.1	INTERFACE HEADERS .....	6
2.1.1	BKO Connector .....	6
2.1.2	Mounting Holes.....	10
2.1.3	JX1 and JX2 MicroZed interface microheaders .....	10
2.2	POWER .....	11
2.2.1	Power Input.....	11
2.2.2	Voltage Regulators .....	11
2.2.3	MicroZed Power Sequencing and control circuits.....	11
2.2.4	Bypassing/Decoupling .....	12
2.3	JUMPERS, CONFIGURATION AND TEST POINTS:.....	13
3	MECHANICAL.....	14
3.1	PROTOTYPE AREA.....	14
3.1.1	10x31 inert 0.1" pitch plated through hole field.....	14
3.1.2	Proto area +5V, +VCCIO and GND pins.....	14
3.2	DIMENSIONS: .....	14
3.3	WEIGHT:.....	15
4	REVISION HISTORY.....	15

# 1 Introduction

The MicroZed Breakout Carrier Card (BKO-CC) is a very low cost evaluation board for the MicroZed series System On Module (SOM) boards.

The function of this board is to provide SoC I/O pin accessibility to the MicroZed SOM board through two dual 2x30 pin connectors. In addition to SoC I/O pin access through the BKO-CC interface, the BKO-CC also provides SOM board power via the JX MicroHeaders. Please refer to the MicroZed Hardware User's guide for the MicroZed's feature set. The features provided by the BKO-CC consist of:

- Interfaces
  - Two 60 pin Dual Inline 0.100" pitch female sockets for JX1 and JX2 access.
    - **NOTE:** these connectors are shipped loose in the box to allow the customer to place as desired. They can be placed on the top side or bottom side of the BKO board.
  - Two 100-pin MicroHeaders (JX1, JX2) for MicroZed SOM insertion.
  - One slide switch for main power.
  - VCCIO EN jumper, J1, to test BKO power on
  - VBAT connection, CON5, for Zynq +1.5V battery back-up.
- Power
  - On Board, REG1
    - Jumper adjustable Regulator (VADJ) for  $1.8V/2.5V/3.3V \leq 2.0$  Amps.
      - For SOM Module VCC<sub>IO</sub> Bank\_34, Bank\_35, and Bank\_13.
  - Micro USB type B input connector, CON4
    - Primary +5V power input. Can be attached to end user PC or the supplied USB wall adapter power supply. The shipped power adapter is capable of sourcing a minimum of 2.0 Amps. This is a power-only connector – no USB communication is possible.

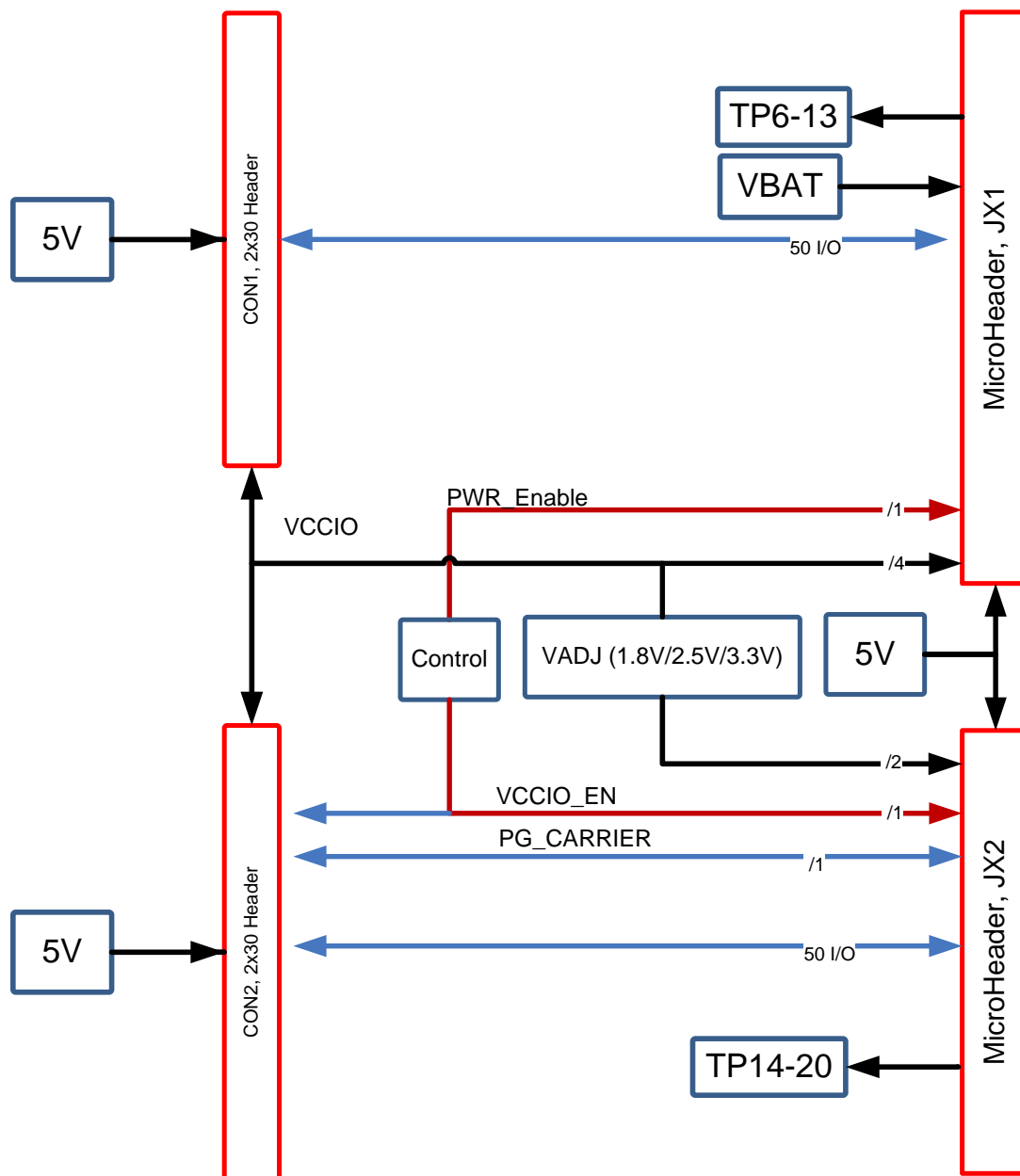
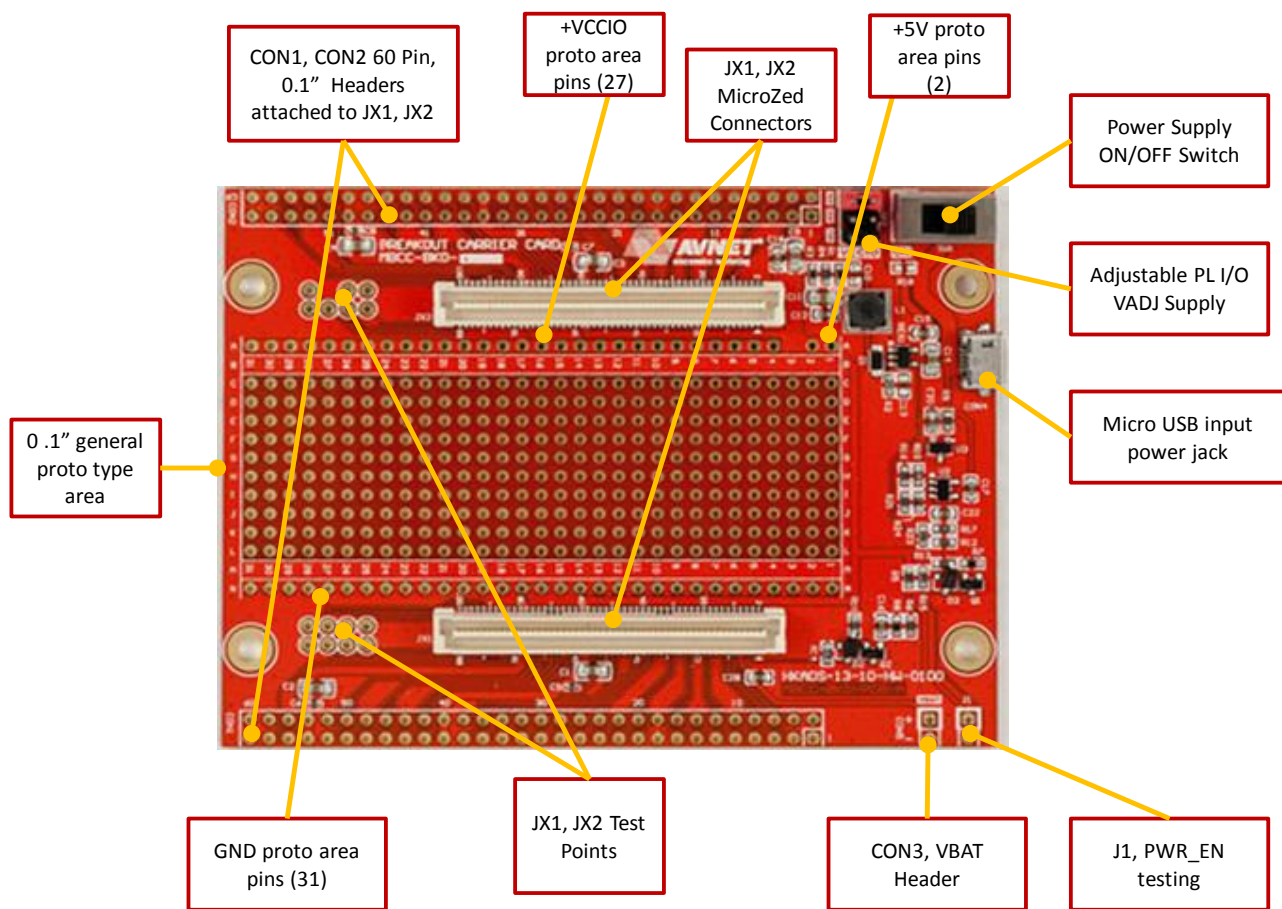


Figure 1 – MicroZed BKO Block Diagram



**Figure 2: BKO-CC Board Functions**

## 1.1 Zynq Bank Pin Assignments

The following figure shows the Zynq bank pin assignments on the MicroZed. See tables Table 1 – BKO JX1 Connections and Table 2 – BKO JX2 Connections **Error! Reference source not found.** Note that Bank 13 is not connected on the BKO-CC.

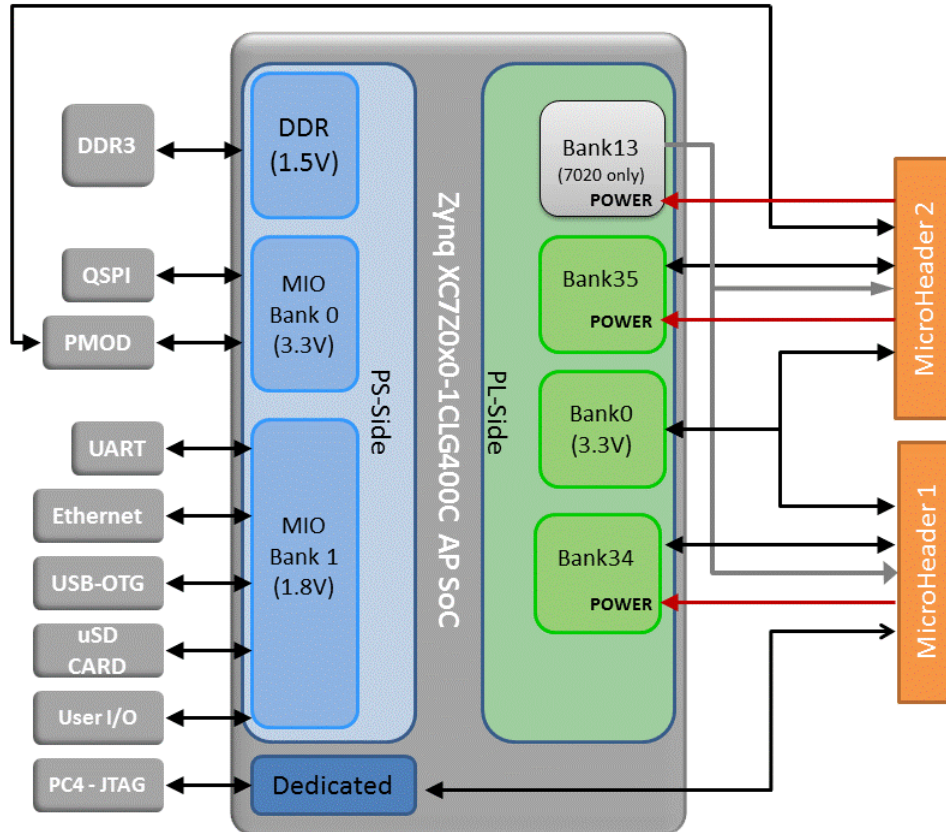


Figure 3 – Zynq CLG400 Bank Assignments

## 2 Functional Description

The BKO Carrier is an expansion board for MicroZed. The BKO-CC bridges Avnet's MicroZed 7Z010 or 7Z020 System On Module (SOM) PL I/Os to very simple, 0.1" footprints.

### 2.1 Interface Headers

#### 2.1.1 BKO Connector

A dual 2x30 socket is implemented on the BKO Carrier to support prototyping.

Table 1 – BKO JX1 Connections

Carrier Connection	Carrier Net Name	MicroHeader Connection	Zynq AP SoC Connection	Zynq AP SoC Pin Name
N/C	N/A	JX1, pin 1	--	--
N/C	N/A	JX1, pin 2	--	--
N/C	N/A	JX1, pin 3	--	--
N/C	N/A	JX1, pin 4	--	--
PWR_Enable	PWR_EN	JX1, pin 5	--	--
N/C	N/A	JX1, pin 6	--	--
CON5, pin 1	VBAT	JX1, pin 7	Bank 0, F11	FPGA_VBATT
N/C	N/A	JX1, pin 8	--	--
CON1, pin 3	IO_0_34	JX1, pin 9	Bank 34, R19	IO_0_34
CON1, pin 4	IO_25_34	JX1, pin 10	Bank 34, T19	IO_25_34
CON1, pin 5	IO_L1P_T0_34	JX1, pin 11	Bank 34, T11	IO_L1P_T0_34
CON1, pin 6	IO_L2P_T0_34	JX1, pin 12	Bank 34, T12	IO_L2P_T0_34
CON1, pin 7	IO_L1N_T0_34	JX1, pin 13	Bank 34, T10	IO_L1N_T0_34
CON1, pin 8	IO_L2N_T0_34	JX1, pin 14	Bank 34, U12	IO_L2N_T0_34
CON1: 1,2,17,18,59,60	GND	JX1, pin 15	GND	GND
CON1: 1,2,17,18,59,60	GND	JX1, pin 16	GND	GND
CON1, pin 9	IO_L3P_T0_34	JX1, pin 17	Bank 34, U13	IO_L3P_T0_34
CON1, pin 10	IO_L4P_T0_34	JX1, pin 18	Bank 34, V12	IO_L4P_T0_34
CON1, pin 11	IO_L3N_T0_34	JX1, pin 19	Bank 34, V13	IO_L3N_T0_34
CON1, pin 12	IO_L4N_T0_34	JX1, pin 20	Bank 34, W13	IO_L4N_T0_34
CON1: 1,2,17,18,59,60	GND	JX1, pin 21	GND	GND
CON1: 1,2,17,18,59,60	GND	JX1, pin 22	GND	GND
CON1, pin 13	IO_L5P_T0_34	JX1, pin 23	Bank 34, T14	IO_L5P_T0_34
CON1, pin 14	IO_L6P_T0_34	JX1, pin 24	Bank 34, P14	IO_L6P_T0_34
CON1, pin 15	IO_L5N_T0_34	JX1, pin 25	Bank 34, T15	IO_L5N_T0_34
CON1, pin 16	IO_L6N_T0_34	JX1, pin 26	Bank 34, R14	IO_L6N_T0_34
CON1, pin 17	GND	JX1, pin 27	GND	GND
CON1, pin 18	GND	JX1, pin 28	GND	GND
CON1, pin 19	IO_L7P_T1_34	JX1, pin 29	Bank 34, Y16	IO_L7P_T1_34
CON1, pin 20	IO_L8P_T1_34	JX1, pin 30	Bank 34, W14	IO_L8P_T1_34
CON1, pin 21	IO_L7N_T1_34	JX1, pin 31	Bank 34, Y17	IO_L7N_T1_34
CON1, pin 22	IO_L8N_T1_34	JX1, pin 32	Bank 34, Y14	IO_L8N_T1_34
CON1: 1,2,17,18,59,60	GND	JX1, pin 33	GND	GND
CON1: 1,2,17,18,59,60	GND	JX1, pin 34	GND	GND
CON1, pin 23	IO_L9P_T1_34	JX1, pin 35	Bank 34, T16	IO_L9P_T1_34
CON1, pin 24	IO_L10P_T1_34	JX1, pin 36	Bank 34, V15	IO_L10P_T1_34
CON1, pin 25	IO_L9N_T1_34	JX1, pin 37	Bank 34, U17	IO_L9N_T1_34
CON1, pin 26	IO_L10N_T1_34	JX1, pin 38	Bank 34, W15	IO_L10N_T1_34

CON1: 1,2,17,18,59,60	GND	JX1, pin 39	GND	GND
CON1: 1,2,17,18,59,60	GND	JX1, pin 40	GND	GND
CON1, pin 27	IO_L11P_T1_34	JX1, pin 41	Bank 34, U14	IO_L11P_T1_SRCC_34
CON1, pin 28	IO_L12P_T1_34	JX1, pin 42	Bank 34, U18	IO_L12P_T1_MRCC_34
CON1, pin 29	IO_L11N_T1_34	JX1, pin 43	Bank 34, U15	IO_L11N_T1_SRCC_34
CON1, pin 30	IO_L12N_T1_34	JX1, pin 44	Bank 34, U19	IO_L12N_T1_MRCC_34
CON1: 1,2,17,18,59,60	GND	JX1, pin 45	GND	GND
CON1: 1,2,17,18,59,60	GND	JX1, pin 46	GND	GND
CON1, pin 31	IO_L13P_T2_34	JX1, pin 47	Bank 34, N18	IO_L13P_T2_MRCC_34
CON1, pin 32	IO_L14P_T2_34	JX1, pin 48	Bank 34, N20	IO_L14P_T2_SRCC_34
CON1, pin 33	IO_L13N_T2_34	JX1, pin 49	Bank 34, P19	IO_L13N_T2_MRCC_34
CON1, pin 34	IO_L14N_T2_34	JX1, pin 50	Bank 34, P20	IO_L14N_T2_SRCC_34
CON1: 1,2,17,18,59,60	GND	JX1, pin 51	GND	GND
CON1: 1,2,17,18,59,60	GND	JX1, pin 52	GND	GND
CON1, pin 35	IO_L15P_T2_34	JX1, pin 53	Bank 34, T20	IO_L15P_T2_DQS_34
CON1, pin 36	IO_L16P_T2_34	JX1, pin 54	Bank 34, V20	IO_L16P_T2_34
CON1, pin 37	IO_L15N_T2_34	JX1, pin 55	Bank 34, U20	IO_L15N_T2_DQS_34
CON1, pin 38	IO_L16N_T2_34	JX1, pin 56	Bank 34, W20	IO_L16N_T2_34
CON1: 39,40	5V	JX1, pin 57	5V	5V
CON1: 39,40	5V	JX1, pin 58	5V	5V
CON1: 39,40	5V	JX1, pin 59	5V	5V
CON1: 39,40	5V	JX1, pin 60	5V	5V
CON1, pin 41	IO_L17P_T2_34	JX1, pin 61	Bank 34, Y18	IO_L17P_T2_34
CON1, pin 42	IO_L18P_T2_34	JX1, pin 62	Bank 34, V16	IO_L18P_T2_34
CON1, pin 43	IO_L17N_T2_34	JX1, pin 63	Bank 34, Y19	IO_L17N_T2_34
CON1, pin 44	IO_L18N_T2_34	JX1, pin 64	Bank 34, W16	IO_L18N_T2_34
CON1: 1,2,17,18,59,60	GND	JX1, pin 65	GND	GND
CON1: 1,2,17,18,59,60	GND	JX1, pin 66	GND	GND
CON1, pin 45	IO_L19P_T3_34	JX1, pin 67	Bank 34, R16	IO_L19P_T3_34
CON1, pin 46	IO_L20P_T3_34	JX1, pin 68	Bank 34, T17	IO_L20P_T3_34
CON1, pin 47	IO_L19N_T3_34	JX1, pin 69	Bank 34, R17	IO_L19N_T3_VREF_34
CON1, pin 48	IO_L20N_T3_34	JX1, pin 70	Bank 34, R18	IO_L20N_T3_34
CON1: 1,2,17,18,59,60	GND	JX1, pin 71	GND	GND
CON1: 1,2,17,18,59,60	GND	JX1, pin 72	GND	GND
CON1, pin 49	IO_L21P_T3_34	JX1, pin 73	Bank 34, V17	IO_L21P_T3_DQS_34
CON1, pin 50	IO_L22P_T3_34	JX1, pin 74	Bank 34, W18	IO_L22P_T3_34
CON1, pin 51	IO_L21N_T3_34	JX1, pin 75	Bank 34, V18	IO_L21N_T3_DQS_34
CON1, pin 52	IO_L22N_T3_34	JX1, pin 76	Bank 34, W19	IO_L22N_T3_34
CON1: 53,54	VCCIO	JX1, pin 77	Bank 34 VCCO	VCCO 34
CON1: 53,54	VCCIO	JX1, pin 78	Bank 34 VCCO	VCCO 34
CON1: 53,54	VCCIO	JX1, pin 79	Bank 34 VCCO	VCCO 34
CON1: 53,54	VCCIO	JX1, pin 80	Bank 34 VCCO	VCCO 34
CON1, pin 55	IO_L23P_T3_34	JX1, pin 81	Bank 34, N17	IO_L23P_T3_34
CON1, pin 56	IO_L24P_T3_34	JX1, pin 82	Bank 34, P15	IO_L24P_T3_34
CON1, pin 57	IO_L23N_T3_34	JX1, pin 83	Bank 34, P18	IO_L23N_T3_34
CON1, pin 58	IO_L24N_T3_34	JX1, pin 84	Bank 34, P16	IO_L24N_T3_34
CON1: 1,2,17,18,59,60	GND	JX1, pin 85	GND	GND
CON1: 1,2,17,18,59,60	GND	JX1, pin 86	GND	GND
TP7	IO_L11P_T1_13	JX1, pin 87	Bank 13, U7	IO_L11P_T1_SRCC_13
TP6	IO_L12P_T1_13	JX1, pin 88	Bank 13, T9	IO_L12P_T1_MRCC_13
TP9	IO_L11N_T1_13	JX1, pin 89	Bank 13, V7	IO_L11N_T1_SRCC_13
TP8	IO_L12N_T1_13	JX1, pin 90	Bank 13, U10	IO_L12N_T1_MRCC_13
TP11	IO_L15P_T2_13	JX1, pin 91	Bank 13, V8	IO_L15P_T2_DQS_13
TP10	IO_L19P_T3_13	JX1, pin 92	Bank 13, T5	IO_L19P_T3_13
TP13	IO_L15N_T2_13	JX1, pin 93	Bank 13, W8	IO_L15N_T2_DQS_13

TP12	IO_L19N_T3_13	JX1, pin 94	Bank 13, U5	IO_L19N_T3_VREF_13
N/C	GND	JX1, pin 95	GND	GND
N/C	GND	JX1, pin 96	GND	GND
N/C	GND	JX1, pin 97	GND	GND
N/C	GND	JX1, pin 98	GND	GND
N/C	GND	JX1, pin 99	GND	GND
N/C	GND	JX1, pin 100	GND	GND

**Table 2 – BKO JX2 Connections**

Carrier Connection	Carrier Net Name	MicroHeader Connection	Zynq AP SoC Connection	Zynq AP SoC Pin Name
N/C	N/A	JX2, pin 1	N/A	N/A
N/C	N/A	JX2, pin 2	N/A	N/A
N/C	N/A	JX2, pin 3	N/A	N/A
N/C	N/A	JX2, pin 4	N/A	N/A
N/C	N/A	JX2, pin 5	N/A	N/A
N/C	N/A	JX2, pin 6	N/A	N/A
N/C	N/A	JX2, pin 7	N/A	N/A
N/C	N/A	JX2, pin 8	N/A	N/A
N/C	N/A	JX2, pin 9	N/A	N/A
CON2, pin 2	VCCIO_EN	JX2, pin 10	Power Supply, PG_1V8	N/A
CON2, pin 1	PG_CARRIER	JX2, pin 11	Bank 500, C7	PS_POR_B_500
CON2: 35,36	5V	JX2, pin 12	VIN_HDR	5V
CON2, pin 3	IO_0_35	JX2, pin 13	Bank 35, G14	IO_0_35
CON2, pin 4	IO_25_35	JX2, pin 14	Bank 35, J15	IO_25_35
CON2:17,18,59,60	GND	JX2, pin 15	GND	GND
CON2:17,18,59,60	GND	JX2, pin 16	GND	GND
CON2, pin 5	IO_L1P_T0_35	JX2, pin 17	Bank 35, C20	IO_L1P_T0_AD0P_35
CON2, pin 6	IO_L2P_T0_35	JX2, pin 18	Bank 35, B19	IO_L2P_T0_AD8P_35
CON2, pin 7	IO_L1N_T0_35	JX2, pin 19	Bank 35, B20	IO_L1N_T0_AD0N_35
CON2, pin 8	IO_L2N_T0_35	JX2, pin 20	Bank 35, A20	IO_L2N_T0_AD8N_35
CON2:17,18,59,60	GND	JX2, pin 21	GND	GND
CON2:17,18,59,60	GND	JX2, pin 22	GND	GND
CON2, pin 9	IO_L3P_T0_35	JX2, pin 23	Bank 35, E17	IO_L3P_T0_DQS_AD1P_35
CON2, pin 10	IO_L4P_T0_35	JX2, pin 24	Bank 35, D19	IO_L4P_T0_35
CON2, pin 11	IO_L3N_T0_35	JX2, pin 25	Bank 35, D18	IO_L3N_T0_DQS_AD1N_35
CON2, pin 12	IO_L4N_T0_35	JX2, pin 26	Bank 35, D20	IO_L4N_T0_35
CON2:17,18,59,60	GND	JX2, pin 27	GND	GND
CON2:17,18,59,60	GND	JX2, pin 28	GND	GND
CON2, pin 13	IO_L5P_T0_35	JX2, pin 29	Bank 35, E18	IO_L5P_T0_AD9P_35
CON2, pin 14	IO_L6P_T0_35	JX2, pin 30	Bank 35, F16	IO_L6P_T0_35
CON2, pin 15	IO_L5N_T0_35	JX2, pin 31	Bank 35, E19	IO_L5N_T0_AD9N_35
CON2, pin 16	IO_L6N_T0_35	JX2, pin 32	Bank 35, F17	IO_L6N_T0_VREF_35
CON2:17,18,59,60	GND	JX2, pin 33	GND	GND
CON2:17,18,59,60	GND	JX2, pin 34	GND	GND
CON2, pin 19	IO_L9P_T1_35	JX2, pin 35	Bank 35, L19	IO_L9P_T1_DQS_AD3P_35
CON2, pin 20	IO_L7P_T1_35	JX2, pin 36	Bank 35, M19	IO_L7P_T1_AD2P_35
CON2, pin 21	IO_L9N_T1_35	JX2, pin 37	Bank 35, L20	IO_L9N_T1_DQS_AD3N_35
CON2, pin 22	IO_L7N_T1_35	JX2, pin 38	Bank 35, M20	IO_L7N_T1_AD2N_35
CON2:17,18,59,60	GND	JX2, pin 39	GND	GND
CON2:17,18,59,60	GND	JX2, pin 40	GND	GND
CON2, pin 23	IO_L8P_T1_35	JX2, pin 41	Bank 35, M17	IO_L8P_T1_AD10P_35
CON2, pin 24	IO_L10P_T1_35	JX2, pin 42	Bank 35, K19	IO_L10P_T1_AD11P_35

CON2, pin 25	IO_L8N_T1_35	JX2, pin 43	Bank 35, M18	IO_L8N_T1_AD10N_35
CON2, pin 26	IO_L10N_T1_35	JX2, pin 44	Bank 35, J19	IO_L10N_T1_AD11N_35
CON2:17,18,59,60	GND	JX2, pin 45	GND	GND
CON2:17,18,59,60	GND	JX2, pin 46	GND	GND
CON2, pin 27	IO_L11P_T1_35	JX2, pin 47	Bank 35, L16	IO_L11P_T1_SRCC_35
CON2, pin 28	IO_L12P_T1_35	JX2, pin 48	Bank 35, K17	IO_L12P_T1_MRCC_35
CON2, pin 29	IO_L11N_T1_35	JX2, pin 49	Bank 35, L17	IO_L11N_T1_SRCC_35
CON2, pin 30	IO_L12N_T1_35	JX2, pin 50	Bank 35, K18	IO_L12N_T1_MRCC_35
CON2:17,18,59,60	GND	JX2, pin 51	GND	GND
CON2:17,18,59,60	GND	JX2, pin 52	GND	GND
CON2, pin 31	IO_L13P_T2_35	JX2, pin 53	Bank 35, H16	IO_L13P_T2_MRCC_35
CON2, pin 32	IO_L14P_T2_35	JX2, pin 54	Bank 35, J18	IO_L14P_T2_AD4P_SRCC_35
CON2, pin 33	IO_L13N_T2_35	JX2, pin 55	Bank 35, H17	IO_L13N_T2_MRCC_35
CON2, pin 34	IO_L14N_T2_35	JX2, pin 56	Bank 35, H18	IO_L14N_T2_AD4N_SRCC_35
CON2: 35,36	5V	JX2, pin 57	5V	5V
CON2: 35,36	5V	JX2, pin 58	5V	5V
CON2: 35,36	5V	JX2, pin 59	5V	5V
CON2: 35,36	5V	JX2, pin 60	5V	5V
CON2, pin 37	IO_L16P_T2_35	JX2, pin 61	Bank 35, G17	IO_L16P_T2_35
CON2, pin 38	IO_L15P_T2_35	JX2, pin 62	Bank 35, F19	IO_L15P_T2_DQS_AD12P_35
CON2, pin 39	IO_L16N_T2_35	JX2, pin 63	Bank 35, G18	IO_L16N_T2_35
CON2, pin 40	IO_L15N_T2_35	JX2, pin 64	Bank 35, F20	IO_L15N_T2_DQS_AD12N_35
CON2:17,18,59,60	GND	JX2, pin 65	GND	GND
CON2:17,18,59,60	GND	JX2, pin 66	GND	GND
CON2, pin 41	IO_L18P_T2_35	JX2, pin 67	Bank 35, G19	IO_L18P_T2_AD13P_35
CON2, pin 42	IO_L17P_T2_35	JX2, pin 68	Bank 35, J20	IO_L17P_T2_AD5P_35
CON2, pin 43	IO_L18N_T2_35	JX2, pin 69	Bank 35, G20	IO_L18N_T2_AD13N_35
CON2, pin 44	IO_L17N_T2_35	JX2, pin 70	Bank 35, H20	IO_L17N_T2_AD5N_35
CON2:17,18,59,60	GND	JX2, pin 71	GND	GND
CON2:17,18,59,60	GND	JX2, pin 72	GND	GND
CON2, pin 45	IO_L20P_T3_35	JX2, pin 73	Bank 35, K14	IO_L20P_T3_AD6P_35
CON2, pin 46	IO_L19P_T3_35	JX2, pin 74	Bank 35, H15	IO_L19P_T3_35
CON2, pin 47	IO_L20N_T3_35	JX2, pin 75	Bank 35, J14	IO_L20N_T3_AD6N_35
CON2, pin 48	IO_L19N_T3_35	JX2, pin 76	Bank 35, G15	IO_L19N_T3_VREF_35
CON2: 49,50	VCCIO	JX2, pin 77	Bank 35 VCCO	VCCO 35
CON2: 49,50	VCCIO	JX2, pin 78	Bank 35 VCCO	VCCO 35
CON2: 49,50	VCCIO	JX2, pin 79	Bank 35 VCCO	VCCO 35
CON2: 49,50	VCCIO	JX2, pin 80	Bank 35 VCCO	VCCO 35
CON2, pin 51	IO_L21P_T3_35	JX2, pin 81	Bank 35, N15	IO_L21P_T3_DQS_AD14P_35
CON2, pin 52	IO_L22P_T3_35	JX2, pin 82	Bank 35, L14	IO_L22P_T3_AD7P_35
CON2, pin 53	IO_L21N_T3_35	JX2, pin 83	Bank 35, N16	IO_L21N_T3_DQS_AD14N_35
CON2, pin 54	IO_L22N_T3_35	JX2, pin 84	Bank 35, L15	IO_L22N_T3_AD7N_35
CON2:17,18,59,60	GND	JX2, pin 85	GND	GND
CON2:17,18,59,60	GND	JX2, pin 86	GND	GND
CON2, pin 55	IO_L23P_T3_35	JX2, pin 87	Bank 35, M14	IO_L23P_T3_35
CON2, pin 56	IO_L24P_T3_35	JX2, pin 88	Bank 35, K16	IO_L24P_T3_AD15P_35
CON2, pin 57	IO_L23N_T3_35	JX2, pin 89	Bank 35, M15	IO_L23N_T3_35
CON2, pin 58	IO_L24N_T3_35	JX2, pin 90	Bank 35, J16	IO_L24N_T3_AD15N_35
CON2:17,18,59,60	GND	JX2, pin 91	GND	GND

CON2:17,18,59,60	GND	JX2, pin 92	GND	GND
TP15	IO_L20P_T3_13	JX2, pin 93	Bank 13, Y12	IO_L20P_T3_13
TP14	IO_L21P_T3_13	JX2, pin 94	Bank 13, V11	IO_L21P_T3_DQS_13
TP17	IO_L20N_T3_13	JX2, pin 95	Bank 13, Y13	IO_L20N_T3_13
TP16	IO_L21N_T3_13	JX2, pin 96	Bank 13, V10	IO_L21N_T3_DQS_13
TP18	IO_L22P_T3_13	JX2, pin 97	Bank 13, V6	IO_L22P_T3_13
CON2: 49,50	VCCIO	JX2, pin 98	VCCIO_13	VCCIO_13
TP20	IO_L22N_T3_13	JX2, pin 99	Bank 13, W6	IO_L22N_T3_13
TP19	IO_L6N_T0_13	JX2, pin 100	Bank 13, V5	IO_L6N_T0_VREF_13

## 2.1.2 Mounting Holes

There are four mounting holes in the BKO card area to facilitate secure SOM mounting.

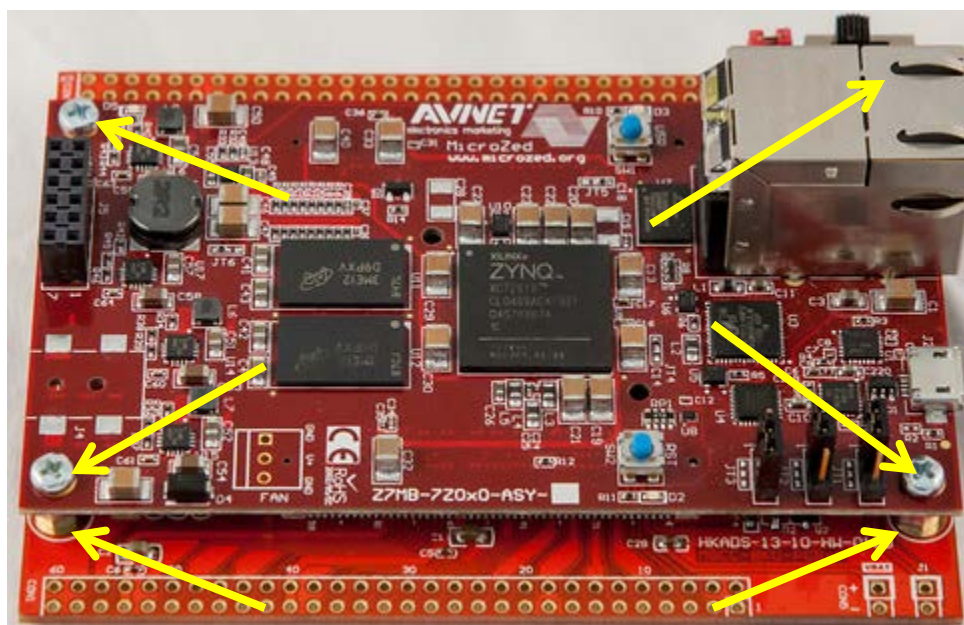


Figure 4 – MicroZed Mounted Securely to BKO-CC with Screws and Stand-offs

## 2.1.3 JX1 and JX2 MicroZed interface microheaders

The Carrier features two MicroHeaders for connection to the MicroZed. Each connector interfaces to Zynq PL I/O.

- The connectors are BERGSTAK 0.8mm pitch. The BERGSTAK family has variable stack heights from 5mm to 20mm. The specific one used on the BKO and MicroZed results in a stack height of 6mm, BKO PCB top to MicroZed PCB bottom.
- Each connector has 100 pins which include I/O, analog signals, as well as power and ground. The Carrier powers the MicroZed as an alternative to the USB-UART. Each pin can carry 500mA of current and has been tested and certified against PCIe Gen2, thus sufficient bandwidth for this interface.
- MicroZed does not power the PL VCC<sub>IO</sub> banks, this is required to be provided by the Carrier. This gives the Carrier the flexibility to control the I/O bank voltages. On the BKO-CC, VCC<sub>IO</sub> is provided by the VADJ regulator for both Banks 34 and 35. The 7Z010 has two PL I/O banks, banks 34 and 35, each containing 50 I/O.

- The 7Z020 has a third I/O bank, bank 13, which is powered on the BKO-CC by VADJ. The BKO-CC does not expose any of the Bank 13 I/Os.
- Within a PL I/O bank, there are 50 I/O. Each differential pair is isolated by a power or ground pin. Additionally, eight of these I/O can be connected as clock inputs (four MRCC and four SRCC inputs).
- Bank 35 exposes several I/Os that *may* be able to be used as analog inputs to the XADC, but the end user is responsible for adding the applicable filtering in the prototype area.

## 2.2 Power

### 2.2.1 Power Input

The board input voltage is through a micro USB header. The current rating of the power supply is determined by the expected power requirements of the interfaced design.

The precise current demand is based on the end-use I/O requirements and therefore the application will determine the minimum current a power supply must source. As shipped from Avnet, a 5V, 2.0 Amp micro USB power supply is provided in the kit.

- Micro USB AC/DC wall adapter:
  - Primary 5V, 2A, Micro USB type B connector.
- On Board:
  - Regulator VADJ. for 1.8V/2.5V/3.3V @ 2A.
    - For Module VCC<sub>IO</sub> Bank\_34, Bank\_35, and Bank\_13.

### 2.2.2 Voltage Regulators

The following table lists the power solution for the BKO Carrier Card. VADJ rail is independent and adjustable supplying power to the Zynq PL I/O banks and connected CON1 and CON2 headers. VADJ drives banks 34, 35 and 13 (if 7Z020 is populated on MicroZed).

The table below shows the minimum required voltage rails, currents, and tolerances.

**Table 3 – Voltage Rails w/ Current Estimates**

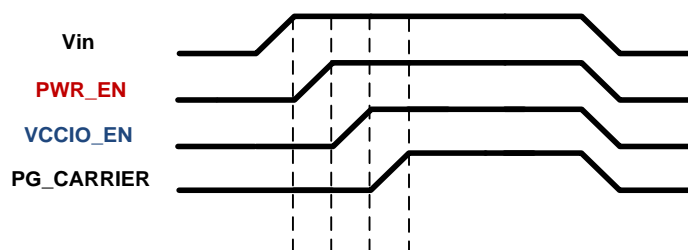
Voltage (V)	7Z010 Current	7Z020 Current	Tolerance	IC	Notes
5V (Main)	N/A	N/A	10%	N/A	Supplied power adapter @ 2A
VADJ (VCC <sub>IO</sub> _13, 34,35) – 1.8V, 2.5V or 3.3V	<0.9A @ 3.3V	<1.3A @ 3.3V	5%	REG1, LMR10510XMF	2A capable

### 2.2.3 MicroZed Power Sequencing and control circuits

- PWR\_EN signal, active high, JX1.5, allows the carrier to turn on or off the MicroZed power supplies. R74 and C106 have been placed to adjust the timing

of this signal during power off conditions. This signal should not be de-asserted until VCCIO\_EN is de-asserted. In the carrier off condition (power plug removed or power switch turned off), this signal is driven low by the on-board MOSFET (Q2) turning on. Because the MicroZed is capable of being powered by the USB UART connection, this carrier board circuit is used to ensure the MicroZed board turns off when the carrier turns off.

- VCCIO\_EN signal, active high, JX2.10, originates on the MicroZed and is the output of the 1.8V regulator, PG\_1V8. This signal enables the carrier's VADJ regulator. When the carrier is turned off (power switch turned off or power plug removed) or the MicroZed's PG\_1V8 signal is de-asserted VCCI\_EN is driven low, which turns off the BKO-CC and the MicroZed.
- PG\_CARRIER signal, active high, JX2.11, is pulled up by MicroZed's +3.3V PG\_MODULE signal. This signal can be pulled low by the BKO-CC or the MicroZed when either board's power circuitry is not 'Good' yet.
- The following diagram illustrates the power supply sequencing on power up. Note Vin and PWR\_Enable can come up simultaneously, but shown staggered as PWR\_Enable can come up later.
- U2 and U3 (TL431A precision voltage reference and AP331AWG Op-Amp) are used to create a voltage comparator circuit to control the power-on of the BKO board. VADJ\_EN drives active when VIN exceeds approximately 4.0V.



**Figure 5 – Power Sequencing**

The PG\_CARRIER (on BKO-CC) and PG\_MODULE (on MicroZed) signals are wired OR and tied to the Zynq Power On Reset signal. When the power supplies are valid on both the SOM and carrier, the PG signal de-asserts the Zynq POR signal.

#### **2.2.4 Bypassing/Decoupling**

The BKO-CC follows the recommended decoupling techniques per each manufacturer's datasheet.

## 2.3 Jumpers, configuration and test points:

The below table is a quick reference to all of the jumpers, configuration settings and test points on the BKO. For detailed information, refer to the appropriate sections in this document.

Reference Designator	Name	Default	Notes:
J1	VCCIO_EN	Not Populated	Used to test the on-board power supplies without a MicroZed inserted.
CON1	CON1	Not Populated	This 2x30 0.100" pitch socket breaks out the JX1 connector for user I/O.
CON2	CON2	Not Populated	This 2x30 0.100" pitch socket breaks out the JX2 connector for user I/O.
CON4	+5Vin	N/A	+5V Micro USB input
CON5	VBAT	Not Populated	JX1 pin 7. Zynq pin F11. +1.5V for SoC battery support.
SW1	PWR	Open	Applies 5V USB power to board. When off, disables PWR_EN & VCCIO_EN on microZed SOM.
TP6-TP13	TP6-TP13	N/A	Generic JX1 test points.
TP14-TP20	TP14-TP20	N/A	Generic JX2 test points.
JP2	VADJ configuration	Jumper Location: 1-2: 3.3V 3-4: 2.5V 5-6: 1.8V	Jumper settings to select VADJ (VCCIO) from 1.8V, 2.5V or 3.3V.

Table 4 - settings

## 3 Mechanical

### 3.1 Prototype Area

The BKO features a center prototyping area for experimental circuit design. This area has the following features:

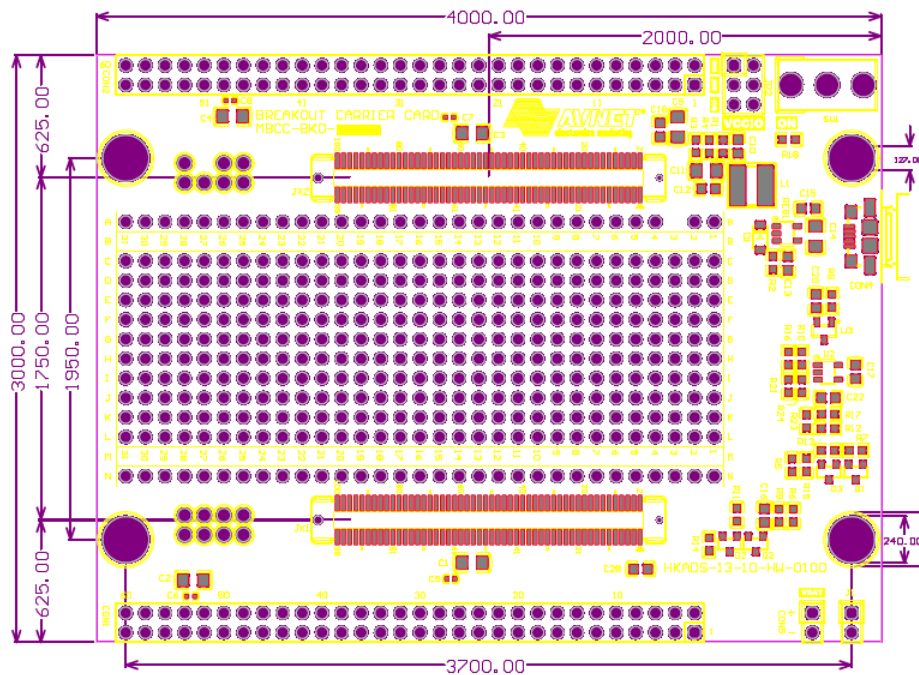
#### 3.1.1 10x31 inert 0.1" pitch plated through hole field

This area contains 310 plated through holes. These holes are not connected to any signals or power connections on the BKO board and can be used to place a variety of components for design evaluations.

#### 3.1.2 Proto area +5V, +VCCIO and GND pins

The proto area (see figure 2) is surrounded by 0.1" pitch power and ground pins. There are 2 +5V pins (A1, A2), 27 +VCCIO pins (A4-31) and 31 ground pins (N1-31).

### 3.2 Dimensions:



### 3.3 Weight:

The weight of the BKO-CC with rubber feet and all jumpers populated is 85.616 grams/  
3.02 ounces.

## 4 Revision History

Rev date	Rev #	Reason for change
31 Mar 2014	1.0	Initial Revision
15 May 2014	1.1	Corrections to Tables 1 and 2