HDMI Input/Output FMC Module with Camera Interface

Hardware Guide

AVNET electronics marketing

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1.0 Introduction

The purpose of this manual is to describe the functionality and contents of the HDMI Input/Output FMC Module with Camera Interface from Avnet Electronics Marketing. This document includes descriptions of the hardware features.

1.1 Description

The HDMI Input/Output FMC Module with Camera Interface is not a stand-alone module, but rather a plug-in module designed to interface with FMC compatible baseboards. In that role, the FMC adapter provides a number of video interfaces to its host via a LPC FMC connector. The FMC Module is shown in Figure 1.

1.2 Features

The HDMI Input/Output FMC Module provides the following features.

Video Input
- — HDMI input interface
- — Camera interface

Video Output
- — HDMI output interface

Clock Source
- — Video clock synthesizer

I2C Configuration
- — IPMI Identification EEPROM
- — Peripheral configuration

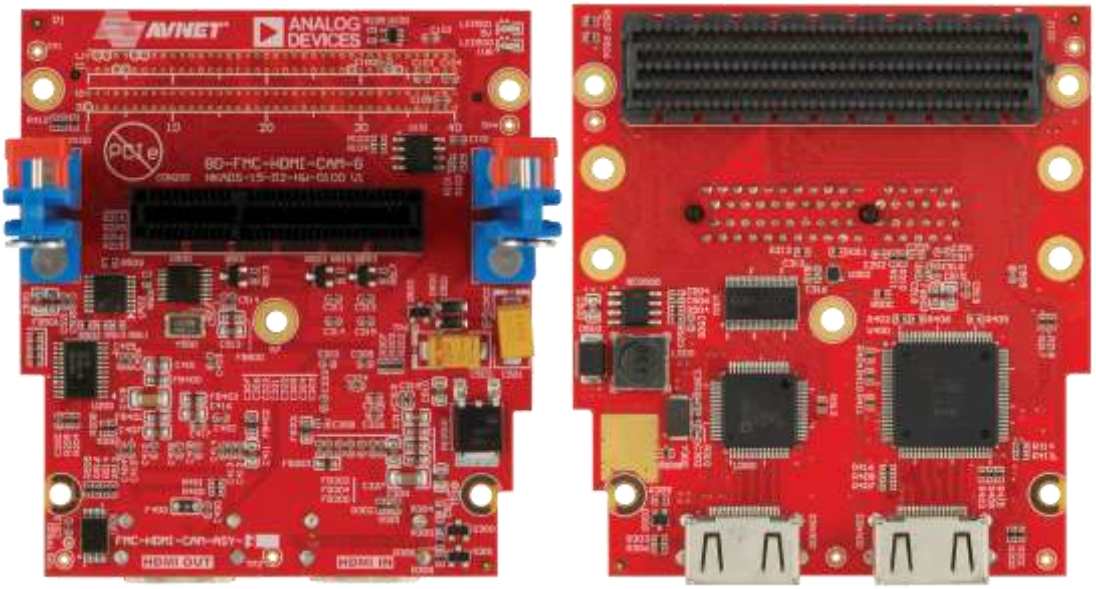

Figure 1 – FMC-HDMI-CAM – Top/Bottom View

1.3 Ordering Information

The following table lists the evaluation kit part numbers and available software options.

Part Number	Hardware
AES-FMC-HDMI-CAM-G (http://www.em.avnet.com/fmc-hdmi-cam)	HDMI Input/output FMC Module (camera module not included)
Optional camera modules	
AES-CAM-TOSH-1080P-G	Toshiba Industrial 1080P60 Camera Module
AES-CAM-ON-P1300C-G	ON Semiconductor PYTHON-1300-C Camera Module

Table 1 - Ordering Information

Figure 2 – FMC-HDMI-CAM – Angle View

1.4 References

Analog Devices Engineering Zone : ADV7611 HDMI Receiver resources
http://ez.analog.com/docs/DOC-1745

Analog Devices Engineering Zone : ADV7511 HDMI Receiver resources
http://ez.analog.com/docs/DOC-1740

Texas Instruments CDCE913 datasheet: Programmable 2-PLL VCXO Clock Synthesizer
http://focus.ti.com/docs/prod/folders/print/cdce913.html

FMC Specification
http://www.vita.com/fmc.html

Platform Management FRU Information Storage Definition V1.0
http://download.intel.com/design/servers/ipmi/FRU1011.pdf

2.0 Functional Description

The FMC-HDMI-CAM is a low pin count (LPC) FMC module containing interfaces intended for video processing. This module contains no processing intelligence and requires that it be plugged into a compatible baseboard for power, control and data processing. The FMC module has a camera interface that allows optional camera modules to be populated..

Figure 3 depicts the architecture of the FMC-HDMI-CAM FMC module.

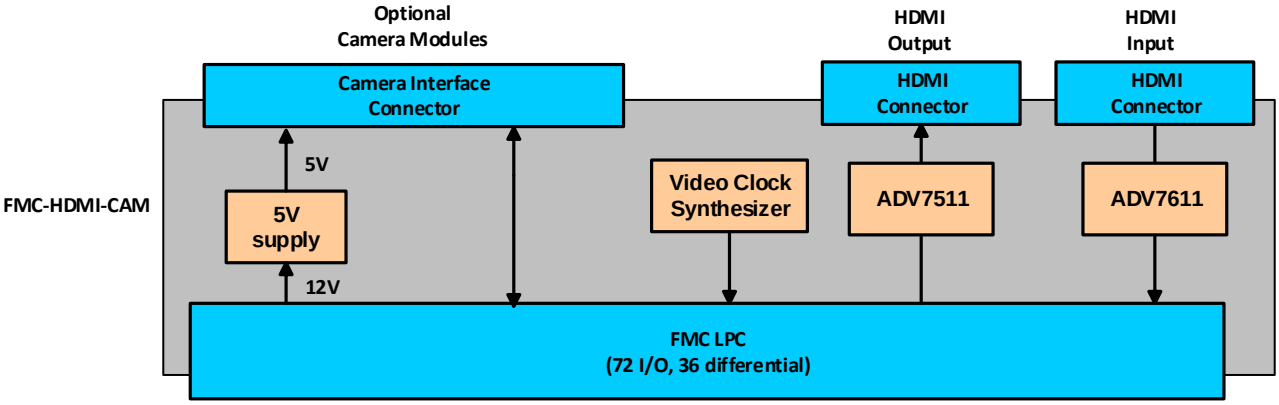

Figure 3 – FMC-HDMI-CAM - Block Diagram

Figure 4 – FMC-HDMI-CAM – Shown with Toshiba camera module

Figure 5 – FMC-HDMI-CAM – Shown with PYTHON-1300-C camera module

2.1 FMC Connector

The FMC LPC connector provides 68 single-ended I/O or 34 differential I/O as defined in Table 2.

	H	G	D	C
1	VREF_A_M2C	GND	PG_C2M	GND
2	PRSNT_M2C_L	CLK1_M2C_P	GND	DP0_C2M_P
3	GND	CLK1_M2C_N	GND	DP0_C2M_N
4	CLK0_M2C_P	GND	GBTCLK0_M2C_P	GND
5	CLK0_M2C_N	GND	GBTCLK0_M2C_N	GND
6	GND	LA00_P_CC	GND	DP0_M2C_P
7	LA02_P	LA00_N_CC	GND	DP0_M2C_N
8	LA02_N	GND	LA01_P_CC	GND
9	GND	LA03_P	LA01_N_CC	GND
10	LA04_P	LA03_N	GND	LA06_P
11	LA04_N	GND	LA05_P	LA06_N
12	GND	LA08_P	LA05_N	GND
13	LA07_P	LA08_N	GND	GND
14	LA07_N	GND	LA09_P	LA10_P
15	GND	LA12_P	LA09_N	LA10_N
16	LA11_P	LA12_N	GND	GND
17	LA11_N	GND	LA13_P	GND
18	GND	LA16_P	LA13_N	LA14_P
19	LA15_P	LA16_N	GND	LA14_N
20	LA15_N	GND	LA17_P_CC	GND
21	GND	LA20_P	LA17_N_CC	GND
22	LA19_P	LA20_N	GND	LA18_P_CC
23	LA19_N	GND	LA23_P	LA18_N_CC
24	GND	LA22_P	LA23_N	GND
25	LA21_P	LA22_N	GND	GND
26	LA21_N	GND	LA26_P	LA27_P
27	GND	LA25_P	LA26_N	LA27_N
28	LA24_P	LA25_N	GND	GND
29	LA24_N	GND	TCK	GND
30	GND	LA29_P	TDI	SCL
31	LA28_P	LA29_N	TDO	SDA
32	LA28_N	GND	3P3VAUX	GND
33	GND	LA31_P	TMS	GND
34	LA30_P	LA31_N	TRST_L	GA0
35	LA30_N	GND	GA1	12P0V
36	GND	LA33_P	3P3V	GND
37	LA32_P	LA33_N	GND	12P0V
38	LA32_N	GND	3P3V	GND
39	GND	VADJ	GND	3P3V
40	VADJ	GND	3P3V	GND
	LPC Connector	LPC Connector	LPC Connector	LPC Connector

Table 2 – FMC LPC Connector Pinout

Note: For the FMC LPC, the connector columns K, J, F, E, B, and A are not used and not shown in the above table.

The FMC pin allocation for the FMC-HDMI-CAM FMC Module is defined in Table 3.

	H	G		D	C	
1	-	GND	1	PG_C2M	GND	1
2	PRSNT_M2C_L	HDMII_CLK (in)	2	GND	-	2
3	GND	HDMIO_CLK (out)	3	GND	-	3
4	VCLK1	GND	4	-	GND	4
5	CAM_RESET_N	GND	5	-	GND	5
6	GND	CLK_OUT_P (in)	6	GND	-	6
7	CAM_D[0]_P	CLK_OUT_N (in)	7	GND	-	7
8	CAM_D[0]_N	GND	8	HDMIIO_INT#	GND	8
9	GND	CAM_D[1]_P	9	I2C_MUX_RESET_N	GND	9
10	CAM_D[3]_P	CAM_D[1]_N	10	GND	CAM_D[2]_P	10
11	CAM_D[3]_N	GND	11	CAM_D[4]_P	CAM_D[2]_N	11
12	GND	CAM_D[6]_P	12	CAM_D[4]_N	GND	12
13	CAM_D[5]_P	CAM_D[6]_N	13	GND	GND	13
14	CAM_D[5]_N	GND	14	CAM_D[7]_P	CAM_SYNC_P	14
15	GND	CAM_SPI_CLK	15	CAM_D[7]_N	CAM_SYNC_N	15
16	CAM_SPI_MOSI	CAM_SPI_SSEL_N	16	GND	GND	16
17	CAM_SPI_MISO	GND	17	CAM_CLK_PLL	GND	17
18	GND	I2C_MUX_SCL	18	CAM_TRIGGER[2]	CAM_TRIGGER[1]	18
19	CAM_MONITOR[1]	I2C_MUX_SDA	19	GND	CAM_TRIGGER[0]	19
20	CAM_MONITOR[0]	GND	20	HDMIO_CBCR[6]	GND	20
21	GND	HDMIO_CBCR[7]	21	HDMIO_CBCR[3]	GND	21
22	HDMIO_CBCR[4]	HDMIO_CBCR[5]	22	GND	HDMIO_CBCR[2]	22
23	HDMIO_CBCR[1]	GND	23	HDMIO_Y[7]	HDMIO_Y[6]	23
24	GND	HDMIO_CBCR[0]	24	HDMIO_Y[3]	GND	24
25	HDMIO_Y[4]	HDMII_Y[5]	25	GND	GND	25
26	HDMIO_Y[2]	GND	26	HDMII_Y[7]	HDMII_Y[6]	26
27	GND	HDMIO_Y[1]	27	HDMII_Y[4]	HDMII_Y[3]	27
28	HDMIO_SPDIF	HDMIO_Y[0]	28	GND	GND	28
29	HDMII_SPDIF	GND	29	-	GND	29
30	GND	HDMII_Y[5]	30	TDI	SCL	30
31	HDMII_Y[1]	HDMII_Y[2]	31	TDO[1]	SDA	31
32	HDMII_Y[0]	GND	32	3P3VAUX	GND	32
33	GND	HDMII_CBCR[7]	33	-	GND	33
34	HDMII_CBCR[5]	HDMII_CBCR[6]	34	-	GA0	34
35	HDMII_CBCR[4]	GND	35	GA1	12P0V	35
36	GND	HDMII_CBCR[3]	36	3P3V	GND	36
37	HDMII_CBCR[1]	HDMII_CBCR[2]	37	GND	12P0V	37
38	HDMII_CBCR[0]	GND	38	3P3V	GND	38
39	GND	VADJ	39	GND	3P3V	39
40	VADJ	GND	40	3P3V	GND	40

Table 3 – FMC-HDMI-CAM - LPC Pinout

[1] TDO is connected to TDI in order not to break the JTAG chain

2.2 Voltage Sources

The following table lists all the voltage sources available on the FMC-HDMI-CAM module.

Voltage Name	Voltage	Current	Description
supplied by **FMC connector**			
3V3AUX	3.3 V		Used by IPMI Identification prior to module power-up.
3V3	3.3 V		Used by ADV7611, ADV7511, CDCE913, and level translators
VADJ	2.5 V or 3.3 V		Used for all single-ended signals connected to FMC connector.
12V	12.0 V		
supplied by the FMC-HDMI-CAM **FMC module**			
REG_5V	5V	1A	Over-designed for VITA-5000 image sensor module
REG_1V8	1.8V	TBD	Used by ADV7611, ADV7511, CDCE913

Table 4 –Voltage Sources

2.3 I2C Chain 1 – IPMI Identification EEPROM

The following I2C section implements the IPMI identification for the FMC module.

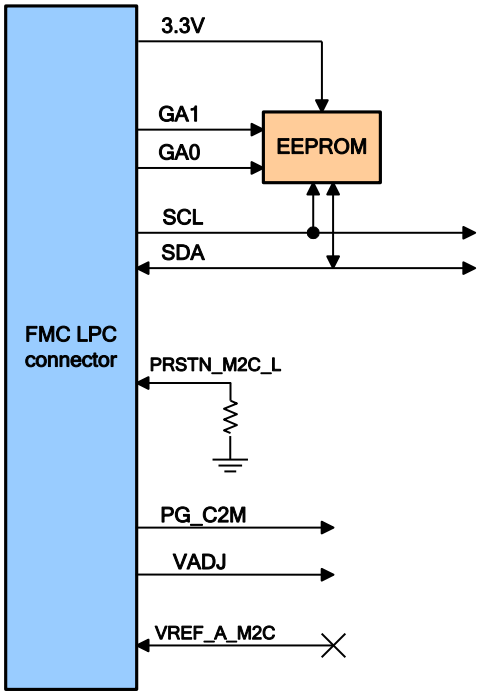

Figure 6 – IPMI Identification, Block Diagram

When the VADJ voltage is valid, the PG_C2M (ie. power good) will be asserted high. An inverted version of this signal is used to enable all the voltage level translators connected to VADJ.

The address of the I2C EEPROM will be determined by the GA[0:1] signals driven by the carrier.

Table 5 describes the EEPROM address for the FMC module.

GA[0:1]	FMC-HDMI-CAM I2C EEPROM Address
00	0xA0
01	0xA2
10	0xA4
11	0xA6

Table 5 – IPMI Identification, I2C EEPROM Address

The EEPROM content is defined by the Platform Management FRU Information Storage Definition V1.0.
http://download.intel.com/design/servers/ipmi/FRU1011.pdf

For the FMC-HDMI-CAM module, the content is described in Table 6.

Content	FMC-HDMI-CAM
Board Information	
- Manufacturer Date/Time	-
- Manufacturer	Avnet
- Product	FMC-HDMI-CAM
- Serial	{programmed during factory testing}
- Part Number	AES-FMC-HDMI-CAM-G
- FRU File ID	-

Table 6 – IPMI Identification, EEPROM Content

2.4 I2C Chain 2 – Peripheral Configuration

The FMC-HDMI-CAM Module implements two I2C chains. The second I2C chain is used to configure the FMC-HDMI-CAM module's peripherals.

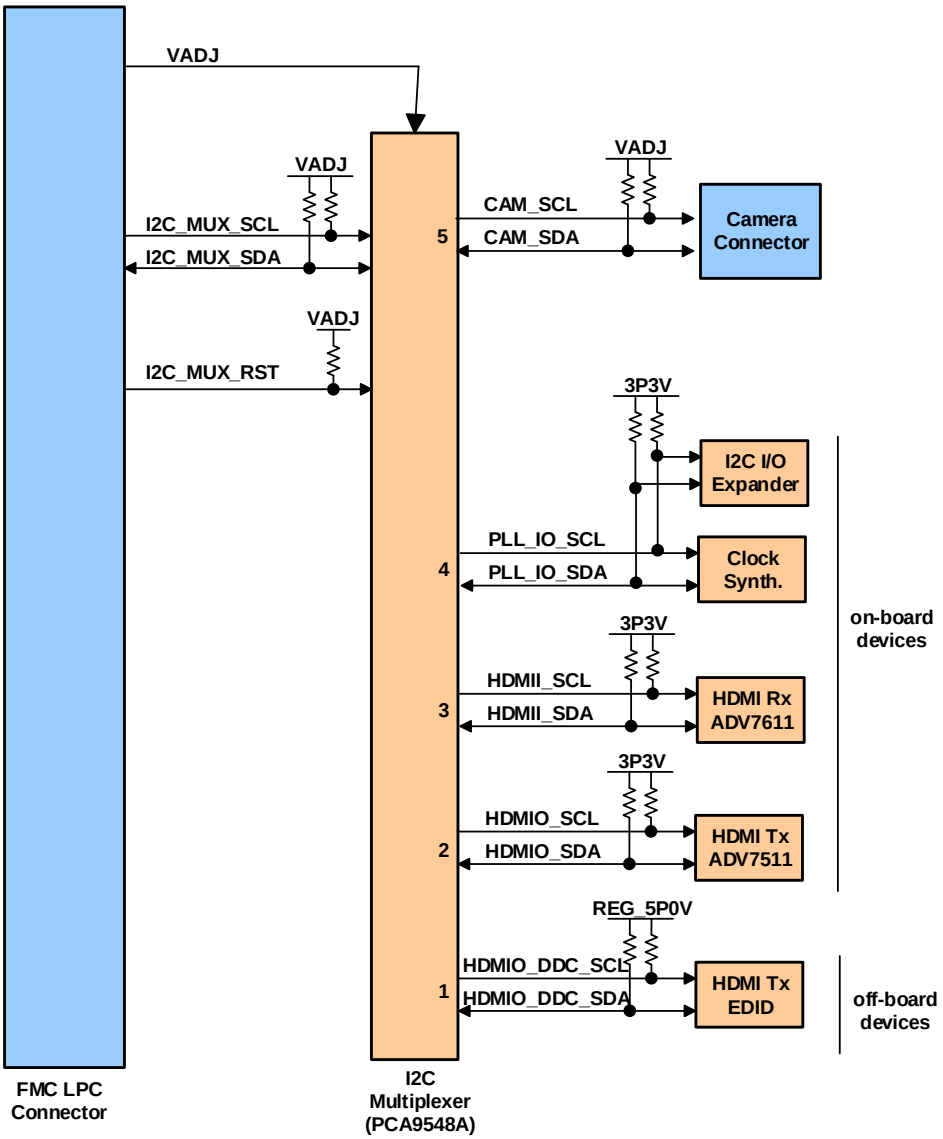

Figure 7 – I2C Peripheral Configuration, Block Diagram

The Texas Instruments PCA9546A I2C Multiplexer performs two purposes:

- Voltage level translation (2.5 V, 3.3 V, 5.0 V)
- I2C address conflict resolution

The following table lists the I2C addresses that may be present on each of the I2C Multiplexer's ports. Notice that the I2C Multiplexer's address is always visible regardless of which port is enabled.

Device	I2C Address
I2C Multiplexer	0xE0 (PCA9546)
Mux Port 1	
HDMI Output DDC EDID	0xA0
Mux Port 2	
HDMI Output	0x72 (ADV7511)
Mux Port 3	
HDMI Input	0x98 (ADV7611)
Mux Port 4	
Video Clock Synth.	0xCA (CDCE913)
I2C I/O Expander	0x40 (PCA9555)
Mux Port 5	
Camera	specific to camera module
Mux Port 6	
unused	
Mux Port 7	
unused	
Mux Port 8	
unused	

Table 7 – I2C Peripheral Configuration, Device Summary

2.5 I2C I/O Expander

The FMC module implements many features that require additional I/Os outside the available I/Os provided via the FMC connector. To accomplish the requirement for the additional I/Os, an I2C I/O Expander was implemented to handle various controls signals attached to peripherals.

The I2C I/O Expander is implemented with the Texas Instruments PCA9534. The I2C I/O Expander takes an I2C interface from the I2C MUX and decodes that to provide 8 USER GPIO on its outputs. This is an ideal device for the control signal support that was required by the peripherals.

The figure below shows a high level diagram of the I2C I/O Expander circuit on the FMC module.

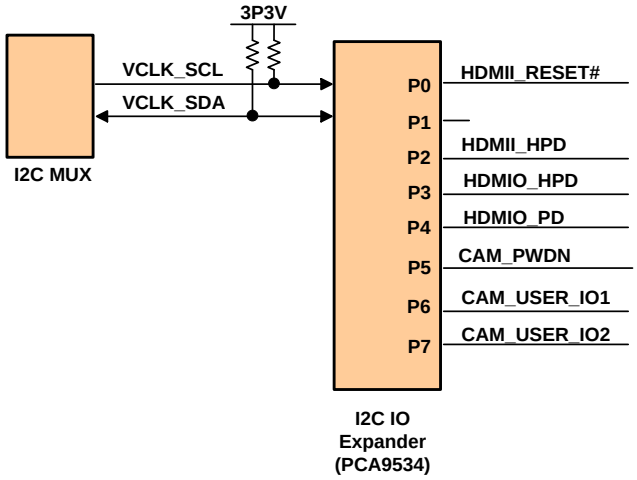

Figure 8 – I2C I/O Expander, Block Diagram

2.6 Video Clock Synthesizer

A Video Clock Generator is included on the FMC module in order to provide a clock for all video applications.

The following block diagram illustrates the connections for the Video Clock Generator.

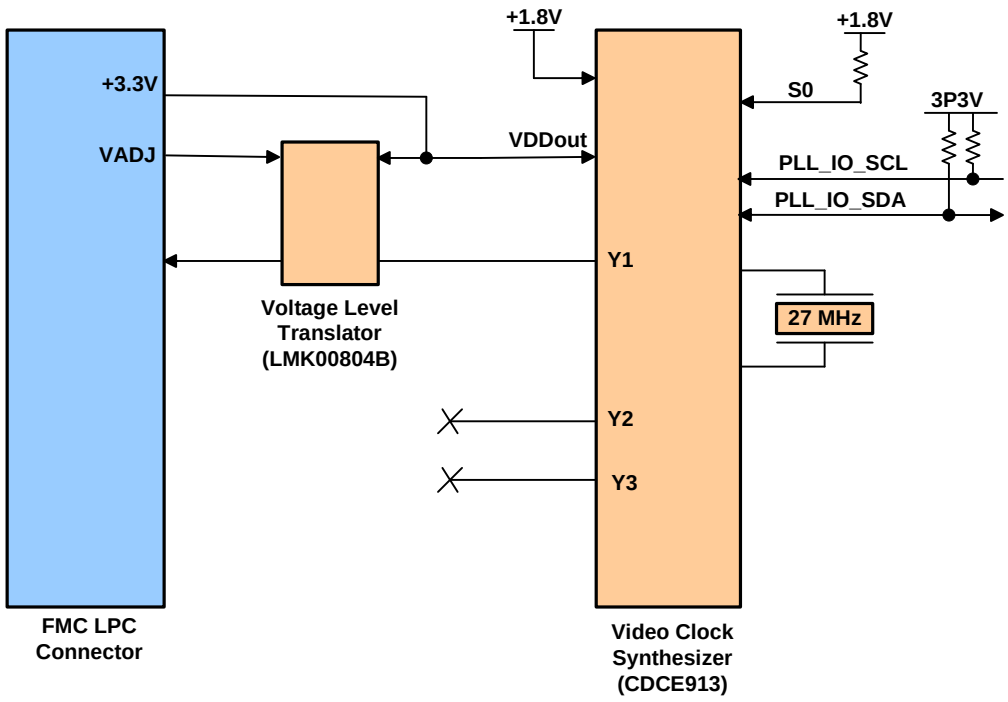

Figure 9 – Video Clock Synthesizer, Block Diagram

The Texas Instruments CDCE913 clock synthesizer has three clock outputs which are used as follows.

Clock	PLL	Description
Y1	PLL1	Can be used for any application
Y2	PLL1	Unused
Y3	PLL1	Unused

Table 8 – Video Clock Generator, Clock Output Usage

The Y1 clock output can be used for any application. One of these applications could be the 62MHz reference clock for the camera interface, another could be the clock source for the HDMI output. The Y2 and Y3 clock outputs are not used.

The default mode of the CDCE913 is to output a 27 MHz clock on all of its outputs.

Configuration is performed via I2C. The SDA/SCL pins of the CDCE913 device are 3.3 V tolerant.
The settings of the CDCE913 video clock synthesizer can be calculated automatically using the TI Pro-Clock™ software.

2.7 HDMI Input

The HDMI input interface is implemented using the Analog Devices ADV7611 device. This device's output video interface supports YCbCr mode with embedded syncs, which significantly reduce the number of I/O required for the FMC side interface.

By using the YCbCr 4:2:2 mode, the pixels are 16 bits instead of 24 bits. This is acceptable since the Xilinx video reference designs use YCbCr 4:2:2 video format.

The following block diagram illustrates the connections between the FMC connector and the HDMI Receiver.

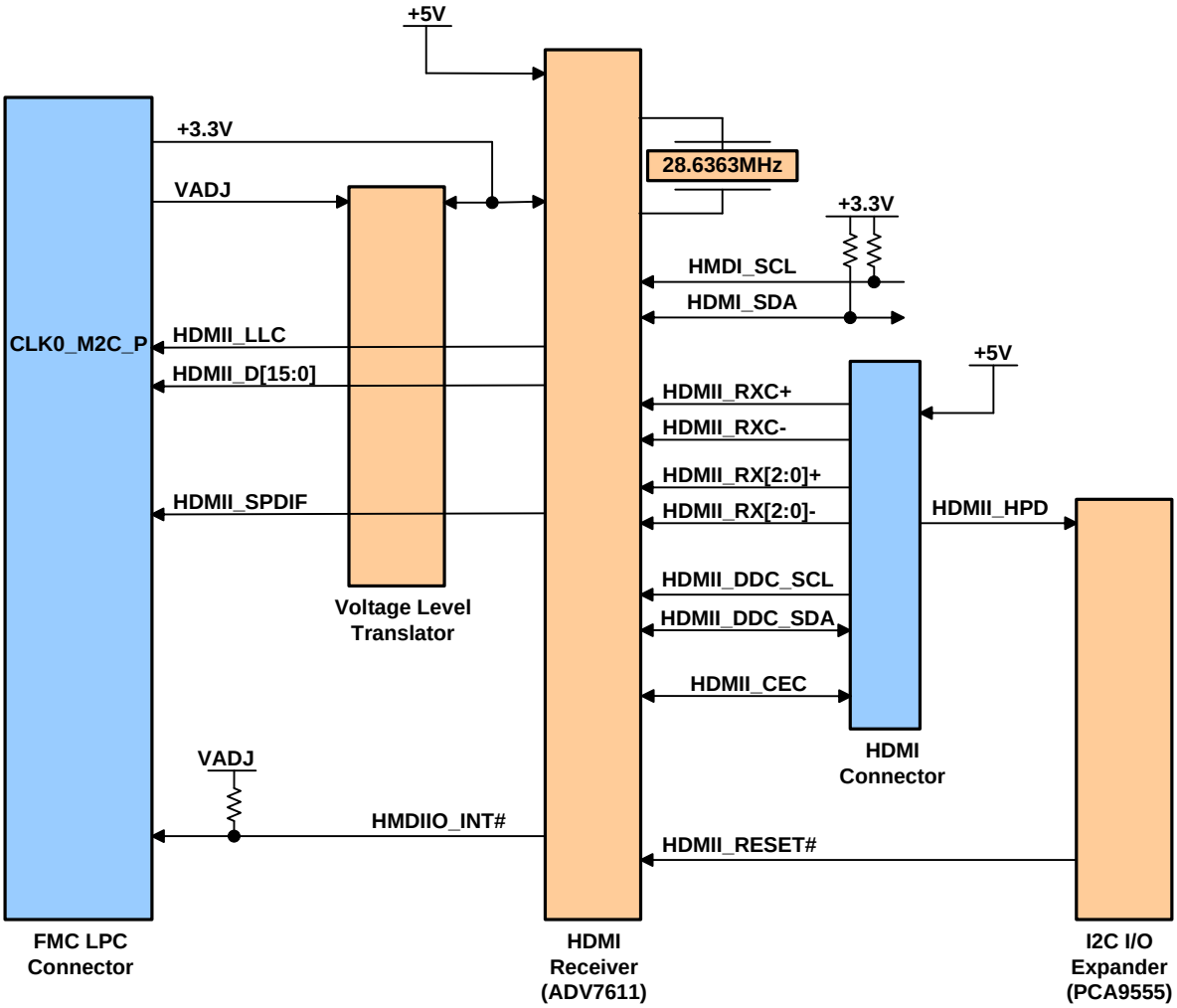

Figure 10 – HDMI Input, Block Diagram

The HDMII_SCL/SDA signals are connected to the I2C MUX device. The HDMII_RST# and HPD signals are connected to an I2C IO Expander device. See the relevant sections for the I2C MUX and I2C IO Expander for details on asserting the signals connected to these devices.

More detailed information on the ADV7611, including a hardware user guide and recommended schematic/layout/bom, can be found on the Analog Devices EngineerZone:
http://ez.analog.com/docs/DOC-1745

2.8 HDMI Output

The HDMI output interface is implemented using the Analog Devices ADV7511 device. This device's input video interface supports YCbCr mode with embedded syncs, which significantly reduce the number of I/O required for the FMC side interface.

By using the YCbCr 4:2:2 mode, the pixels are 16 bits instead of 24 bits. This is acceptable since the Xilinx video reference designs use YCbCr 4:2:2 video format.

The following block diagram illustrates the connections between the FMC connector and the HDMI Transmitter.

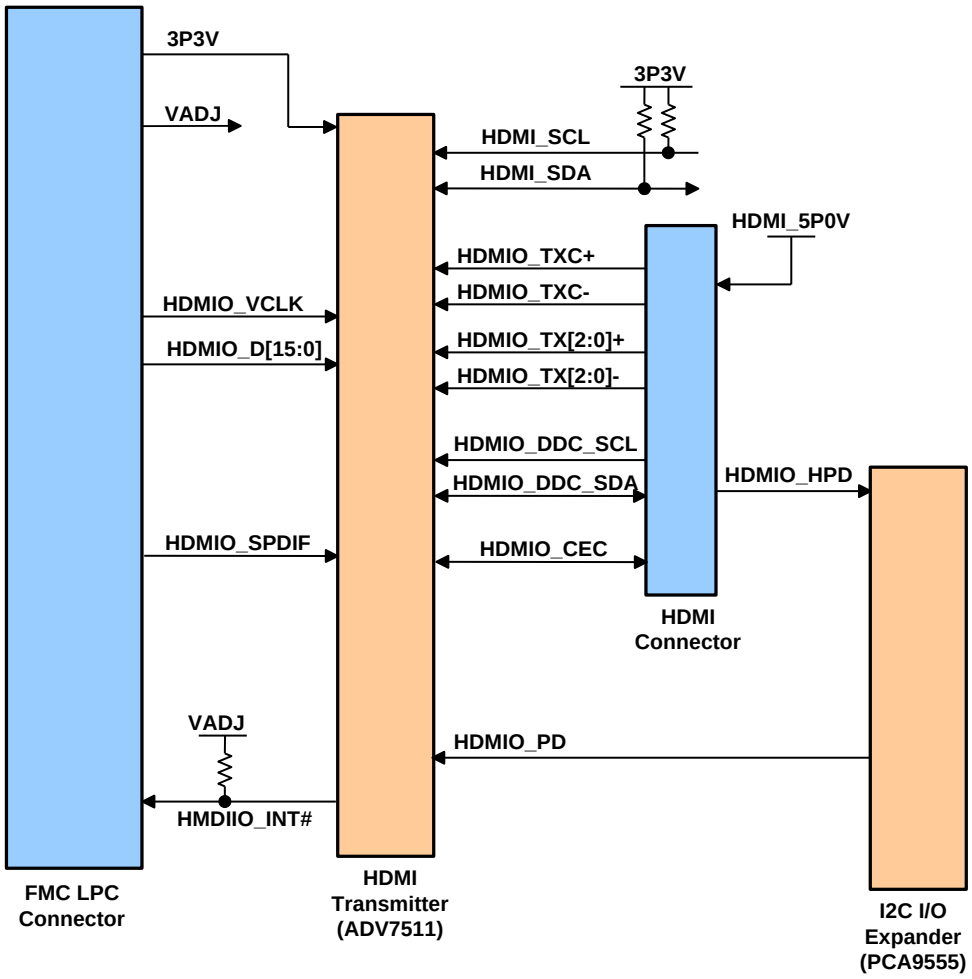

Figure 11 – HDMI Output, Block Diagram

The HDMIO_SCL/SDA and HDMIO_DDC_SCL/SDA signals are connected to an I2C MUX device. The HDMIO_PD and HDMIO_HPD signals connected to an I2C IO Expander device. See the relevant sections for the I2C MUX and I2C IO Expander for details on asserting the signals connected to these devices.

More detailed information on the ADV7511, including a hardware user guide and example schematics/layout, can be found on the Analog Devices EngineerZone:
http://ez.analog.com/docs/DOC-1740

2.9 Camera Interface

The Embedded Vision Carrier Card can accommodate a variety of camera modules with its camera interface, which defines pins for the following functions:

- Configuration & Control (single-ended signals)
  - I2C
  - SPI
  - Reset/Reference Clock
  - Trigger
  - Monitor
  - LED control
- Video (differential signals)
  - CLK
  - SYNC
  - DATA[7:0]
- Power
  - 5V, used by camera modules to create on-board voltages
  - VIO, same as VCCO used for single-ended I/O

2.10 Camera Connector

The connector used to house the Camera Modules is a standard PCI Express connector. The x4 connector is chosen in order to support all the signals required by the camera interface (10 differential pairs, 16 single-ended signals).

The connector chosen for the PCI Express connector is a thru-hole (TH) version depicted in the image below, PCIE-064-02-F-D-TH. The thru-hole (TH) connector is used with vertical PCB guides to hold the camera board at right-angle to the carrier card.

More information is available for the PCI Express connectors at Samtec's website:
http://www.samtec.com/documents/webfiles/pdf/pcie.pdf .

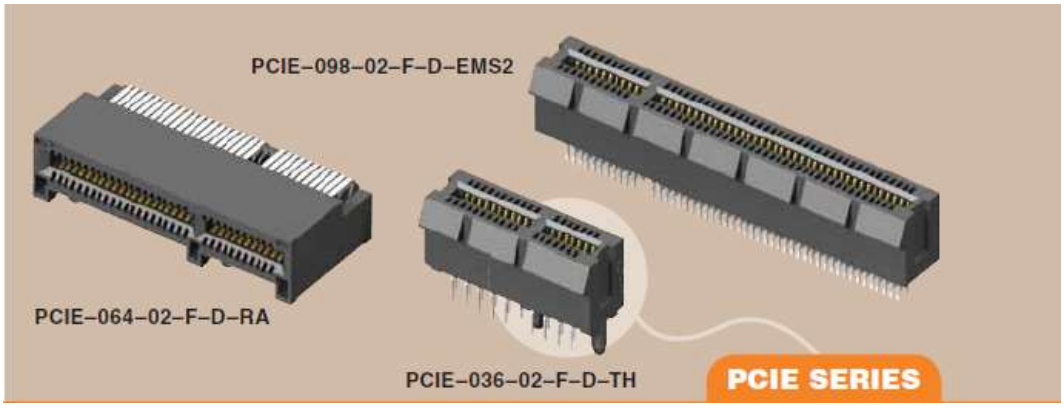

Figure 12 – PCIEx4 Camera Connector

The following table describes the proprietary camera interface pin assignment on the thru-hole (TH) PCIe x4 Lane Connector (Samtec: PCIE-064-02-F-D-TH).

Mapping for Camera Interface	
Side B	**Side A**
PCI Express x1	
GND	GND
+5V	**CAM_REFCLK**
+5V	GND
+5V	**CAM_CLK_P**
+5V	**CAM_CLK_N**
CAM_I2C_SCL	GND
+2.5V	**CAM_DATA0_P**
+2.5V	**CAM_DATA0_N**
CAM_I2C_SDA	GND
+2.5V	**CAM_DATA1_P**
+2.5V	**CAM_DATA1_N**
Key Notch	
CAM_SPI_CLK	GND
GND	**CAM_DATA2_P**
CAM_SPI_CS	**CAM_DATA2_N**
CAM_SPI_MISO	GND
GND	**CAM_DATA3_P**
GND	**CAM_DATA3_N**
CAM_SPI_MOSI	GND
PCI Express x4	
GND	**CAM_DATA4_P**
CAM_RST#	**CAM_DATA4_N**
CAM_PWDN	GND
GND	**CAM_DATA5_P**
CAM_TRIGGER0	**CAM_DATA5_N**
CAM_MONITOR0	GND
CAM_TRIGGER1	**CAM_DATA6_P**
CAM_TRIGGER2	**CAM_DATA6_N**
CAM_MONITOR1	GND
GND	**CAM_DATA7_P**
CAM_USER_IO1	**CAM_DATA7_N**
CAM_USER_IO2	GND
GND	**CAM_SYNC_P**
GND	**CAM_SYNC_N**

Table 9 – Camera Interface Pin Assignments

3.0 Known Issues & Limitations

This section describes the known issues and limitations for the FMC Module.

There currently are no known issues and limitations for the FMC module.

4.0 Revisions

V0.1	First Version (AES-FMC-HDMI-CAM-G)	September 14, 2015