Table of Contents

1.0 Introduction ...............................................................................................................................................................................3
1.1 Description..................................................................................................................................................................................3
1.2 Features .....................................................................................................................................................................................3
1.3 Target Applications ....................................................................................................................................................................3
1.4 Ordering Information ..................................................................................................................................................................4
2.0 Functional Description .................................................................................................................................................................5
  2.1 DAC ..........................................................................................................................................................................................6
    2.1.1 DAC5682Z Digital to Analog Converter ............................................................................................................................6
    2.1.2 DAC5682Z Interface to Baseboard FPGA ........................................................................................................................8
    2.1.3 DAC Serial Interface ............................................................................................................................................................9
    2.1.4 Analog Outputs .................................................................................................................................................................9
  2.2 Quadrature Modulator ...............................................................................................................................................................10
  2.3 DAC Clocking .............................................................................................................................................................................11
  2.4 Power Supply ............................................................................................................................................................................11
3.0 Performance Test Results ...............................................................................................................................................................12

Figures

Figure 1 - Board Picture ......................................................................................................................................................................4
Figure 2 - EXP High-Speed DAC Module Simplified Block Diagram .............................................................................................5
Figure 3 - EXP High-Speed DAC Module ......................................................................................................................................6
Figure 4 - DAC5682Z Functional Block Diagram ...........................................................................................................................7
Figure 5 - DAC Analog Reconstruction Filter Driving Quadrature Modulator ..................................................................................10
Figure 6 - Test Conditions: Complex Tone Generated by DDS ....................................................................................................12

Tables

Table 1 - Ordering Information ..........................................................................................................................................................4
Table 2 - DAC5682Z Data Signals .....................................................................................................................................................8
Table 3 - DAC5682Z Serial Interface .................................................................................................................................................9
Table 4 - EXP High-Speed DAC Module Power Rails .......................................................................................................................11

Copyright © 2009 Avnet, Inc. AVNET and the AV logo are registered trademarks of Avnet, Inc. All other brands are property of their respective owners.
1.0 Introduction

The purpose of this manual is to describe the functionality and contents of the Avnet EXP High-Speed Digital-to-Analog (DAC) Converter Module from Avnet Electronics Marketing. This document includes instructions for operating the board, descriptions of the hardware features and explanations of the example projects.

1.1 Description

The Avnet High-Speed Digital-to-Analog (DAC) Converter Module provides an advanced analog interface in a half EXP form factor to Avnet Xilinx® development platforms with EXP expansion slots. It is compatible with Xilinx Virtex®-5 LX50, LXT/SXT, as well as Xilinx Spartan®-3A DSP development platforms. The module enables dual-channel wideband analog output functions for FPGA-based DSP applications in communications, test and measurement instrumentation, and general-purpose mixed-signal applications.

The EXP High-Speed DAC Converter Module provides two analog outputs using a Texas Instruments DAC5682Z 16-bit, 1 GSPS, 2x–4x interpolating dual-channel DAC. The DAC5682Z features optional signal processing blocks including integrated 2x/4x digital interpolation filters, and onboard PLL-based clock multiplier, programmable via a serial interface port. The 50 Ω transformer coupled DAC outputs include analog reconstruction filters. The combined I & Q channels of the DAC5682Z are available as a 3rd analog output through a Texas Instruments TRF3703 quadrature modulator.

The Avnet Electronics Marketing EXP High-Speed DAC Module, with full support in Xilinx System Generator for DSP, simplifies application development and enables designers to quickly and effectively meet their time-to-market requirements.

1.2 Features

- Half EXP module format
- Dual Channel Digital-to-Analog Converter
  - 1 GSPS sample rate
  - 16-bit resolution
  - Selectable 2x-4x interpolation
  - PLL-based clock multiplier
  - LVDS data interface to FPGA
  - SPI control port
- Transformer coupled, single-ended output
- External or FPGA sourced clock input
- RF output from quadrature modulator

1.3 Target Applications

- Communication systems
- Test and measurement
- Wireless systems
- Mixed signal systems
1.4 Ordering Information

The following table lists the evaluation kit part numbers and available software options. Internet link at http://www.em.avnet.com/drc

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td>AES-EXP-DAC-G</td>
<td>EXP High-Speed Digital-to-Analog Converter Module</td>
</tr>
</tbody>
</table>

Table 1 - Ordering Information
2.0 Functional Description

Figure 2 - EXP High-Speed DAC Module Simplified Block Diagram
2.1 DAC

Figure 3 shows a detailed block diagram of the EXP High-Speed DAC Module.

2.1.1 DAC5682Z Digital to Analog Converter

The EXP High-Speed DAC Module employs the TI DAC5682Z dual-channel 16-bit 1 GSPS digital-to-analog converter (DAC) with wideband LVDS data input, integrated 2x/4x interpolation filters, onboard PLL-based clock multiplier and internal voltage reference.

The DAC5682Z wideband LVDS bus provides full 1.0 GSPS data transfer into a single DAC channel or, by interleaving samples, half-rate data can be interpolated by 2x for the dual DAC mode. An additional 4x interpolation filter is provided for ¼ rate input data bandwidths. Each interpolation filter is configurable in either Low-Pass or High-Pass mode, allowing selection of a higher order output spectral image.

The DAC5682Z supports complex or real output. An optional Fs/4 coarse mixer in complex mode provides coarse frequency upconversion and the dual DAC output produces a complex Hilbert Transform pair.

The DAC5682Z contains internal registers to define the operating modes, configured through its serial interface. A detailed listing of DAC5682Z register settings is available in the datasheet.

The DAC5682Z functional block diagram is shown in Figure 4.
Figure 4 - DAC5682Z Functional Block Diagram
2.1.2 DAC5682Z Interface to Baseboard FPGA

The following signals constitute the digital data interface between the DAC5682Z and the baseboard FPGA:

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>IO Type (relative to DAC5682Z)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SYNC</td>
<td>Input / LVDS</td>
<td>Functions as a combination of Transmit Enable (TXENABLE) and Synchronization trigger. If SYNC is low, the transmit chain is disabled so input data from the FIFO is ignored while zeros are inserted into the data path to the DAC. If SYNC is raised from low to high, a synchronization event occurs with behavior defined by individual control bits in registers CONFIG1, CONFIG5 and CONFIG6. SYNC is sampled synchronous with the data bus.</td>
</tr>
<tr>
<td>CLKIN/CLKINC</td>
<td>Input pair</td>
<td>External clock input. With the clock multiplier PLL enabled, CLKIN provides lower frequency reference clock. If the PLL is disabled, CLKIN directly provides clock for DAC up to 1GHz.</td>
</tr>
<tr>
<td>D(15 … 0)</td>
<td>Input / LVDS</td>
<td>Data bits 0 through 15 D15 is most significant data bit (MSB)</td>
</tr>
<tr>
<td>DCLK</td>
<td>Input / LVDS</td>
<td>Digital clock driven into the DAC synchronous to D(15 … 0)</td>
</tr>
<tr>
<td>RESETB</td>
<td>Input</td>
<td>Resets the chip when low</td>
</tr>
</tbody>
</table>

Table 2 - DAC5682Z Data Signals
2.1.3 DAC Serial Interface

The serial port of the DAC5682Z is a flexible serial interface which provides read/write access to all registers used to define the operating modes of the DAC5682Z. It can be configured as a 3 or 4 pin interface by sif4 in register config_msb. In both configurations, SCLK is the serial interface input clock and SDENB is the serial interface enable signal.

For 3-pin configuration, SDIO is a unidirectional pin for both data in and data out. For 4-pin configuration, SDIO is data in only and SDO is data out only.

The following signals constitute the serial interface between the DAC5682Z and the baseboard FPGA:

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>IO Type (relative to DAC5682Z)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>SDO</td>
<td>Output or Hi-Z</td>
<td>Serial Interface Data, uni-directional data output, if SDIO is an input. SDO is 3-stated when the 3-pin interface mode is selected.</td>
</tr>
<tr>
<td>SDIO</td>
<td>Bidirectional or Input</td>
<td>Serial interface data, bidirectional. Default setting sets SDIO as an input</td>
</tr>
<tr>
<td>SDENB</td>
<td>Active LOW Input</td>
<td>Serial data enable, always an input to the DAC5682Z</td>
</tr>
<tr>
<td>SCLK</td>
<td>Input</td>
<td>Serial Interface Clock</td>
</tr>
</tbody>
</table>

Table 3 - DAC5682Z Serial Interface

2.1.4 Analog Outputs

Each analog output of the EXP High-Speed DAC module can drive a doubly terminated 50 Ω cable through an RF transformer with 4:1 impedance ratio. Note that the center tap of the primary input of the transformer is connected to AVDD to enable a dc current flow.

Applying a 20 mA full-scale output current will produce a 1 VPP output at the secondary of the 4:1 transformer. The low dc-impedance between IOU1 or IOU2 and the transformer center tap sets the center of the ac-signal at AVDD, so the 1 VPP output for the 4:1 transformer results in an output between AVDD +0.5 V and AVDD -0.5 V.
2.2 Quadrature Modulator

The TRF3703 is a low-noise direct quadrature modulator, capable of converting complex modulated signals from baseband or IF directly up to RF. The TRF3703 is ideal for high-performance direct RF modulation from 400 MHz up to 4 GHz. The modulator is implemented as a double-balanced mixer. The RF output block consists of a differential to single-ended converter and an RF amplifier capable of driving a single-ended 50-Ω load without any need of external components. A local oscillator signal should drive SMA connector RF_LO_IN.

Each DAC5682Z channel drives the TRF3703 quadrature modulator through an analog low-pass reconstruction filter.

---

**Figure 5 - DAC Analog Reconstruction Filter Driving Quadrature Modulator**
2.3 DAC Clocking

The DAC5682Z sampling clock is generated by a Texas Instruments CDCM7005 providing accurate low jitter LVPECL differential clock outputs. The CDCM7005 can be configured as a PLL using the on-board 983.04 MHz VCXO, or as a buffer driven from an external clock.

When configured as a PLL, the CDCM7005 synchronizes its output clocks to the VCXO and a single-ended reference clock signal with maximum frequency of 200 MHz. The reference clock signal can be supplied by a choice of:

- On-board 10 MHz oscillator (primary reference input to the CDCM7005)
- External 50-Ohm clock input through an SMA connector (primary reference input to the CDCM7005)
- FPGA-supplied reference clock (secondary reference input to the CDCM7005)

When configured as a buffer, the CDCM7005 is driven from an external clock source connected to SMA connector EXT_VC XO.

Virtex-5 ChipSync LVDS outputs are capable of sourcing data at 1 GSPS, double-data rate to the DAC5682Z. Alternatively, the FPGA may source data at a lower sampling rate; the DAC5682Z contains an internal wideband PLL/VCO to multiply the input sampling clock CLKIN by 2x-32x for digital interpolation in the DAC.

2.4 Power Supply

Power is supplied to the EXP High-Speed DAC Module via +2.5 V and +3.3 V supplies from the baseboard through the EXP High-Speed connector JX1. Several DC-DC converters and voltage regulators generate the appropriate voltage rails for the different devices on the board, as follows:

<table>
<thead>
<tr>
<th>Voltage Rail</th>
<th>Regulator</th>
<th>Devices Powered</th>
</tr>
</thead>
<tbody>
<tr>
<td>+2.0V</td>
<td>TI recommended</td>
<td>DAC5682Z (DVDD)</td>
</tr>
<tr>
<td>+2.0VCLK</td>
<td></td>
<td>DAC5682Z (CLKVDD)</td>
</tr>
<tr>
<td>+3.3V_A</td>
<td></td>
<td>DAC5682Z (AVDD)</td>
</tr>
<tr>
<td>+3.3V</td>
<td></td>
<td>DAC5682Z (IOVDD)</td>
</tr>
<tr>
<td>1.8/3.3/1.8V</td>
<td></td>
<td>CDCM7005 (DVDD/ IOVDD / DVDD)</td>
</tr>
</tbody>
</table>

Table 4 - EXP High-Speed DAC Module Power Rails
3.0 Performance Test Results

<table>
<thead>
<tr>
<th>Baseband Analog Outputs A &amp; B</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCXO ¹</td>
</tr>
<tr>
<td>SFDR</td>
</tr>
<tr>
<td>SNR</td>
</tr>
</tbody>
</table>

DAC Outputs

1. VCXO 983.04 MHz / Vectron VS-705-LFF-GAAN
2. VCXO 983.04 MHz / Silicon Labs 550AD983M040DG
3. Agilent 8644 983.04 MHz

Figure 6 - Test Conditions: Complex Tone Generated by DDS

<table>
<thead>
<tr>
<th>TRF3703 Quadrature Modulator RF Output</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Local oscillator and sideband suppression</td>
<td>-40 dBc</td>
</tr>
</tbody>
</table>