256MB DDR3 1600 MEMORY

DDR3 ADDR & CNTRL TERMINATION RESISTORS

DDR3 TERMINATION REGULATOR

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DDDR single-ended traces are 40 Ohm impedance.
DDDR Differential traces are 80 Ohm differential impedance.

AS DDR RAM traces are matched length and less than
2540 mils (65 mm). The below information is general guidance
and is pending the P44 board material composition and stock up.
Address and command trace spacing is 10 mil min for short runs,
4 mils clearance for parallel runs less than 500 mils.
Data trace spacing is 10 mil min for short runs, 4 mils clearance
for parallel runs less than 500 mils.

Place clock signals on internal layers to minimize EMI.

For further information, see Micron's Tech Notes: TN4113 &
TN-52-02
VCCD = +3.3V

PROG_PB RESET

BOOT MODE SELECT

FPGA DONE LED

DUAL JTAG

SMT2 JTAG

PC4 JTAG

Layout Note:
JTAG circuit routing should adhere to the following guidelines:
1. JTAG signals should be routed on the outer layers away from noisy analog sources
2. Route TCK and TMS in a star topology away from noisy analog sources

Avnet Engineering Services

Artix_7A50T

06 - BANK 0, SMT2 JTAG, BOOT MODE.SchDoc

Project Name:

Artix_7A50T

Date: 4/7/2015

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LAYOUT NOTE:
All PMOD signals routed differentially (PIN pairs) and length tuned to each other on each header.

LAYOUT NOTE:
Place resistors and capacitors as close as possible to FPGA.
LAYOUT NOTE:
Place FB resistors close to REGs.
Place Monitor points (VM) close to loads.
BOARD POWER SUPPLIES

POWER SEQUENCE:
1V -> 1.9V -> VDDR & 3.3V

DESIGN NOTES - VDDR ADJUSTMENTS:
For VDDR = 1.35V, R106 = 19.6K, R105 = 28.7K
For VDDR = 1.5V (default), R106 = 23.2K, R105 = 26.7K

DESIGN NOTES - VRAM ADJUSTMENTS:
For VRAM = 1.00V, R95 = 16.2K
For VRAM = 0.95V, R95 = 13.3K

LAYOUT NOTE:
Place FB resistors close to U13. Place VM monitor points close to loads.