AN11243

Failure signature of electrical overstress on power MOSFETs

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Document information

Info	Content
Keywords	Power MOSFETs, Electrical Overstress (EOS), Unclamped Inductive Switching (UIS)
Abstract	When Power MOSFETs fail, there is often extensive damage. Examination of the size and location of the burn mark, the failure signature, provides information about the type of fault condition which caused the failure. This document provides a catalogue of failure signatures from common electrical overstress failure modes. The catalogue can be used in forensic investigation of the underlying root cause of failure to improve module design and reliability.

Revision history

Rev	Date	Description
01	20121029	first issue

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1. Introduction

Power MOSFETs are used to switch high voltages and currents, while minimizing their own internal power dissipation. Under fault conditions however, it is possible to apply voltage, current and power exceeding the MOSFET capability. Fault conditions can be either due to an electrical circuit failure or a mechanical fault with a load such as a seized motor. This leads to Electrical Overstress (EOS). Typically the consequence of EOS is the short circuiting of at least 2 of the 3 MOSFET terminals (gate, drain, source). In addition, high local power dissipation in the MOSFET leads to MOSFET damage which manifests as burn marks, die crack and in extreme cases as plastic encapsulation damage.

Examination of the size and location of the burn mark, the failure signature, provides information about the type of fault condition which caused the failure. Common fault conditions are:

- ElectroStatic Discharge (ESD)
- Unclamped Inductive Switching (UIS) - commonly called Avalanche or Ruggedness
- Linear Mode operation
- Over-current

Packaged MOSFETs have been deliberately destroyed under these conditions. Images recorded of the ensuing burn marks on the silicon surface, provide a ‘Rogue’s Gallery’ to aid the explanation of EOS failures.

Section 1.1 to Section 1.5 gives an overview of the common failure signatures.

Appendices in Section 2.1 to Section 2.15 provide further images.

1.1 ESD - Machine Model

1.1.1 EOS method

ESD pulses were applied using a standard Machine Model ESD circuit; for details see *AEC - Q101-002 - REV-A - July 18, 2005*. Voltage of the applied pulse was progressively increased until device failure was observed.

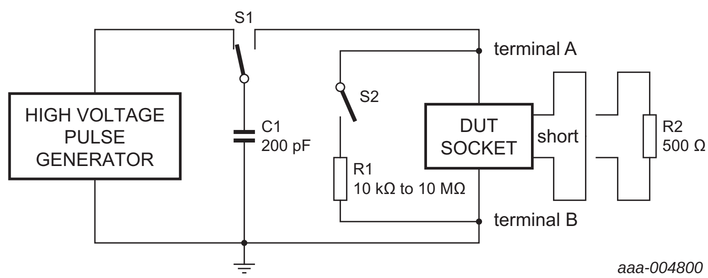


Fig 1. Typical circuit for Machine Model ESD simulation

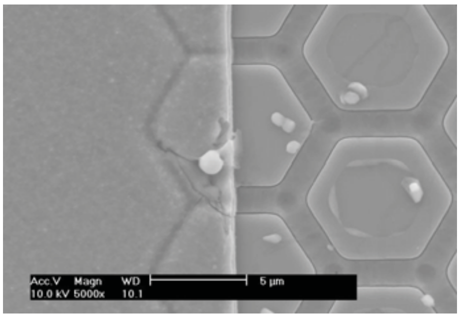
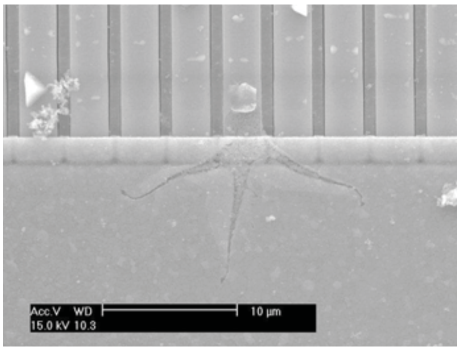
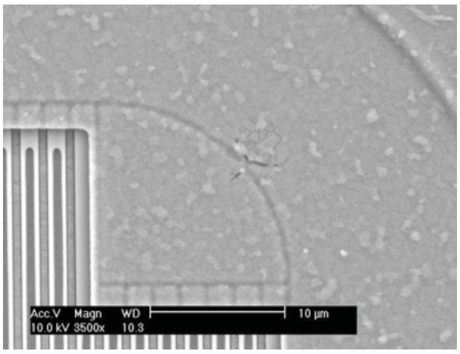
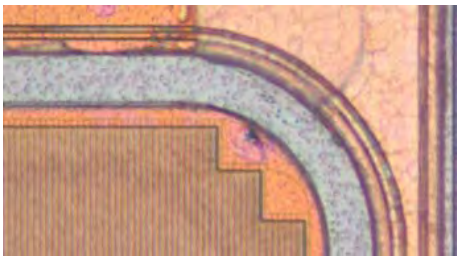
1.1.2 Fault condition simulated

Machine model ESD simulates situations when a voltage spike is applied to the MOSFET exceeding the maximum voltage that can be sustained by the gate oxide between either gate-source or gate-drain. The pulse is applied with minimal series resistance between the voltage origin and the MOSFET, resulting in rapid rise of the MOSFET gate voltage. Electrical test equipment or malfunctioning circuits can easily apply such voltage pulses.

1.1.3 Signature

An edge cell of the MOSFET structure is a failure site that is normally located close to the gate. Outer edge cells and cells near the gate are the first to be subjected to the incoming voltage pulse. As a result, these cells are the first sites where the voltage exceeds the gate-oxide capability.

Table 1. Examples of Machine Model ESD failure signature

Device name	Cell pitch (µm)	Image	Comments
BUK9508-55A	9 (hexagon)	 aaa-004801	Fail site is gate oxide of edge cell; see Section 2.1 "Machine model EOS of BUK9508-55A" for further images
BUK9Y40-55B	4 (stripe)	 aaa-004803	Fail site is gate oxide of edge cell; see Section 2.2 "Machine model EOS of BUK9Y40-55B" for further images
PSMN7R0-30YL	2 (stripe)	 aaa-004853	Fail site is gate oxide of edge cell; see Section 2.3 "Machine model EOS of PSMN7R0-30YL" for further images
PSMN011-30YL	2 (stripe)	 aaa-004854	Fail site is gate oxide of edge cell; see Section 2.4 "Machine model EOS of PSMN011-30YL" for further images

1.2 ESD - Human body model

1.2.1 EOS method

ESD pulses were applied using a standard Human-body Model ESD circuit; for details see *AEC - Q101 - REV - May 15, 1996*. Voltage of the applied pulse was progressively increased until device failure was observed.

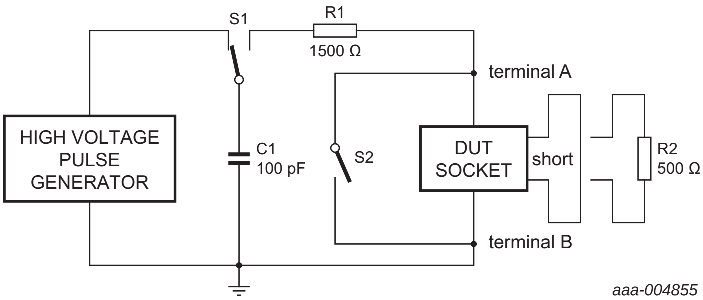


Fig 2. Typical circuit for Human body Model ESD simulation

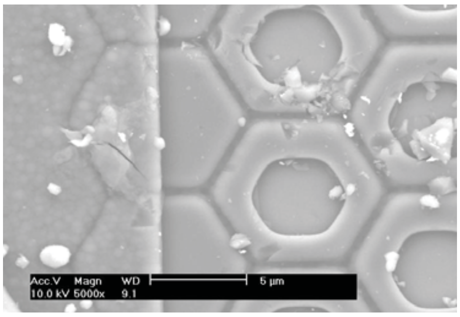
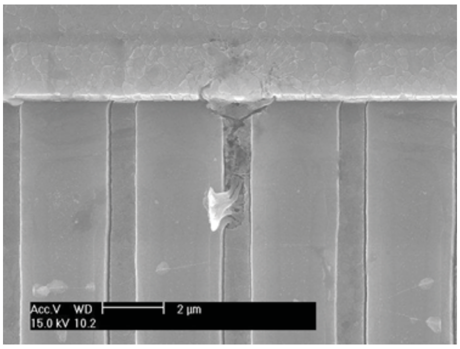
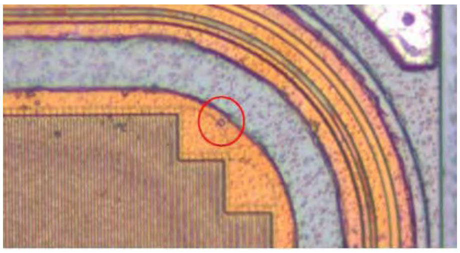
1.2.2 Fault condition simulated

Human body model ESD simulates situations when a voltage spike is applied to the MOSFET exceeding the maximum voltage that can be sustained by the gate oxide of either gate-source or gate-drain. The pulse is applied with 1500 Ω series resistance between the voltage origin and the MOSFET, which limits the rate of rise of the MOSFET gate voltage. Either human handling, electrical test equipment or malfunctioning circuits can easily apply such voltage pulses.

1.2.3 Signature

Failure site is found in an edge cell of the MOSFET structure. Outer edge cells and cells near the gate are the first to be subjected to the incoming voltage pulse and are thus the first sites where the voltage exceeds the gate-oxide capability. The signature differs from Machine Model failures in that the fail site does not show such a strong tendency to group near the gate, due to the slower rise in gate voltage.

Table 2. Examples of Human Body Model ESD failure signature

Device name	Cell pitch (µm)	Image	Comments
BUK9508-55A	9 (hexagon)	 aaa-004856	Fail site is gate oxide of edge cell; see Section 2.5 “Human body model EOS of BUK9508-55A” for further images
BUK9Y40-55B	4 (stripe)	 aaa-004857	Fail site is gate oxide of edge cell; see Section 2.6 “Human body model EOS of BUK9Y40-55B” for further images
PSMN011-30YL	2 (stripe)	 aaa-004858	Fail site is gate oxide of edge cell; see Section 2.7 “Human body model EOS of PSMN011-30YL” for further images

1.3 Unclamped Inductive Switching (UIS) (Avalanche or Ruggedness)

1.3.1 EOS method

Inductive energy pulses were applied using a standard UIS circuit; for details see *AEC - Q101-004 - REV - May 15, 1996*. A fixed inductance value is elected. Current in the inductance prior to switching the MOSFET was progressively increased until device failure was observed.

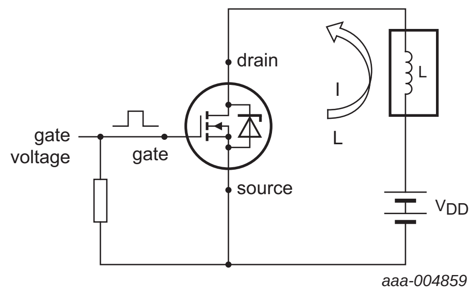


Fig 3. Circuit diagram for UIS ruggedness test

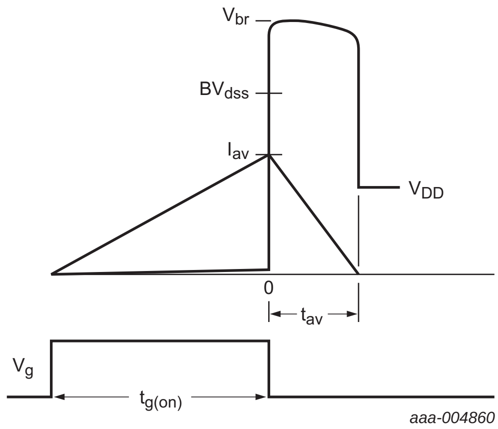


Fig 4. Waveforms obtained from UIS test

1.3.2 Fault condition simulated

UIS simulates situations when a MOSFET is switched off in a circuit in which there is inductance. The inductance can be deliberate (such as an injector coil in a diesel engine system), or parasitic. As the current cannot decay to zero instantaneously through the inductance, the MOSFET source-drain voltage increases to take the device into avalanche breakdown. The energy stored in the inductance is then dissipated in the MOSFET.

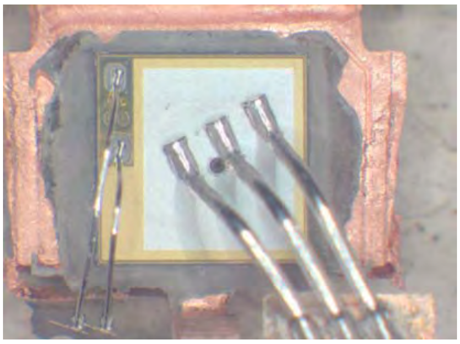
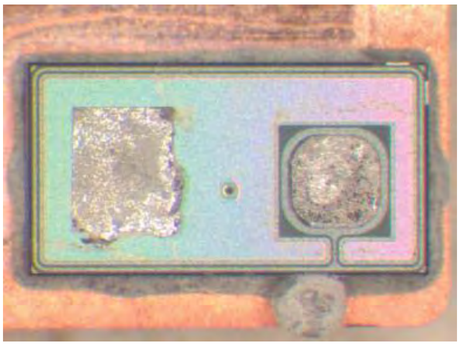
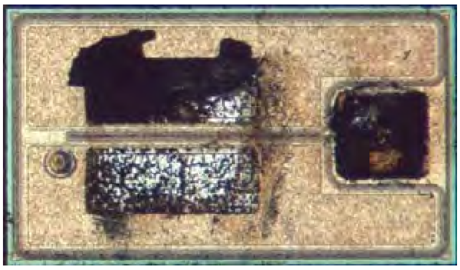
1.3.3 Signature

Failure site is found in an active MOSFET cell. The burn-mark is usually round in shape, indicating a central failure site and subsequent thermal damage.

If the avalanche event is long in duration (~ ms), then burn marks locate at central sites on the die, where there is maximum current flow and reduced heat dissipation. The sites are often adjacent to wire bonds/clip bonds where current density is high, but not directly under the wire bond/clip bond as it provides a local heat sink. Failure is at the hottest location of the die.

For short avalanche events (~ μs), the burn marks can take on more random locations over the die surface. The temperature rise in the chip is more uniform with negligible chance for current crowding and local heating on these time scales. For even shorter avalanche events, the burn marks can locate at die corners due to the discontinuity in cell structure at these locations.

Table 3. Examples of unclamped inductive switching failure signature

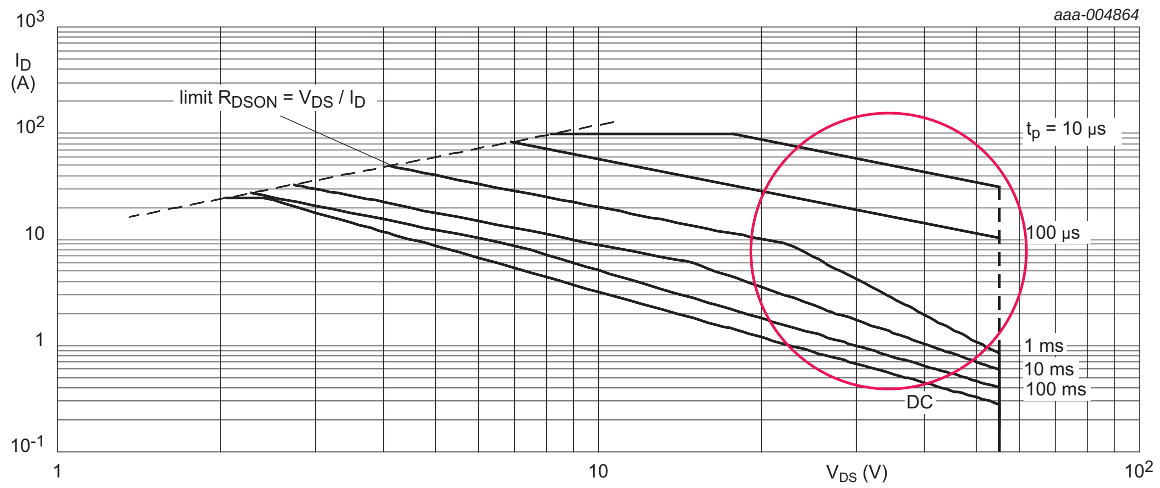
Device name	Cell pitch (µm)	Image	Comments
BUK7L06-34ARC	9 (hexagon)	 aaa-004861	round burn in active area; see Section 2.8 “Unclamped inductive switching EOS of BUK7L06-34ARC” for further images
BUK9Y40-55B	4 (stripe)	 aaa-004862	round burn in active area; see Section 2.9 “Unclamped Inductive Switching EOS of BUK9Y40-55B” for further images
PSMN7R0-30YL	2 (stripe)	 aaa-004863	round burn in active area; see Section 2.10 “Unclamped inductive switching EOS of PSMN7R0-30YL” for further images

1.4 Linear mode operation

1.4.1 EOS method

A Safe Operating Area (SOA) graph is included in all power MOSFET data sheets. Outside the defined safe region, the power dissipated in the FET cannot be removed, resulting in heating beyond the device capability and then device failure.

MOSFETs were taken and a fixed source-drain voltage applied. Current pulses of defined duration were applied and the current was increased until MOSFET failure was observed.



T_{mb} = 25 °C; I_{DM} is a single pulse.

Fig 5. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

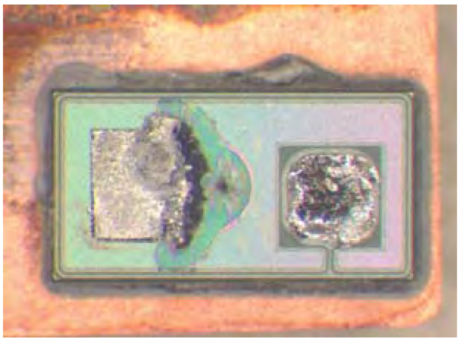
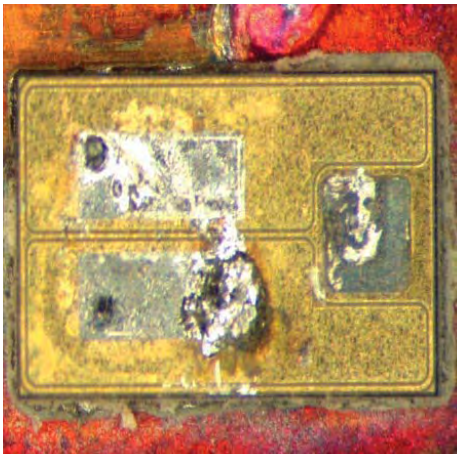
1.4.2 Fault condition simulated

Linear mode operation is common during device switching or clamped inductive switching and is not a fault condition unless the SOA is exceeded. Linear mode EOS simulates situations when a MOSFET is operated in Linear mode for too long. This situation can also occur if, when intending to turn the FET on, the gate signal voltage to the FET is too low. This condition can also arise when intending to hold the FET in the Off-state with high drain-source voltage. If the gate connection is lost, the gate voltage capacitively rises and the same Linear mode fault condition occurs.

1.4.3 Signature

The hottest location of the die is a failure site that is usually at central sites on the die. The center of the die is where there is maximum current flow and reduced heat dissipation. The sites are often adjacent to wire bonds/clip bonds where current density is high, but not directly under the wire bond/clip bond as it provides a local heat sink.

Table 4. Examples of linear mode failure signature

Device name	Cell pitch (μm)	Image	Comments
BUK7L06-34ARC	9 (hexagon)	 aaa-004865	Burns located in center of die adjacent to wire-bonds; see Section 2.11 "Linear mode EOS of BUK7L06-34ARC" for further images
BUK9Y40-55B	4 (stripe)	 aaa-004866	Burn adjacent to location of clip bond in center of die; see Section 2.12 "Linear mode EOS of BUK9Y40-55B" for further images
PSMN7R0-30YL	2 (stripe)	 aaa-004867	Burn adjacent to location of clip bond in center of die; see Section 2.13 "Linear mode EOS of PSMN7R0-30YL" for further images

1.5 Over-current

1.5.1 EOS method

The maximum current-handling capability is specified on the data sheet for Power MOSFETs. This capability is based on the current handling capability of wires or clips, before which fusing will onset, combined with the ability to dissipate heat. Exceeding this rating can result in catastrophic failure.

I_D	drain current	V_{GS} = 10 V; T_{mb} = 100 °C; see Figure 1	-	53	A
		V_{GS} = 10 V; T_{mb} = 25 °C; see Figure 1	-	76	A
I_{DM}	peak drain current	t_p ≤ 10 µs; pulsed; T_{mb} = 25 °C; see Figure 3	-	260	A

aaa-005071

Fig 6. Example of maximum current rating from the data sheet of PSMN7R0-30YL

1.5.2 Fault condition simulated

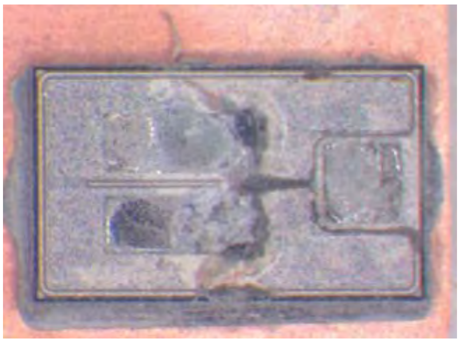
Over-current occurs if a FET is turned on with no element in the circuit to limit the current, resulting in a supply voltage being applied fully over the drain-source terminals of the FET. Typically this occurs if a load has been short-circuited. Alternatively if 2 FETs are operating in a half-bridge, over-current can ensue if both are turned on together.

1.5.3 Signature

Failure site is initially where the current handling connections (wires or clips) meet the die. Normally damage is extensive however in over-current conditions, and spreads over the entire die surface with evidence of melted metallization and solder joints.

For wire-bonded packages, there is often evidence of fused wires. For clip-bonded packages, die crack is commonly observed.

Table 5. Examples of over-current failure signature

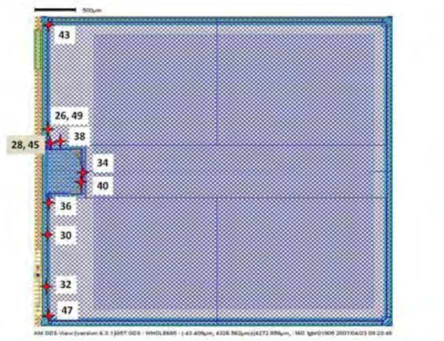
Device name	Cell pitch (μm)	Image	Comments
BUK7L06-34ARC	9 (hexagon)	 aaa-004868	Burns located in center of die adjacent to wire-bonds. Secondary damage of remelted top metal and solder die attach; see Section 2.14 "Over-current EOS of BUK7L06-34ARC" for further images
PSMN7RO-30YL	2 (stripe)	 aaa-004869	Burn adjacent to location of clip bond in center of die; see Section 2.15 "Over-current EOS of PSMN7R0-30YL" for further images

2. Appendices

2.1 Machine model EOS of BUK9508-55A

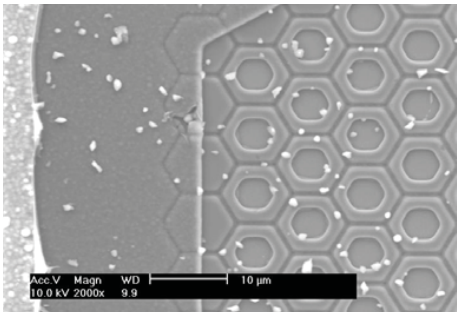
Table 6. Machine model EOS

BUK9508-55A	
Cell structure:	9 mm hexagons
Package:	TO-220
Die size:	5.5 mm × 4.5 mm
EOS condition:	1.1 kV MM pulse



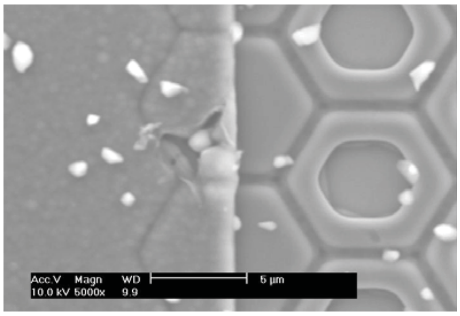
aaa-004875

Fails located in edge cells, in the vicinity of the gate contact



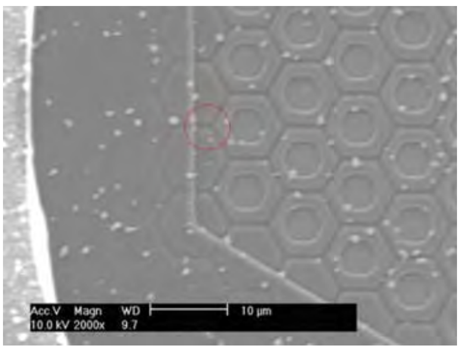
aaa-004876

Fig 7. Sample image 43; after Al removal



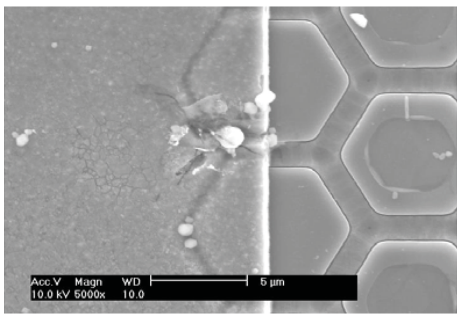
aaa-004877

Fig 8. Sample image 43; after Al removal, close-up



aaa-004878

Fig 9. Sample image 47; after Al removal, no visible damage at hot spot



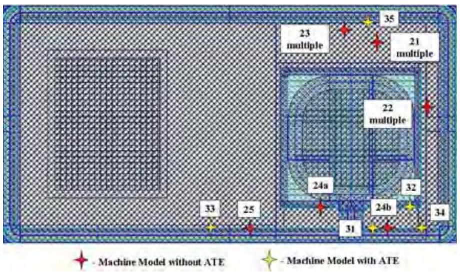
aaa-004879

Fig 10. Sample image 47; after TEOS removal, close-up

2.2 Machine model EOS of BUK9Y40-55B

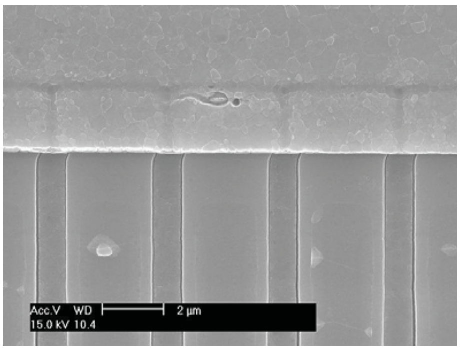
Table 7. Machine model EOS

BUK9Y40-55B	
Cell structure:	4 µm stripe
Package:	LFPAK (clip bond)
Die size:	2.5 mm × 1.35 mm
EOS condition:	200 V to 240 V MM pulse



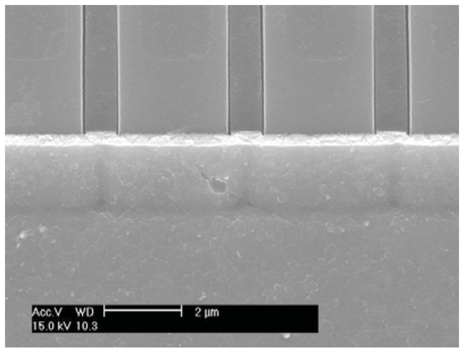
aaa-004880

Fails located mostly in edge cells, in the vicinity of the gate contact. Some fails subjected to ATE testing to create additional damage to highlight fail site



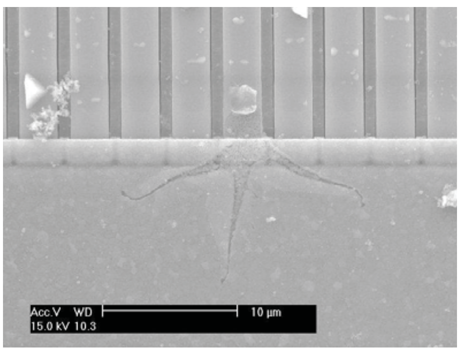
aaa-004881

Fig 11. Sample image 24; after TEOS removal



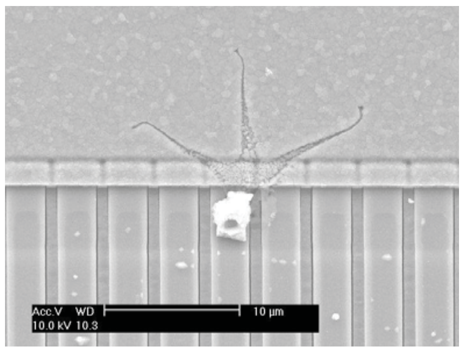
aaa-004882

Fig 12. Sample image 25; after TEOS removal



aaa-004883

Fig 13. Sample image 31; after ATE testing and after TEOS removal



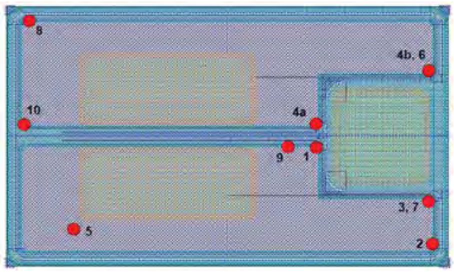
aaa-004884

Fig 14. Sample image 32; after ATE testing and after TEOS removal

2.3 Machine model EOS of PSMN7R0-30YL

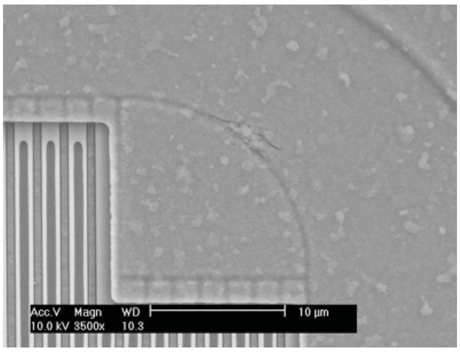
Table 8. Machine model EOS

PSMN7R0-30YL	
Cell structure:	2 μm stripe
Package:	LFPAK (clip bond)
Die size:	2.5 mm × 1.35 mm
EOS condition:	200 V to 270 V MM pulse



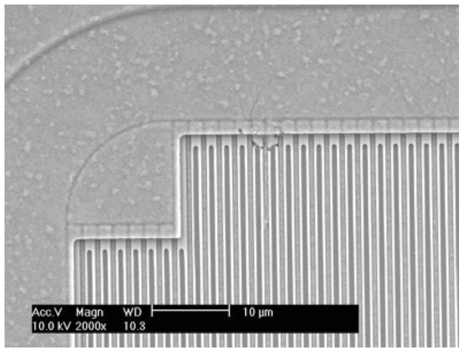
aaa-004885

Fails located mostly in edge cells, in the vicinity of the gate contact



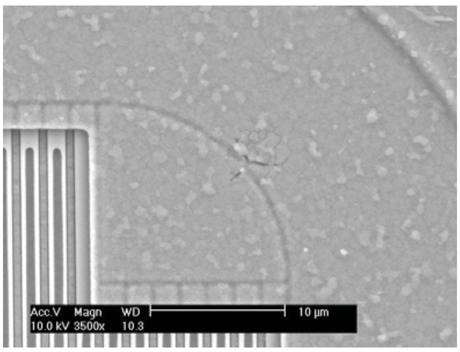
aaa-004886

Fig 15. Sample image 1; after TEOS removal



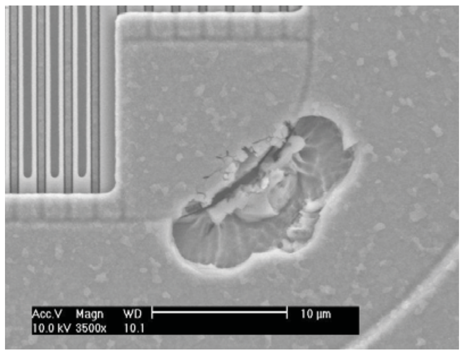
aaa-004887

Fig 16. Sample image 8; after TEOS removal



aaa-004888

Fig 17. Sample image 3; after TEOS removal



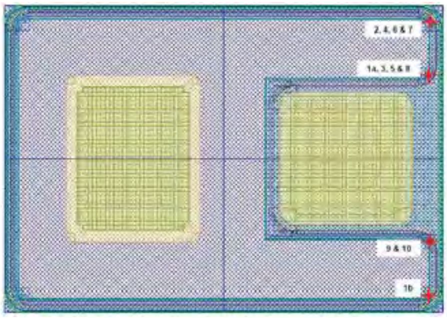
aaa-004889

Fig 18. Sample image 6; after TEOS removal

2.4 Machine model EOS of PSMN011-30YL

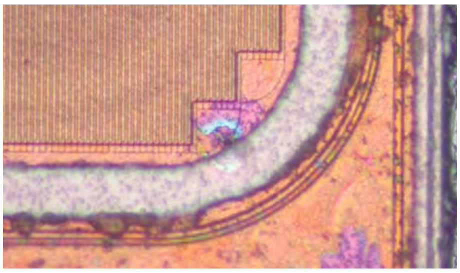
Table 9. Machine model EOS

PSMN011-30YL	
Cell structure:	2 µm stripe
Package:	LFPAK (clip bond)
Die size:	1.7 mm × 1.2 mm
EOS condition:	200 V to 210 V MM pulse



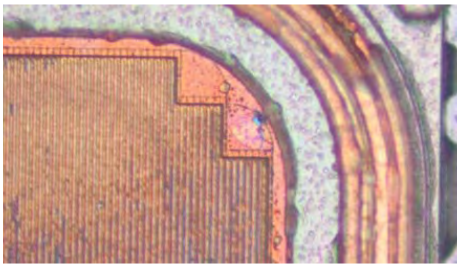
aaa-004890

Fails located mostly in corner edge cells, in the vicinity of the gate contact



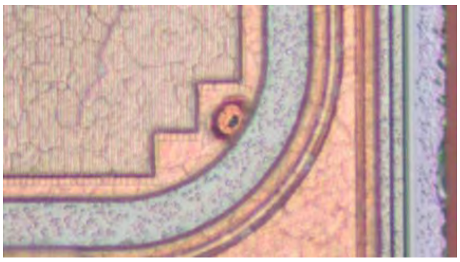
aaa-004891

Fig 19. Sample image 3; after Al removal



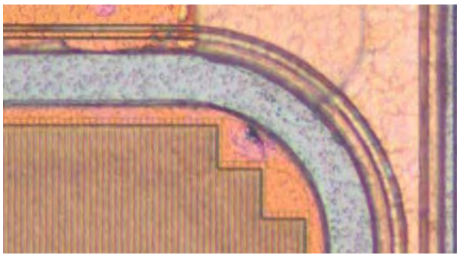
aaa-004892

Fig 20. Sample image 6; after Al removal



aaa-004893

Fig 21. Sample image 8; after Al removal



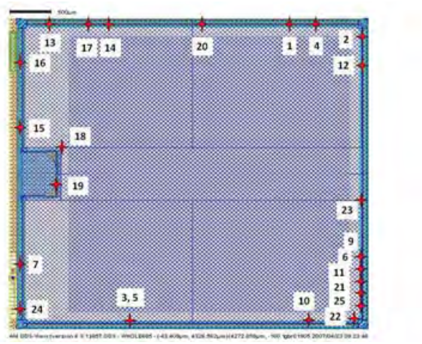
aaa-004894

Fig 22. Sample image 10; after Al removal

2.5 Human body model EOS of BUK9508-55A

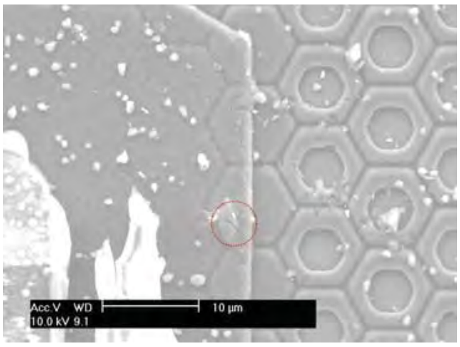
Table 10. Human body model EOS

BUK9508-55A	
Cell structure:	9 mm hexagons
Package:	TO-220
Die size:	5.5 mm × 4.5 mm
EOS condition:	5 kV HBM pulse



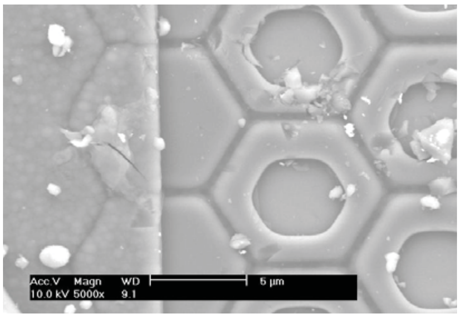
aaa-004899

Fails located in edge cells, distributed around edge of device



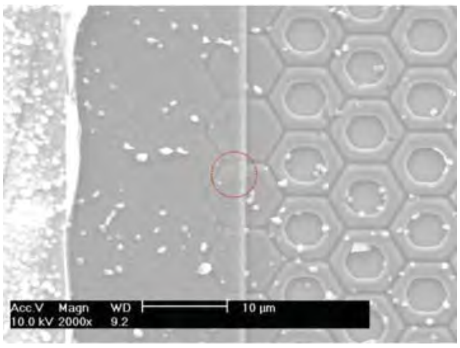
aaa-004900

Fig 23. Sample image 4; after Al removal



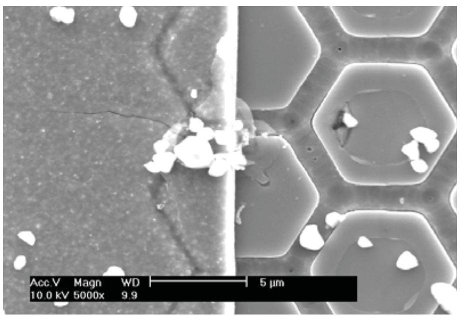
aaa-004901

Fig 24. Sample image 4; after Al removal, close-up



aaa-004902

Fig 25. Sample image 19; after Al removal



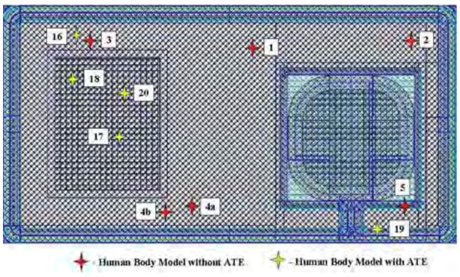
aaa-004903

Fig 26. Sample image 19; after TEOS removal, close-up

2.6 Human body model EOS of BUK9Y40-55B

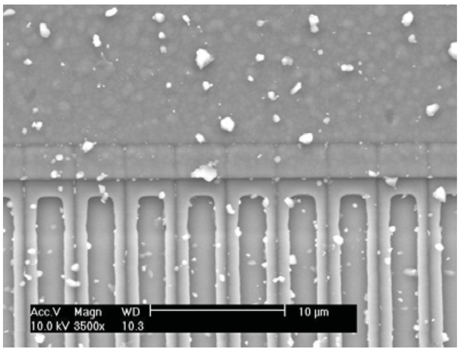
Table 11. Human body model EOS

BUK9Y40-55B	
Cell structure:	4 μm stripe
Package:	LFPAK (clip bond)
Die size:	2.5 mm × 1.35 mm
EOS condition:	450 V to 650 V HBM pulse



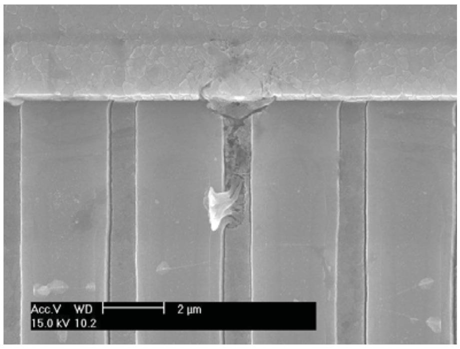
aaa-004904

Fails located randomly over die with increased grouping in edge cells. Some fails subjected to ATE testing to create additional damage to highlight fail site



aaa-004905

Fig 27. Sample image 5; after Al removal



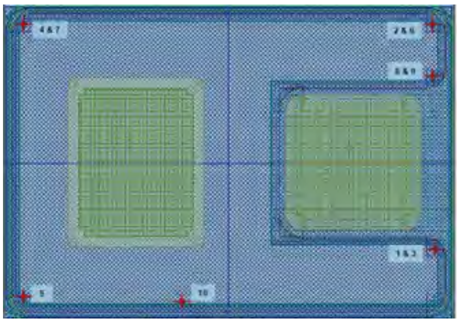
aaa-004906

Fig 28. Sample image 5; after TEOS removal, close-up

2.7 Human body model EOS of PSMN011-30YL

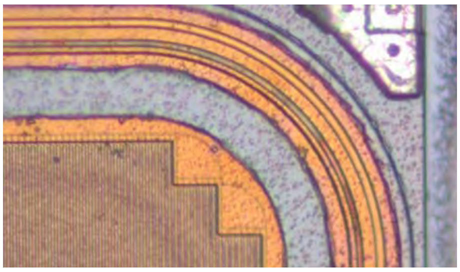
Table 12. Human body model EOS

PSMN011-30YL	
Cell structure:	2 µm stripe
Package:	LFPAK (clip bond)
Die size:	1.7 mm × 1.2 mm
EOS condition:	200 V to 210 V HBM pulse



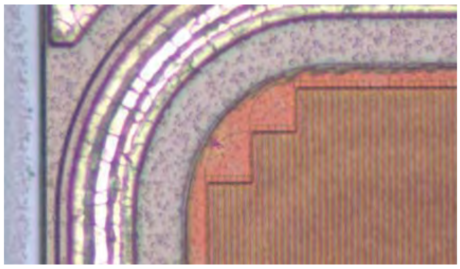
aaa-004907

Fails located in edge cells



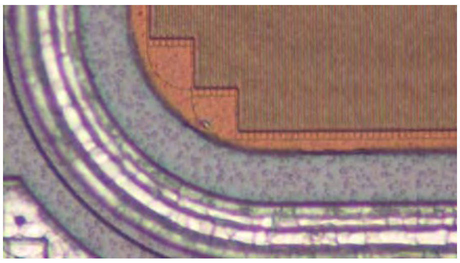
aaa-004908

Fig 29. Sample image 2; after Al removal



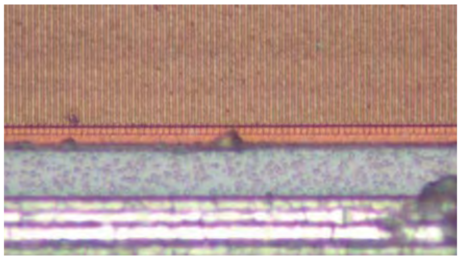
aaa-004909

Fig 30. Sample image 4; after Al removal



aaa-004910

Fig 31. Sample image 5; after Al removal



aaa-004911

Fig 32. Sample image 10; after Al removal

2.8 Unclamped inductive switching EOS of BUK7L06-34ARC

Table 13. Unclamped inductive switching EOS

BUK7L06-34ARC		
Cell structure:	9 mm hexagons	Small round burn marks, randomly distributed over active area, close to but not directly under wire-bonds
Package:	TO-220 (clip bond)	
Die size:	4.3 mm × 4.3 mm	
EOS condition:	0.2 mH; 80 A to 110 A	

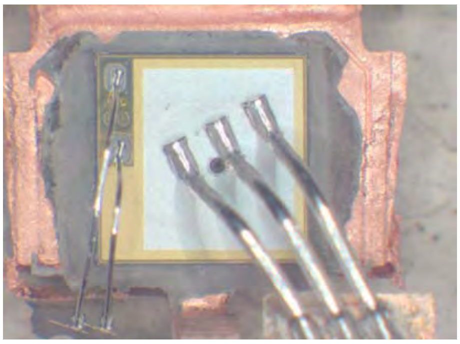

aaa-004912

Fig 33. Sample image 1

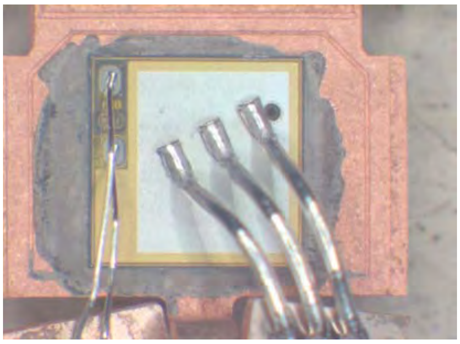

aaa-004913

Fig 34. Sample image 2

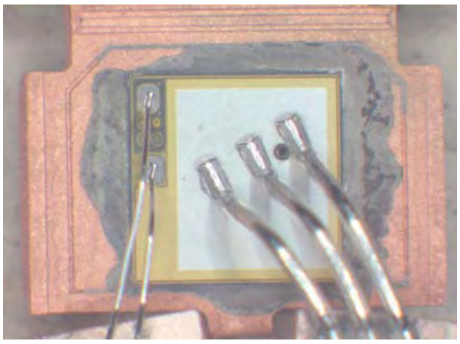

aaa-004914

Fig 35. Sample image 3

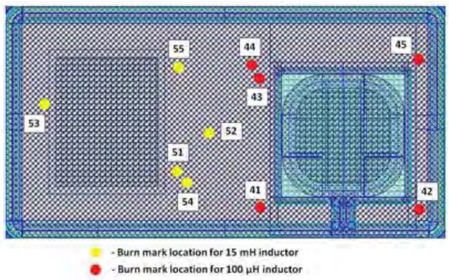

aaa-004915

Fig 36. Sample image 4

2.9 Unclamped Inductive Switching EOS of BUK9Y40-55B

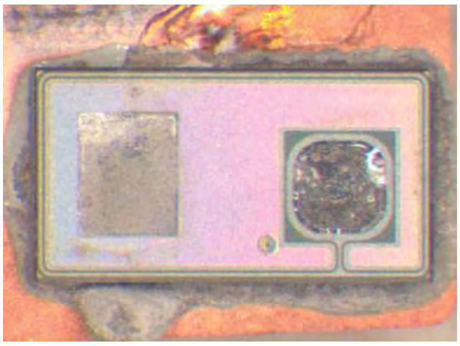
Table 14. Unclamped inductive switching EOS

BUK9Y40-55B	
Cell structure:	4 µm stripe
Package:	LFPAK (clip bond)
Die size:	2.5 mm × 1.35 mm
EOS condition:	Red dots: 0.1 mH, 76 A to 80 A Yellow dots: 15 mH, 7 A to 9 A



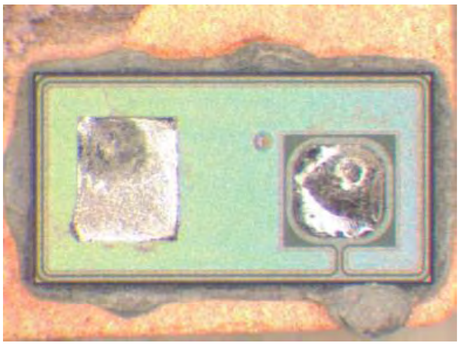
aaa-004916

Small round burn marks, randomly distributed over active area, close to but not directly under clip bond



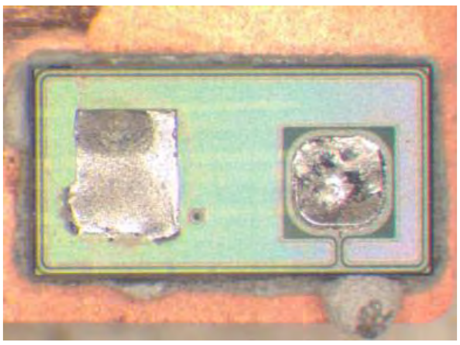
aaa-004917

Fig 37. Sample image 41; 0.1 mH



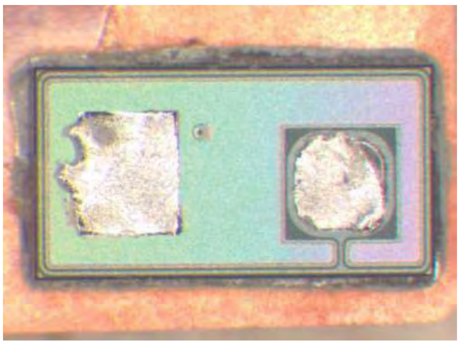
aaa-004918

Fig 38. Sample image 43; 0.1 mH



aaa-004919

Fig 39. Sample image 51; 15 mH

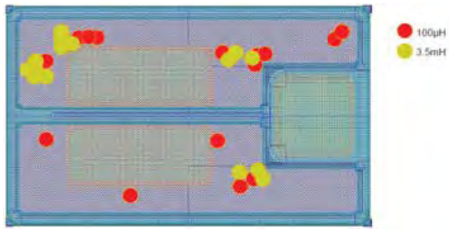


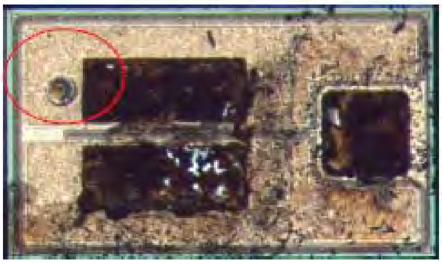
aaa-004920

Fig 40. Sample image 55; 15 mH

2.10 Unclamped inductive switching EOS of PSMN7R0-30YL

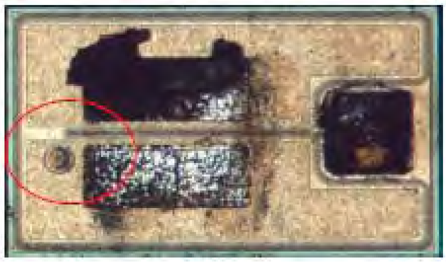
Table 15. Unclamped inductive switching EOS

PSMN011-30YL		
Cell structure:	2 µm stripe	 aaa-004921
Package:	LFPAK (clip bond)	
Die size:	2.3 mm × 1.35 mm	
EOS condition:	Red dots: 0.1 mH, 48 A to 51 A Yellow dots: 3.5 mH, 16 A to 18 A	
		Small, round, burn marks, randomly distributed over active area, close to but not directly under clip bond



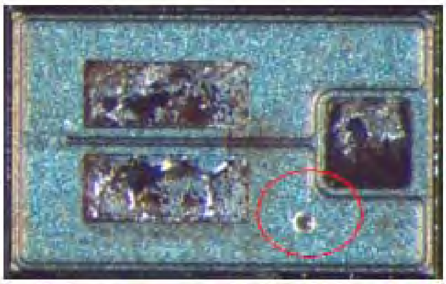
aaa-004922

Fig 41. Sample image 6; 0.1 mH



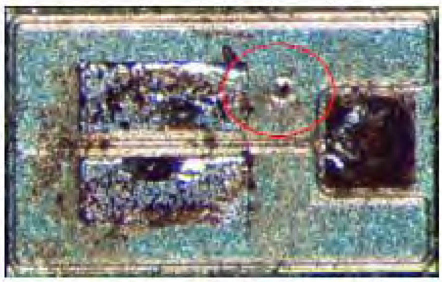
aaa-004923

Fig 42. Sample image 8; 0.1 mH



aaa-004924

Fig 43. Sample image 18; 3.5 mH



aaa-004925

Fig 44. Sample image 20; 3.5 mH

2.11 Linear mode EOS of BUK7L06-34ARC

Table 16. Linear mode EOS

BUK7L06-34ARC	
Cell structure:	9 mm hexagon
Package:	TO-220 (clip bond)
Die size:	4.3 mm × 4.3 mm
EOS condition:	
15 V, 3 A	Burn marks located in middle of the die adjacent to wire bonds
30 V, 1.5 A	Burn mark and location are more discrete at 20 V, 1.5 A

aaa-004926

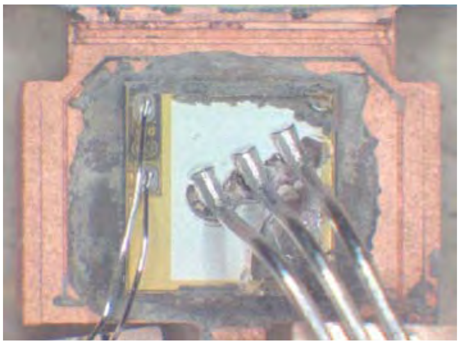
Fig 45. Sample image 1: 15 V, 3 A

aaa-004927

Fig 46. Sample image 2: 15 V, 3 A

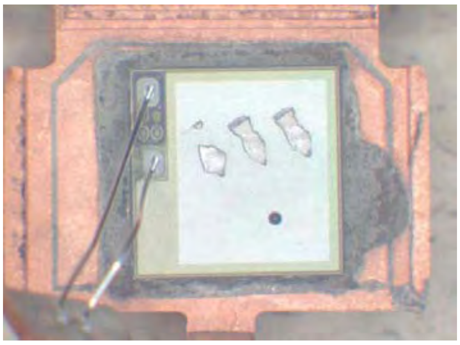
aaa-004928

Fig 47. Sample image 3: 15 V, 3 A



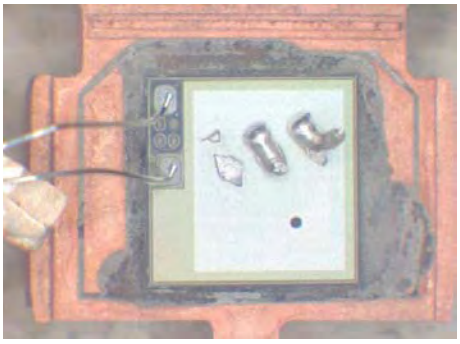
aaa-004929

Fig 48. Sample image 4: 15 V, 3 A



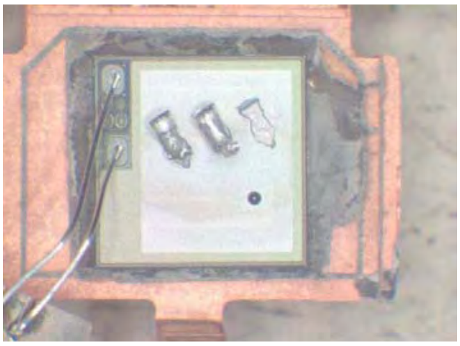
aaa-004930

Fig 49. Sample image 1: 30 V, 1.5 A



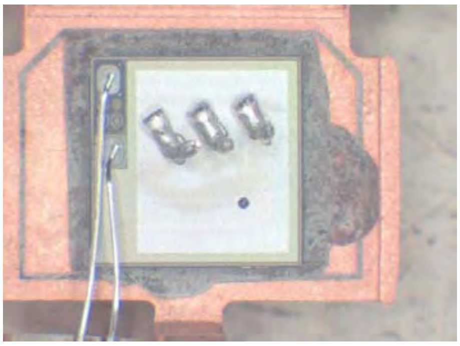
aaa-004931

Fig 50. Sample image 2: 30 V, 1.5 A



aaa-004932

Fig 51. Sample image 3: 30 V, 1.5 A



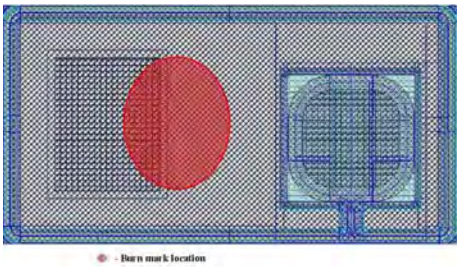
aaa-004933

Fig 52. Sample image 4: 30 V, 1.5 A

2.12 Linear mode EOS of BUK9Y40-55B

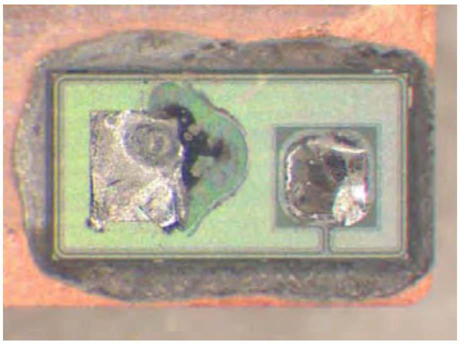
Table 17. Linear mode EOS

BUK9Y40-55B	
Cell structure:	4 µm stripe
Package:	LFPAK (clip bond)
Die size:	2.5 mm × 1.35 mm
EOS condition:	20 V, 3.5 A, 30 ms 20 V, 3 A, 60 ms 30 V, 1.4 A, 60 ms



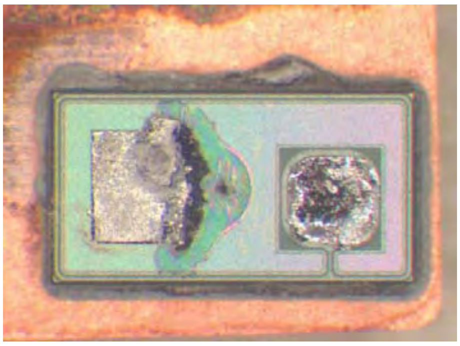
aaa-004934

Burn marks in center of die, adjacent but not directly under clip bond – can cause die cracking



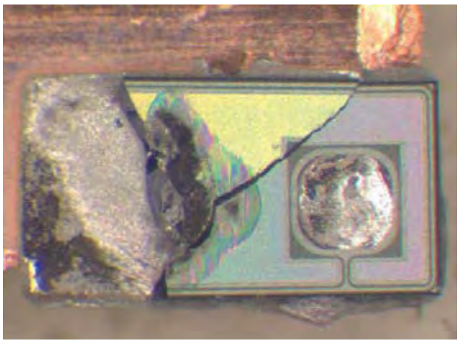
aaa-004935

Fig 53. Sample image 61; 20 V, 3.5 A, 30 ms



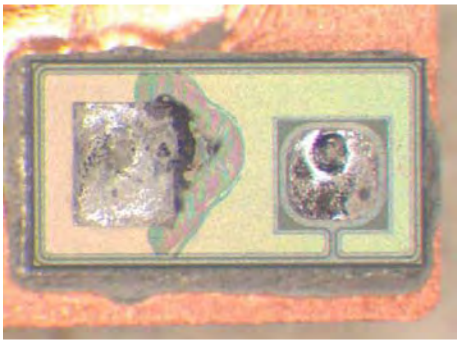
aaa-004936

Fig 54. Sample image 62; 20 V, 3.5 A, 30 ms



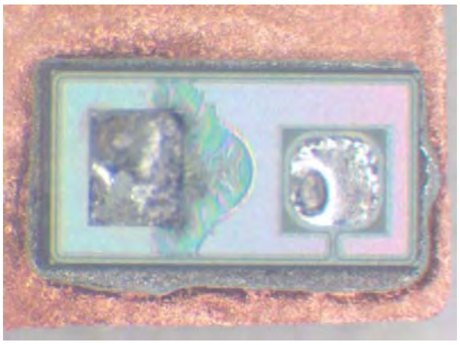
aaa-004937

Fig 55. Sample image 63; 20 V, 3.5 A, 30 ms



aaa-004938

Fig 56. Sample image 64; 20 V, 3.5 A, 30 ms

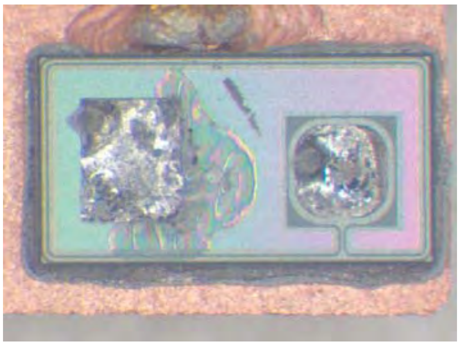


aaa-004939

Fig 57. Sample image 66; 20 V, 3 A, 60 ms

aaa-004941

Fig 58. Sample image 67; 20 V, 3 A, 60 ms

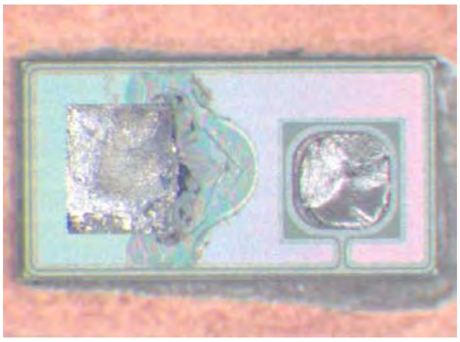


aaa-004942

Fig 59. Sample image 68; 20 V, 3 A, 60 ms

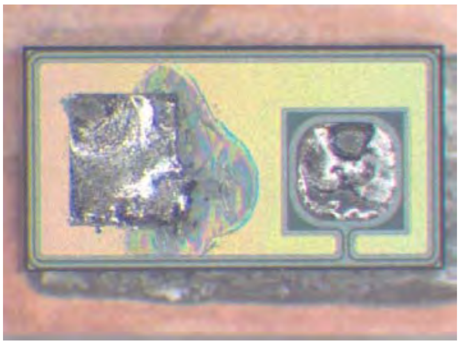
aaa-004943

Fig 60. Sample image 69; 20 V, 3 A, 60 ms



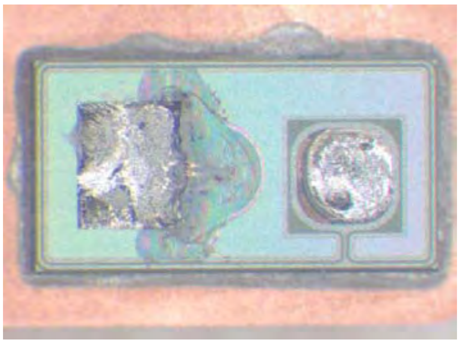
aaa-004944

Fig 61. Sample image 71; 30 V, 1.4 A, 60 ms



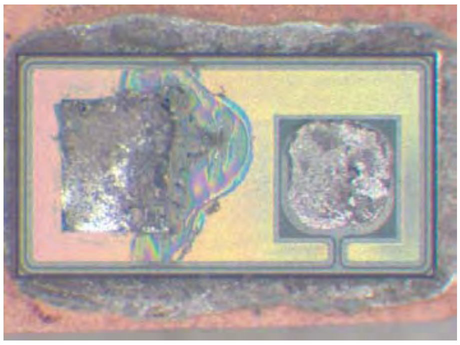
aaa-004946

Fig 62. Sample image 72; 30 V, 1.4 A, 60 ms



aaa-004945

Fig 63. Sample image 73; 30 V, 1.4 A, 60 ms



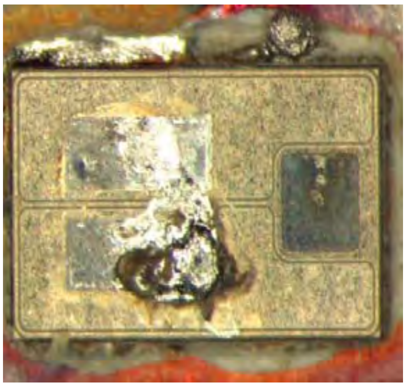
aaa-004947

Fig 64. Sample image 74; 30 V, 1.4 A, 60 ms

2.13 Linear mode EOS of PSMN7R0-30YL

Table 18. Linear mode EOS

PSMN7R0-30YL	
Cell structure:	2 μm stripe
Package:	LFPAK (clip bond)
Die size:	2.3 mm × 1.35 mm
EOS condition:	Burn marks in center of die, adjacent but not directly under clip bond
0.1 mH, 48 A to 51 A	
3.5 mH, 16 A to 18 A	

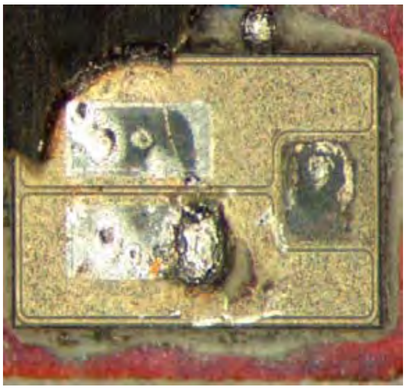


aaa-004948

Fig 65. Sample image 1; 15 V, 2.5 A, 100 ms

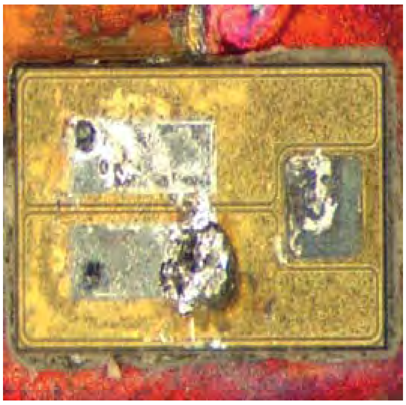
aaa-004951

Fig 66. Sample image 2; 15 V, 2.5 A, 100 ms



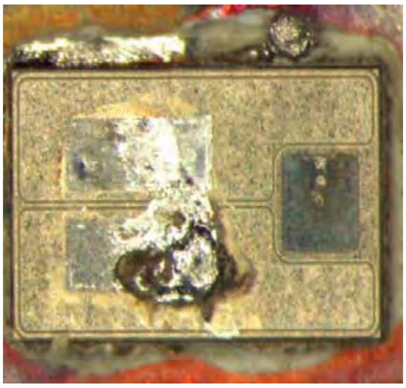
aaa-004953

Fig 67. Sample image 4; 15 V, 2.5 A, 100 ms



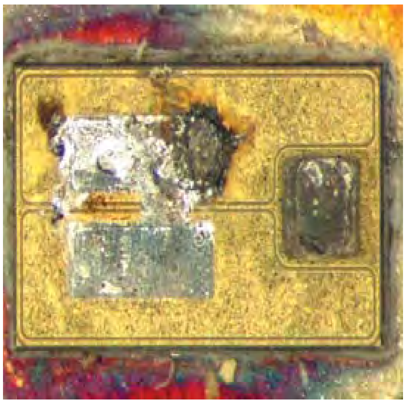
aaa-004954

Fig 68. Sample image 5; 15 V, 2.5 A, 100 ms



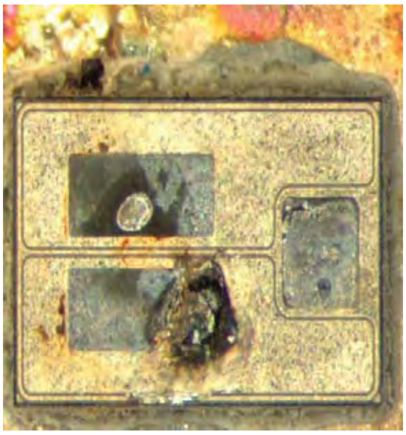
aaa-004955

Fig 69. Sample image 11; 15 V, 5 A, 1 ms



aaa-004956

Fig 70. Sample image 12; 15 V, 5 A, 1 ms



aaa-004957

Fig 71. Sample image 13; 15 V, 5 A, 1 ms

aaa-004958

Fig 72. Sample image 14; 15 V, 5 A, 1 ms

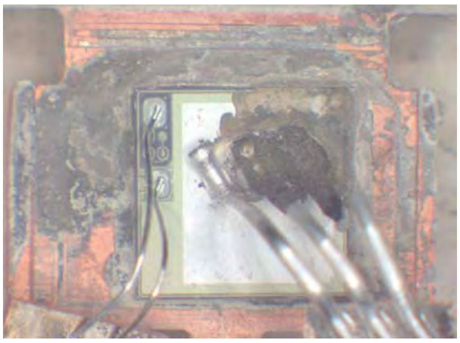
2.14 Over-current EOS of BUK7L06-34ARC

Table 19. Over-current EOS

BUK7L06-34ARC	
Cell structure:	9 μm hexagon
Package:	TO-220 (clip bond)
Die size:	4.3 mm × 4.3 mm
EOS condition:	120 A
	Extensive damage starting from die where wire bonds meet die. Secondary damage of reflowed solder and even fused wires are visible

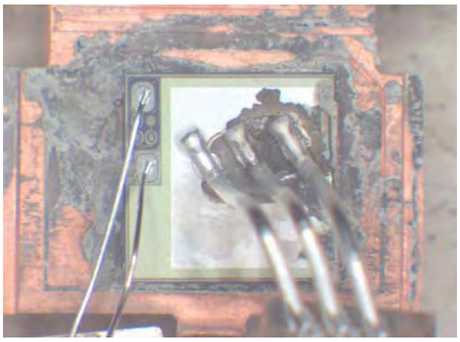
aaa-004959

Fig 73. Sample image 1



aaa-004960

Fig 74. Sample image 2



aaa-004961

Fig 75. Sample image 3

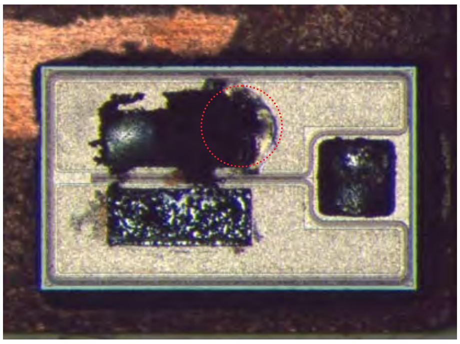
aaa-004962

Fig 76. Sample image 4: source wires fused

2.15 Over-current EOS of PSMN7R0-30YL

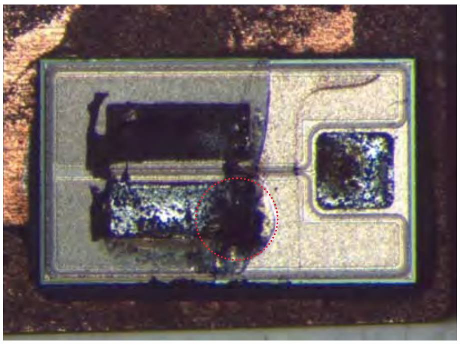
Table 20. Over-current EOS

PSMN7R0-30YL	
Cell structure:	2 μm stripe
Package:	LFPAK (clip bond)
Die size:	2.3 mm × 1.35 mm
EOS condition:	35 A, 35 ms
	Burn marks located in center of die under and adjacent to clip bond. Some evidence of die-cracking



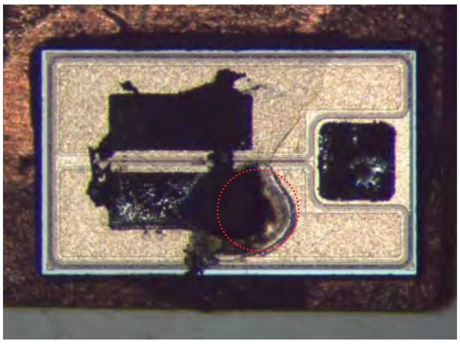
aaa-004963

Fig 77. Sample image 6



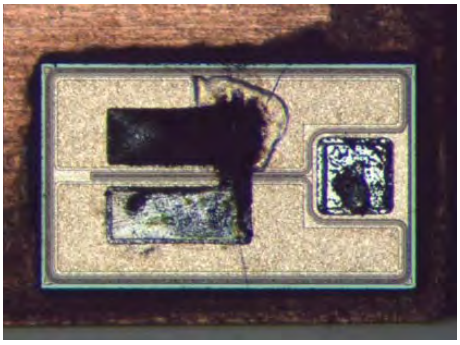
aaa-004964

Fig 78. Sample image 7



aaa-004965

Fig 79. Sample image 8; die is cracked through burn



aaa-004966

Fig 80. Sample image 10; die is cracked through burn

3. Abbreviations

Table 21. Abbreviations

Acronym	Description
EOS	Electrical Overstress
ESD	ElectroStatic Discharge
UIS	Unclamped Inductive Switching

4. Legal information

4.1 Definitions

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5. Tables

6. Figures

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