AN10273

Power MOSFET single-shot and repetitive avalanche ruggedness rating

Rev. 02 — 27 March 2009 Application note

Document information

Info	Content
Keywords	Power MOSFET, single-shot, avalanche, ruggedness, safe operating condition
Abstract	Power MOSFETs are normally measured based on single-shot Unclamped Inductive Switching (UIS) avalanche energy. This note describes in detail the avalanche ruggedness performance, fundamentals of UIS operation and appropriate quantification method for the safe operating condition.

Revision history

Rev	Date	Description
02	20090327	Updated
Modifications:		• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.
01	20030901	Initial version

Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

1. Introduction

Electronic applications have progressed significantly in recent years and have inevitably increased the demand for an intrinsically rugged power MOSFET. Device ruggedness is defined by the capacity of a device to sustain an avalanche current during an unclamped inductive load switching event. However, the avalanche ruggedness performance of a power MOSFET is normally measured within the industry as a single-shot Unclamped Inductive Switching (UIS) avalanche energy or E_{AS}. Whilst this provides an easy and quick method of quantifying the robustness of a MOSFET in avalanche, it does not necessarily reflect the true device avalanche capability (see Ref. 1, Ref. 2 and Ref. 3) in an application.

This note explains the fundamentals of UIS operation and reviews the appropriate method of quantifying the safe operating condition for a power MOSFET subjected to UIS operating condition. The note also covers the much-discussed repetitive avalanche ruggedness capability and how this operation can be quantified to operate safely.

2. Understanding power MOSFET single-shot avalanche events

Single-shot avalanche capability of a device has been well established by both researchers and the industry (see Ref. 1, Ref. 2 and Ref. 3). The test can be carried out on a simple unclamped inductive load switching circuit as shown in Figure 1.

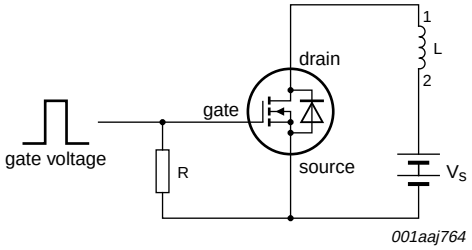

Fig 1. Unclamped inductive load test circuit for MOSFET ruggedness evaluation

2.1 Single-shot UIS operation

A voltage pulse is applied to the gate to turn the MOSFET ON as shown in Figure 2. This allows the load current to ramp up according to the inductor value (L) and the drain supply voltage (V_S) as shown in Figure 3 and Figure 4. At the end of the gate pulse, the MOSFET is turned OFF. The current in the inductor continues to flow causing the voltage across the MOSFET to rise sharply. This overvoltage is clamped at breakdown voltage (V_{BR}) until the load current reaches zero as illustrated in Figure 3. Typically V_{BR} is:

$$V_{BR} \approx 1.3 \times BV_{DSS} \quad (1)$$

The peak load current passing through the MOSFET before turn OFF will be the single-shot avalanche current (I_{AS}) of the UIS event as illustrated in Figure 4. The rate at which the avalanche current decays is dependent on inductor value and can be determined by:

$$\frac{dI_{AS}}{dt_{AV}} = -\frac{V_{BR} - V_S}{L} \quad (2)$$

The peak avalanche power ($P_{AV(pk)}$) dissipated in the MOSFET shown in Figure 5 is a product of the breakdown voltage (V_{BR}) and the avalanche current (I_{AS}) as shown in Figure 3 and Figure 4, respectively. The avalanche energy dissipated is the area under the P_{AV} waveform and can be estimated from the following expression:

$$E_{AS} = \frac{P_{AV(pk)} \times t_{AV}}{2} \quad (3)$$

or

$$E_{AS} = \frac{1}{2} \cdot \frac{V_{BR}}{V_{BR} - V_S} \cdot LI_{AS}^2 \quad (4)$$

Another crucial parameter involved in a MOSFET avalanche event is the junction temperature. The transient junction temperature rise during device avalanching at a time after the beginning of the avalanche event (τ) can be determined by the following expression:

$$T_{jrise}(\tau) = \int_0^{\tau} P_{AV}(t) \frac{dZ_{th(\tau - t)}}{dt} dt \quad (5)$$

where Z_{th} is the power MOSFET transient thermal impedance. Alternatively, the maximum T_{jrise} can be approximated by:

$$T_{jrise(max)} \approx \frac{2}{3} P_{av(pk)} Z_{th(t_{AV}/2)} \quad (6)$$

Assuming $T_{j(max)}$ occurs at $t_{AV}/2$

where $Z_{th(t_{AV}/2)}$ is the device transient thermal impedance at half the t_{AV} period.

The maximum junction temperature resulting from the avalanche event will therefore be:

$$T_{j(max)} \approx T_{jrise(max)} + T_j \quad (7)$$

where T_j refers to the junction temperature prior to turn OFF.

2.1.1 Single-shot UIS waveforms

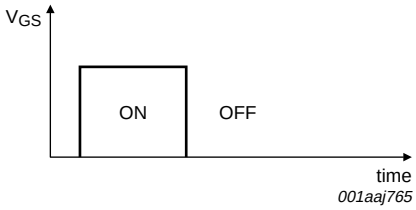

Fig 2. Gate pulse, V_{GS}

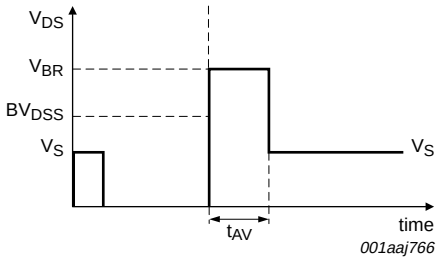

Fig 3. MOSFET Drain-Source Voltage, V_{DS}

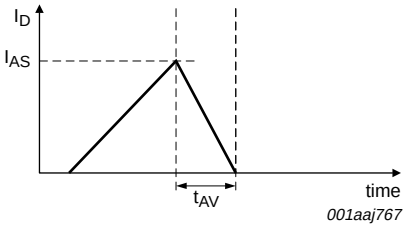

Fig 4. Current passing through MOSFET, I_D

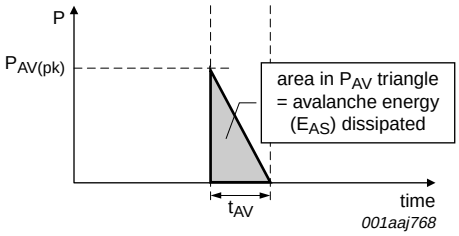

Fig 5. Peak avalanche power, $P_{AV(pk)}$

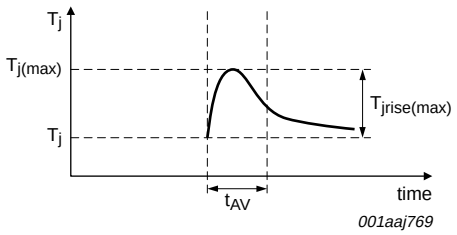

Fig 6. Transient junction temperature profile of MOSFET during an avalanche event

2.2 Single-shot avalanche ruggedness rating

The failure mechanism for a single-shot avalanche event in a power MOSFET is known to be due to the junction exceeding a maximum temperature above which catastrophic damage is done to the MOSFET. If the transient temperature resulting from an avalanche event, as illustrated in Figure 6, rises beyond a recommended rated value, the device risks being degraded. The recommended rated value is derated from the maximum temperature for optimum reliability.

Blackburn (see Ref. 2) has discussed a general guideline in detail on the appropriate method of quantifying the single-shot avalanche capability of a device by taking avalanche current and initial junction temperature into consideration. Safe operation for a device single-shot UIS event can be defined by a maximum allowed avalanche current as a function of avalanche time. The maximum allowed avalanche current is set so that a safe maximum junction temperature, $T_{j(max)}$ of 175 °C, is never exceeded. Using Equation 7, Figure 7 can be plotted.

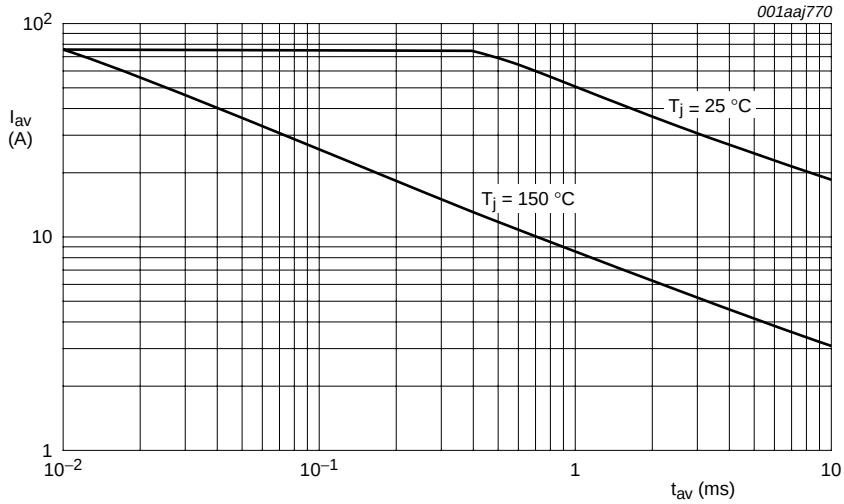

Fig 7. Single-shot avalanche ruggedness SOAR curves of BUK764R0-55B limited to a $T_{j(max)}$ of 175 °C

Figure 7 shows the SOAR curves of a device single-shot avalanche capability. The 25 °C junction temperature curve shows the maximum allowable I_{AS} for a given t_{AV} at an initial T_j of 25 °C. This maximum I_{AV} will give rise to a maximum junction temperature, $T_{jrise(max)}$ of 150 °C resulting in a $T_{j(max)}$ of 175 °C.

The area under the SOAR curve will be the safe operating area (SOA). Similarly the 150 °C junction temperature curve will be the maximum operating limit for an initial T_j of 150 °C. The $I_{AS(max)}$ will induce a $T_{jrise(max)}$ of 25 °C resulting in a $T_{j(max)}$ of 175 °C. Again the area under the curve will be the SOA.

The maximum junction temperature resulting in catastrophic device avalanche failure is approximately 380 °C, which is well in excess of the rated $T_{j(max)}$ of 175 °C. However, operating beyond the rated $T_{j(max)}$ may induce long-term detrimental effects to the power MOSFET and is not recommended.

3. Understanding power MOSFET repetitive avalanche events

Repetitive avalanching simply refers to an operation involving repeated single-shot avalanche events as discussed earlier. Until recently, most manufacturers have avoided the issues pertaining to the power MOSFET repetitive avalanche capability. This is primarily due to the complexity in such operation and the difficulties in identifying the underlying physical degradation process in the device.

Due to the traumatic nature of the avalanche event, a repetitive avalanche operation can be hazardous for a MOSFET, even when individual avalanche events are well below the single-shot UIS rating. This type of operation involves additional parameters such as the frequency, duty cycle and the thermal resistance (R_{th}) of the application during the repetitive avalanche event. However, it is possible to derate the single-shot rating to define a repetitive avalanche safe operating area.

3.1 Repetitive UIS operation

Referring to Figure 1, in a repetitive UIS test the gate is fed with a train of voltage pulses at frequency, f for a duty cycle as shown in Figure 8. The resulting breakdown voltage (V_{BR}) and current passing through the load (I_D) are the same as for a single-shot UIS except that the peak I_D will now be denoted as repetitive avalanche current (I_{AR}) as shown in Figure 9.

To obtain the average repetitive avalanche power dissipated ($P_{AV(R)}$) resulting from the repetitive UIS operation as shown in Figure 10. It is necessary to first calculate the E_{AS} for a single avalanche event using Equation 3. Subsequently substituting E_{AS} into the expression gives:

$$P_{AV(R)} = E_{AS} \times f \tag{8}$$

3.1.1 Repetitive UIS waveforms

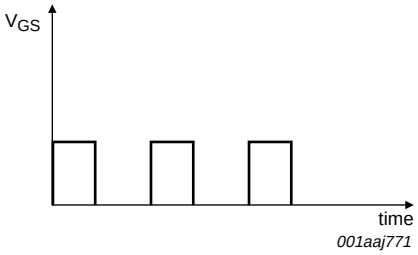

Fig 8. Gate pulse, V_{GS}

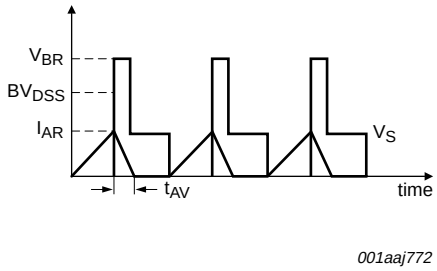

Fig 9. MOSFET drain-source voltage, V_{DS} and repetitive avalanche current, I_{AR}

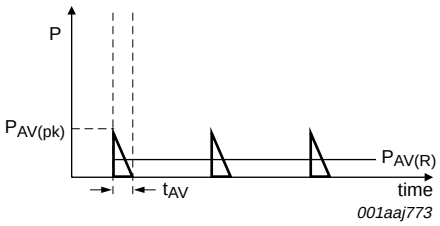

Fig 10. Repetitive avalanche power $P_{AV(R)}$

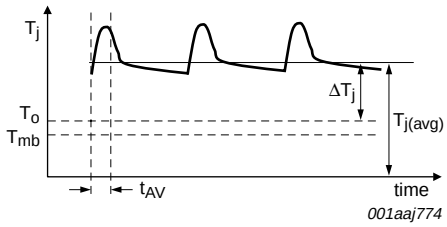

Fig 11. Transient junction temperature components of MOSFET during repetitive avalanching

3.2 Temperature Components

The temperature rise from the repetitive avalanching mode in the power MOSFET can be defined as shown in Figure 11.

The temperature (T_o) comprises the mounting base temperature (T_{mb}) and the temperature rise resulting from any ON state conduction (T_{cond}).

$$T_O = T_{mb} + T_{cond} \tag{9}$$

In addition there is a steady-state average junction temperature rise (ΔT_j) resulting from the average repetitive avalanche power loss.

$$\Delta T_j = P_{AV(R)} \times R_{th(j-amb)} \quad (10)$$

where $R_{th(j\text{-}amb)}$ is the thermal resistance of the device in the application. The summation of equations Equation 9 and Equation 10 will give the average junction temperature, $T_{j(avg)}$ of a power MOSFET in repetitive UIS operation.

$$T_{j(avg)} = T_O + \Delta T_j \quad (11)$$

4. Repetitive avalanche ruggedness rating

Following extensive investigation, it is clear that there is more than one failure or wear-out mechanism involved in repetitive avalanching. Temperature is **not** the only limiting factor to a repetitive avalanche operation. However, by limiting the temperature together with the repetitive avalanche current (I_{AR}) it is possible to define an operating environment such that the avalanche conditions do not activate any device degradation. This allows the power MOSFET to operate under repetitive UIS conditions safely.

Figure 12 shows the avalanche SOAR curves for BUK764R0-55B where 'Rep. Ava' represents the repetitive avalanche SOAR curve.

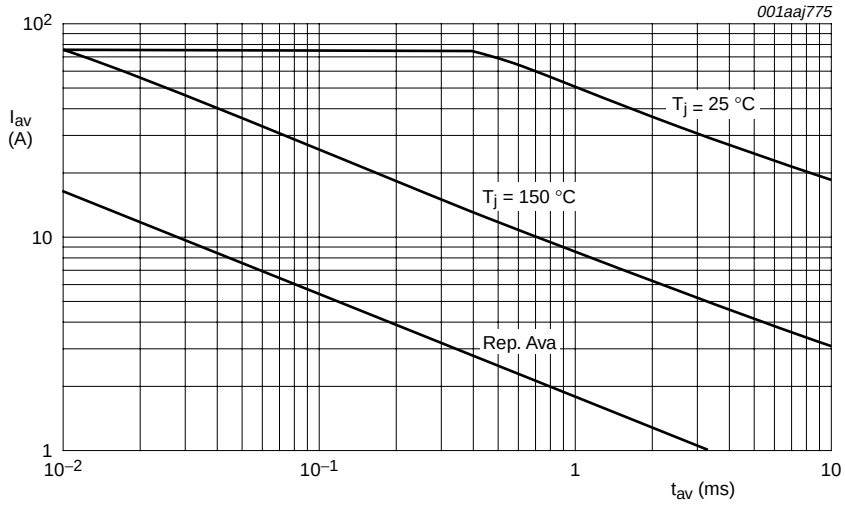

Fig 12. Single-shot (initial T_j = 25 °C and 150 °C) and repetitive (Rep. Ava) avalanche ruggedness SOAR curves of BUK764R0-55B limited to a $T_{j(max)}$ of 175 °C and $T_{j(avg)}$ of 170 °C, respectively

The two conditions which must be satisfied for safe operation of a power MOSFET under repetitive avalanching mode are as follows:

1. I_{AR} should **not** exceed the Repetitive Avalanche SOAR Curve
2. $T_{j(avg)}$ should **not** exceed 170 °C

5. Conclusion

Power MOSFETs can sustain single-shot and repetitive avalanche events. Simple design rules and SOAR regions have been provided.

6. Examples

The following examples examine cases of avalanche operation acceptance evaluation.

6.1 Single-shot avalanche case

- Device: BUK764R0-55B refer to Figure 12
- L = 2 mH
- I_{AS} = 40 A
- $R_{th(j\text{-}amb)}$ = 5 K/W

6.1.1 Calculation steps

1. Using the above information, t_{AV} can be determined using Equation 2, which in this case is 1.11 ms. Transferring the I_{AV} and t_{AV} conditions onto Figure 12. The operating point is under the T_j = 25 °C SOAR curve but over the T_j = 150 °C SOAR curve suggesting the operating condition maybe feasible.
2. To check, calculate the $T_{jrise(max)}$ using Equation 6, where $Z_{th(556\ \mu s)}$ on the data sheet is approximately 0.065 K/W. This will give a $T_{jrise(max)}$ of 124.8 °C.

Based upon the above calculations, the operating condition is acceptable if the device T_j < 50 °C.

6.2 Repetitive avalanche case

- Device: BUK764R0-55B refer to Figure 12
- L = 0.5 mH
- I_{AR} = 6 A
- f = 3 kHz
- $R_{th(j\text{-}amb)}$ = 5 K/W
- T_O = 100 °C

6.2.1 Calculation steps

1. t_{AV} can be determined from the above information using Equation 2 which in this case is ~0.042 ms. Transferring the I_{AV} and t_{AV} conditions onto Figure 12. The operating point is under the boundary of the ‘Rep. Ava’ SOAR curve suggesting the operating condition is acceptable. Therefore, condition 1 is achieved.
2. Calculate the Single-shot avalanche energy dissipation (E_{AS}) using Equation 3 (E_{AS} = 9 mJ).
3. Calculate the average repetitive avalanche power ($P_{AV(R)}$) using Equation 8 ($P_{AV(R)}$ = 27 W).

4. Calculate the average ΔT_j rise from repetitive avalanche (ΔT_j) using Equation 10 (ΔT_j = 135 °C).
5. Determine the average junction maximum temperature in repetitive avalanche operation ($T_{j(avg)}$) using Equation 11 ($T_{j(avg)}$ = 235 °C). Therefore, condition 2 is not achieved.

Based on the above calculations, the operating conditions satisfied the first but not the second requirement for safe repetitive avalanche operation. This was because the maximum $T_{j(avg)}$ exceeded 170 °C.

To make the above operation viable, the design engineer has to achieve the 2nd condition by reducing the $T_{j(avg)}$. This can be achieved simply by improving the heat sinking of the device. Reducing the $R_{th(j-amb)}$ from 5 K/W to 2.5 K/W will give a $T_{j(avg)}$ of 167.5 °C satisfying condition 2 for safe repetitive avalanche operation.

7. Appendix A

The following table describes the symbols used throughout this application note.

Table 1. Description of symbols

Symbol	Description	Remark
BV_{DSS}	device rated breakdown voltage	
E_{AS}	single-shot avalanche energy	
I_D	MOSFET drain current	
I_{AS}	single-shot avalanche current	
I_{AR}	repetitive avalanche current	
I_{AV}	avalanche current	
L	inductor	
$P_{AV(pk)}$	peak avalanche power	
$P_{AV(R)}$	average repetitive avalanche power	
R_{th}	device thermal resistance	
$R_{th(j\text{-}amb)}$	device junction to ambient thermal resistance	
T_o	initial temperature	summation of T_{mb} and T_{cond}
T_{cond}	ON-state conduction temperature	
T_j	junction temperature	
T_{jrise}	junction temperature rise	
$T_{jrise(max)}$	maximum junction temperature rise	
$T_{j(max)}$	maximum Junction temperature	
$T_{j(avg)}$	average junction temperature	for repetitive avalanche
T_{mb}	mounting base/case temperature	
ΔT_j	average temperature rise from average	
t_{AV}	avalanche period/duration	
V_{BR}	breakdown voltage	
V_{DS}	MOSFET drain-source voltage	
V_{GS}	MOSFET gate-source voltage	
Z_{th}	device Transient thermal impedance	
$Z_{th(t_{AV}/2)}$	device transient thermal impedance	measured at half the avalanche period
V_S	supply voltage	

8. References

[1] **Turn-off Failure of Power MOSFETs —** D.L. Blackburn, Proc. 1985 IEEE Power Electronics Specialists Conference, pp 429-435, June 1985.

[2] **Power MOSFET Failure Revisited —** D.L. Blackburn, Proc. 1988 IEEE Power Electronics Specialists Conference, pp 681-688, April 1988.

[3] **Boundary of Power-MOSFET, Unclamped Inductive-Switching (UIS) Avalanche-Current Capability —** Rodney R. Stoltenburg, Proc. 1989 Applied Power Electronics Conference, pp 359-364, March 1989.

9. Legal information

9.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

9.2 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

9.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

10. Figures

11. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 27 March 2009
Document identifier: AN10273_2