AES-S32V-NXP-G EVK Designer's Guide

Version 1.1

LIT# AES-S32V-NXP-G EVK Designer's Guide rev-1.1

Contents

1. Introduction

AES-S32V-NXP-G enables designers to build ADAS, NCAP front camera, object detection and recognition, surround view, automotive and industrial image processing, and also machine learning and sensor fusion applications.

This document provides guidelines for designing custom ADAS devlopment kit base on AES-S32V-NXP-G. It includes reference schematics for implementing AES-S32V-NXP-G (Core board) as well as the AES-S32V-NXP-G (Carrier board) PCB design guidelines.

1.1.Glossary

Term	Definition
SOM	System-on-Module
GPU	Graphics Processing Unit
ISP	Image Sensor Processor
POR	Power On Reset
IPU	Image Processing Unit
VIU	Video-In-Lite module
2D-ACE	Two Dimensional Animation and Compositing Engine
DCU	Display Control Unit, as a token of “2D-ACE”
FCCU	Fault Collection and Control Unit
FTM	FlexTimer module
LFAST	LVDS Fast Asynchronous Serial Transmission module

1.2.Additional Documentation:

- Additional information and documentation on NXP’s S32V234 MPU can be found at https://www.nxp.com/products/processors-and-microcontrollers/arm-based-processors-and-mcus/s32-automotive-platform/vision-processor-for-front-and-surround-view-camera-machine-learning-and-sensor-fusion:S32V234

- Additional information and documentation on AES-S32V-NXP-G (Core board) or AES-S32V-NXP-G (Carrier board) can be found at http://to-be-referenced under the appropriate product page.

- Please Chapter 5, Getting Help and Support for further links.

2. AES-S32V-NXP-G (Core board)

AES-S32V-NXP-G (Core board) is a high performance, full-featured, System-On-Module (SOM) based on the NXP ARM®-Based Processor and MCUs S32 MPU family of devices. Designed in a small form factor, the AES-S32V-NXP-G (Core board) packages all the necessary functions such as boot from external memory (SDcard/EMMC/SPI flash), JTAG debug, boot mode configuration, 2GB DDR3L SDRAM, and provides peripheral interfaces for carrier board such as 1Gb Ethernet, PCIe 2.0, 2 x MIPI CSI2, 2 x 16 bits VIU (video interface unit), RGB24 bits parallel display output, 2 x FD-CAN.

The AES-S32V-NXP-G (Core board) is offered in extended and industrial temperatures and supports the following features:

- 2GB DDR3L SDRAM (Qual 16-bit DDR3L interface)
- microSD card port
- eMMC falsh(32GB, 8-bit)
- QSPI flash(256MB)
- JTAG interface
- Boot configuration
- PMIC_PF8200
- I2C interface
- 2-channel Uart interface
- PCIE interface
- 18-pin Trace port interface
- 2-channel VIU interface(upto 1280x800 input/output resolution)
- 2-channel MIPI-CSI interface (Data rate up to 1.5 Gbit/s; supported input: RGB888, RGB565, YUV422 8- and 10-bit, RAW8, RAW10, RAW12, RAW14)
- DCU interface (up to a maximum resolution of 2032 x 2047; 8 graphics layers; RGB888 output; Gamma correction with 8-bit resolution)
- 2-channel CAN interface
- ADC interface (8-bit)
- SPI interface (4-channel)
- RGMII interface

Carrier Board:

- 12V power supply port
- HDMI Out
- Debug Uart (Micro USB port)
- User LED (PWM control)
- 2 x SPI port
- 2 x CAN connector
- 88Q5050 Ethernet Switch
- 6-channel T1 (100M Base)
- RJ-45 (100M Base)
- MAX9286 4-Camera In
- MAX96706 Camera In
- 2 x USB3.0

The AES-S32V-NXP-G high-level block diagram is shown in the following figure. It is a small computer system consisting of the AES-S32V-NXP-G (Core board) and AES-S32V-NXP-G (Carrier Board). It targets on both evaluation of S32v234 vision processing MPU and direct usage as an

industrial ADAS computing solution. The following sections describe the AES-S32V-NXP-G (Core board) on-board resources and external interfaces to the AES-S32V-NXP-G (Carrier Cards).

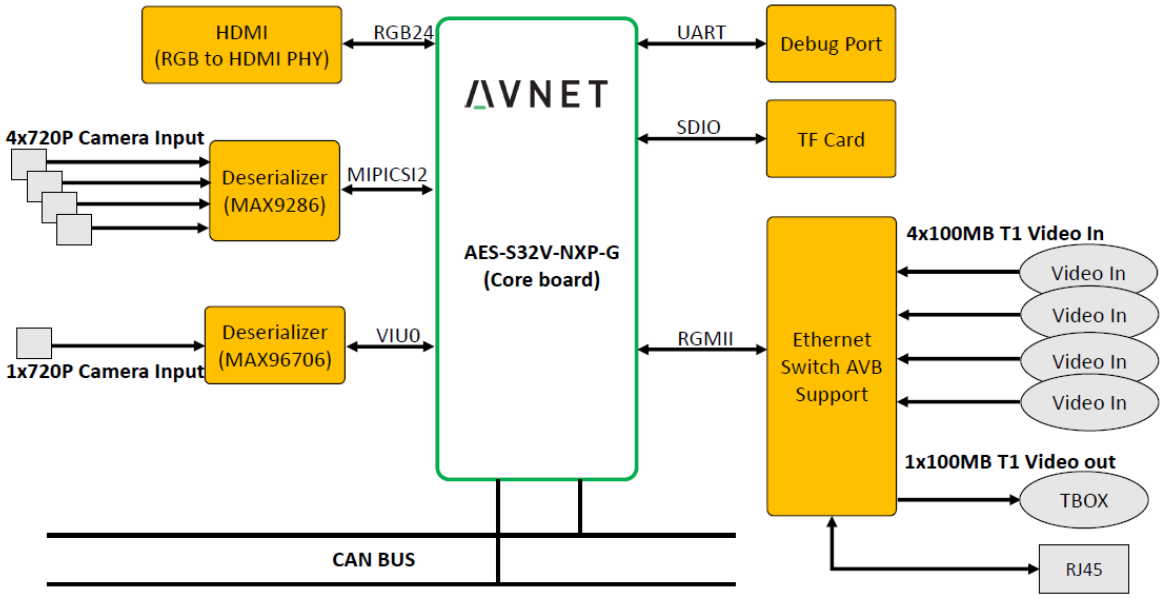


Figure 1 – AES-S32V-NXP-G (Core board) diagram

3. AES-S32V-NXP-G (Core board) Resources

The following sections provide a brief description of each component/resource available on the AES-S32V-NXP-G (Core board). Please refer to the Avnet AES-S32V-NXP-G (Core board) schematic at the end of this document for more information on the AES-S32V-NXP-G (Core board) on-board resources.

3.1.S32v234 vision processing MPU

The AES-S32V-NXP-G (Core board) is based on NXP's S32v234 vision processing MPU, the device is consisted of four ARM® Cortex®-A53, one Cortex-M4, dedicated modules and processors for acceleration of image vision processing tasks. The AES-S32V-NXP-G (Core board) is designed for following key applications:

- Surround View
- DMS
- FCW
- Car Ethernet

S32v234 Soc device features the following resources:

- 186 multiplexing IO pins
  - PA0 ~ PA15
  - PB0 ~ PB15
  - PC0 ~ PC15
  - PD0 ~ PD15
  - PE0 ~ PE15
  - PF0 ~ PF15
  - PG0 ~ PG15
  - PH0 ~ PH15
  - PI0 ~ PI15
  - PJ0 ~ PJ15
  - PK0 ~ PK15
  - PL0 ~ PL9
- analog pins
- reset/test pins
- misc pins
- SAR ADC inputs
- PCIe pins
- LFAST/PCIe reference clock outputs
- MIPI-CSI0
- MIPI-CSI1
- DDR0 pins
- DDR1 pins

More information please refer to S32v234RM3.0 attachment,
S32V234_IO_Signal_Description_Input_Multiplexing_Table.xlsx.

The following table provide brief descriptions of how each S32v234 Soc resources is used on the Avnet AES-S32V-NXP-G (Core board) followed by detail descriptions in subsequent sections.

Table 1 – Port bank assignments for function module

Port	Module
PA0~15	BOOT_RCON[0:8], CAN, JTAG, UART
PB0~15	BOOT_RCON[9:22], SPI0, SPI1, SPI2
PC0~15	BOOT_RCON[23:31], SPI2_CS, SPI3
PD0~15	RGMII, VIU0
PE0~15	VIU0
PF0~15	VIU1, eMMC
PG0~15	VIU1
PH0~15	Display
PJ0~15	Display
PK0~15	Display, QSPI_A, QSPI_B, eMMC, SDIO
PL0~15	QSPI_B, JTAG
DDR0 Pins	DDR0
DDR1 Pins	DDR1
SAR ADC inputs	ADC
MIPI-CSI0	MIPI-CSI0
MIPI-CSI1	MIPI-CSI1
PCIe pins	PCIe

3.2. 32 Boot Config Pins

The S32v234 SoC provides 32 boot config pins. The AES-S32V-NXP-G (Core board) connect some of these boot pins to switches, S1 and S2, and all boot config pins are exported to external connector J2, J3. More information about boot configuration, please refer to chapter 4.3 Boot Configuration Switches.

Refer to following table for FCBGA map and port number. More information please refer to S32V234_IO_Signal_Description_Input_Multiplexing_Table.xlsx in S32v234_RM_3.0.pdf attachment.

Table 2 – Boot Rcon Interface Pin Assignments

Signal Name	Port #	Notes	FCBGA #
RCON0_FLXR_TXEN_B	PA7	Boot Configuration Input 0	C11
RCON1_FLXR_TXD_A	PA8	Boot Configuration Input 1	A11
RCON2_FLXR_RXD_A	PA9	Boot Configuration Input 2	B11
RCON3_UART0_RXD	PA11	Boot Configuration Input 3	G10
RCON4_UART0_TXD	PA12	Boot Configuration Input 4	G11
RCON5_UART1_RXD	PA13	Boot Configuration Input 5	AA20
RCON6_UART1_TXD	PA14	Boot Configuration Input 6	AA21
RCON7_GPIO15	PA15	Boot Configuration Input 7	F11
RCON8_GPIO16	PB0	Boot Configuration Input 8	F12
RCON9_GPIO17	PB1	Boot Configuration Input 9	D11
RCON10_GPIO18	PB2	Boot Configuration Input 10	D12

RCON11_I2C2_SDA	PB3	Boot Configuration Input 11	AC18
RCON12_SPI0_SCK	PB5	Boot Configuration Input 12	AA18
RCON13_SPI0_SOUT	PB6	Boot Configuration Input 13	AB20
RCON14_SPI0_SIN	PB7	Boot Configuration Input 14	AB18
RCON15_SPI0_CS0	PB8	Boot Configuration Input 15	AB19
RCON16_SPI1_SCK	PB9	Boot Configuration Input 16	AD20
RCON17_SPI1_SOUT	PB10	Boot Configuration Input 17	AD21
RCON18_SPI1_SIN	PB11	Boot Configuration Input 18	AE20
RCON19_SPI1_CS0	PB12	Boot Configuration Input 19	AE21
RCON20_SPI2_SCK	PB13	Boot Configuration Input 20	AC24
RCON21_SPI2_SOUT	PB14	Boot Configuration Input 21	AC22
RCON22_SPI2_SIN	PB15	Boot Configuration Input 22	AC23
RCON23_SPI2_CS0	PC0	Boot Configuration Input 23	AB23
RCON24_SPI3_SCK	PC1	Boot Configuration Input 24	W19
RCON25_SPI3_SOUT	PC2	Boot Configuration Input 25	Y19
RCON26_SPI3_SIN	PC3	Boot Configuration Input 26	Y20
RCON27_SPI3_CS0	PC4	Boot Configuration Input 27	Y21
RCON28_FXT0_CH0	PC5	Boot Configuration Input 28	AD23
RCON29_FXT0_CH1	PC6	Boot Configuration Input 29	AD24
RCON30_FXT0_CH2	PC7	Boot Configuration Input 30	AE23
RCON31_FXT0_CH3	PC8	Boot Configuration Input 31	AE22
BOOT_MODE0	PC9	Boot Mode Configuration 0 Input	AC20
BOOT_MODE1	PC10	Boot Mode Configuration 1 Input	AC21

3.3.AES-S32V-NXP-G (Core board) Power Supply

The AES-S32V-NXP-G (Core board) receives input voltages of 1.8 – 5V from the custom Carrier Board and generates the voltage rails needed on AES-S32V-NXP-G (Core board).

AES-S32V-NXP-G (Core board) provide power supply for following modules:

- VDD 1.0V for VDD0~34, VDD_ARM1~3, VDD_GPU1~4, LV_CSI1~2, LV_PLL, PCIE_VP
- VDD 1.35V for DDR;
- VDD 1.8V for HV_EFUSE, HV_LFASTPLL, HV_PMC, HV_XOSC, HV_CSI, HV_AVD, REF_ADC
- VDD 3.3V for GPIO, VIU, ETH1~2, DIS1~3

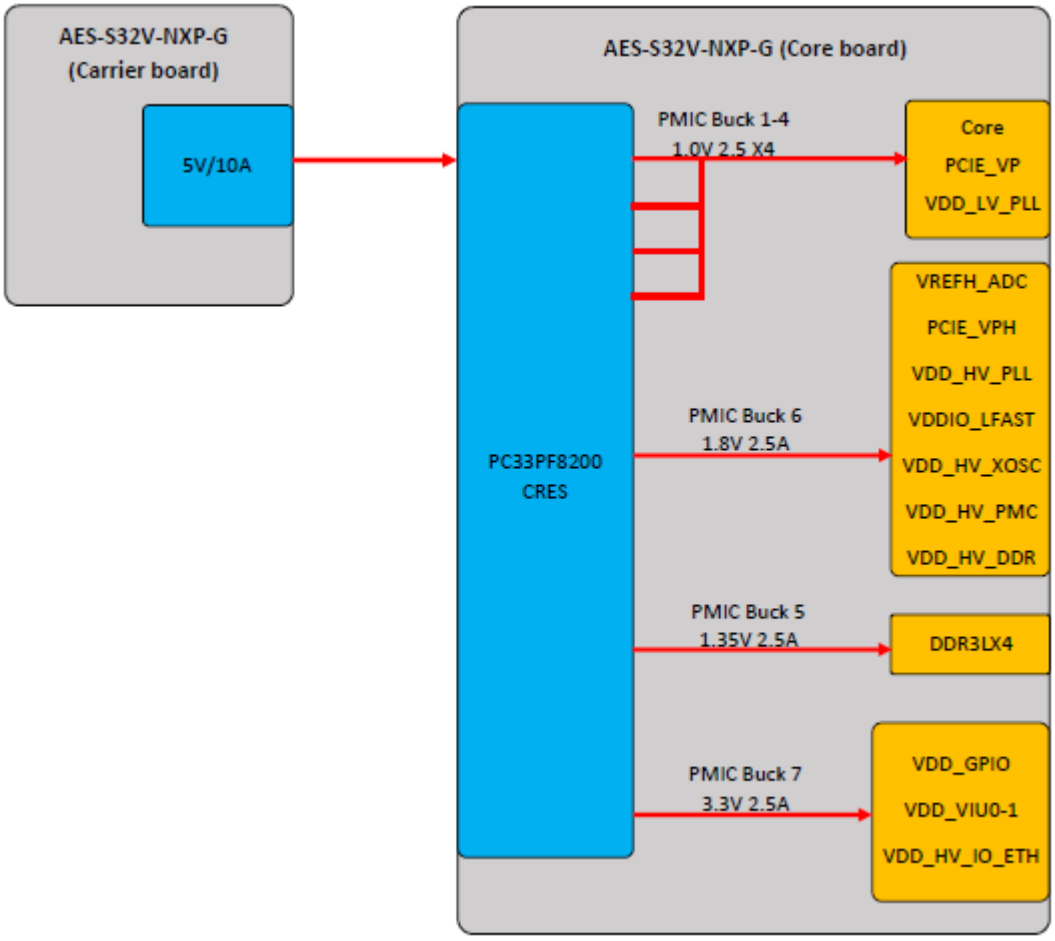


Figure 2 – Avnet AES-S32V-NXP-G (Core board) Power Supply Diagram

3.4.Reference Clock Input

The AES-S32V-NXP-G (Core board) provides a 40 MHz single-ended 1.8V reference clock input to the S32v234 SoC.

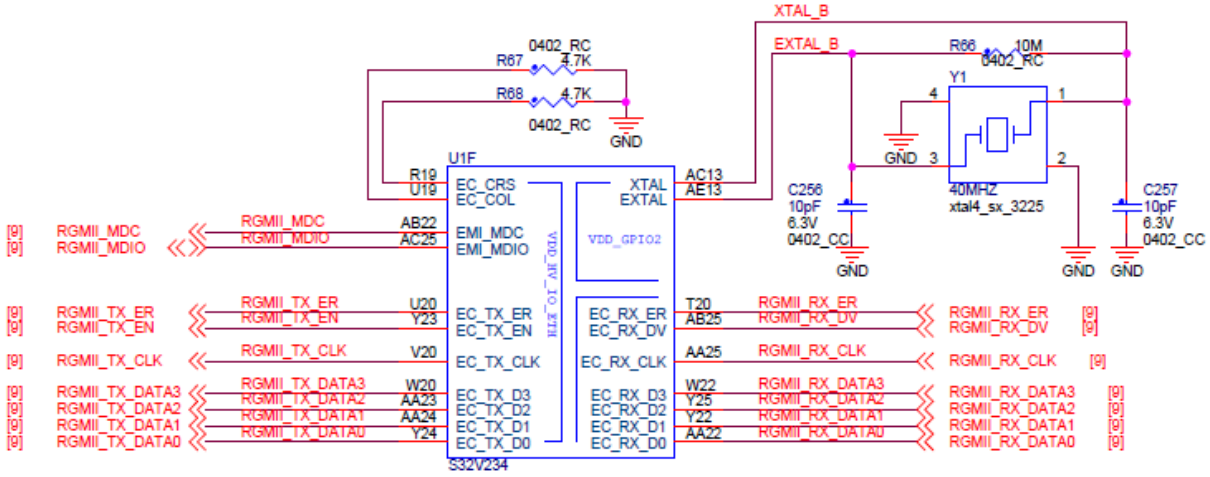


Figure 3 – Avnet AES-S32V-NXP-G (Core board) Reference Clock Input

3.5. Reset Interface

The AES-S32V-NXP-G (Core board) exports power reset input and hard reset IO to J2 for customer carrier board control.

Table 3 - Reset Interface Pad Assignment

Signal Name	Pad Type/Port #	FCBGA #	Note
MCU_RESET	Analog	C13	Power On Reset Input
RESET_B	PL9	G13	Hard Reset Input/Ouput

3.6.DDR3L SDRAM

The S32v234 SoC provides 2 Multi Mode DDR Controller (MMDC), MMDC0 and MMDC1, supporting DDR3/DDR3L mode and LPDDR2 mode.

The AES-S32V-NXP-G (Core board) provides 2GB of DDRL3 memory using 4 Micron MT41J256M16RE-15E (96-pin FBGA package) devices, connected to MMDC0 and MMDC1 to 2 256Mbx16 DDR3 SDRAM respectively. The SDRAM is implemented in 256Mb x 16 configuration and supports up to 1066MT/s data rate. The DDRL3 devices are connected to S32v234 SoC DDR0 and DDR1 ports and operated at 1.35V. Following figure showing how each DDR ports connect to 2 SDRAM.

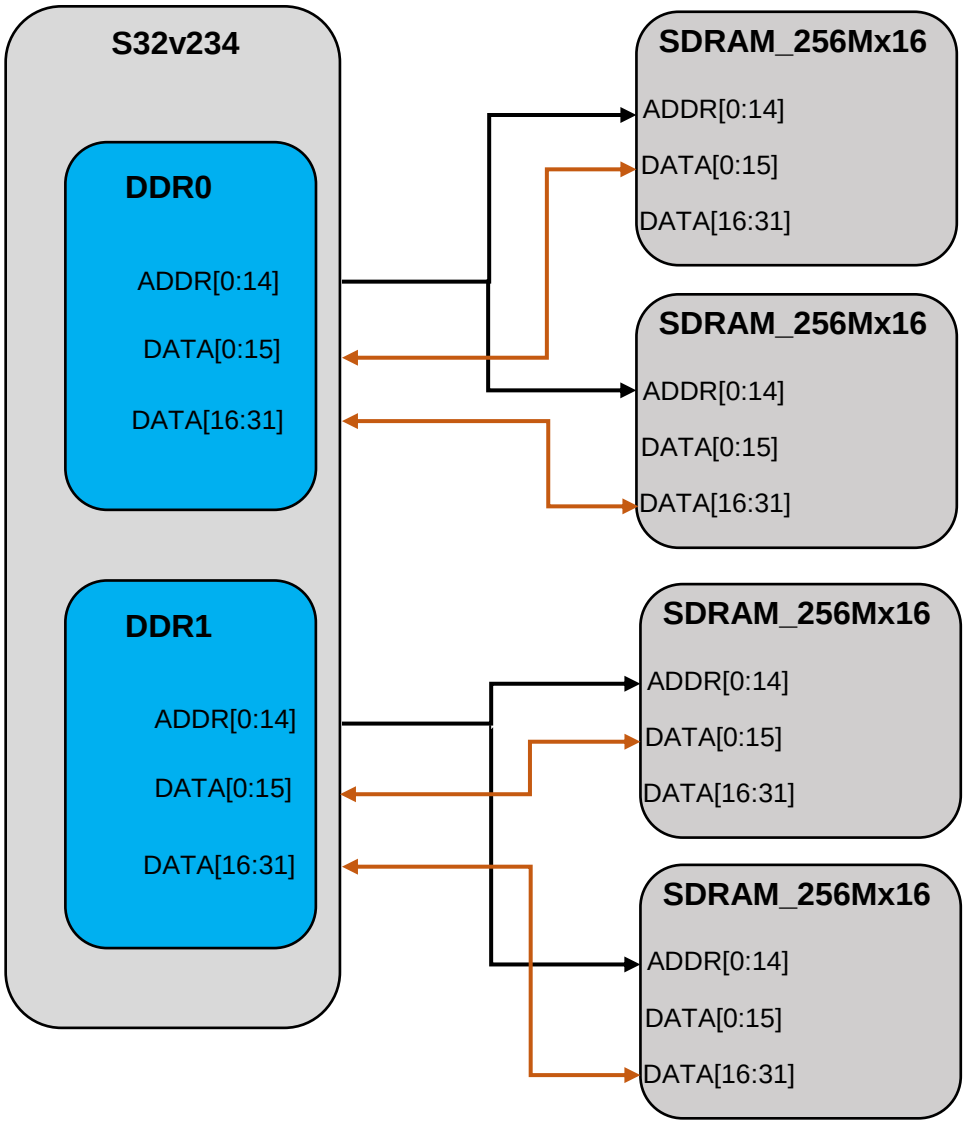


Figure 4 - DDR Block Diagram

Table 4 – Pinout for DDR3L Interface

DDR Port #	FCBGA #	Notes
DDR0_A00	**AE8**	DDR3 DRAM 0 Addr 0
DDR0_A01	**AD8**	DDR3 DRAM 0 Addr 1
DDR0_A02	**AC8**	DDR3 DRAM 0 Addr 2
DDR0_A03	**AE7**	DDR3 DRAM 0 Addr 3
DDR0_A04	**AE6**	DDR3 DRAM 0 Addr 4
DDR0_A05	**AA8**	DDR3 DRAM 0 Addr 5
DDR0_A06	**AA6**	DDR3 DRAM 0 Addr 6
DDR0_A07	**Y8**	DDR3 DRAM 0 Addr 7
DDR0_A08	**W5**	DDR3 DRAM 0 Addr 8

DDR0_A09	**Y6**	DDR3 DRAM 0 Addr 9
DDR0_A10	**N7**	DDR3 DRAM 0 Addr 10
DDR0_A11	**P6**	DDR3 DRAM 0 Addr 11
DDR0_A12	**U6**	DDR3 DRAM 0 Addr 12
DDR0_A13	**U7**	DDR3 DRAM 0 Addr 13
DDR0_A14	**R6**	DDR3 DRAM 0 Addr 14
DDR0_CAS_B	**T7**	DDR3 DRAM 0 CAS
DDR0_BA0	**P5**	DDR3 DRAM 0 Bank Addr 0
DDR0_BA1	**R5**	DDR3 DRAM 0 Bank Addr 1
DDR0_BA2	**T5**	DDR3 DRAM 0 Bank Addr 2
DDR0_D00	**AA2**	DDR3 DRAM 0 DATA 0
DDR0_D01	**AD2**	DDR3 DRAM 0 DATA 1
DDR0_D02	**AE3**	DDR3 DRAM 0 DATA 2
DDR0_D03	**AC2**	DDR3 DRAM 0 DATA 3
DDR0_D04	**Y1**	DDR3 DRAM 0 DATA 4
DDR0_D05	**AD3**	DDR3 DRAM 0 DATA 5
DDR0_D06	**AA1**	DDR3 DRAM 0 DATA 6
DDR0_D07	**AA3**	DDR3 DRAM 0 DATA 7
DDR0_D08	**AE4**	DDR3 DRAM 0 DATA 8
DDR0_D09	**AA5**	DDR3 DRAM 0 DATA 9
DDR0_D10	**AE5**	DDR3 DRAM 0 DATA 10
DDR0_D11	**Y4**	DDR3 DRAM 0 DATA 11
DDR0_D12	**AC3**	DDR3 DRAM 0 DATA 12
DDR0_D13	**AD5**	DDR3 DRAM 0 DATA 13
DDR0_D14	**AC5**	DDR3 DRAM 0 DATA 14
DDR0_D15	**Y3**	DDR3 DRAM 0 DATA 15
DDR0_D16	**R2**	DDR3 DRAM 0 DATA 16
DDR0_D17	**V2**	DDR3 DRAM 0 DATA 17
DDR0_D18	**R1**	DDR3 DRAM 0 DATA 18
DDR0_D19	**V1**	DDR3 DRAM 0 DATA 19
DDR0_D20	**Y2**	DDR3 DRAM 0 DATA 20
DDR0_D21	**P2**	DDR3 DRAM 0 DATA 21
DDR0_D22	**W1**	DDR3 DRAM 0 DATA 22
DDR0_D23	**P1**	DDR3 DRAM 0 DATA 23
DDR0_D24	**V3**	DDR3 DRAM 0 DATA 24
DDR0_D25	**V4**	DDR3 DRAM 0 DATA 25
DDR0_D26	**W3**	DDR3 DRAM 0 DATA 26
DDR0_D27	**N3**	DDR3 DRAM 0 DATA 27
DDR0_D28	**R4**	DDR3 DRAM 0 DATA 28

DDR0_D29	**P3**	DDR3 DRAM 0 DATA 29
DDR0_D30	**R3**	DDR3 DRAM 0 DATA 30
DDR0_D31	**P4**	DDR3 DRAM 0 DATA 31
DDR0_DQS0_P	**AB1**	DDR3 DRAM 0 DQS 0 Positive
DDR0_DQS0_N	**AC1**	DDR3 DRAM 0 DQS 0 Nagetive
DDR0_DQS1_P	**AB4**	DDR3 DRAM 0 DQS 1 Positive
DDR0_DQS1_N	**AC4**	DDR3 DRAM 0 DQS 1 Nagetive
DDR0_DQS2_P	**T1**	DDR3 DRAM 0 DQS 2 Positive
DDR0_DQS2_N	**U1**	DDR3 DRAM 0 DQS 2 Nagetive
DDR0_DQS3_P	**U3**	DDR3 DRAM 0 DQS 3 Positive
DDR0_DQS3_N	**T3**	DDR3 DRAM 0 DQS 3 Nagetive
DDR0_CKE0	**AC6**	DDR3 DRAM 0 CKE 0
DDR0_CS0_B	**AD6**	DDR3 DRAM 0 CS 0
DDR0_CLK0_P	**AB7**	DDR3 DRAM 0 CLK 0
DDR0_CLK0_N	**AB6**	DDR3 DRAM 0 CLK 0
DDR0_DM0	**AB3**	DDR3 DRAM 0 Data Mask 0
DDR0_DM1	**AB5**	DDR3 DRAM 0 Data Mask 1
DDR0_DM2	**U2**	DDR3 DRAM 0 Data Mask 2
DDR0_DM3	**U4**	DDR3 DRAM 0 Data Mask 3
DDR0_ODT0	**R7**	DDR3 DRAM 0 ODT 0
DDR0_ODT1	**U5**	DDR3 DRAM 0 ODT 1
DDR0_RAS_B	**V5**	DDR3 DRAM 0 RAS
DDR0_RESET	**Y7**	DDR3 DRAM 0 RESET
DDR0_WE_B	**V6**	DDR3 DRAM 0 WE
DDR1_A00	**A8**	DDR3 DRAM 1 Addr 0
DDR1_A01	**B8**	DDR3 DRAM 1 Addr 1
DDR1_A02	**C8**	DDR3 DRAM 1 Addr 2
DDR1_A03	**A7**	DDR3 DRAM 1 Addr 3
DDR1_A04	**A6**	DDR3 DRAM 1 Addr 4
DDR1_A05	**E8**	DDR3 DRAM 1 Addr 5
DDR1_A06	**E6**	DDR3 DRAM 1 Addr 6
DDR1_A07	**F8**	DDR3 DRAM 1 Addr 7
DDR1_A08	**G5**	DDR3 DRAM 1 Addr 8
DDR1_A09	**F6**	DDR3 DRAM 1 Addr 9
DDR1_A10	**N5**	DDR3 DRAM 1 Addr 10
DDR1_A11	**M6**	DDR3 DRAM 1 Addr 11
DDR1_A12	**J6**	DDR3 DRAM 1 Addr 12
DDR1_A13	**J7**	DDR3 DRAM 1 Addr 13
DDR1_A14	**L6**	DDR3 DRAM 1 Addr 14

DDR1_CAS_B	**K7**	DDR3 DRAM 1 CAS
DDR1_BA0	**M5**	DDR3 DRAM 1 Bank Addr 0
DDR1_BA1	**L5**	DDR3 DRAM 1 Bank Addr 1
DDR1_BA2	**K5**	DDR3 DRAM 1 Bank Addr 2
DDR1_D00	**E2**	DDR3 DRAM 1 DATA 0
DDR1_D01	**B2**	DDR3 DRAM 1 DATA 1
DDR1_D02	**A3**	DDR3 DRAM 1 DATA 2
DDR1_D03	**C2**	DDR3 DRAM 1 DATA 3
DDR1_D04	**F1**	DDR3 DRAM 1 DATA 4
DDR1_D05	**B3**	DDR3 DRAM 1 DATA 5
DDR1_D06	**E1**	DDR3 DRAM 1 DATA 6
DDR1_D07	**E3**	DDR3 DRAM 1 DATA 7
DDR1_D08	**A4**	DDR3 DRAM 1 DATA 8
DDR1_D09	**E5**	DDR3 DRAM 1 DATA 9
DDR1_D10	**A5**	DDR3 DRAM 1 DATA 10
DDR1_D11	**F4**	DDR3 DRAM 1 DATA 11
DDR1_D12	**C3**	DDR3 DRAM 1 DATA 12
DDR1_D13	**B5**	DDR3 DRAM 1 DATA 13
DDR1_D14	**C5**	DDR3 DRAM 1 DATA 14
DDR1_D15	**F3**	DDR3 DRAM 1 DATA 15
DDR1_D16	**L2**	DDR3 DRAM 1 DATA 16
DDR1_D17	**H2**	DDR3 DRAM 1 DATA 17
DDR1_D18	**L1**	DDR3 DRAM 1 DATA 18
DDR1_D19	**H1**	DDR3 DRAM 1 DATA 19
DDR1_D20	**F2**	DDR3 DRAM 1 DATA 20
DDR1_D21	**M1**	DDR3 DRAM 1 DATA 21
DDR1_D22	**G1**	DDR3 DRAM 1 DATA 22
DDR1_D23	**N1**	DDR3 DRAM 1 DATA 23
DDR1_D24	**H3**	DDR3 DRAM 1 DATA 24
DDR1_D25	**H4**	DDR3 DRAM 1 DATA 25
DDR1_D26	**G3**	DDR3 DRAM 1 DATA 26
DDR1_D27	**M3**	DDR3 DRAM 1 DATA 27
DDR1_D28	**L4**	DDR3 DRAM 1 DATA 28
DDR1_D29	**M2**	DDR3 DRAM 1 DATA 29
DDR1_D30	**L3**	DDR3 DRAM 1 DATA 30
DDR1_D31	**M4**	DDR3 DRAM 1 DATA 31
DDR1_DQS0_P	**D1**	DDR3 DRAM 1 DQS 0 Positive
DDR1_DQS0_N	**C1**	DDR3 DRAM 1 DQS 0 Nagetive
DDR1_DQS1_P	**D4**	DDR3 DRAM 1 DQS 1 Positive

DDR1_DQS1_N	**C4**	DDR3 DRAM 1 DQS 1 Nagetive
DDR1_DQS2_P	**K1**	DDR3 DRAM 1 DQS 2 Positive
DDR1_DQS2_N	**J1**	DDR3 DRAM 1 DQS 2 Nagetive
DDR1_DQS3_P	**J3**	DDR3 DRAM 1 DQS 3 Positive
DDR1_DQS3_N	**K3**	DDR3 DRAM 1 DQS 3 Nagetive
DDR1_CKE0	**C6**	DDR3 DRAM 1 CKE 0
DDR1_CS0_B	**B6**	DDR3 DRAM 1 CS 0
DDR1_CLK0_P	**D7**	DDR3 DRAM 1 CLK 0
DDR1_CLK0_N	**D6**	DDR3 DRAM 1 CLK 0
DDR1_DM0	**D3**	DDR3 DRAM 1 Data Mask 0
DDR1_DM1	**D5**	DDR3 DRAM 1 Data Mask 1
DDR1_DM2	**J2**	DDR3 DRAM 1 Data Mask 2
DDR1_DM3	**J4**	DDR3 DRAM 1 Data Mask 3
DDR1_ODT0	**L7**	DDR3 DRAM 1 ODT 0
DDR1_ODT1	**J5**	DDR3 DRAM 1 ODT 1
DDR1_RAS_B	**H5**	DDR3 DRAM 1 RAS
DDR1_RESET	**F7**	DDR3 DRAM 1 RESET
DDR1_WE_B	**H6**	DDR3 DRAM 1 WE

3.7.RGMII Interface

The AES-S32V-NXP-G (Core board) provides a single Gigabit Ethernet PHY interface for the Marvell 88E5050 RGMII PHY device in 56-pin QFN package located on the custom Carrier Board. The AES-S32V-NXP-G (Core board) Gigabit Ethernet PHY connector side (J1 connector) connected to Marvell 88E5050 on Carrier Board, which provides an RJ45 connector and four T1 connected located on the custom Carrier Card can be used to implement Gigabit Ethernet port and AVB applications.

The Marvell 88E5050 RGMII Ethernet PHY host side I/O is connected to the PC and PD bank ports and operated at 1.8V on the AES-S32V-NXP-G (Core board).

Table 5 – RGMII PHY Interface Host Interface Side Pin Assignments

Signal Name	Port #	FCBGA #	Notes
RGMII_MDC	PC13	AB22	Management Data Clock
RGMII_MDIO	PC14	AC25	Management Data I/O
RGMII_TX_ER	PD12	U20	Transmit data error input
RGMII_TX_EN	PD11	Y23	Transmit enable
RGMII_TX_CLK	PC15	V20	Transmit clock
RGMII_TX_DATA	PD7	Y24	Transmit DATA[0]
RGMII_TX_DATA	PD8	AA24	Transmit DATA[1]
RGMII_TX_DATA	PD9	AA23	Transmit DATA[2]
RGMII_TX_DATA	PD10	W20	Transmit DATA[3]
RGMII_RX_ER	PD6	T20	Receive data error input
RGMII_RX_DV	PD5	AB25	Receive data valid input
RGMII_RX_CLK	PD0	AA25	Receive clock
RGMII_RX_DATA	PD1	AA22	Receive DATA[0]
RGMII_RX_DATA	PD2	Y22	Receive DATA[1]
RGMII_RX_DATA	PD3	Y25	Receive DATA[2]
RGMII_RX_DATA	PD4	W22	Receive DATA[3]

3.8. I2C Interfaces

The S32v234 SoC contains three identical instances of I2C. The AES-S32V-NXP-G (Core board) exports I2C interfaces to J3 for customer carrier board.

Table 6 - I2C Interfaces Pads Assignment

Signal Name	Port #	FCBGA #	Notes
I2C0_SDA	PG3	AC15	IIC 0 Serial Data
I2C0_SCL	PG4	AE15	IIC 0 Serial Clock
I2C1_SDA	PG5	Y16	IIC 1 Serial Data
I2C1_SCL	PG6	Y15	IIC 1 Serial Clock
RCON11_I2C2_SDA	PG7	AC18	IIC 2 Serial Data
I2C2_SCL	PG8	AC19	IIC 2 Serial Clock

3.9. SPI Interfaces

The S32v234 SoC has four channels SPI, SPI0~SPI3. TheAES-S32V-NXP-G (Core board) connects SPI0~SPI3 to J3 for custom Carrier Board. On Avnet Carrier Board, only SPI0 and SPI1 are implemented, connected to J14 and J15 via NX3DV2567HR (NC) switch on each channel.

Table 7 - SPI Interface Pads Assignment

Signal Name	Port #	FCBGA #	Notes
RCON15_SPI0_CS	PB8	AB19	SPI 0 Chip Select 0
RCON12_SPI0_SC	PB5	AA18	SPI 0 Serial Clock
RCON14_SPI0_SI	PB7	AB18	SPI 0 Serial Data In
RCON13_SPI0_S	PB6	AB20	SPI 0 Serial Data Out
RCON19_SPI1_CS	PB12	AE21	SPI 1 Chip Select 0
RCON16_SPI1_SC	PB9	AD20	SPI 1 Serial Clock
RCON18_SPI1_SI	PB11	AE20	SPI 1 Serial Data In
RCON17_SPI1_S	PB10	AD21	SPI 1 Serial Data Out
RCON23_SPI2_CS	PC0	AB23	SPI 2 Chip Select 0
RCON20_SPI2_SC	PB13	AC24	SPI 2 Serial Clock
RCON22_SPI2_SI	PB15	AC23	SPI 2 Serial Data In
RCON21_SPI2_S	PB14	AC22	SPI 2 Serial Data Out
RCON27_SPI3_CS	PC4	Y21	SPI 3 Chip Select 0
RCON24_SPI3_SC	PC1	W19	SPI 3 Serial Clock
RCON26_SPI3_SI	PC3	Y20	SPI 3 Serial Data In
RCON25_SPI3_S	PC2	Y19	SPI 3 Serial Data Out

3.10. QSPI NOR Flash

The AES-S32V-NXP-G (Core board) provides 256MB of QSPI. A Winbond W25Q16JVSSIQ (8-pin SOIC package) devices are used to select the boot device on the AES-S32V-NXP-G (Core board) SOM. The QSPI Flash devices are connected to the PK IO bank (QSPI_A) and operated at 1.8V I/O. The QSPI Flash can be used as a primary boot device on the AES-S32V-NXP-G (Core board) if QSPI_EMMC_SW signal is asserted.

The S32v234 SoC has two QSPI-ports, QSPI_A and QSPI_B. The AES-S32V-NXP-G (Core board) implements QSPI A as NOR flash communication ports. Multiplexing IO ports PK [6:11] connect with Winbond Nor flash/micro SD card via a NX3DV642GU switch, controlling by software to decide QSPI_A or SDIO function implements.

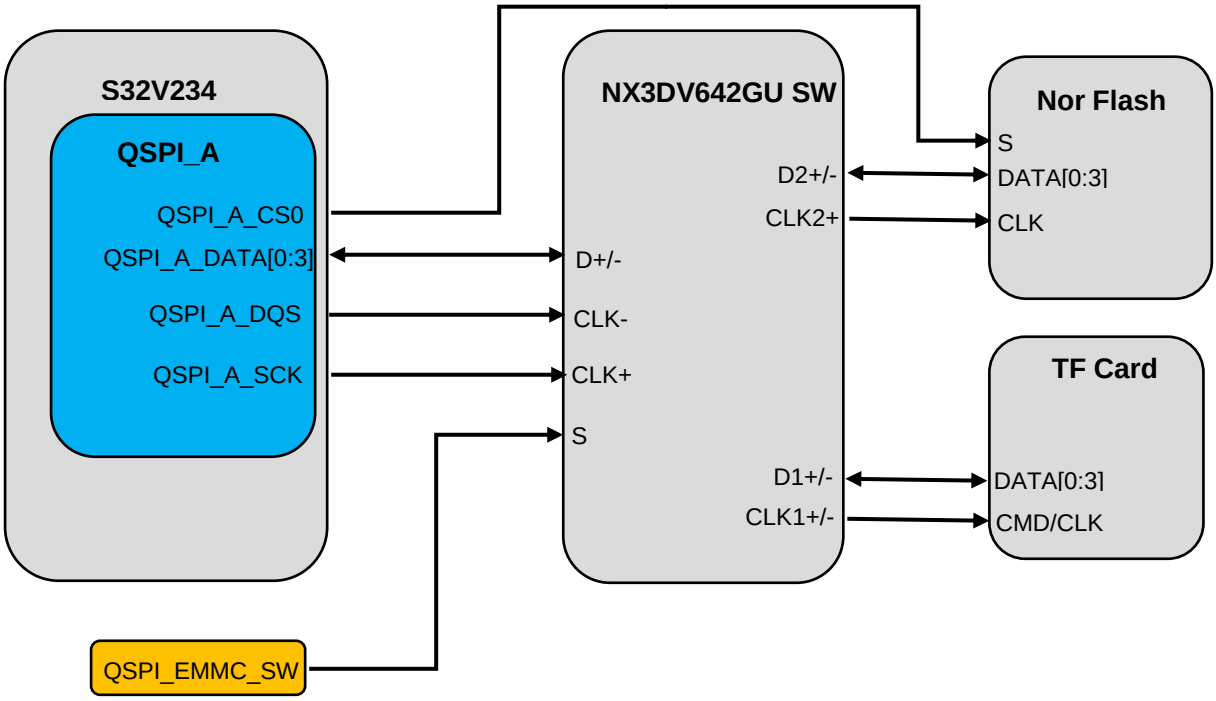


Figure 5 - QSPI_A to NOR Flash / SD Card Switch

Table 8 - QSPI Flash Pin Assignments

Signal Name	Port #	FCBGA #	Notes
QSPI_A_CS0	PK5	U25	QuadSPI A Chip Select 0
QSPI_A_DATA0	PK8	V23	QuadSPI A Data 0
QSPI_A_DATA1	PK9	U23	QuadSPI A Data 1
QSPI_A_DATA2	PK10	V21	QuadSPI A Data 2
QSPI_A_DATA3	PK11	V22	QuadSPI A Data 3
QSPI_A_DQS	PK7	U22	QuadSPI A Data Strobe Input
QSPI_A_SCK	PK6	V25	QuadSPI A Serial Clock Output

3.11. Micro SD Card

The S32v234 Soc provides a 4-bit SDIO channel on multiplexing IO ports PK [6:11]. On AES-S32V-NXP-G (Core board), QSPI Nor flash and micro SD card share the PK[6:11], the multiplex mode should be decided by software. And NX3DV642GU switch connect micro SD card port and Winbond Nor flash to PK [6:11]. Please refer to Figure. QSPI_A to NOR Flash / SD Card Switch

The AES-S32V-NXP-G (Core board) provides a micro SD card port to for supporting system boot from SD card. The supported maximum memory for SD card is 16GB.

Table 9 - USDHC SDIO Ports Mapping

Signal Name	Port #	FCBGA #	Notes
QSPI_A_DATA0	PK8	V23	SD Data 0
QSPI_A_DATA1	PK9	U23	SD Data 1

QSPI_A_DATA2	**PK10**	**V21**	**SD Data 2**
QSPI_A_DATA3	**PK11**	**V22**	**SD Data 3**
QSPI_A_DQS	**PK7**	**U22**	**SD Command**
QSPI_A_SCK	**PK6**	**V25**	**SD Clock**

3.12. QSPI Interface

AES-S32V-NXP-G (Core board) connect QSPI_B ports to external connector J1 [57:62] for custom Carrier Board use.

Table 10 - QSPI Interface Assignments

Signal Name	Port #	FCBGA #	Notes
QSPI_B_CS0	**PK12**	**W25**	**QuadSPI B Chip Select 0 Output**
QSPI_B_DATA0	**PK15**	**W23**	**QuadSPI B Data 0**
QSPI_B_DATA1	**PL0**	**U21**	**QuadSPI B Data 1**
QSPI_B_DATA2	**PL1**	**U24**	**QuadSPI B Data 2**
QSPI_B_DATA3	**PL2**	**R21**	**QuadSPI B Data 3**
QSPI_B_DQS	**PK14**	**R20**	**QuadSPI B Data Strobe Input**
QSPI_B_SCK	**PK13**	**V24**	**QuadSPI B Serial Clock Output**

3.13. CAN Interface

The S32v234 SoC contains 2 instances of FlexCAN. The S23v234-EVK SOM exports 2 CAN interfaces, CAN0 and CAN1, exporting to J2 [1:4] for custom Carrier Board.

Table 11 - CAN Interface Ports Assignment

Signal Name	Port #	FCBGA #	Notes
CAN_FD0_RXD	PA3	B10	CAN_FD 0 Receive Input
CAN_FD0_TXD	PA2	A10	CAN_FD 0 Transmit Output
CAN_FD1_RXD	PA5	B12	CAN_FD 1 Receive Input
CAN_FD1_TXD	PA4	A12	CAN_FD 1 Transmit Output

3.14. ADC Interface

The S32v234 Soc provides a 12-bit resolution Analog-to-Digital Converter and uses the Successive Approximation Register method. It provides fast and accurate conversion, and is highly configurable for a wide range of applications.

The AES-S32V-NXP-G (Core board) exports the ADC interface to J2 [49:56] for custom Carrier Board.

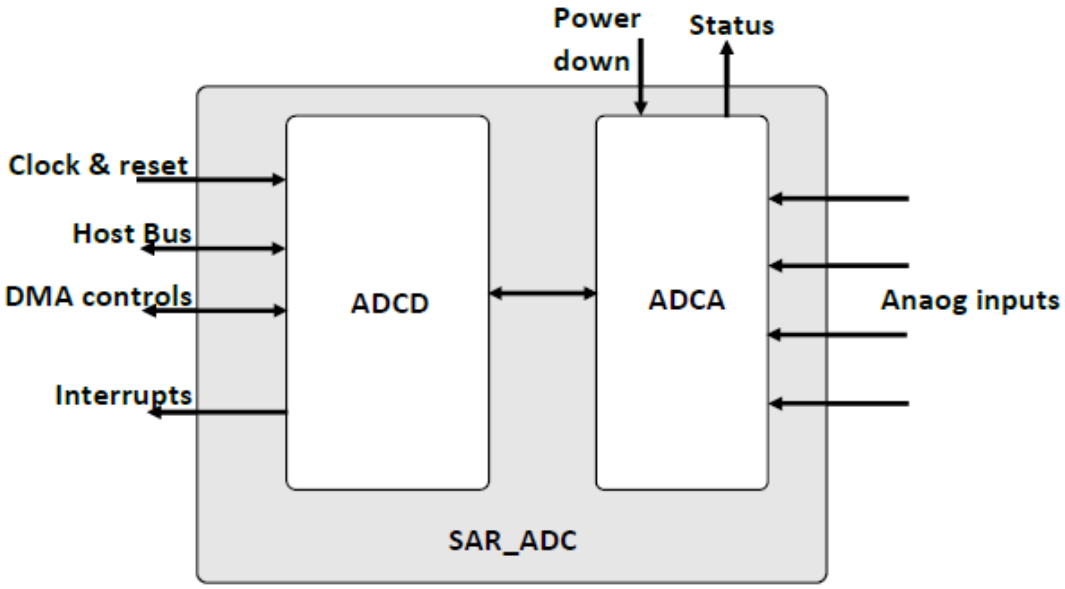


Figure 6 - SAR_ADC High-level interface Diagram

Table 12 - ADC Interface Pads Assigment

Signal Name	Pad Type	FCBGA #	Notes
ADC_SE0	Analog	A23	ADC Single Ended Input 0
ADC_SE1	Analog	A22	ADC Single Ended Input 1
ADC_SE2	Analog	A24	ADC Single Ended Input 2
ADC_SE3	Analog	B23	ADC Single Ended Input 3
ADC_SE4	Analog	B22	ADC Single Ended Input 4
ADC_SE5	Analog	B21	ADC Single Ended Input 5
ADC_SE6	Analog	B25	ADC Single Ended Input 6
ADC_SE7	Analog	B24	ADC Single Ended Input 7

3.15. Uart Interface

The S32v234 SoC contains 2 LINFlexD instances. The LINFlexD controller is designed to manage a high number of LIN messages efficiently with a minimum of CPU load. The LINFlexD also provides support for some of the basic UART transfers of 8-bit, 9-bit frames.

The AES-S32V-NXP-G (Core board) exports the UART0 and UART1 to J2 [15:16] and J3 [71:72] respectively. Note that UART ports is multiplexing with BOOT RCON IO.

Table 13 - Uart Interface Pads Mapping

Signal Name	Port #	FCBGA #	Notes
RCON3_UART0_RXD	PA11	G10	UART 0 Receive Data
RCON4_UART0_TXD	PA12	G11	UART 0 Transmit Output
RCON5_UART1_RXD	PA13	AA20	UART 1 Receive Data

RCON6_UART1_TXD	PA14	AA21	UART 1 Transmit Output

3.16. JTAG Interface

The S32v234 SoC contains JTAG Controller. The AES-S32V-NXP-G (Core board) exports JTAG interface to on-board 10-pin JTAG connector J4.

Table 14 - JTAG Interface Pads Assignment

Signal Name	Port #	FCBGA #	Notes
JTAG_TDI	PA0	A9	JTAG Test Data Input
JTAG_TDO	PA1	E10	JTAG Test Data Output
JTAG_TMS	PL3	D9	JTAG Test Mode Input
JTAG_TCK	PL4	B9	JTAG Test Clock Input

The pin assignment of J4 is not stander mini-10 JTAG interface. Customers need to do pin transform to stander JTAG interface.

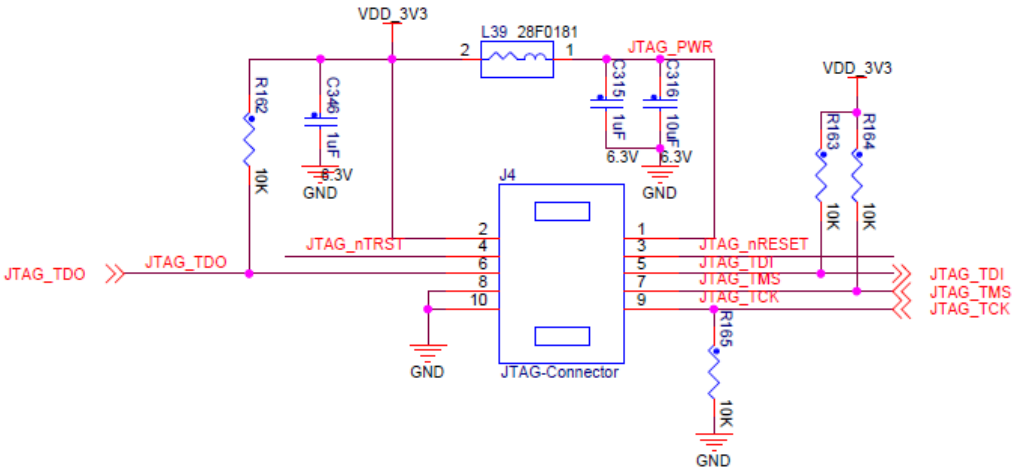


Figure 7 - Schematic of JTAG Connector

Figure 8 - Stander 10-pin JTAG Interface

3.17. Trace Interface

The S32V234 SoC generates the trace via the ARM Trace port. The trace port consists of TRACECLK, TRACECTL and TRACEDATA[15:0] pads. The TRACEDATA and TRACECTL toggle on both edges of TRACECLK. These pads can toggle at a maximum 150MHz frequency. When not being used for trace, these pads can be used for alternate GPIO functions. Refer to S32V234 IOMuxing sheet for the

alternate pin-muxing details.

The AES-S32V-NXP-G (Core board) exports Trace interface to J3 [22:38] for Custom Carrier Board.

Table 15 - Trace Port Pads Assignment

Signal Name	Port #	FCBGA #	Notes
TRACE_D00	PG8	AD18	Trace Port Data 0 Output
TRACE_D01	PG9	Y18	Trace Port Data 1 Output
TRACE_D02	PG10	AB17	Trace Port Data 2 Output
TRACE_D03	PG11	W17	Trace Port Data 3 Output
TRACE_D04	PG12	AC16	Trace Port Data 4 Output
TRACE_D05	PG13	Y17	Trace Port Data 5 Output
TRACE_D06	PG14	AA16	Trace Port Data 6 Output
TRACE_D07	PG15	AD15	Trace Port Data 7 Output
TRACE_D08	PH0	AE19	Trace Port Data 8 Output
TRACE_D09	PH1	AA17	Trace Port Data 9 Output
TRACE_D10	PH2	AE18	Trace Port Data 10 Output
TRACE_D11	PH3	AD17	Trace Port Data 11 Output
TRACE_D12	PH4	AE17	Trace Port Data 12 Output
TRACE_D13	PH5	AD16	Trace Port Data 13 Output
TRACE_D14	PH6	AE16	Trace Port Data 14 Output
TRACE_D15	PH7	AB16	Trace Port Data 15 Output
TRACE_CLK	PG7	AB15	Trace Port Clock Output

3.18. 2 x MIPI CSI Interface

The S32v234 SOC contains two identical instances of MIPICSI2- MIPICSI2_0 and MIPICSI2_1. The AES-S32V-NXP-G (Core board) exports MIPICSI2 interfaces J2 [27:46] for custom Carrier Board.

Table 16 - MIPI-CSI0 port mapping

Signal Name	Pad Type	FCBGA #	Notes
CSI0_CLK_P	MIPI_PAD	G17	MIPI CSI-2 Clock Positive Input
CSI0_CLK_N	MIPI_PAD	G18	MIPI CSI-2 Clock Negative Input
CSI0_DATA0_P	MIPI_PAD	A17	MIPI CSI-2 Positive Input Data Lane 0
CSI0_DATA0_N	MIPI_PAD	B17	MIPI CSI-2 Negative Input Data Lane 0
CSI0_DATA1_P	MIPI_PAD	B18	MIPI CSI-2 Positive Input Data Lane 1
CSI0_DATA1_N	MIPI_PAD	A18	MIPI CSI-2 Negative Input Data Lane 1
CSI0_DATA2_P	MIPI_PAD	D17	MIPI CSI-2 Positive Input Data Lane 2
CSI0_DATA2_N	MIPI_PAD	E17	MIPI CSI-2 Negative Input Data Lane 2
CSI0_DATA3_P	MIPI_PAD	E18	MIPI CSI-2 Positive Input Data Lane 3
CSI0_DATA3_N	MIPI_PAD	D18	MIPI CSI-2 Negative Input Data Lane 3

Table 17 - MIPI-CSI1 port mapping

Signal Name	Pad Type	FCBGA #	Notes
CSI1_CLK_P	MIPI_PAD	G14	MIPI CSI-2 Clock Positive Input
CSI1_CLK_N	MIPI_PAD	G15	MIPI CSI-2 Clock Negative Input
CSI1_DATA0_P	MIPI_PAD	A14	MIPI CSI-2 Positive Input Data Lane 0
CSI1_DATA0_N	MIPI_PAD	B14	MIPI CSI-2 Negative Input Data Lane 0
CSI1_DATA1_P	MIPI_PAD	B15	MIPI CSI-2 Positive Input Data Lane 1
CSI1_DATA1_N	MIPI_PAD	A15	MIPI CSI-2 Negative Input Data Lane 1
CSI1_DATA2_P	MIPI_PAD	D14	MIPI CSI-2 Positive Input Data Lane 2
CSI1_DATA2_N	MIPI_PAD	E14	MIPI CSI-2 Negative Input Data Lane 2
CSI1_DATA3_P	MIPI_PAD	E15	MIPI CSI-2 Positive Input Data Lane 3
CSI1_DATA3_N	MIPI_PAD	D15	MIPI CSI-2 Negative Input Data Lane 3

3.19. Display Interface

The 2D-ACE (Two Dimensional Animation and Compositing Engine, or DCU) is a system master that fetches graphics stored in DDR memory and displays them on a TFT LCD panel. A wide range of panel sizes is supported and the timing of the interface signals is highly configurable. Graphics are read directly from memory and then blended in real-time, which allows for dynamic content creation with minimal CPU intervention. Graphics may be encoded in a variety of formats to optimize memory usage.

The AES-S32V-NXP-G (Core board) exports DCU interface to J1 [13:40] for custom Carrier Board.

Table 18 - DCU port mapping

Signal Name	Port #	FCBGA #	Notes
DISP0_DAT00	PJ13	L21	DCU Blue 0 Output
DISP0_DAT01	PJ14	M25	DCU Blue 1 Output
DISP0_DAT02	PJ15	L23	DCU Blue 2 Output
DISP0_DAT03	PK0	M22	DCU Blue 3 Output
DISP0_DAT04	PK1	L22	DCU Blue 4 Output
DISP0_DAT05	PK2	L25	DCU Blue 5 Output
DISP0_DAT06	PK3	K23	DCU Blue 6 Output
DISP0_DAT07	PK4	L24	DCU Blue 7 Output
DISP0_DAT08	PJ5	K22	DCU Green 0 Output
DISP0_DAT09	PJ6	K25	DCU Green 1 Output
DISP0_DAT10	PJ7	J24	DCU Green 2 Output
DISP0_DAT11	PJ8	K20	DCU Green 3 Output
DISP0_DAT12	PJ9	J22	DCU Green 4 Output
DISP0_DAT13	PJ10	J25	DCU Green 5 Output
DISP0_DAT14	PJ11	H24	DCU Green 6 Output
DISP0_DAT15	PJ12	J23	DCU Green 7 Output

DISP0_DAT16	PH13	H23	DCU Red 0 Output
DISP0_DAT17	PH14	H25	DCU Red 1 Output
DISP0_DAT18	PH15	J21	DCU Red 2 Output
DISP0_DAT19	PJ0	H22	DCU Red 3 Output
DISP0_DAT20	PJ1	H21	DCU Red 4 Output
DISP0_DAT21	PJ2	G25	DCU Red 5 Output
DISP0_DAT22	PJ3	K19	DCU Red 6 Output
DISP0_DAT23	PJ4	G23	DCU Red 7 Output
DISP0_VSYNC	PH9	M21	DCU Vertical Sync Output
DISP0_HSYNC	PH8	M24	DCU Horizontal Sync Output
DISP0_DE	PH10	M23	DCU Data Enable Output
DISP0_PCLK	PH12	L20	DCU Pixel Clock Output

3.20. LFAST Interface

The LFAST module implements the LVDS Fast Asynchronous Serial Transmission (LFAST) module. LFAST is used in dual mode (software configurable master/slave operation) for interprocessor communications.

LFAST is a five pin interface with the following signals:

- lfast_sysclk - Reference clock of the LFAST master and slave
- txdatap/txdatan - Differential transmit (Tx) interface pair
- rxdatap/rxdatan - Differential receive (Rx) interface pair

LFAST interface is an asynchronous high speed LVDS interface.

The AES-S32V-NXP-G (Core board) exports LFAST interface to J3 for customer carrier board. Note that LFAST_REF_CLK pin is multiplexing with RCON31_FXT0_CH3.

Table 19 - LFAST Interface Pads Assignment

Signal Name	Pad Type	FCBGA #	Notes
LFAST_RX_N	LFAST_PAD	AA14	High-Speed LFAST Receive Neg Terminal
LFAST_RX_P	LFAST_PAD	AA13	High-Speed LFAST Receive Pos Terminal
LFAST_TX_N	LFAST_PAD	W14	High-Speed LFAST Transmit Neg Terminal/ PCI Express Clock Neg Terminal output (select via SRC_SOC.GPR3[4])
LFAST_TX_P	LFAST_PAD	W13	High-Speed LFAST Transmit Pos Terminal/ PCI Express Clock Pos Terminal output (select via SRC_SOC.GPR3[4])
LFAST_REF_CLK	PC8	AE22	LFAST Reference Clock

3.21. FlexTimer Interfaces

The FlexTimer module (FTM) is a two-to-eight channel timer that supports input capture, output compare, and the generation of PWM signals to control electric motor and power management applications. The FTM time reference is a 16-bit counter that can be used as an unsigned or signed counter.

The S32v234 SoC contains 2 FTM, FTM0 and FTM1. More information please referto S32v234RM3.0.pdf.

Table 20 – FlexTimer Features

Feature	FTM0	FTM1
Number of channels	6	6
Channel input filter	Channel 0, 1, 2 and 3	Channel 0, 1, 2 and 3
Number of fault inputs	0	0
Initial counting value	Yes	Yes
Input capture mode	Yes	Yes

The AES-S32V-NXP-G (Core board) exports FTM0 channel0~3 to J3 for customer carrier board.

Table 21 - FlexTimer Interface Pads assignment

Signal Name	Port #	FCBGA #	Notes
RCON28_FXT0_CH0	PC5	AD23	FlexTimer 0 Channel 0 Input/Output
RCON29_FXT0_CH1	PC6	AD24	FlexTimer 0 Channel 1 Input/Output
RCON30_FXT0_CH2	PC7	AE23	FlexTimer 0 Channel 2 Input/Output
RCON31_FXT0_CH3	PC8	AE22	FlexTimer 0 Channel 3 Input/Output

3.22. FlexRay Interface

The S32v234 SoC contains a FlexRay Communication Controller. That implements the FlexRay Communications System Protocol Specification, Version 2.1 Rev A.

The CC has three main components:

- Controller host interface (CHI)
- Protocol engine (PE)
- Clock domain crossing unit (CDC)

A block diagram of the CC with its surrounding modules is given in the below figure.

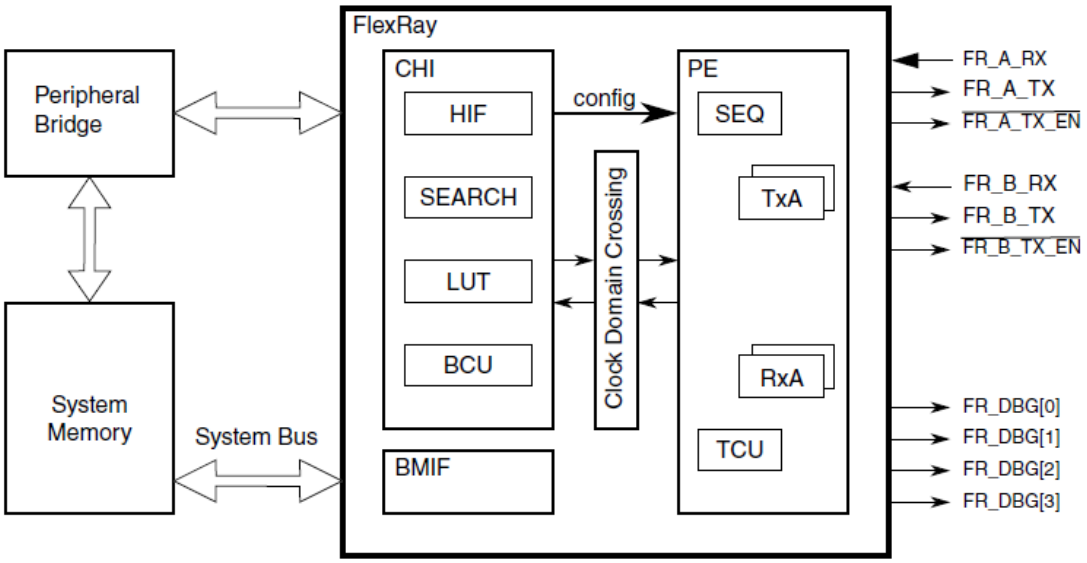


Figure 9 – FlexRay Block Diagram

The AES-S32V-NXP-G (Core board) exports following FlexRay interface to J2 [7:10] for customer carrier board.

Table 22 - FlexRay Interface Pads Assignment

Signal Name	Port #	FCBGA #	Notes
RCON2_FLXR_RXD_A	PA9	B11	FlexRay Receive Data Channel A Input
RCON1_FLXR_TXD_A	PA8	A11	FlexRay Transmit Data Channel A Output
FLXR_TXEN_A	PA6	C12	FlexRay Transmit Enable Channel A Output
RCON0_FLXR_TXEN_B	PA7	C11	FlexRay Transmit Enable Channel B Output

3.23. FCCU Outputs

The Fault Collection and Control Unit (FCCU) offers a hardware channel to collect faults and to place the device into a safe state when a failure in the device is detected. No CPU intervention is requested for collection and control operation. More information please refer to S32v234RM3.0.pdf

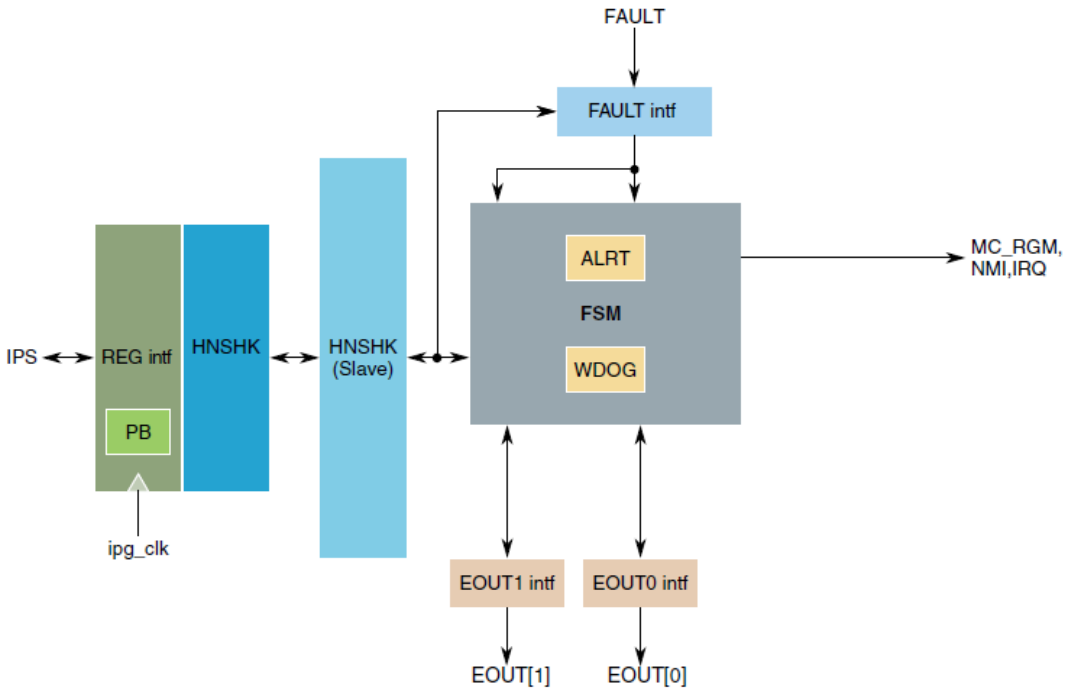


Figure 10 - FCCU block diagram

The AES-S32V-NXP-G (Core board) exports FCCU_F0 and FCCU_F1 to J2 for customer carrier board.

Table 23 - FCCU Output Pads Assignment

Signal Name	FCBGA #	Notes
FCCU_F0	E11	FCCU Fault 0
FCCU_F1	E12	FCCU Fault 1

3.24. PCIE Interface

The AES-S32V-NXP-G (Core board) export PCIe Interface to J3 for custom Carrier Board.

Tabel 24 - PCIe Interface

Signal Name	Pad Type	FCBGA #	Notes
PCIE_CK_N	PCIE_PAD	AA10	PCI Express Clock Neg Terminal
PCIE_RX_N	PCIE_PAD	AA11	PCI Express Receive Neg Terminal
PCIE_CK_P	PCIE_PAD	AE11	PCI Express Clock Pos Terminal
PCIE_RX_P	PCIE_PAD	AE10	PCI Express Receive Pos Terminal
PCIE_TX_N	PCIE_PAD	AC11	PCI Express Transmit Neg Terminal
PCIE_TX_P	PCIE_PAD	AC10	PCI Express Transmit Pos Terminal

3.25. 2xVIU Interface

The VIULite is a bridge between external image sensor and system memory. It decodes different input image format, packs them as the expected data, and transfers them to

system memory via its own master bus interface.
The device contains two instances of VIULite - VIU0 and VIU1.
VIU0 supports upto 20 bit pixel data inputs and VIU1 supports upto 16 bit pixel data inputs with lower 4 bits multiplexed. Please refer to I/O Signal Description and Input Multiplexing Tables (Excel files) of chapter "Signal Description" for details.
The AES-S32V-NXP-G (Core board) VIU0 supports 16 bit pixel data inputs, and VIU1 support 8 bit pixel data inputs. The AES-S32V-NXP-G (Core board) exports VIU0 ports to J2 [59:77], and VIU1 ports to J1 [45:52] for custom Carrier Board.

Table 25 - VIU0 Ports Mapping

Signal Name	Port #	FCBGA #	Notes
IPL_VIU0_D08	PE0	E20	Parallel Data 0 Data Input
IPL_VIU0_D09	PE1	J20	Parallel Data 0 Data Input
IPL_VIU0_D10	PE2	G20	Parallel Data 0 Data Input
IPL_VIU0_D11	PE3	D20	Parallel Data 0 Data Input
IPL_VIU0_D12	PE4	H20	Parallel Data 0 Data Input
IPL_VIU0_D13	PE5	D21	Parallel Data 0 Data Input
IPL_VIU0_D14	PE6	F21	Parallel Data 0 Data Input
IPL_VIU0_D15	PE7	D22	Parallel Data 0 Data Input
IPL_VIU0_D16	PE8	D24	Parallel Data 0 Data Input
IPL_VIU0_D17	PE9	F22	Parallel Data 0 Data Input
IPL_VIU0_D18	PE10	D23	Parallel Data 0 Data Input
IPL_VIU0_D19	PE11	E23	Parallel Data 0 Data Input
IPL_VIU0_D20	PE12	E22	Parallel Data 0 Data Input
IPL_VIU0_D21	PE13	G21	Parallel Data 0 Data Input
IPL_VIU0_D22	PE14	F23	Parallel Data 0 Data Input
IPL_VIU0_D23	PE15	F25	Parallel Data 0 Data Input
IPL_VIU0_HSYNC	PD14	F24	Parallel Data 0 Horizontal Sync Input
IPL_VIU0_PCLK	PD13	D25	Parallel Data 0 Clock Input
IPL_VIU0_VSYNC	PE0	E25	Parallel Data 0 Vertical Sync Input

Table 26 - VIU1 Ports Mapping

Signal Name	Port #	FCBGA #	Notes
IPL_VIU1_D17	PF12	T23	Parallel Data 1 Data Input
IPL_VIU1_D18	PF13	P20	Parallel Data 1 Data Input
IPL_VIU1_D19	PF14	T25	Parallel Data 1 Data Input
IPL_VIU1_D20	PF15	R22	Parallel Data 1 Data Input
IPL_VIU1_D21	PG0	R24	Parallel Data 1 Data Input
IPL_VIU1_D22	PG1	R23	Parallel Data 1 Data Input
IPL_VIU1_D23	PG2	R25	Parallel Data 1 Data Input
IPL_VIU1_PCLK	PF0	P23	Parallel Data 1 Clock Input

3.26. EMMC memory

The S32v234 SoC supports one ultra Secure Digital Host Controller (uSDHC) module. The uSDHC provides the interface between the host system and the SD/SDIO/MMC cards.

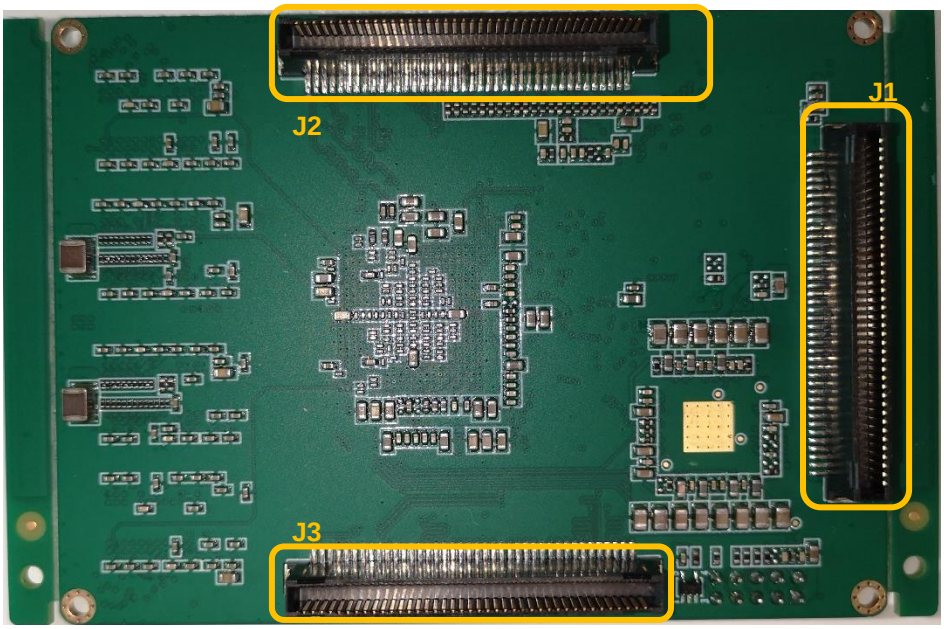
The AES-S32V-NXP-G (Core board) provides a 32GB eMMC memory as one of booting devices. The EMMC device connect to multiplexing IO ports PF [1:11], and PK14 as eMMC data strobe input.

Table 27 - USDHC eMMC Ports Mapping

Signal Name	Port #	FCBGA #	Notes
eMMC_DATA0	PF3	M20	SD Data 0
eMMC_DATA1	PF4	N23	SD Data 1
eMMC_DATA2	PF5	N20	SD Data 2
eMMC_DATA3	PF6	N25	SD Data 3
eMMC_DATA4	PF7	N19	SD Data 4
eMMC_DATA5	PF8	N22	SD Data 5
eMMC_DATA6	PF9	P24	SD Data 6
eMMC_DATA7	PF10	P25	SD Data 7
eMMC_RESET	PF11	T22	SD Reset Output
eMMC_CMD	PF2	P22	SD Command
eMMC_CLK	PF1	P21	SD Clock
eMMC_DATA_STROBE	PK14	R20	General Purpose I/O 158

3.27. J1~J3 Micro Connectors

The AES-S32V-NXP-G (Core board) utilizes 3 80-pin micro headers to provide connections to the Carrier Card. These connectors carry most of module signals of S32v234 SoC. Following diagram shows modules exported on J1 – J3.



Picture 1 - J1 – J3

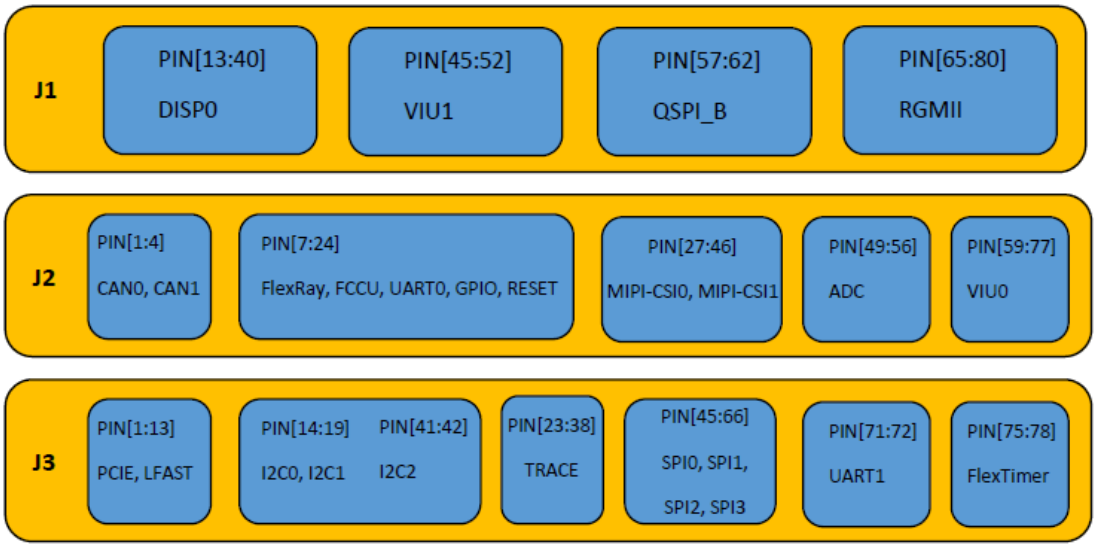
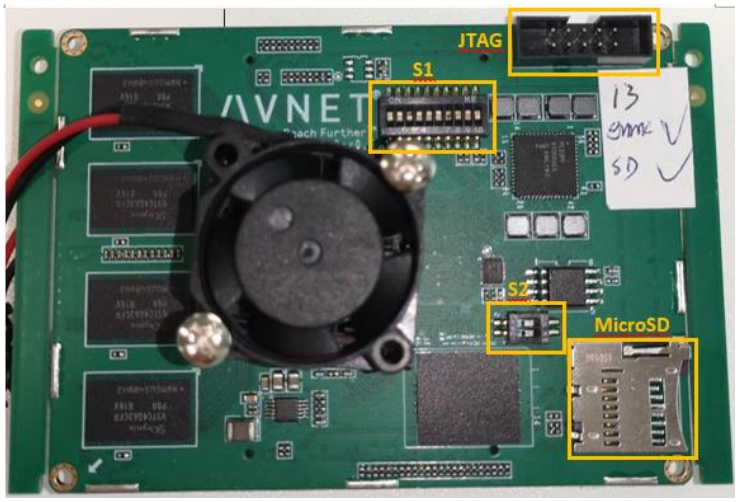


Figure 11 - J1, J2, J3 Exporting Module Diagram

3.28. Boot Configuration Switches

The AES-S32V-NXP-G (Core board) provides 2 switches to select boot configurations, S1 and S2.



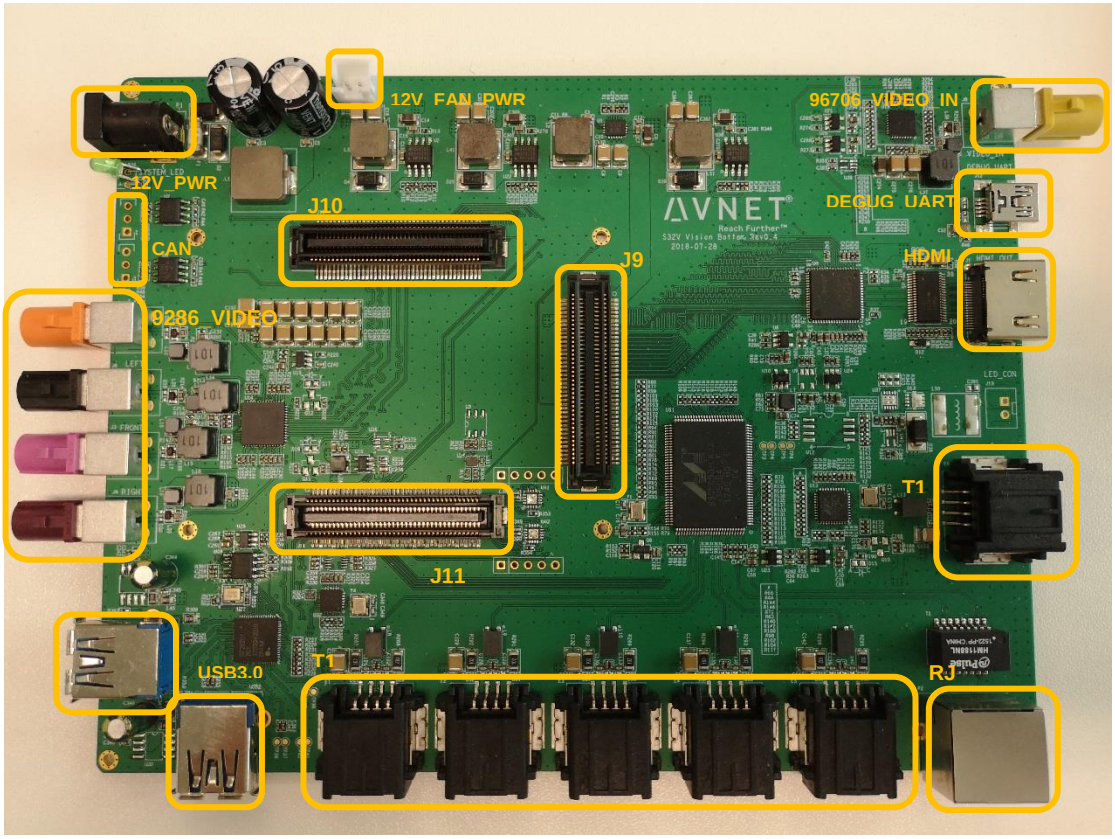
Picture 2 - Boot Configuration Switches, S1, S2

Table 28 - Boot Configuration Signal to Switch Pin Mapping

Signal Name	Switch #	Switch Pos #
QSPI_EMMC_SW	S2	1
RCON6_UART1_TXD	S2	2
RCON0_FLXR_TXEN_B	S1	1
RCON7_GPIO15	S1	2
RCON9_GPIO17	S1	3
RCON13_SPI0_SOUT	S1	4
RCON17_SPI1_SOUT	S1	5

RCON21_SPI2_SOUT	S1	6
RCON31_FXT0_CH3	S1	7
RCON23_SPI2_CS0	S1	8
BOOT_MODE1	S1	9
BOOT_MODE0	S1	10

4. AES-S32V-NXP-G (Carrier board) Resources



Picture 3 – AES-S32V-NXP-G (Carrier board) Connects

4.1. Power Input

The Avnet AES-S32V-NXP-G (Carrier board) requires 12V-DC power input from P1.Voltage regulators are used on the Avnet AES-S32V-NXP-G (Carrier board) to provide power to all components/interfaces used on the Avnet AES-S32V-NXP-G (Carrier board), and provide voltages, VDD_1V8, VDD_3V3, PMIC_FEED_5V0, to the AES-S32V-NXP-G (Core board) via J9. Please refer to schematic s32v234_carrier_board_rev0_6.pdf for more information.

- 1.8V via J9[9:10]
- 3.3V via J9[7:8]
- PMIC feed 5.0V via J9[1:6]

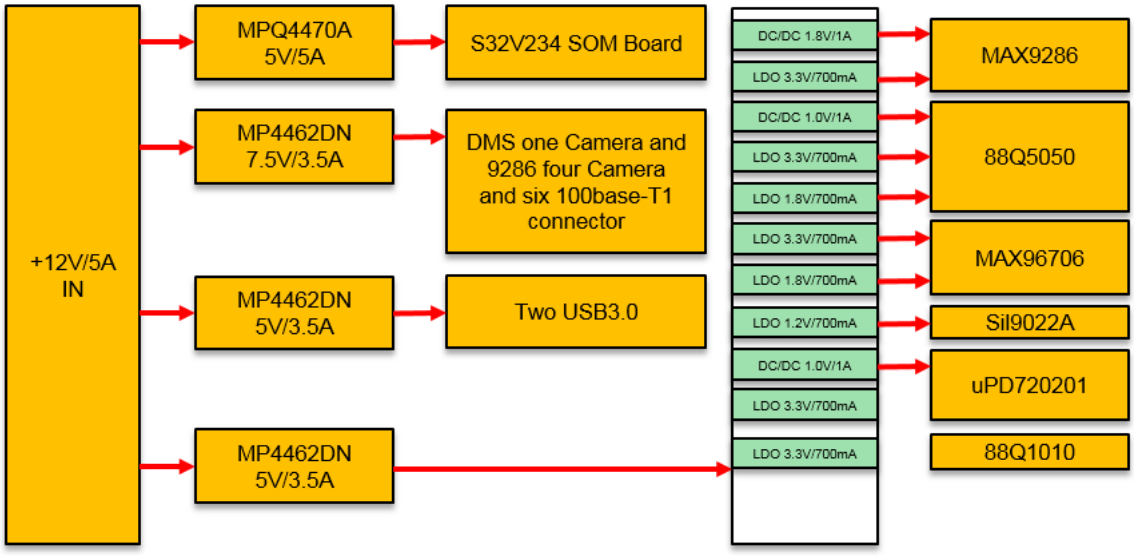


Figure 12 – AES-S32V-NXP-G (Carrier board) Power Supply Diagram

4.2. Soc Heat Fan Power Input

The AES-S32V-NXP-G (Core board) uses a heat sink with fan for S32v234 SoC device. Users can use either a 5V or a 12V fan with the AES-S32V-NXP-G (Core board) heat sink (The AES-S32V-NXP-G (Core board) is shipped with a 12V fan). The fan header are located on the Avnet AES-S32V-NXP-G (Carrier board) and must be designed to match the fan voltage used on the SOM.

NOTE: The heatsink with fan provided with the AES-S32V-NXP-G (Core board) is designed to be appropriate for most use cases except for the industrial high temperature extremes. It is expected that a system designer will perform worst case analysis of the thermal environment of the final solution and devise a proper thermal solution for the challenges presented in the operating environment.

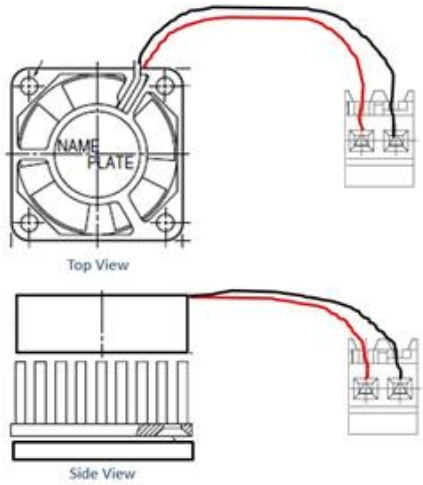


Figure 10 – AES-S32V-NXP-G (Carrier board) 12VDC HeatSink and Fan Assembly

4.3. 2 x CAN Connector

The Avnet AES-S32V-NXP-G (Carrier board) contains two CAN connectors. Between the CAN connector and each channel of FlexCAN signals from AES-S32V-NXP-G (Core board), there is a high speed CAN transceiver TJA1040.

The TJA1040 is the interface between the Controller Area Network (CAN) protocol controller and the physical bus. It is primarily intended for high speed applications, up to 1 MBaud, in passenger cars. The device provides differential transmit capability to the bus and differential receive capability to the CAN controller.

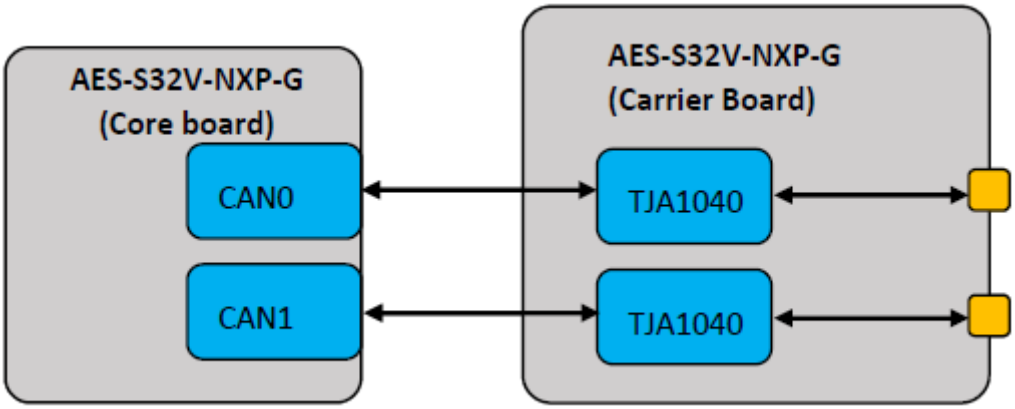


Figure 13 - CAN Block Diagram

4.4. 2 x SPI Connectors

The Avnet AES-S32V-NXP-G (Carrier board) contains two SPI connectors. Between the SPI connector and each channel of SPI signals from AES-S32V-NXP-G (Core board), there is a four-pole double-throw analog switch NX3DV2567HR.

The NX3DV2567 is a four-pole double-throw analog switch (4PDT) optimized for switching WLAN-SIM supply, data and control signals. It has one digital select input (S) and four switches each with two independent input/outputs (nY0 and nY1) and a common input/output (nZ). Schmitt trigger action at S makes the circuit tolerant to slower input rise and fall times across the entire VCC range from 1.4 V to 4.3 V

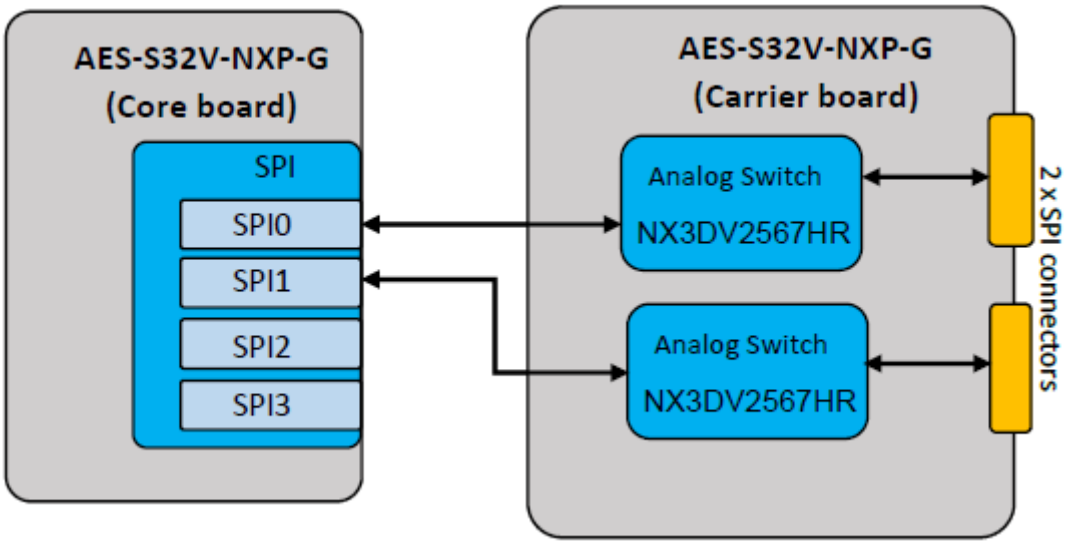


Figure 14 - SPI Block Diagram

4.5. Debug UART Port

The Avnet AES-S32V-NXP-G (Carrier board) provide a debug uart via Micro-USB port.The TX/RX signals come from AES-S32V-NXP-G (Core board) LinFlexD0 controller.

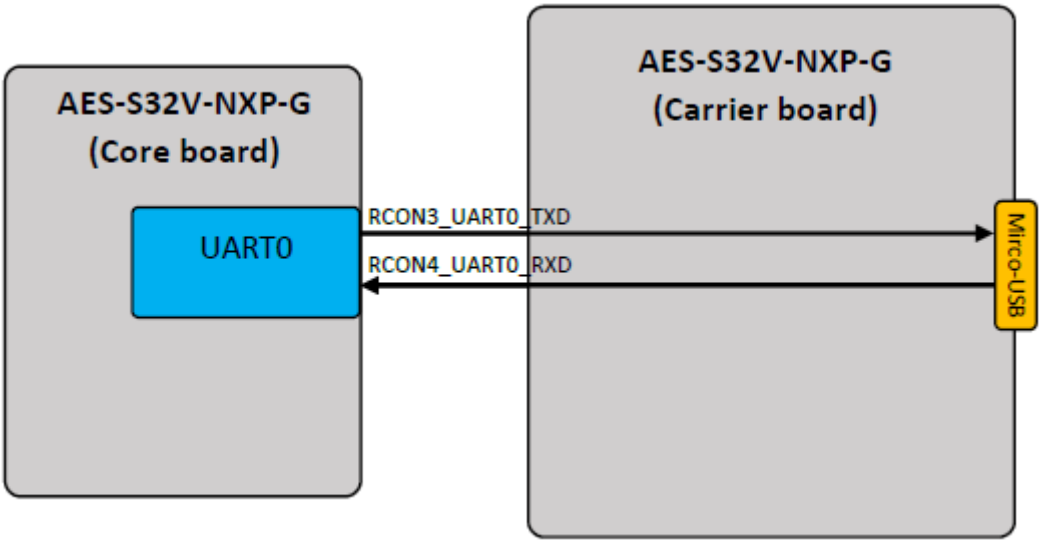


Figure 15 - Debug UART Block Diagram

4.6. PWM Output

The AES-S32V-NXP-G (Carrier board) provides a PWM header intended for DMS camera LED. The PWM sigal comes from FlexTimer module of S32v234 SoC, exported by AES-S32V-NXP-G (Core board) J3 header.

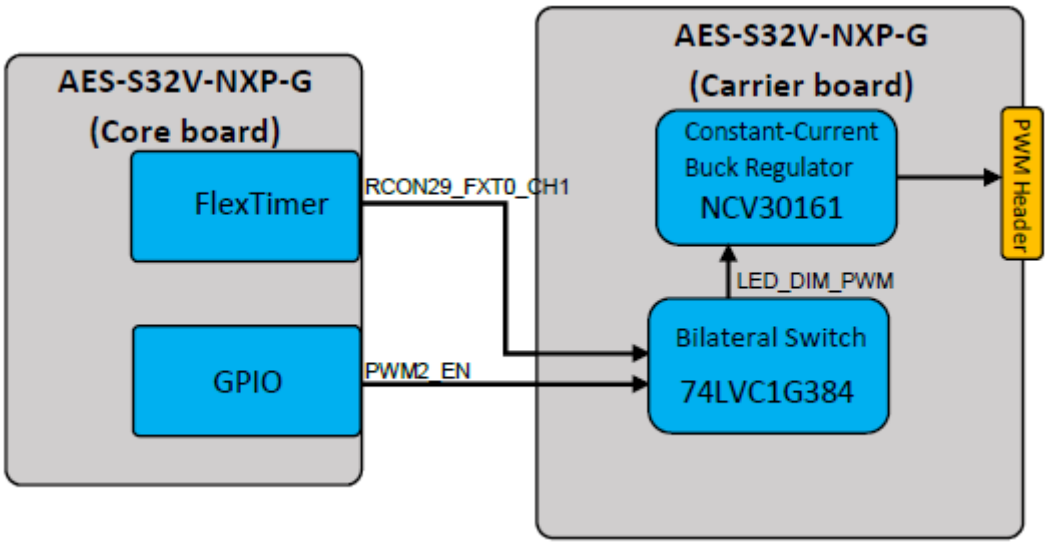


Figure 16 - PWM Interface block diagram

4.7. PHY connectors

The Avnet AES-S32V-NXP-G (Carrier board) provides following kinds of PHY connectors:

- 1 x RJ45 for DEBUG
- 5 x 100MB T1 for video in (one for front view, other four for surround view)
- 1 x 100MB T1 for video out

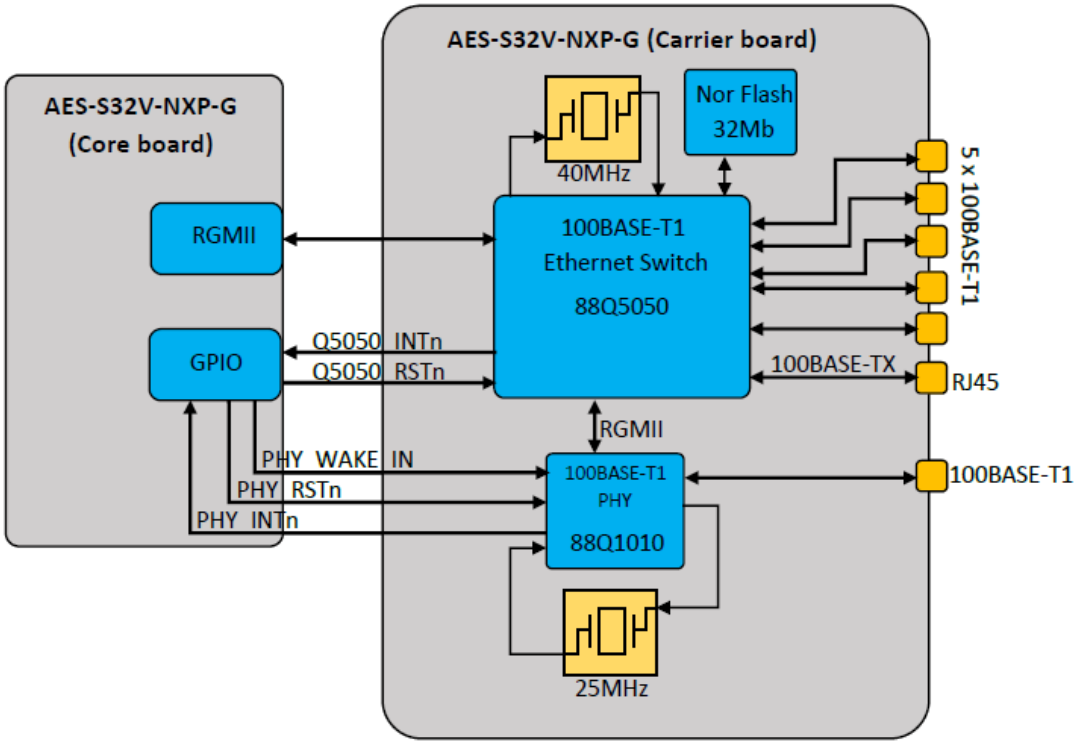


Figure 17 - PHY Block Diagram

4.7.1 Introduction of 88Q5050

The Ethernet switch, 88Q5050, is an 8-port Ethernet gigabit capacity switch that is fully compliant with IEEE802.3 automotive standard and utilizes advanced security features to guard against hacking and denial of service (DoS) attacks.

The 8-port Ethernet switch offers 4 fixed IEEE 100BASE-T1 ports, and a configurable selection of an additional 4 ports from 1x IEEE 100BASE-T1 port, 1x IEEE 100BASE-TX, 2x MII/RMII/RGMII ports, 1 GMII port, and 1 SGMII port. The switch offers local and remote management capabilities, providing easy access and configuration of the device.

Table 29 - 88Q5050 Key Features and Benefits

Features	Benefits
Processor	Integrated ARM Cortex-M7 CPU, 250MHz
IO Interfaces	4 IEEE 100BASE-T1
	Additional 4 ports confi gured from: • 1 IEEE 100BASE-T1 port • 1 IEEE 100BASE-TX • 2 MII/RMII/RGMII ports • 1 GMII port • 1 SGMII port
	2 SMI • Master interface to connect to external PHYs or additional switches • Slave interface to manage the switch
	Configurable GPIOs
	QSPI with confi gurable frequencies (19.2MHz-83.3MHz)
	TWSI Master interface
	JTAG
Package Characteristics	88Q5050 : 128-pin LQFP package, 0.5 mm pitch, 14mmx20mm
	88Q5054: 228-pin BGA package , 0.8mm pitch , 13mmx13mm
EEPROM	Slave interface with loader to confi gure the switch (32Kb-512kb)

4.7.2 Introduction of 88Q1010

The 88Q1010 is a single pair Ethernet physical layer transceiver (PHY) which implements the Ethernet physical layer portion of the 100BASE-T1 standard as defi ned by the IEEE 802.3bw task force. Ideally suited for a wide range of automotive applications, it is manufactured using a standard digital CMOS process and contains all the active circuitry required to implement the physical layer functions to transmit and receive data on a single balanced twisted pair.

88Q1010 integrates media dependent interface (MDI) termination resistors into the PHY which simplifi es the board layout and reduces board cost by reducing the number of external components. It has an integrated linear voltage regulator to generate all required voltages so the device can run off a single 3.3V supply. The solution supports 1.8V, 2.5V, and 3.3V LVCMOS I/O standards.

In addition, 88Q1010 uses advanced mixed-signal processing to perform

equalization, echo, data recovery, and error correction at a 100Mbps data rate to achieve robust performance and exceed automotive electromagnetic interference (EMI) requirements in noisy environments with very low power dissipation.

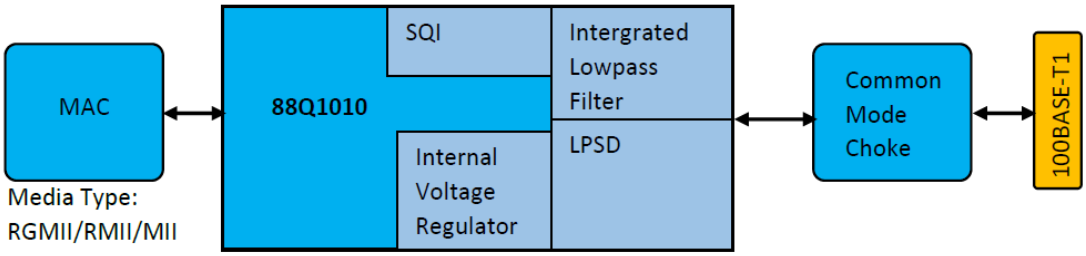


Figure 18 – 88Q1010 Block Diagram

4.8. HDMI

The AES-S32V-NXP-G (Core board) exports DCU signals from S32v234 SoC, which contains:

- DCU_PCLK
- DCU_VSYNC
- DCU_HSYNC
- DCU_DE
- DCU_R[0:7], DCU_G[0:7], DCU_B[0:7]

On the Avnet AES-S32V-NXP-G (Carrier board), above signals are sent to HDMI Transmitter Sil9022A which transform DCU signals to HDMI signals. Then the HDMI signals were sent to level shifter and ESD protection TPD12S521DBTR. The final HDMI signals were connected with HDMI input device via HDMI-TYPE-A-19 connector.

The S32v234 SoC can send control commands to HDMI tansmitter by I2C1, while GPIO[65] as HDMI_RESET signal and GPIO[67] as HDMI_CHIP_INT signal.

The TPD12S521 is a single-chip electro-static discharge (ESD) circuit protection device for the highdefinition multimedia interface (HDMI) transmitter port. While providing ESD protection with transient voltage suppression (TVS) diodes, the TVS protection adds little or no additional glitch in the high-speed differential signals. The high-speed transition minimized differential signaling (TMDS) ESD protection lines add only 0.8-pF capacitance. The low-speed control lines offer voltage-level shifting to eliminate the need for an external voltage levelshifter IC. The control line TVS diodes add 3.5-pF capacitance to the control lines. The 38-pin DBT package offers a seamless layout routing option to eliminate the routing glitch for the differential signal pairs. The DBT package pitch (0.5 mm) matches with the HDMI connector pitch. In addition, the pin mapping follows the same order as the HDMI connector pin mapping. The TPD12S521 provides an on-chip current limiting switch with output ratings of 55 mA at pin 38. This enables HDMI receiver detection even when the receiver device is powered off.

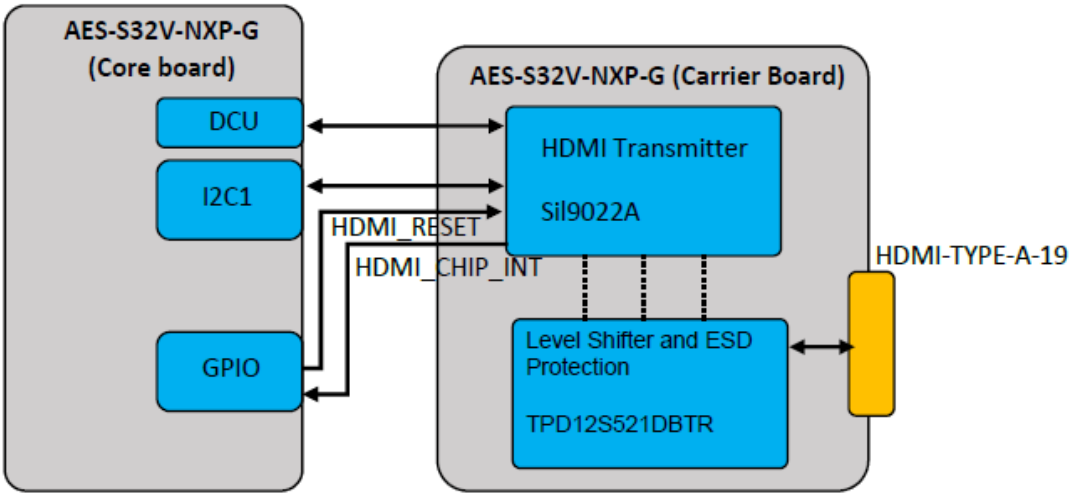


Figure 19 - HDMI Interface diagram

4.9. Camera Inputs

The Avnet AES-S32V-NXP-G (Carrier board) provides 5 coax cable connectors for 720P camera inputs, which can fulfill most ADAS applications, one for front view, other four for surround view. Camera data will be deserialized by MAX9286 and MAX96705, and transfer to S32v234 SoC via MIPI-CSI2 and VIU0 interface on the AES-S32V-NXP-G (Core board).

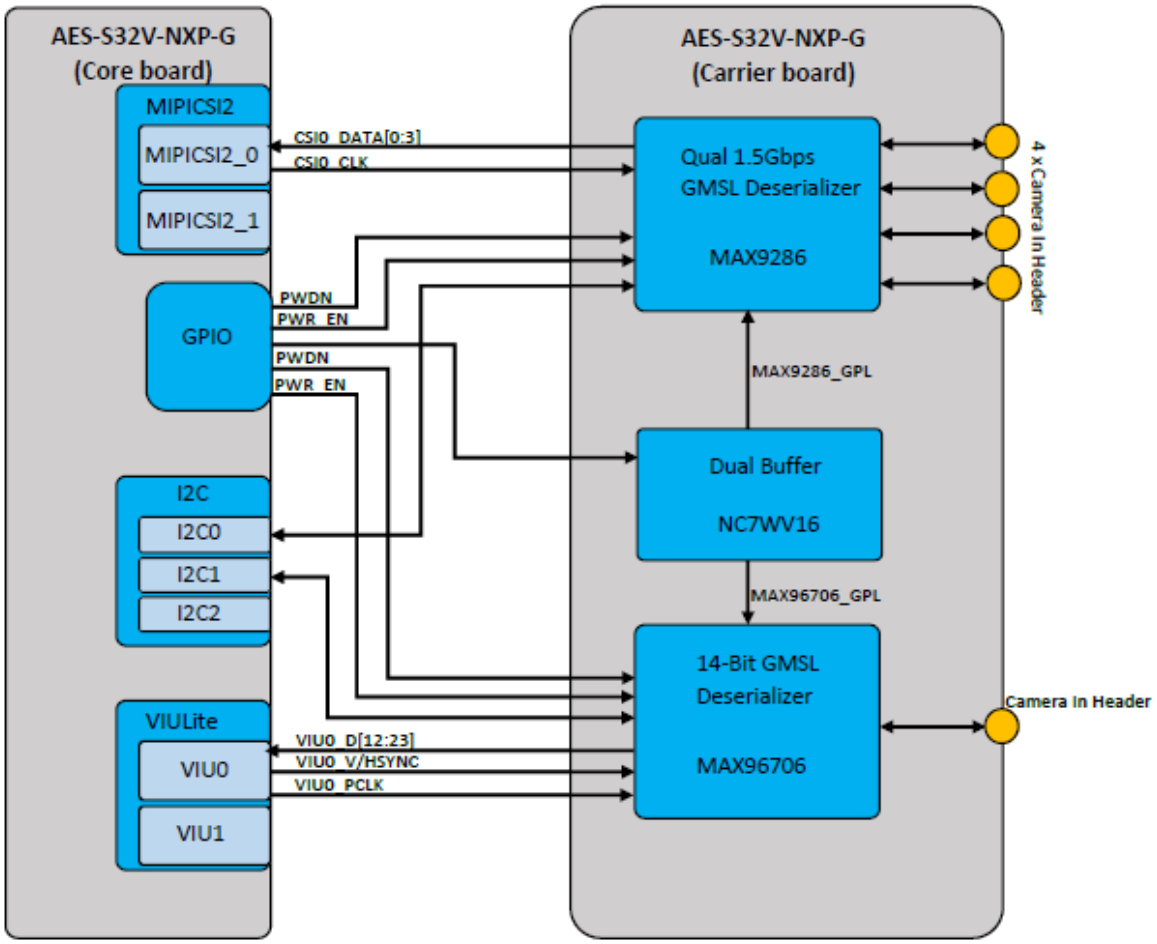


Figure 20 - Camera Inputs Block Diagram

4.9.1 Introduction of MAX9286

The MAX9286 Gigabit multimedia serial link (GMSL) deserializer receives data from up to four GMSL serializers over 50Ω coax or 100Ω shielded twisted-pair (STP) cables and output data on four CSI-2 lanes. Each serial link has an embedded control channel operating from 9.6kbps to 1Mbps in UART-to-UART, UART-to-I²C, and I²C-to-I²C mode. Using the control channel, a µC can program the serializers, deserializer, and peripheral device registers at any time, independent of video timing. A maskable broadcast write speeds programming of image sensor registers.

For use with longer cables, the deserializer has a programmable cable equalizer and programmable error detection and correction. The serial input meets ISO 10605 and IEC 61000-4-2 ESD standards. The core supply is 1.7V to 1.9V and the I/O supply is 1.7V to 3.6V.

The device is available in lead(Pb)-free, 56-pin, 8mm × 8mm SWTQFN and TQFN packages with exposed pad and 0.5mm lead pitch.

Key Features:

- Ideal for Multicamera Stream Applications
    - Works with Low-Cost 50Ω Coax Cable and FAKRA Connectors or 100Ω STP
    - Data from Image Sensors Are Synchronized to the Same Pixel
    - Automatic Internal/External Generation of Camera Sync
    - Equalization Allows 15m Length Cable Operation at Full Speed
- Multiple Input/Output Features for System Flexibility
    - 1 to 4 Lane CSI-2 Output with 80Mbps to 1200Mbps Per Lane
    - Swappable/Selectable Serial Input/Output with Swappable Polarity
    - 9.6kbps to 1Mbps Control Channel in UART, Mixed UART/I²C, or I²C Mode with Clock Stretch Capability
- Peripheral Features for System Power-Up and Verification
    - Built-In PRBS Tester for BER Testing of the Serial Link
    - Programmable Choice of Nine Default Device Addresses
    - Two Dedicated GPIO Ports
    - High-Immunity Mode for Maximum Control-Channel Noise Rejection
- Meets Rigorous Automotive and Industrial Requirements
    - -40°C to +105°C Operating Temperature
    - ±8kV Contact, ±20kV Air ISO 10605 and ±8kV Contact, ±12kV IEC 61000-4-2 ESD Protection

4.9.2 Introduction of MAX96706

The MAX96706 is a compact deserializer especially suited for automotive camera applications. Features include adaptive equalization and an output crosspoint switch. An embedded control channel operates at 9.6kbps to 1Mbps in UART, I2C, and mixed UART/ I2C modes, allowing programming of serializer, deserializer (SerDes), and camera registers, independent of video timing.

Key Features:

- Ideal for Safety Camera Applications
    - Works with Low-Cost 50Ω Coax (100Ω STP) Cable
    - Error Detection of Video/Control Data
    - High-Immunity Mode for Robust Control-Channel EMC Tolerance
    - Retransmission of Control Data Upon Error
    - Best-in-Class Supply Current: 190mA (max)
    - Adaptive Equalization for 15m Cable at Full Speed
    - 32-Pin (5mm × 5mm) TQFN/SWTQFN Package
    - Horizontal- and Vertical-Sync Encoding and Tracking
- High-Speed Deserialization for Megapixel Cameras
    - Up to 1.74Gbps Serial-Bit Rate
    - 6.25MHz to 87MHz × 12-Bit + H/V Data
    - 36.66MHz to 116MHz × 12-Bit + H/V Data (through Internal Encoding)
- Multiple Modes for System Flexibility

- 9.6kbps to 1Mbps Control Channel in UART, I2C (with Clock Stretch), or UART-to-I2C Modes
- 2:1 Input Mux for Camera Selection
- 15 Hardware-Selectable I2C-Device Addresses
- Pairs with Any Maxim GMSL Serializer
- Crosspoint Switch Maps Data to any Output

- Reduces EMI and Shielding Requirements
  - Spread-Spectrum Serial-Input Tracking and Transfer to the Parallel Output
  - 1.7V to 1.9V Core and 1.7V to 3.6V I/O Supply
- Peripheral Features for System Verification
  - Built-In PRBS Receiver for BER Testing
  - Eye-Width Monitor Allows In-System Test of High-Speed Serial Link
  - Dedicated “Up/Down” GPI for Camera Frame Sync Trigger and Other Uses
- Meets AEC-Q100 Automotive Specification
  - -40°C to +115°C Operating Temperature Range
  - ±8kV Contact and ±15kV Air IEC 61000-4-2 and ISO 10605 ESD Protection

4.10. PCIe to USB3.0

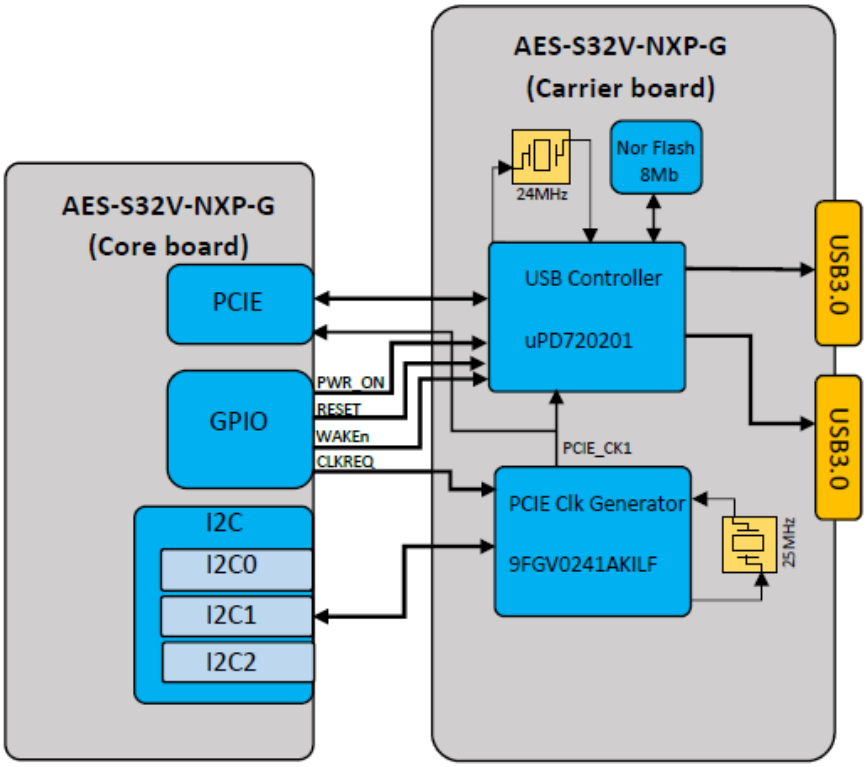


Figure 21 - PCIe to USB3.0 diagram

The Avnet AES-S32V-NXP-G (Carrier board) provides 2 USB3.0 ports. Converting PCIE signals from AES-S32V-NXP-G (Core board) to USB3.0 signals via a USB host controller, µPD720201.

The µPD720201 is a USB host controller LSI compatible with the USB 3.0 and xHCI (eXtensible Host Controller Interface) 1.0 specifications. The system bus is compatible with the PCIe Gen2 specification.The controller provides four USB ports with LS (low-Speed) / FS (full-Speed) / HS (high-Speed) / SS (SuperSpeed) support.

System I/F: PCIe Gen2 x 1 Lane

- USB ports: 4 ports (SS/HS/FS/LS)
- Comply spec to: PCIe 2.0 Base Spec
  USB3.0 rev1.0 (USB-IF certified: Test ID = 380000050)
  Intel xHCI rev 1.0
- VDD: 1.05V, 3.3V
- Clock: 24MHz Xtal clock input
- Package: 68 pin QFN (8x8mm, 0.4mm ball pitch)
- Ta: 0 ~ 85°C (µPD720201K8-701-BAC-A)
- Ta:-40 ~ 85°C (µPD720201K8-711-BAC-A)

4.11. J9~J11 Micro Connector

The Avnet AES-S32V-NXP-G (Carrier board) utilizes 3 micro headers to provide connections to AES-S32V-NXP-G (Core board). These connectors will carry the following signals and power/ground pins (signal directions are with respect to the AES-S32V-NXP-G (Core board)):

J9 Connector (80-pin IMSA-9827S-80ZXX-GF)

- Power and ground pins (VDD_1V8, VDD_3V3, PMIC_FEED_5V0 and GND)
- DCU pins (DISP0_DAT[00 :23], DISP0_VSYNC, DISP0_HSYNC, DISP0_DE, DISP0_PCLK)
- PWM enable pin (PWM2_EN)
- RGMII pins (RGMII_TX/RX_DATA[0:3], RGMII_MDC, RGMII_TX_EN, RGMII_MDIO, RGMII_TX/RX_CLK, RGMII_RX_DV)

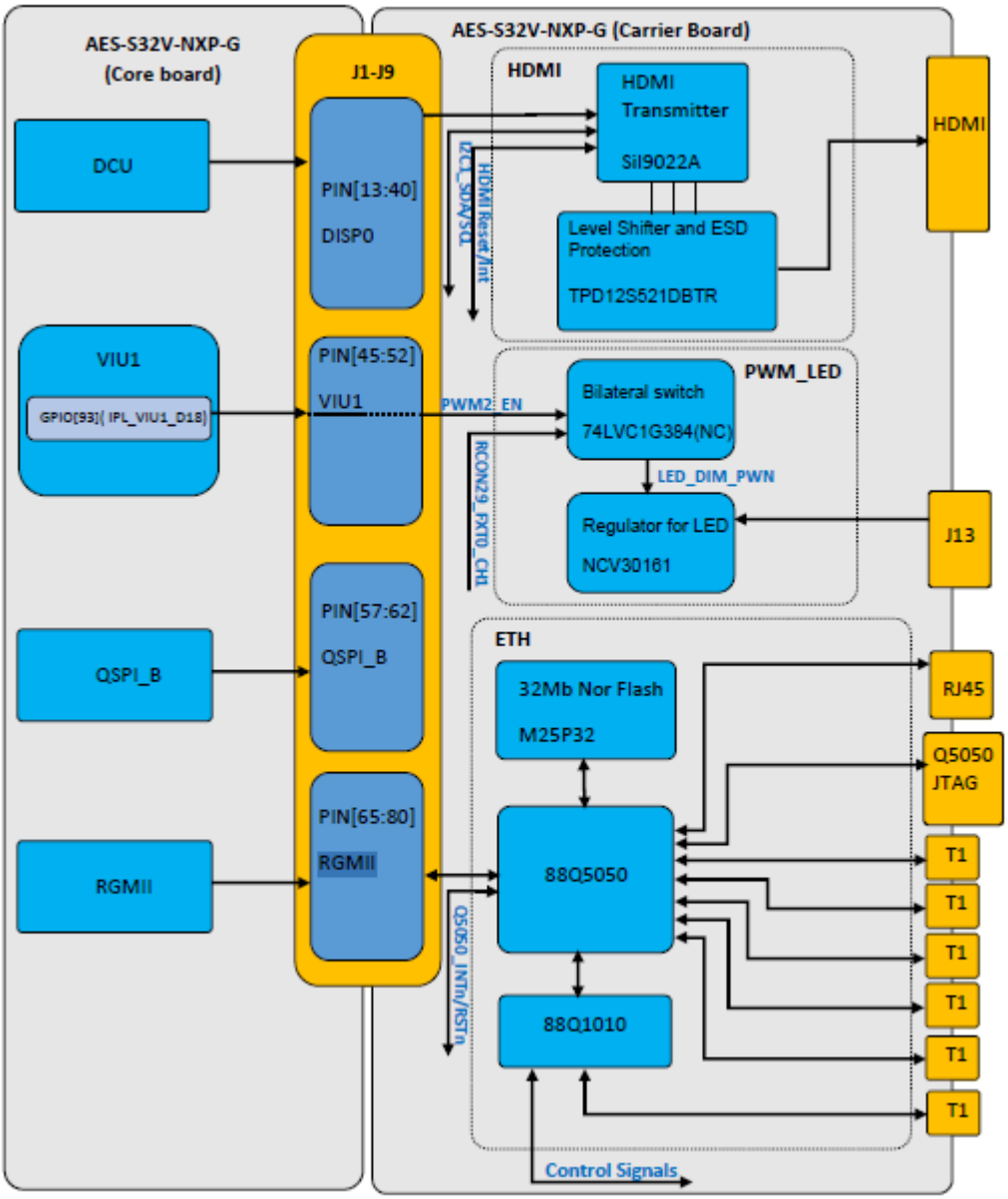


Figure 22 - AES-S32V-NXP-G (Core board) Signals to Avnet Carrier Board via J9

***J10* Connector (80-pin IMSA-9827S-80ZXX-GF)**

- CAN pins (CAN_FD0_RXD/RXD, CAN_FD1_RXD/TXD)
- System LED pin (SYS_LED)
- Debug Uart pins (RCON3_UART0_TXD, RCON4_UART0_RXD)
- Test points (MCU_RESET, RESET_B)
- MIPI-CSI0 pins (CSI0_DATA[0:3]_N/P, CSI0_CLK_N/P)
- HDMI control pins (HDMI_PWR_EN, HDMI_RESET, HDMI_CHIP_INT)
- CCD power control pin (CCD_PWR_EN)
- VIU0 pins (IPL_VIU_D[12:23], IPL_VIU0_VSYNC, IPL_VIU0_HSYNC, IPL_VIU0_PCLK)

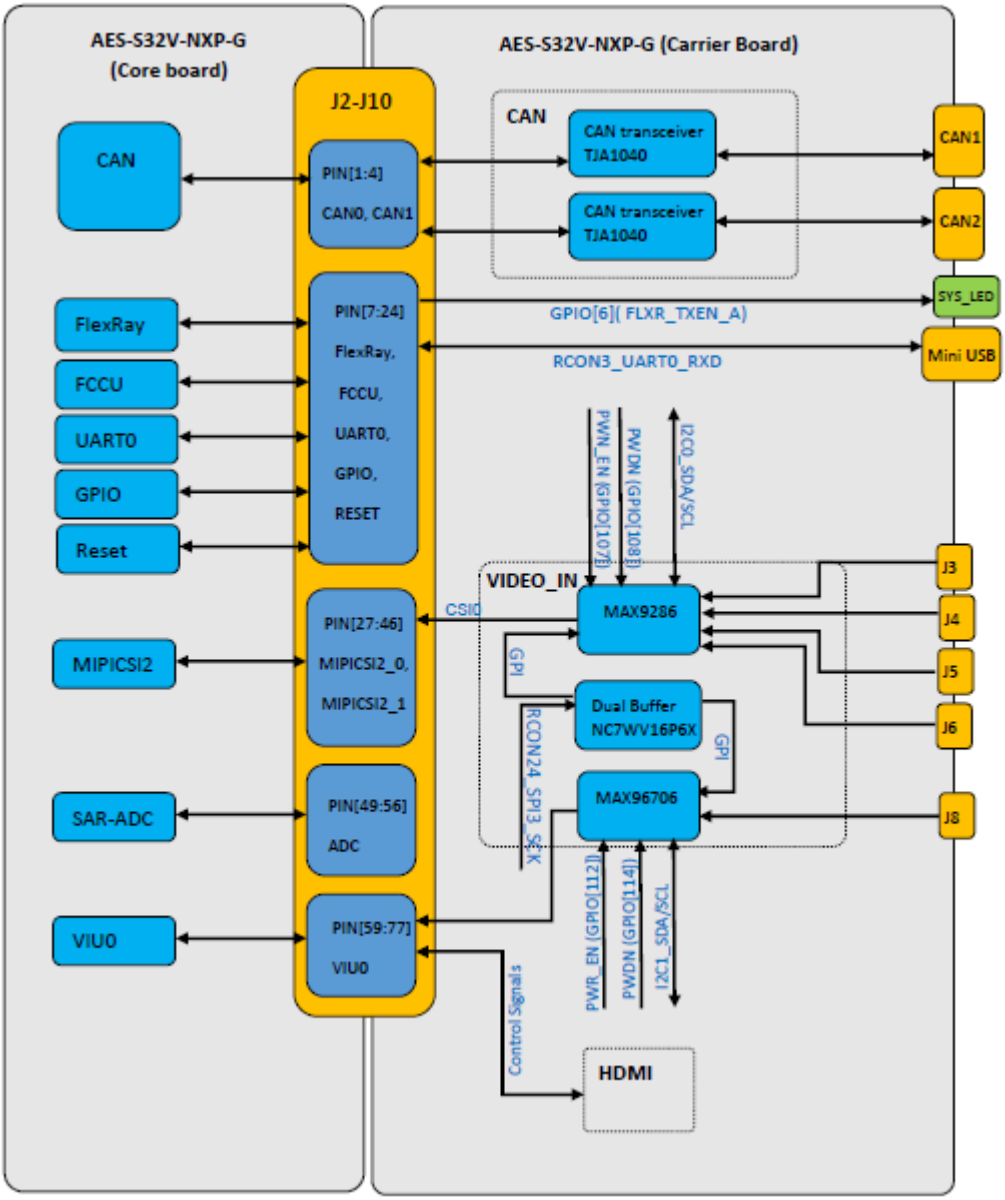


Figure 23 - AES-S32V-NXP-G (Core board) Signals to Avnet Carrier Board via J10

J11 Connector (80-pin IMSA-9827S-80ZXX-GF)

- PCIE pins (PCIE_RX_P/N, PCIE_TX_P/N, PCIE_CK1_P/N, PCIE_CK2_P/N, PCIE_PWR_ON, PCIE_CLKREQ, PCIE_WAKEn, PCIE_RESET)
- I2C pins (I2C0_SCL, I2C0_SDA, I2C1_SCL, I2C1_SDA)
- SPI pins (SPI0/1_SW, SPI0/1_CS0, SPI0/1_SCK, SPI0/1_SIN, SPI0/1_OUT)
- MAX9286/MAX96706 control pins (MAX9286_PWR_EN, MAX9286_PWDN, MAX96706_PWR_EN, MAX96706_PWDN, RCON24_SPI3_SCK)
- UART1 pins (UART1_EN, RCON5_UART1_RXD, RCON6_UART1_TXD)
- PHY control pins (PHY_INTn, PHY_WAKE_IN, PHY_RSTn)

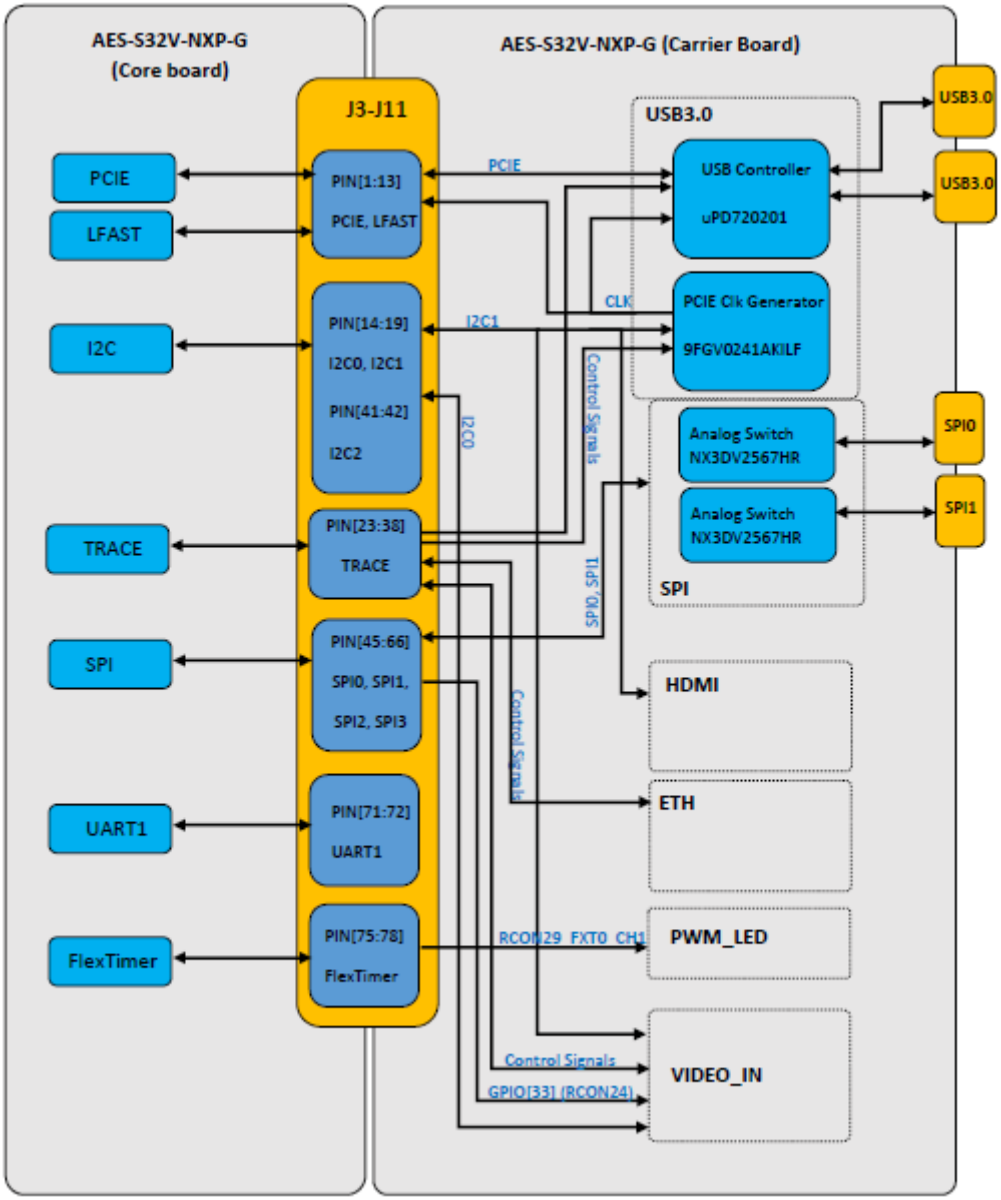


Figure 24 - AES-S32V-NXP-G (Core board) Signals to Avnet Carrier Board via J11

5. AES-S32V-NXP-G PCB Layout Notes

The PCB layout of AES-S32V-NXP-G (Core board) and Carrier board is designed with following rules:

- PCIE - For the two traces in a differential pair equal lengths to 10 mil, ground impedance is 85 Ω
- MIPI_CSI – Five groups of differential pair, equal lengths for the two traces in a differential pair, ground impedance is 100 Ω
- RGMII – Two groups of differential pair, RX and TX, equal lengths to 10 mil for the two traces in a differential pair
- SD Port - Equal lengths to 10 mil for the two traces in a differential pair, ground impedance is 50 Ω

- DISP - Equal lengths to 10 mil for the two traces in a differential pair

5.1. S32v234 DDR3L PCB Layout

The DDR interface is one of the most critical interfaces for chip routing. S32V adopts Fly_by Square.Impedance has to be controlled for the single ended traces to equal to 50 Ω and for the differential pairs to equal to 100 Ω. The following figure shows the physical connection scheme for both top and bottom placement of the DDR chips, showing the final placement of the DDR memory and the decoupling capacitors. The two channels of the data line are equal in length.

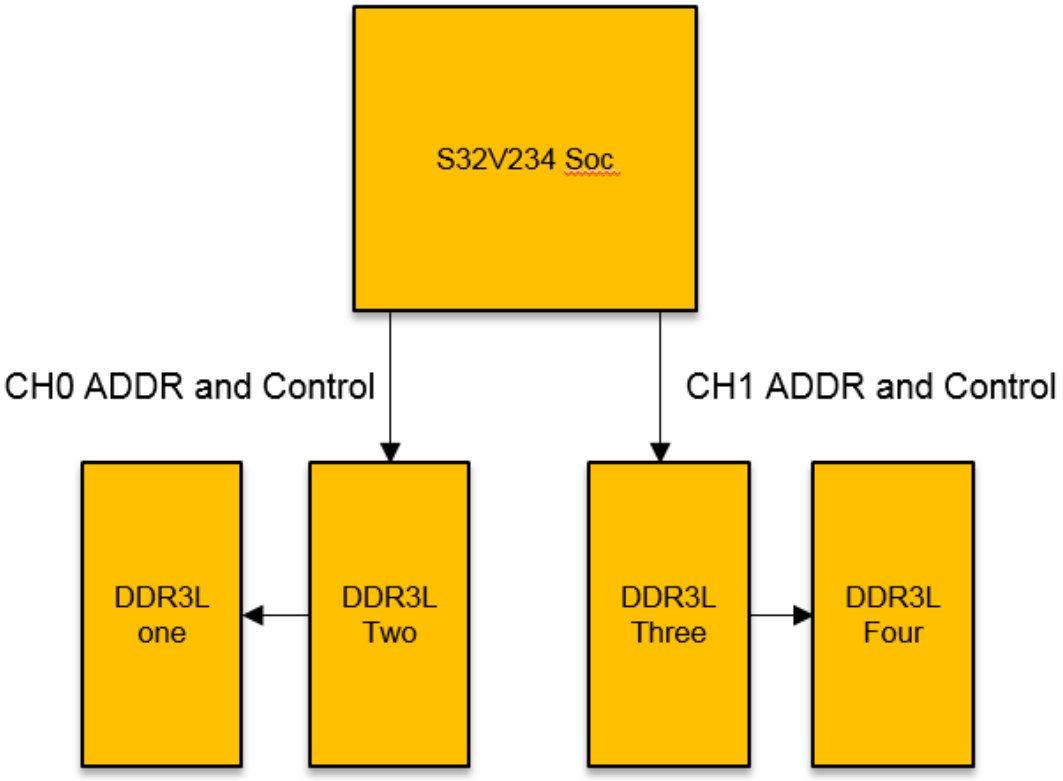


Figure 25 - AES-S32V-NXP-G DDR3L Control Diagram

6. Getting Help and Support

If additional support is required, Avnet has many avenues to search depending on your needs.For general question regarding AES-S32V-NXP-G (Core board) and Carrier Card or accessories, please visit our website athttp://to-be-referenced . Here you can find documentation, technical specifications, videos and tutorials, reference designs and other support.

Detailed questions regarding S32v234-EVK hardware design, software application development, using NXP tools, training and other topics can be posted on the S32v234-EV Support Forums at http://to-be-referenced. Avnet's technical support team monitors the forum during normal business hours.

Those interested in customer-specific options on S32v234-EVK can send inquiries to http://to-be-referenced@avnet.com.

7. Avnet AES-S32V-NXP-G (Core board) Schematics

The Avnet AES-S32V-NXP-G (Core board) schematics are located on the documentation page. You can locate that here: http://to-be-referenced

8. Avnet AES-S32V-NXP-G (Carrier board) Schematics

The Avnet AES-S32V-NXP-G (Carrier board) schematics are located on the documentation page. You can locate that here: http://to-be-referenced

9. Release Note

Version	Release date	Author	Note
Rev-1.0	03-May-2019	Air.Xu	First version
Rev-1.1	20-Sept-2019	Air.Xu	Changed part number