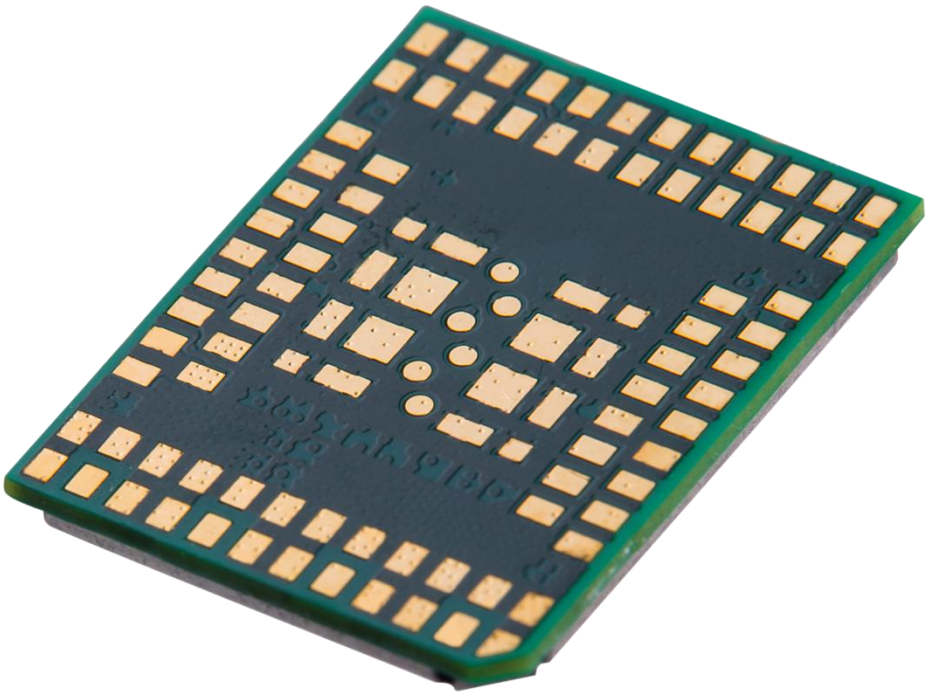

Product Technical Specifications & Design Guide

Project Name: IMA2A
Author: Wistron NeWeb Corporation
Revision: 1.1
Revision Date: 2018/11/10

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Technical Support Website	https://supportiot.wnc.com.tw/
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Revision History

Rev. #	Author	Summary of Changes	Date
0.1	WNC	Draft release	2018/1/15
0.2	WNC	Change 2.2 LGA Module Pin Definitions 87 pin name and description	2018/2/2
0.3	WNC	2.2 LGA Module Pin Definitions add Notes 4/5 Add Table3-4 ADC characteristics	2018/4/13
0.4	WNC	Update power consumption	2018/5/7
0.5	WNC	1.Update RF supported bandwidth 2.Update antenna design requirement 3.Update power consumption of PSM	2018/7/2
1.0	WNC	1.Add MSL level 2.Update Stencils design comments and Stencil-foil drawing 3. Update USIM interface	2018/9/3
1.1	WNC	1.Update power consumption 2.Delete GPS option 3.Update LTE Sensitivity data 4.Update packing information 5.Update IC ID	2018/11/10

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Contents

1. Introduction

The WNC IMA2A module includes the Altair ALT1250 Cat. M1 baseband, a complete LTE RF front-end, memory, and required circuitry to fulfill 3GPP E-UTRA and AT&T Wireless LTE Cat. M1 UE specifications. The following table enumerates the frequencies supported by the IMA2A module.

Band	Uplink (MHz)	Downlink (MHz)
LTE Band 2	1,850–1,910	1,930–1,990
LTE Band 4	1,710–1,755	2,110–2,155
LTE Band 12	699–716	729–746

Table 1-1. Band support

1.1 General Features

The table below summarizes the IMA2A module features.

General interfaces	• JTAG
	• USIM
	• GPIO
	• UART
Supported frequency bands	• LTE Band 2
	• LTE Band 4
	• LTE Band 12
Operating voltage	• V_{CC} (range: 3.3 V–4.2 V)
Packaging	• LGA module
	• 104 pads (19.2 mm × 14.7 mm × 2.152 mm)
	• RoHS compliant

Table 1-2. General features of the IMA2A

Standards compliance	• 3GPP Release 13–compliant; software upgradable to Release 14
PHY	• Category M1: Up to 300 Kbps DL/375 Kbps UL
	• HD-FDD duplexing support
	• Power-saving mode

MAC	• Random access procedure in normal subframes
	• Scheduling request, buffer status reporting, and power headroom reporting
	• Discontinuous reception (eDRX) with long and short cycles
	• IPv4, IPv6
NAS and above	• NAS
	• SMS over SG

Table 1-3. LTE-related features of the IMA2A

1.2 Architecture

The architecture block diagram of the IMA2A is presented in Figure 1-1 below.

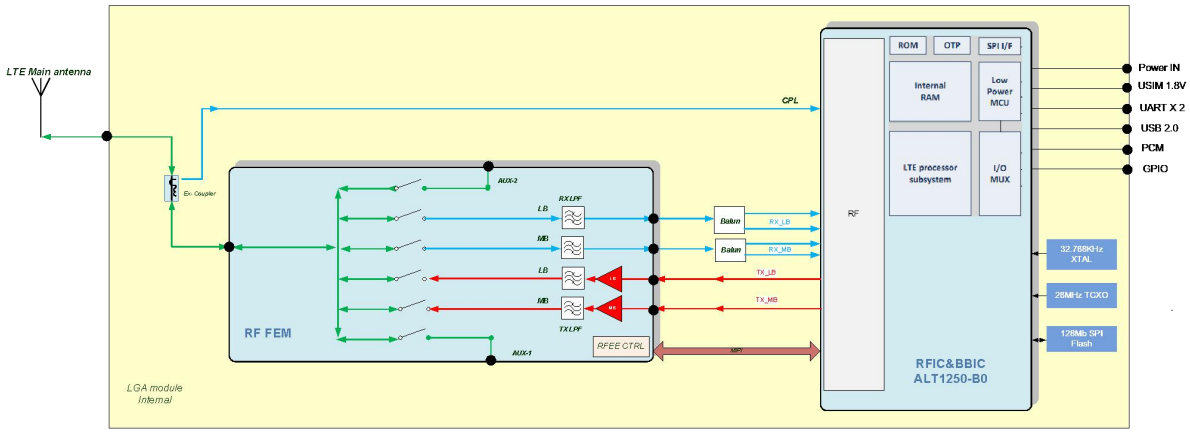


Figure 1-1. IMA2A block diagram

1.3 Connection Interface

The IMA2A module is a LGA device. All electrical and mechanical connections are made through the 104 pads on the bottom side of the PCB.

1.4 Environmental Specifications and Certifications

1.4.1 Environmental Specifications

The environmental specifications for both operating and storage conditions are defined in the table below.

Condition	Temperature Range	Remark
Normal ambient operating temp. range	–20 °C to 60 °C	Fully functional and complies with 3GPP specifications
Extended ambient operating temp. range	–40 °C to 85°C	RF performance may be affected outside normal ambient operating range temp., although the module will still function.
Storage	–40 °C to 85 °C	

Table 1-4. Temperature range

1.4.2 Certifications

The IMA2A module is compliant with the following regulations: PTCRB, FCC and AT&T TA.

1.4.3 Green Product Compliance

RoHS (2011/65/EU)

2. Pin Definitions

2.1 LGA Module Pin Diagram

The IMA2A LGA module pin layout is illustrated below.

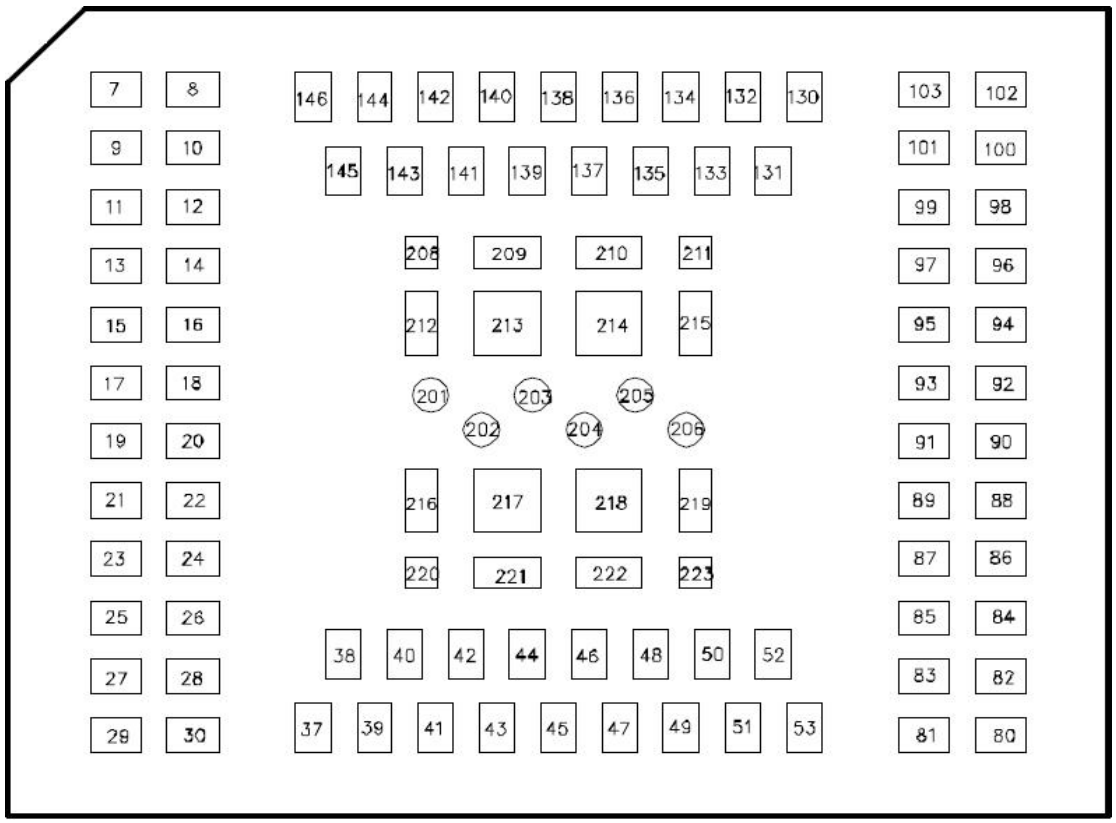


Figure 2-1. IMA2A LGA module pin layout (top view)

2.2 LGA Module Pin Definitions

The signals and all the related details are listed in the below table.

Pin No.	Name	Description
7	GND	GND
8	GND	GND
9	RF_GNSS	Not used
10	GND	GND
11	GND	GND
12	GND	Ground
13	GND	Ground

14	GND	Ground
15	Main antenna	Main antenna port
16	GND	Ground
17	GND	Ground
18	GND	Ground
19	GND	Ground
20	GND	Ground
21	NC	Not connected
22	GND	Ground
23	GND	Ground
24	GND	Ground
25	GND	Ground
26	GND	Ground
27	NC	Not connected
28	GND	Ground
29	GND	Ground
30	GND	Ground
37	Power	Power
38	Power	Power
39	Power	Power
40	Power	Power
41	Power	Power
42	Power	Power
43	PMU_VBACKUP	Power input for real time clock
44	GND	Ground
45	GND	Ground
46	PCM_FS/GPIO46	PCM/General purpose input/output
47	PCM_IN/GPIO47	PCM/General purpose input/output
48	PCM_OUT/GPIO48	PCM/General purpose input/output
49	PCM_CLK/GPIO49	PCM/General purpose input/output
50	GND	Ground
51	GND	Ground
52	I2C1_SCL/GPIO01	I2C/General purpose input/output
53	I2C1_SDA/GPIO02	I2C/General purpose input/output
80	PMU_AT_IN	Anti-tamper input
81	PMU_AT_OUT	Anti-tamper output
82	PMU_EXT_ALARM	Alarm output
83	DEBUG_SEL	Hardware pin for EJTAG chain selection

84	GND	Ground
85	GND	Ground
86	USB_Dp	USB data positive
87	VBUS	USB 3.3V input voltage supply
88	USB_Dn	USB data negative
89	GND	Ground
90	GND	Ground
91	GND	Ground
92	UART0_CTS	Clear to send for UART 0
93	UART0_TX	Transmit for UART 0
94	UART2_TX	Transmit for UART 2
95	UART0_RX	Receive for UART 0
96	UART2_RX	Receive for UART 2
97	UART0_RTS	Request to send for UART 0
98	UART2_RTS	Request to send for UART 2
99	UART2_CTS	Clear to send for UART 2
100	GPIO100	General purpose input/output
101	GNSS_EN	Not used
102	GPIO102	General purpose input/output
103	GPIO103	General purpose input/output
130	ADC1	Analog-to-digital converter
131	ADC2	Analog-to-digital converter
132	GPIO08	General purpose input/output
133	UIM_VCC	SIM card power
134	UIM DATA	SIM card data line
135	UIM CLK	SIM card clock line
136	UIM RESET	SIM card reset line
137	UIM DETECT	SIM card detect line
138	NC	Not connected
139	GND	Ground
140	GND	Ground
141	WWAN_STATE	Wireless WAN radio state
142	Power on[1]	Power-on of the module (RFU)
143	WAKEUP_OUT	Module wake-up of the host
144	WAKEUP_IN[2]	Host wake-up of the module
145	RESET	Hardware reset signal
146	VREF[3]	Reference logic voltage (1.8 V voltage)
201	EJ_TCK	EJ_TCK
202	EJ_TDI	EJ_TDI

203	EJ_TDO	EJ_TDO
204	EJ_TMS	EJ_TMS
205	EJ_TRST	EJ_TRST
206	DEBUG_RSTN	Reset pin for the JTAG probe
208	GND	Ground
209	GND	Ground
210	GND	Ground
211	GND	Ground
212	GND	Ground
213	GND	Ground
214	GND	Ground
215	GND	Ground
216	GND	Ground
217	GND	Ground
218	GND	Ground
219	GND	Ground
220	GND	Ground
221	GND	Ground
222	GND	Ground
223	GND	Ground

Table 2-1. IMA2A module pin definitions

Notes:

1: Leave pin 142 floating; the module can be turned on automatically when a power supply exists.

2: Pin 144 can be used as a wake-up as the module enters deep-sleep status. The default configuration is active high to wake up the LGA module.

3: The VREF voltage will turn off when entering the deep sleep state.

4:UART signal is better to retain in low state before the ALT1250 voltage is ready.

5:145 pin EXT_RST_N should use external 1.8V for pull up voltage

3. Electrical Specifications

3.1 Power Supply

The IMA2A module is supplied through the power signal with the following characteristics.

	Direction	Minimum	Typical	Maximum
Power (37–42)	In	3.3 V	3.8 V	4.2 V
VREF	Out	1.71 V	1.8 V	1.89 V
SIM_VCC (1.8 V)	Out	1.71 V	1.8 V	1.89 V

Table 3-1. Power supply

3.2 Power Consumption

This section describes the typical power consumption of the IMA2A (for reference).

Powering on	**Conditions**	**Result**
Peak power consumption		
	Max transient current consumption when the module runs at the maximum power.	720mA
Power off	**Conditions**	**Result**
Power off consumption		
	Only the module; no other devices; only RTC functions in deep sleep.	1.7μA
Working Mode	**Conditions**	**Result**
LTE Band 2 working mode		
	Max Tx power without throughput, power voltage 3.8 V; average current, CMW500 eMTC mode.	239.4mA
LTE Band 4 working mode		
	Max Tx power without throughput, power voltage 3.8 V; average current, CMW500 eMTC mode.	255.2mA
LTE Band 12 working mode		
	Max Tx power without throughput, power voltage 3.8 V; average current, CMW500 eMTC mode.	259.7mA

Low power Mode	Conditions	Result
Idle mode		
	LTE Standby, 1.28s	3.7mA
	LTE Standby, 2.56s	2.69mA
e-DRX mode		
	e-DRX cycle =81.92s,DRX=1.28s,PTW=1.28s	0.114mA
PSM mode		
	T3412-Extended=24H,T3324=10s One PSM cycle per day.	0.0041mA
Rock bottom current		
	Only the module; no other devices; only RTC functions in deep sleep.	1.7 µA

Note： The power consumption is under optimizing.

Table 3-2. LTE power consumption

3.3 Control Interfaces

This section describes the power on/off, wake-up, and reset interface for controlling the module.

3.3.1 Power-On Signal

This function is not available in the present firmware; the module will be turned on automatically when the power supply exists. Set this pin as “floating” or use 0 Ω as a reserve.

3.3.2 Wake-Up Interface

In applications where power consumption is a major factor in performance metrics (such as battery-operated sensors that are based on IOT/M2M modem solutions and also include a third-party host), it is necessary to define a simple interface that will enable the modem or the host to independently enter low power states whenever possible and the other respective modem or host side to wake it up once required.

For example, if the host has no data to transmit or any other tasks to perform, it may enter some low power state according to its own capabilities and configurations. If during that period the host is in a low power state and the modem then receives data, it must wake-up the host.

A similar converse requirement exists. For example, if the modem is in a low power

state and the host then must transmit data, it must be able to wake-up the modem.

The interface consists of two signals: One is driven by the host and received by the modem; the other is driven by the modem and received by the host.

Each side can wake the other by toggling a wakeup signal high and allowing the other to enter sleep mode when not required by toggling it low.

- "WAKEUP_IN" (Host: Output; Modem: Input):
  - LOW: The SoC does not require the Modem (allowing it to sleep).
  - HIGH: The SoC requires the Modem or acknowledges it is ready following a wakeup request from the Modem.
- "WAKEUP_OUT" (Host: Input; Modem: Output):
  - LOW: The Modem does not require the Host (allowing it to sleep).
  - HIGH: The Modem requires the Host or acknowledges it is ready following a wakeup request from the SoC.

Note: WAKEUP_OUT function will be updated in the future.

3.3.3 Reset Signal

The Reset Signal is a hardware reset signal to control the system reset directly. You can connect it to a key or a control signal. Reserve a 100k resistor to pull up to VREF and maintain a sufficient physical distance between the reset signal trace and noise and radiating signals on the PCB.

3.3.4 WWAN state

Note:WWAN_STATE function will be updated in the future.

3.4 UART Interface

There are two UART interfaces: a 4-bit for high-speed data transfer, and the UARTs. Definitions of the IMA2A are listed below.

1. UART0 for PPP and AT

2. UART2 for firmware download, recovery mode, and firmware debug view

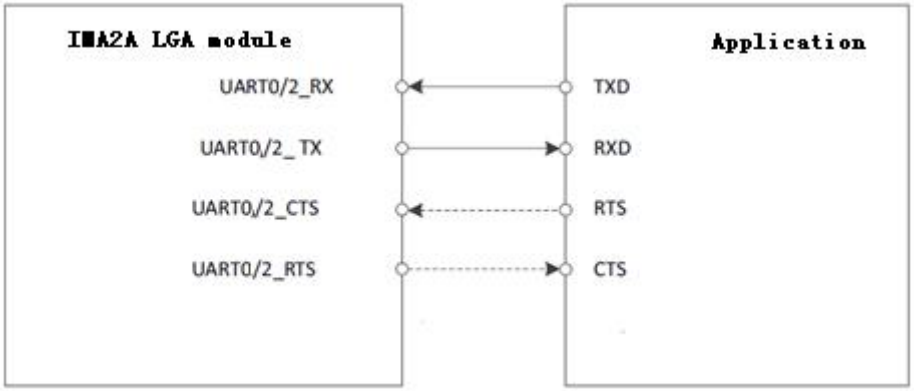


Figure 3-1. UART connection (example)

3.5 UIM Interface

IMA2A modules provide a UIM_DETECT input pin for UIM connectors to detect a UIM card. When a UIM card is present, UIM_DETECT should be high (1.8 V). If a UIM card is absent, UIM_DETECT should be low. Pulling UIM_DETECT to VREF with a 100k resistor is necessary. We recommend placing a 0.1 µF and a 33 pF capacitor between UIM_VCC and the Ground in parallel. We also recommend placing a 33 pF capacitor between UIM_RESET, UIM_CLK, and UIM_DATA and the Ground in parallel. Refer to Figure 5 for details.

We also recommend placing an electrostatic discharge (ESD) protection circuit near the UIM socket as close as possible. The Ground pin of the ESD protection component must be well-connected to the Ground plane.

The following figure shows an example of a UIM card circuit. The default configuration is active High.

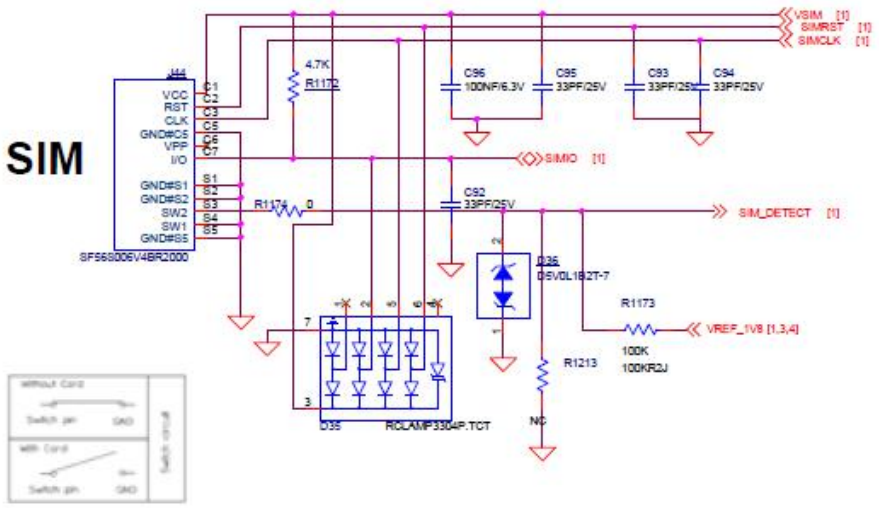


Figure 3-2. UIM card circuit example

It's highly suggested to make sure that SIM electrical characteristics can meet ETSI TS 102 221 requirement before going to certification like PTCRB. Refer to the following capture from ETSI TS 102 221 section 5 for critical requirement:

5.3 Class C operating conditions

5.3.1 Supply voltage Vcc (contact C1)

The terminal shall operate the UICC within the following limits.

Table 5.9: Electrical characteristics of Vcc under normal operating conditions

Symbol	Minimum	Maximum	Unit
Vcc	1,62	1,98	V

5.3.2 Reset (RST) (contact C2)

The terminal shall operate the UICC within the following limits.

Table 5.10: Electrical characteristics of RESET (RST) under normal operating conditions

Symbol	Conditions	Minimum	Maximum	Unit
V_{OH}	I_{OHmax} = +20 µA	0,8 x Vcc	Vcc (see note)	V
V_{OL}	I_{OLmax} = -200 µA	0 (see note)	0,2 x Vcc	V
t_R t_F	C_{in} = C_{out} = 30 pF		400	µs
NOTE: To allow for overshoot the voltage on RST should remain between -0,3 V and Vcc + 0,3 V during dynamic operations.				

5.3.3 Clock CLK (contact C3)

Table 5.11: Electrical characteristics of Clock (CLK) under normal operating conditions

Symbol	Conditions	Minimum	Maximum	Unit
V_{OH}	I_{OHmax} = +20 µA	0,7 x Vcc	Vcc (see note)	V
V_{OL}	I_{OLmax} = -20 µA	0 (see note)	0,2 x Vcc	V
t_R t_F	C_{in} = C_{out} = 30 pF		50	ns
NOTE: To allow for overshoot the voltage on CLK should remain between -0,3 V and Vcc + 0,3 V during dynamic operations.				

5.3.4 I/O (contact C7)

Table 5.12 defines the electrical characteristics of the I/O (contact C7). The values given in the table allow the derivation of the values of the pull-up resistor in the terminal and the impedance of the drivers and receivers in the terminal and UICC.

Table 5.12: Electrical characteristics of I/O under normal operating conditions

Symbol	Conditions	Minimum	Maximum	Unit
V_{IH}	I_{IHmax} = ±20 µA (see note 2)	0,7 x Vcc	Vcc + 0,3	V
V_{IL}	I_{ILmax} = +1 mA	-0,3	0,2 x Vcc	V
V_{OH} (see note 1)	I_{OHmax} = +20 µA	0,7 x Vcc	Vcc (see note 3)	V
V_{OL}	I_{OLmax} = -1mA	0 (see note 3)	0,3	V
t_R t_F	C_{in} = C_{out} = 30 pF		1	µs
			100 (see note 4)	ns
NOTE 1: It is assumed that a pull-up resistor is used on the interface device (recommended value: 20 kΩ). NOTE 2: During static conditions (idle state) only the positive value can apply. Under dynamic operating conditions (transmissions) short-term voltage spikes on the I/O line may cause a current reversal. NOTE 3: To allow for overshoot the voltage on I/O shall remain between -0,3 V and Vcc + 0,3 V during dynamic operation. NOTE 4: This value applies when the low impedance buffer is selected.				

3.6 I/O Characteristics

The voltage and current characteristics of the various IO pads of the IMA2A versus IO bank supply voltage are illustrated in the tables below.

Parameter	Drive Strength	Min.	Nom.	Max.	Unit
VIL Input Low Voltage				0.3 × VIO	V
VIH Input High Voltage		0.7 × VIO			V
VOL Output Low Voltage				0.2 × VIO	V
VOH Output High Voltage		0.8 × VIO			

VH Input Hysteresis		0.1 × VIO			V
IRATED IO Drive Strength	2 mA			12	mA

Table 3-3. DC characteristics for digital IOs, voltage 1.8 V—BIDIR and IN types

3.6 EJTAG Interface

The IMA2A provides one EJTAG interface; leave JTAG pins floating if not used.

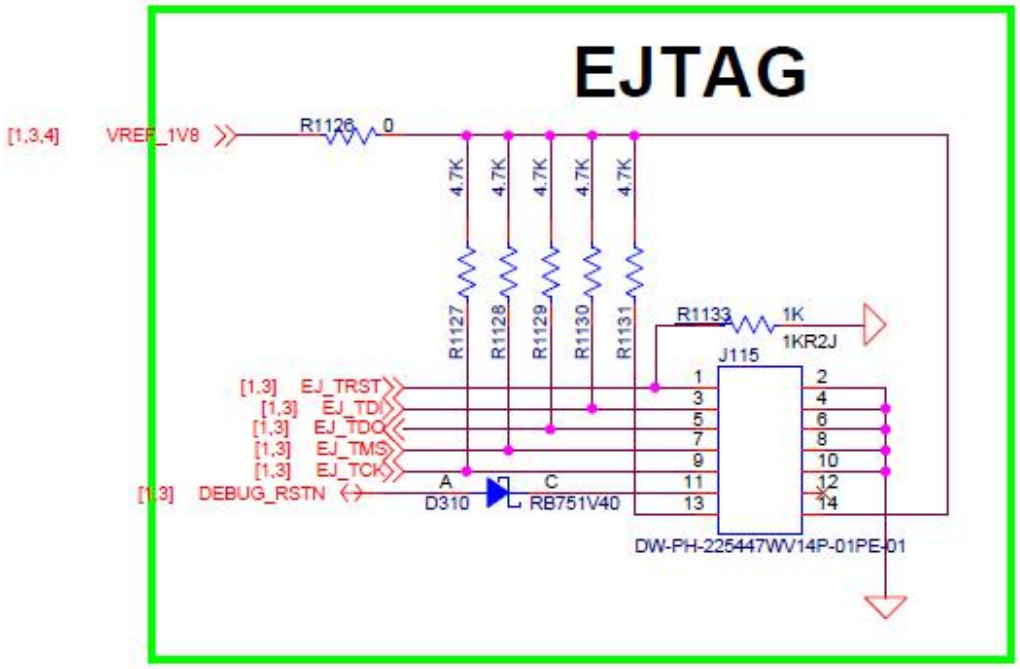


Figure 3-3. EJTAG schematic (example)

3.7 ADC Interface

The IMA2A contains two ADC ports; the characteristics will be updated according to the ALT1250 datasheet in the future.

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution	6		12	Bits
FCLK	Clock rate	4	40	52	MHz
FS	Conversion rate per channel(1)		Fc /(N+3)	0.2 × VIO	MSPS
VIN	Input voltage range		1.8		V

Symbol	Parameter	Min.	Typ.	Max.	Unit
INL	Integral Nonlinearity		±1	±2	LSB
DNL	Differential Nonlinearity	-0.9		0.9	LSB
SINAD	Signal to Noise and Distortion ratio(2)		64.5		dB
OE	Offset error		±1	±2	%Fs
GE	Gain error		±1	±2	%Fs
RIN	Input resistance			0.5	KΩ
CIN	Input capacitance during sampling		2.6		pF

Table 3-4. ADC characteristics

(1) The general formula for this conversion rate is: FS=FCLK/(N+3)/Number of sources.
(2) Conversion rate at 3.46 MSPS and 12bit resolution

3.8 RF Interface

Each IMA2A module has only one RF pad; developers must connect it via the 50 Ω traces to the main board.

Main antenna pad (Pin15) – RX/TX path

3. 8.1 Bandwidth Support

Band	Bandwidth					
	1.4 MHz	3 MHz	5 MHz	10 MHz	15 MHz	20 MHz
LTE Band 2	✓	✓	✓	✓	✓	✓
LTE Band 4	✓	✓	✓	✓	✓	✓
LTE Band 12	✓	✓	✓	✓	-	-

Table 3-5. Bandwidth support

3. 8.2 RF Transmission Specifications

Band	Item	Parameter	Unit	Min.	Typ.	Max.

LTE Band 2	Max. TX Power	20 MHz 1 RBs/QPSK	dBm	20.3	23	25.7
LTE Band 4	Max. TX Power	20 MHz 1 RBs/QPSK	dBm	20.3	23	25.7
LTE Band 12	Max. TX Power	10 MHz 1 RBs/QPSK	dBm	20.3	23	25.7

Table 3-6. Conductive Tx output power

Notes: 1.The RF transmission specification is defined at the LGA pad.
2. Complies with 3GPP test standards.Power class is 3.

3. 8.3 RF Receiver Specifications

Band	Item	Parameter	Unit	Min.	Typ.	Max.
LTE Band 2	RX Sensitivity	5 MHz with 4 RBs	dBm		-104.5	–100.3
LTE Band 4	RX Sensitivity	5 MHz with 4 RBs	dBm		-104	–102.3
LTE Band 12	RX Sensitivity	5 MHz with 4 RBs	dBm		-106	–99.3

Table 3-7. Conductive Rx sensitivity—3GPP

Notes: 1. The RF receiver specification is defined at the LGA pad.
2. Compliant with 3GPP test standards

4. Mechanical Information

4.1 Physical Dimensions

Physical dimensions are illustrated in Figure 4-1 and Figure 4-2 below.

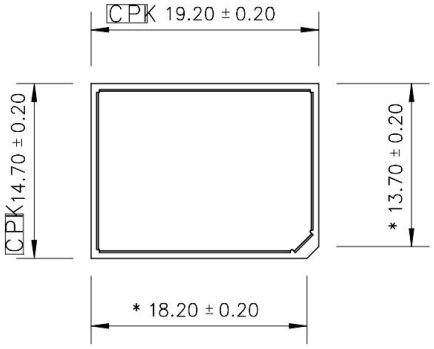


Figure 4-1. Top view

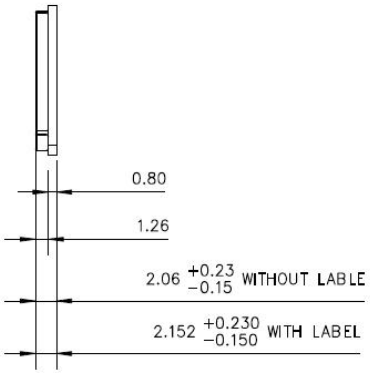


Figure 4-2. Right view

4.2 Pin Dimensions

Pin dimensions are illustrated in Figure 4-3, Figure 4-4, and Figure 4-5 below.

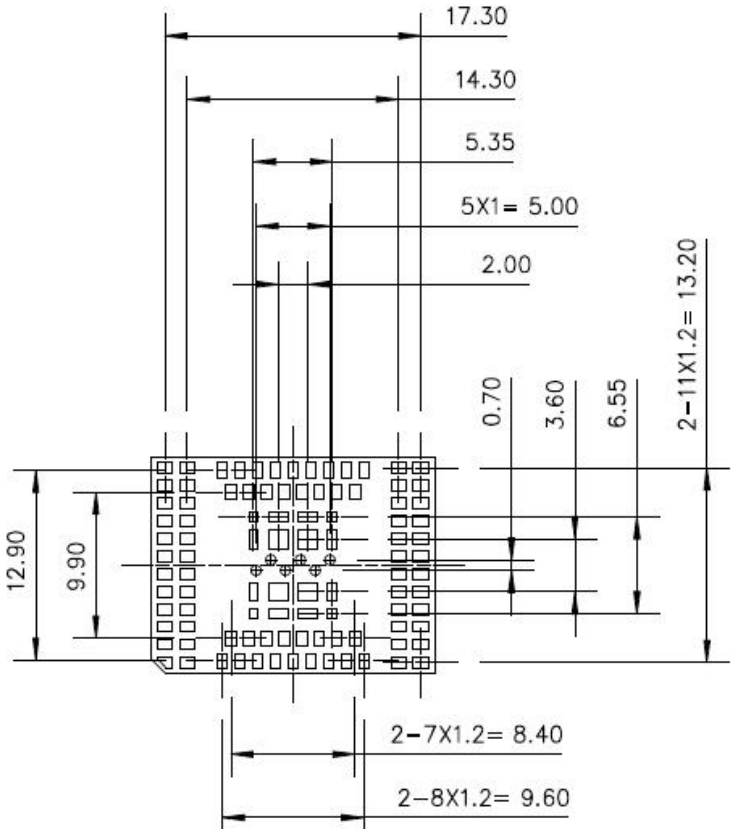
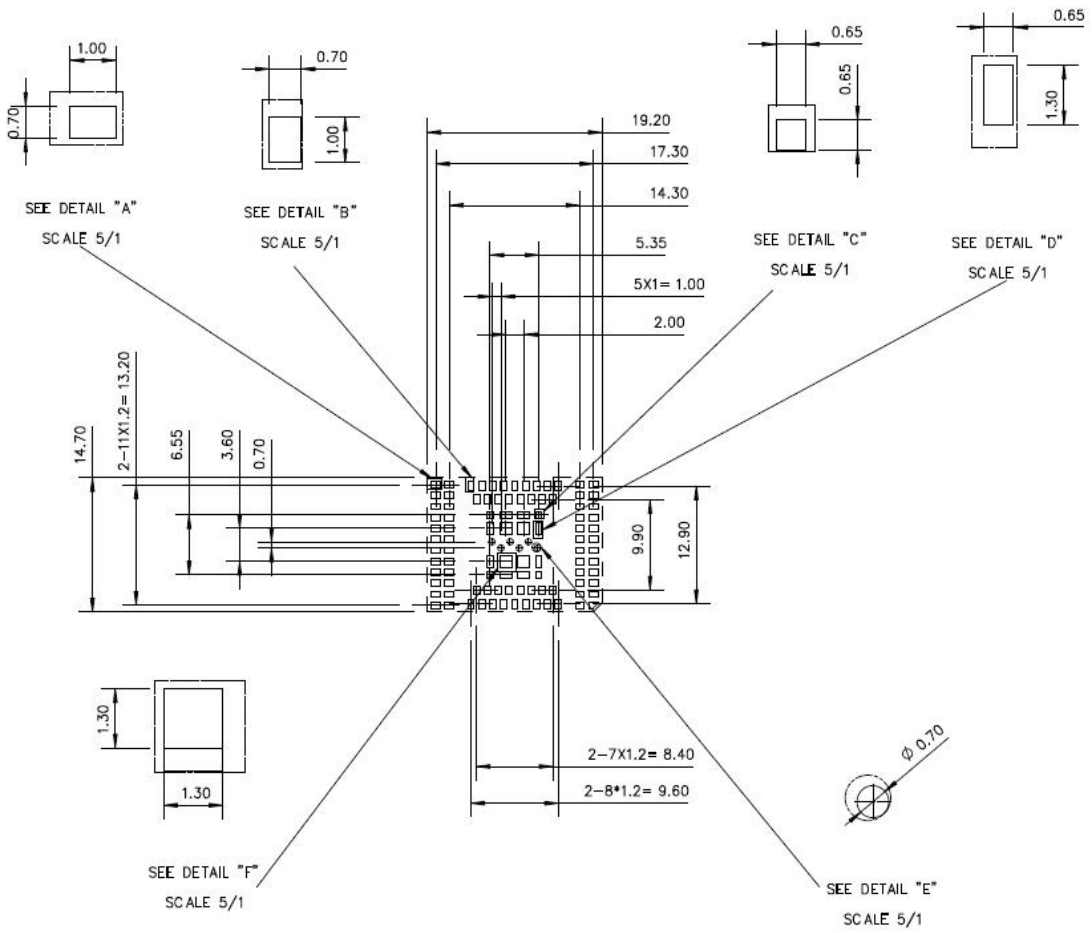


Figure 4-3. PIN dimensions (bottom view)



SUGGESTION PCB FOOTPRINT

Figure 4-4. Pin dimensions

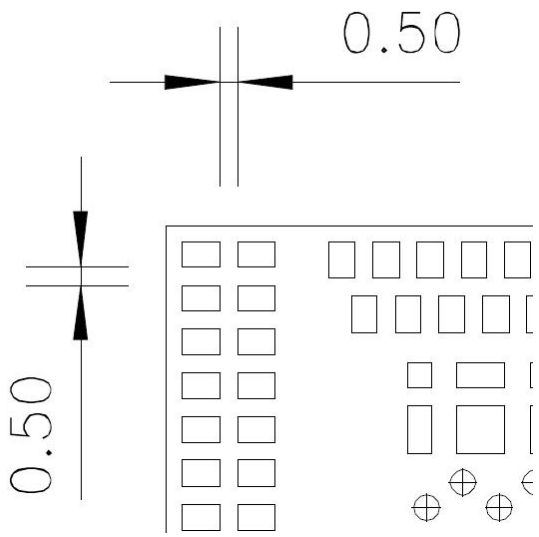


Figure 4-5. Pin dimensions

4.3 Marking Information

The IMA2A module label is illustrated below.

P/N: Variable; for the specific customer

S/N: Variable; unique for each module

IMEI: Variable; unique for each module

FCC: NKRIMA2A

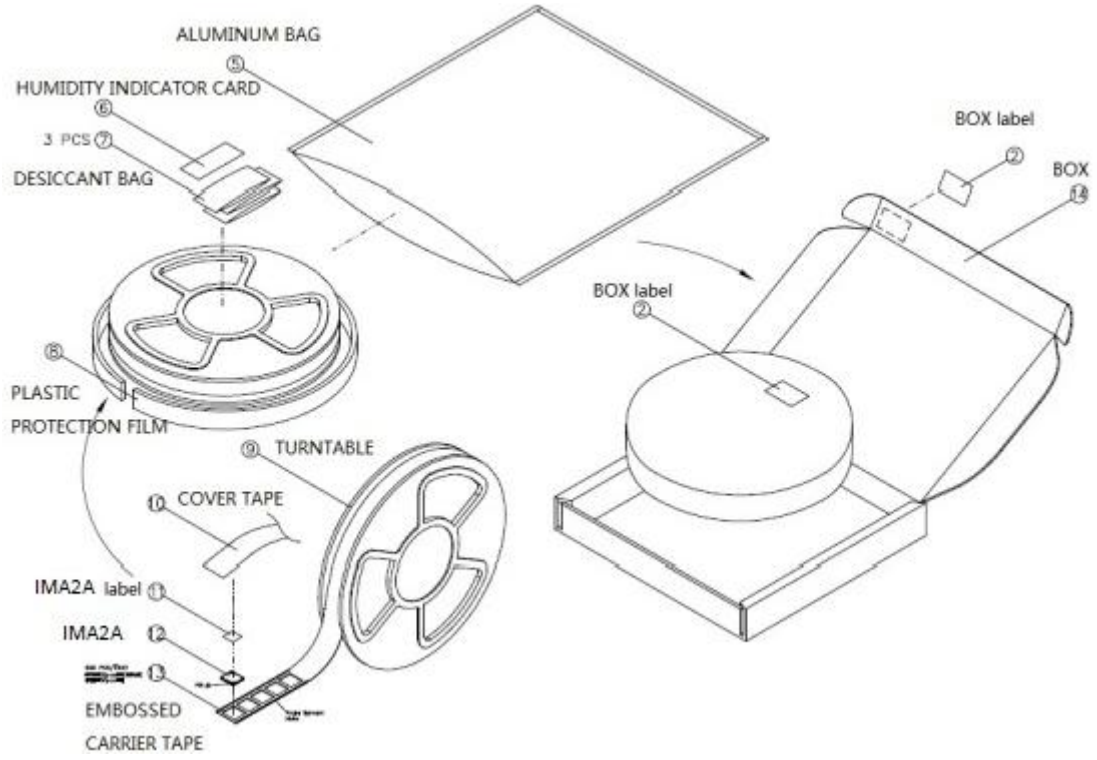
IC: 4441A-IMA2A

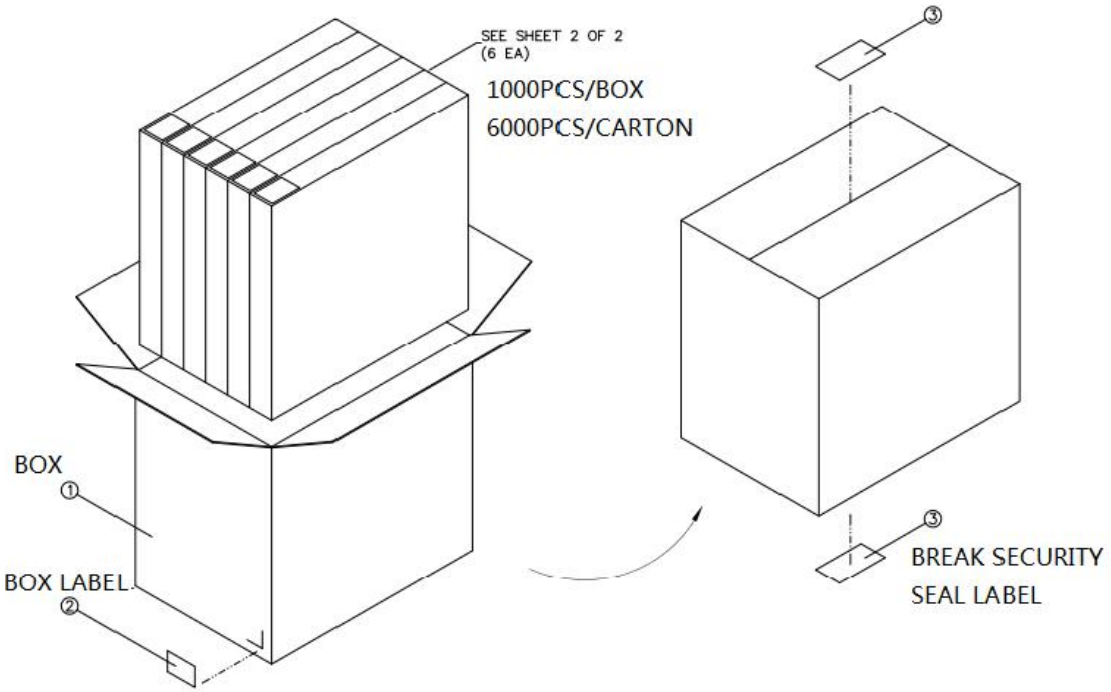
If customers request their own S/Ns and IMEIs, they should inform WNC before production. The S/N and IMEI only can be written once onto each unit.

5. Packing Information

5.1 Tape-and-Reel Package

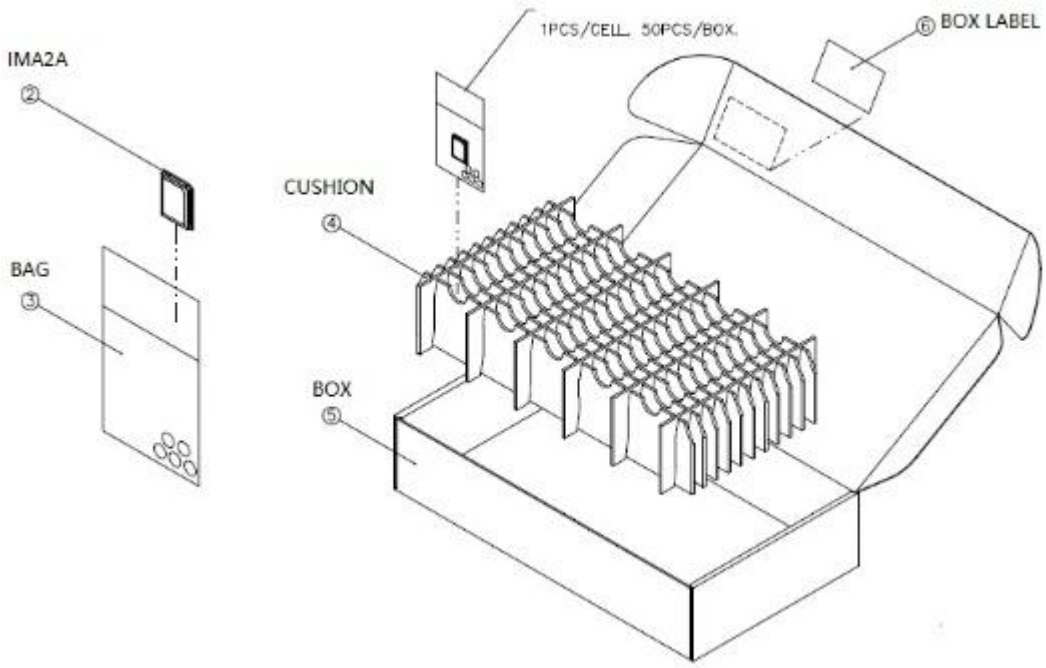
The module is delivered in tape-and-reel packaging based on MPQ (1000 pcs./reel; 6 reels/carton).





5.2 Single Packaging for Samples

Samples are packaged at 50 pcs./box. There is no vacuum packaging. Samples must be baked for 8 hours at least at 85 °C before SMT.



5.3 MSL level

The IMA2A module MSL level is 3.

6. Design Guide

6.1 Power Trace Design

Power trace layout suggestion: At least 22 µF, 0.1 µF, and 100 pF capacitors are required; place the capacitors as close to the power pins as possible. Power trace should possess sufficient line width to withstand its respective current listed in the table below.

Net Name	Peak Current Value for PCB Power Trace Design
Power (37–42) total	1 A
VREF	50 mA
UIM_VCC	30 mA

Table 6-1. Reference current for power trace

Please select the DCDC that can satisfy the output (1 A) as the power supply of the module.

6.2 RF Pad Design

We recommend that a ground not be present under the surface of the RF pads in the layout. Details are included below. Layer 2 has the same exclusion area as Layer 1.

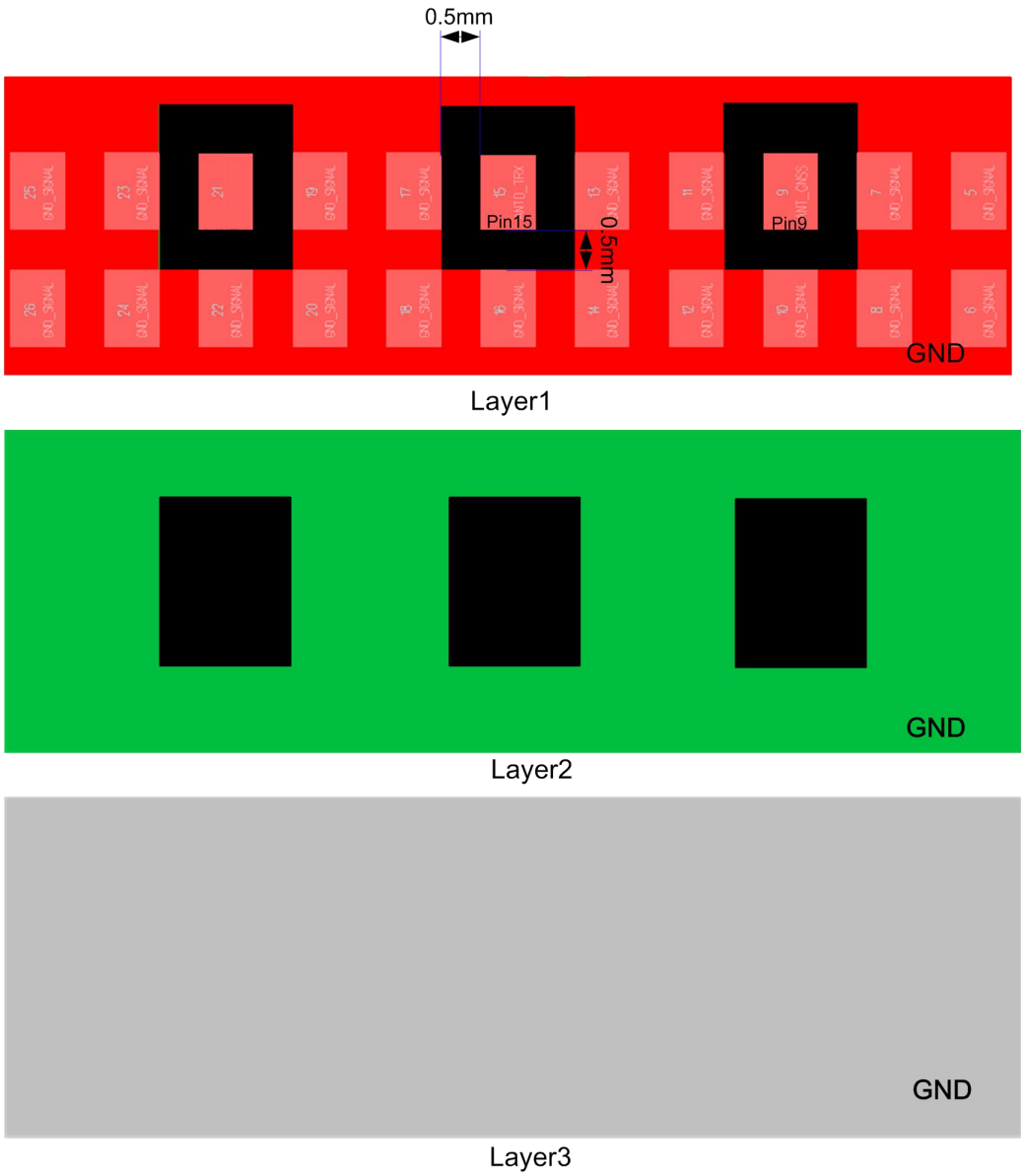


Figure 6-1. Sample RF pad layout

6.3 RF Matching Guide

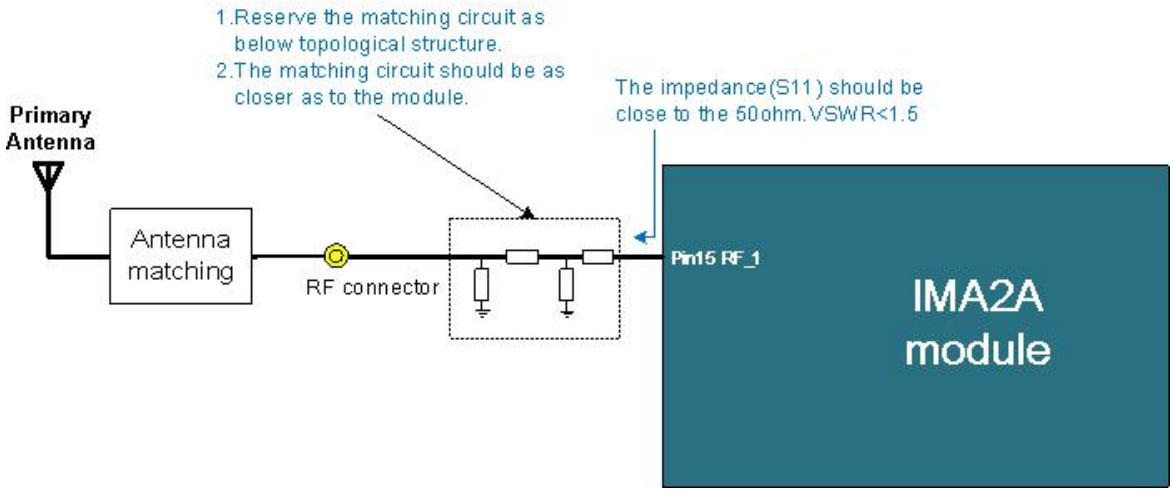


Figure 6-2. RF matching guide

6.4 Interference and Sensitivity

This section includes tips to help developers identify interferences that may affect the IMA2A module when used in systems.

- Interference from other wireless devices
  - We highly recommend checking the RX performance of entire systems within the shielding environment.
  - Good isolation (ex.: Wi-Fi antenna, GPS antenna) is required between the other wireless system antenna and the IMA2A module LTE antenna.
- Interference from the host interface
  - High-speed signal-switching elements in systems can easily couple noise into the module (ex.: DDR memory, LCD modules, DC-to-DC converters, PCM signals).

- Methods to avoid sources of interference
  - Antenna location is important; we recommend directing the antenna away from high-speed switching signals. Furthermore, the trace from the module to the antenna should be as short as possible and must be shielded by complete grounding.
  - The IMA2A module is well shielded; high-speed elements (Ex.: DDR memory, LCD modules, DC-to-DC converters, PCM signals) on a system should have shielding reserved during the early stages of development.

6.5 Antenna design requirement

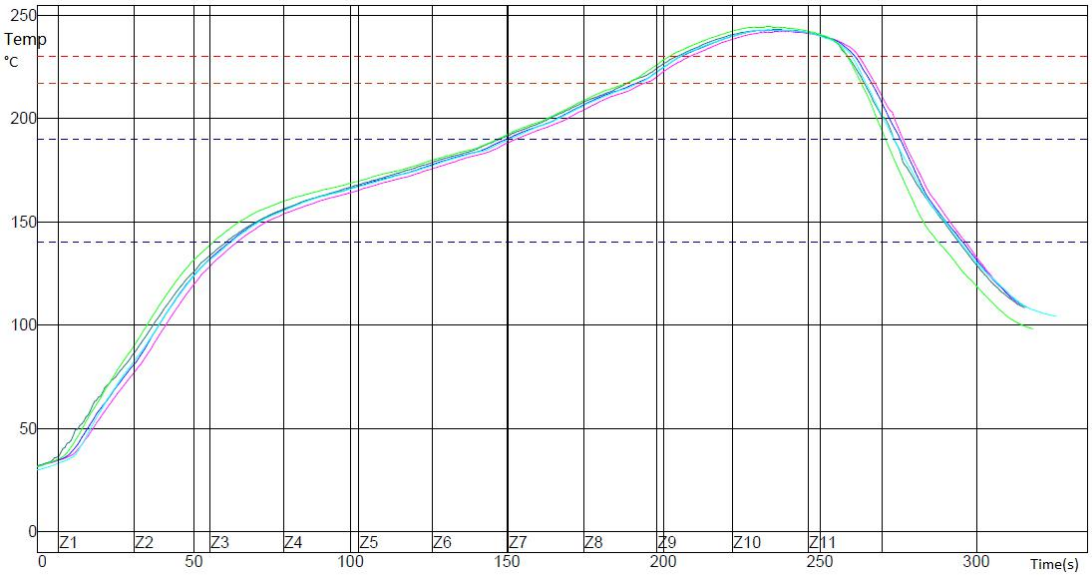
The antennas shall must meet below specification:

ANTENNA REQUIREMENTS for IMA2A	
Frequency range	LTE band II(1900) : 1850MHz-1910MHz, 1930MHz-1990MHz
	LTE Band IV(1700) : 1710MHz-1755MHz, 1710MHz-1755MHz
	LTE Band XII(700) : 699MHz-716 MHz, 729 MHz-746 MHz
Bandwidth	LTE band II(1900) : 60 MHz
	LTE Band IV(1700) : 45 MHz
	LTE Band XII(700) : 17 MHz
Polarization	Linear
Radiation pattern	Omni-directional
Impedance	50 ohm
Input power	> 24dBm Average power in LTE
Efficiency recommended	>40% (below 960MHz) >50% (over 1710MHz)
VSWR absolute max	≤ 3:1
VSWR absolute recommended	≤ 2:1
Antenna ruggedness(Output RF load mismatch ruggedness at ANT pins)	10:1 (max) VSWR

6.6 Mounting Considerations

This section details the recommended reflow profile when the module is mounted onto other boards.

Temp. Region	1	2	3	4	5	6	7	8	9	10	11
Upper temp. region	160	175	175	175	180	180	215	230	250	255	240
Lower temp. region	160	175	175	175	180	180	215	230	250	255	240
Conveyer band speed	90 cm/minute										



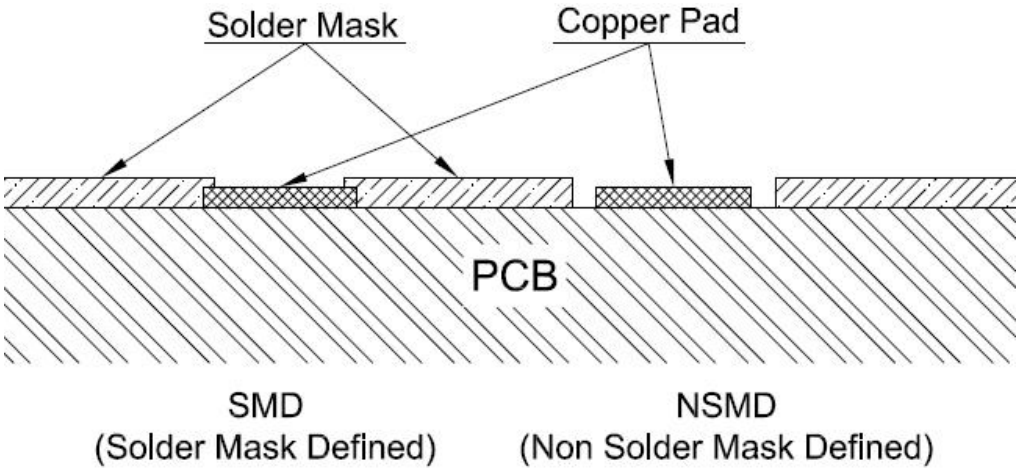
PWI = 91%	U13-1	U13-4	J45-2	U29-2	J44-3	Temp. Difference
Preheat from 140–190°C						
	89.22	88.45	87.27	89.00	90.95	3.68
	10%	5%	–1%	9%	20%	
Melt-out Time/230°C						
	54.12	55.80	54.72	55.01	56.98	2.86
	41%	58%	47%	50%	70%	
Max Temp						
	242.12	242.73	243.00	242.88	244.45	2.33
	21%	27%	30%	29%	45%	
Total Time/217°C						
	73.89	75.48	75.89	72.9	75.31	2.99
	-44%	-38%	-36%	–48%	-39%	
Gradient1 (100–150°C)						
	1.85	1.88	1.84	1.9	1.93	0.09
	23%	25%	23%	27%	29%	

Process limit:

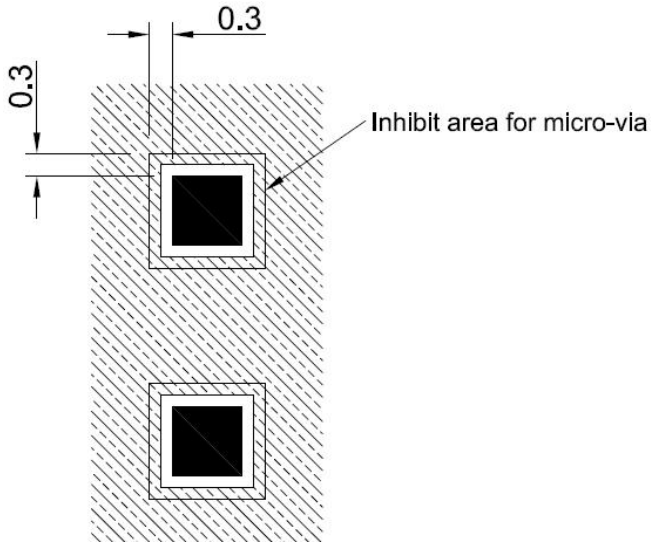
Solder Paste	Lead-free		
Profile feature	Min.	Max.	Unit
Gradient1 (Target = 1.5) (100 °C–150 °C) (Time period = 20 s)	0	3	°C/S
Preheat time from 140 °C to 190 °C	70	105	S
Time maintained above 230 °C	40	60	S
Peak package body temperature	230	250	°C
Time maintained above 217 °C	60	110	S

6.7 PCB Pad Design

We recommend a non-solder mask with defined (NSMD) type for the solder pads of the PCB on which IMA2A modules will be mounted. This type of design enables high soldering reliability during the SMT process.



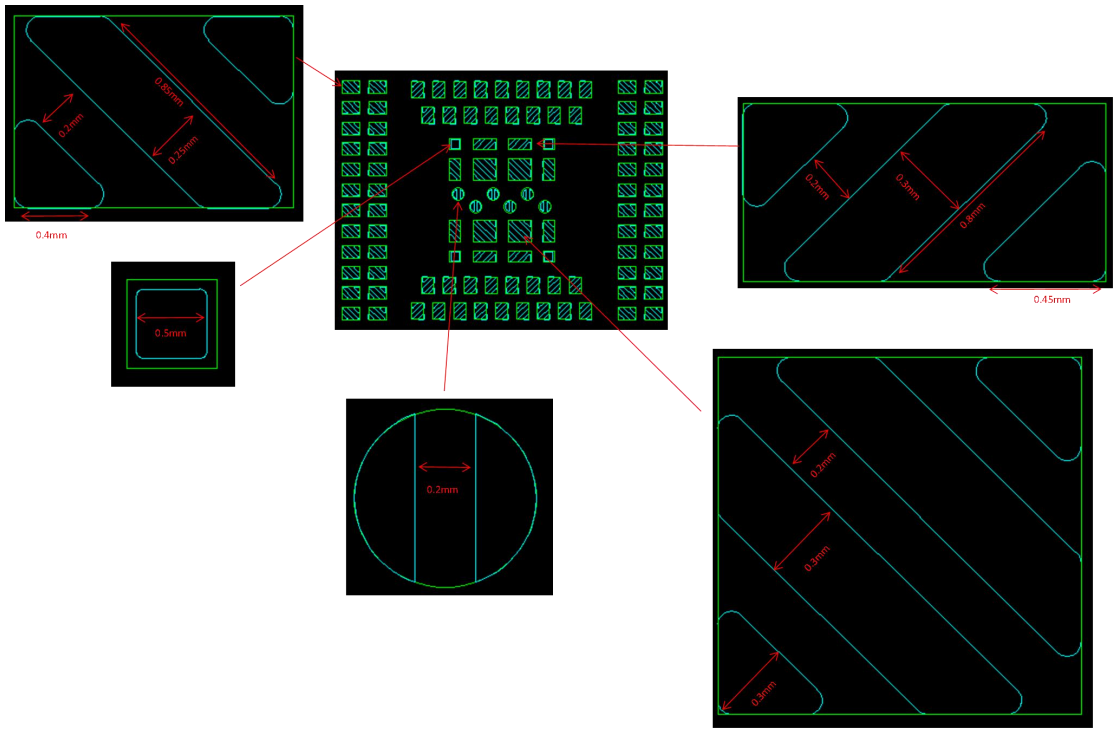
We recommend not placing via or micro-via that is not covered by solder resistance within 0.3 mm around the pads unless it carries the same signal of the pad itself. Refer to the following figure.



Only blind holes are allowed in the pad. Through holes are not allowed.

6.8 Stencils

0.15mm stencil-foil thickness is recommended to obtain the best performance to prevent voids during SMT reflow, 0.12mm is the minimum requirement if there is any restrictions.



Stencil-foil drawing

6.9 LTE Power Saving Mode

Note: Details will be provided in a future revision of this document.

7. Safety Recommendations

Be sure use of this product is allowed in the country and in the environment required. Use of this product may be dangerous and must be avoided in the following areas:

- Where it may interfere with other electronic devices in environments such as hospitals, airports, and aircraft
- Where there is a risk of explosion such as gasoline stations and oil refineries

The user is responsible for compliance with the legal and environmental regulations of their location of use.

Do not disassemble the product; any evidence of tampering will compromise the warranty's validity.

We recommend following the instructions of the hardware user guides for a correct wiring of the product. The product must be supplied with a stabilized voltage source, and the wiring must conform to relevant security and fire-prevention regulations.

This product must be handled with care; avoid any contact with the pins because electrostatic discharge may damage the product. Exercise the same level of caution regarding the UIM card; carefully check the instructions for its use. Do not insert or remove the UIM when the product is in power-saving mode.

The system integrator is responsible for the functioning of the final product; therefore, care must be taken for the external components of the module as well as for project or installation issues—there may be a risk of disturbing the GSM network or external devices or of impacting device security. If you have any questions, refer to the technical documentation and the relevant regulations in force.

Every module must be equipped with a proper antenna with specific characteristics. The antenna must be installed with care in order to avoid any interference with other electronic devices.

8. Initialisms

Initialisms and Definitions

Initialism	Definition
AC	Alternating current
DC	Direct current
ETSI	European Telecommunications Standards Institute
GND	Ground
GPIO	General purpose input output
I/O	Input/output
IoT	Internet of Things
I2C	Inter-integrated circuit
LGA	Land grid array
LTE	Long Term Evolution
N/A	Not/applicable
OS	Operating system
PIN	Personal identification number
SIM	Subscriber identity module
SPI	Serial peripheral interface
UART	Universal asynchronous receiver-transmitter
UIM	User identity module
USB	Universal serial bus
Vref	Voltage reference
RFU	Reserved for future use
WNC	Wistron NeWeb Corporation