Avnet Embedded Vision Multi-Sensor FMC

Hardware User Guide

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	0.9	11/27/17	Change GMSL connectors to stacked FAKRA
	0.10	04/30/18	Add I/O locs for strobe propagated pins Add details on IPMI EEPROM content
	0.11	06/06/18	Change GMSL connectors to Rosenberger High-Speed FAKRA Mini (HFM)
Comments:	Add comments as necessary.		

Contents

1. Introduction

The purpose of this manual is to describe the functionality and contents of the Avnet Embedded Vision Multi Sensor FMC Module. This document includes descriptions of the hardware features.

1.1 Description

The Avnet Embedded Vision Multi Sensor FMC Module is not a stand-alone module, but rather a plug-in module designed to interface with FMC compatible baseboards. In that role, the FMC adapter supports multiple cameras for Xilinx Zynq UltraScale+ embedded vision applications in automotive ADAS, augmented reality and UAV / drones.

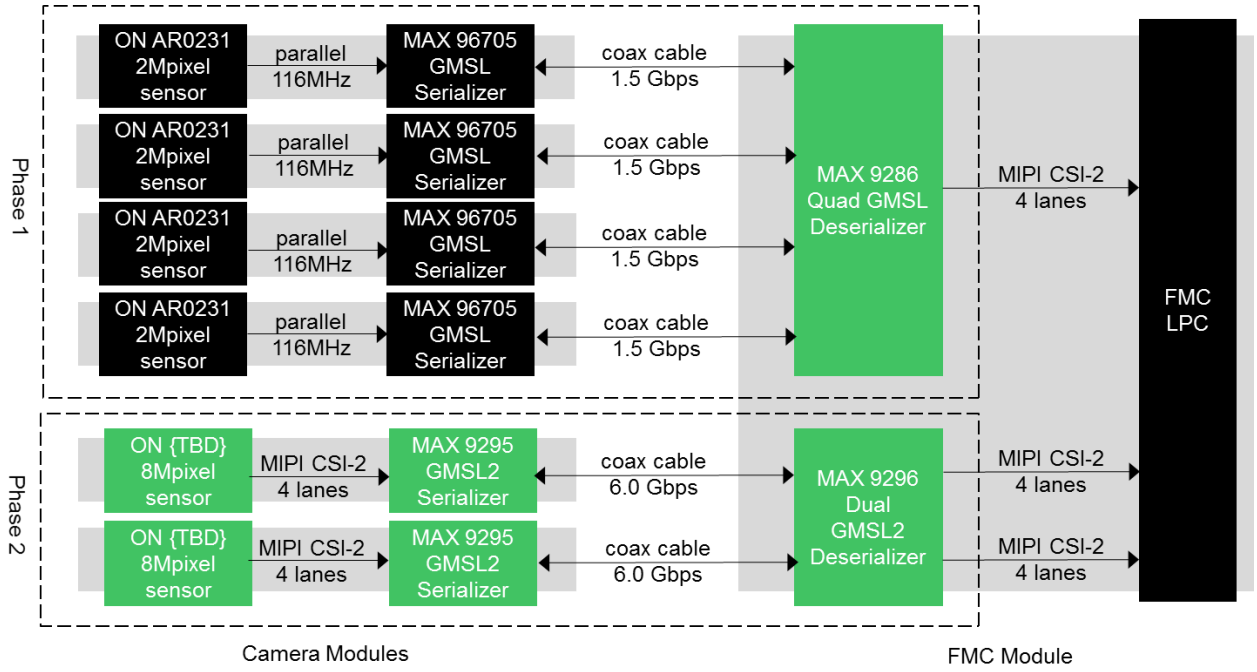


Figure 1 - Avnet Embedded Vision Multi Sensor FMC – System Diagram

As shown in the system diagram above, the FMC Module supports 6 Camera Modules connected remotely over 50Ω Coax (100Ω STP) Cables.

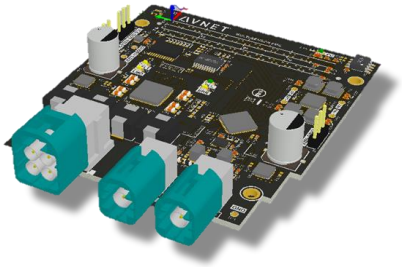
1.2 Ordering Information

The Multi-Camera FMC module will be available in two phases.

- Phase 1 - only the Quad GSML circuit will be available.
- Phase 2 – both Quad GMSL and Dual GMSL2 circuits will be available

In order to differentiate between the two versions, two part numbers are used:

Supplier	Part Number	Description	Resale
Avnet	AES-FMC-MULTICAM**4**-G	Multi-Camera FMC Module (Quad GMSL only)	$399
Avnet	AES-FMC-MULTICAM**6**-G	Multi-Camera FMC Module (Quad GMSL + Dual GMSL2)	TBD

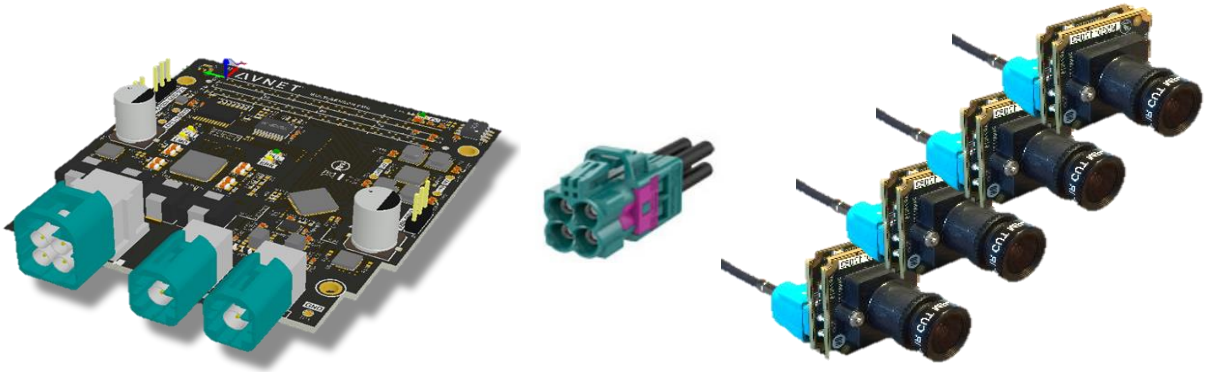


The following table lists the components required to create a complete Quad Camera FMC solution.

Supplier	Part Number	Description	Resale
Avnet	AES-FMC-MULTICAM4-G	Multi-Camera FMC Module (Quad GMSL only)	$399
Rosenberger	L02-026-1000-Z-ZZZZ_V2	Quad HFM to 4 FAKRA Cable Assembly	$69
ON Semiconductor	MARS1-MAX96705-GEVK	MAX96705 Serializer Kit	4 x $250
ON Semiconductor	MARS1-AR0231AT7-GEVB	AR0231AT Image Sensor Board	4 x $250
		TOTAL	**$2468**

Avnet will be providing the following bundle, with 30% discount over individual pricing.

Supplier	Part Number	Description	Resale
Avnet	AES-FMC-MC4-AR0231AT-G	Quad Camera FMC Bundle	**$1699**



1.3 References

ON Semiconductor MARS – Modular Automotive Reference System
http://www.onsemi.com/PowerSolutions/content.do?id=18780

ON Semiconductor MARS AR0231 Camera Board
http://www.onsemi.com/PowerSolutions/evalBoard.do?id=MARS1-AR0231AT6-GEVB

ON Semiconductor MARS MAX96705 Serializer Board
http://www.onsemi.com/PowerSolutions/evalBoard.do?id=MARS1-MAX96705-GEVB

ON Semiconductor AR0231AT
http://www.onsemi.com/PowerSolutions/product.do?id=AR0231AT

MAXIM MAX96705 Serializer
https://www.maximintegrated.com/en/products/interface/high-speed-signaling/MAX96705.html

MAXIM MAX9286 Quad GMSL Deserializer
https://www.maximintegrated.com/en/products/interface/high-speed-signaling/MAX9286.html

MAXIM MAX9295 GMSL2 Serializer
… advanced device …

MAXIM MAX9296 GMSL2 Deserializer
… advanced device …

Xilinx MIPI D-PHY v3.3 (PG202)
https://www.xilinx.com/support/documentation/ip_documentation/mipi_dphy/v3_1/pg202-mipi-dphy.pdf

Xilinx MIPI CSI-2 RX Sub-system v2.2 (PG232)
https://www.xilinx.com/support/documentation/ip_documentation/mipi_csi2_rx_subsystem/v2_2/pg232-mipi-csi2-rx.pdf

Xilinx package pinout References:
UZEV CC – https://www.xilinx.com/support/packagefiles/zuppackages/xczu7evfbvb900pkg.txt
ZCU102 – https://www.xilinx.com/support/packagefiles/zuppackages/xczu9egffvb1156pkg.txt
ZCU104 –

2. Block Diagram and Features

This section summarizes the features of the Avnet Embedded Vision Multi-Sensor FMC module, followed by functional descriptions.

2.1 Features

The Avnet Embedded Vision Multi Sensor FMC Module provides the following features:

- FMC LPC (Low Pin Count)
- Quad 2Mpixel Camera Module support, via
  - Quad GSML Deserializer – MAX9286
- Dual 8Mpixel Camera module support, via
  - Dual GSML2 Deserializer – MAX9296A
- FAKRA connectors, supporting:
  - low cost 50Ω Coax (100Ω STP) cables

2.2 Block Diagram

The following block diagram provides an overview of the major interfaces (all control signals omitted for clarify).

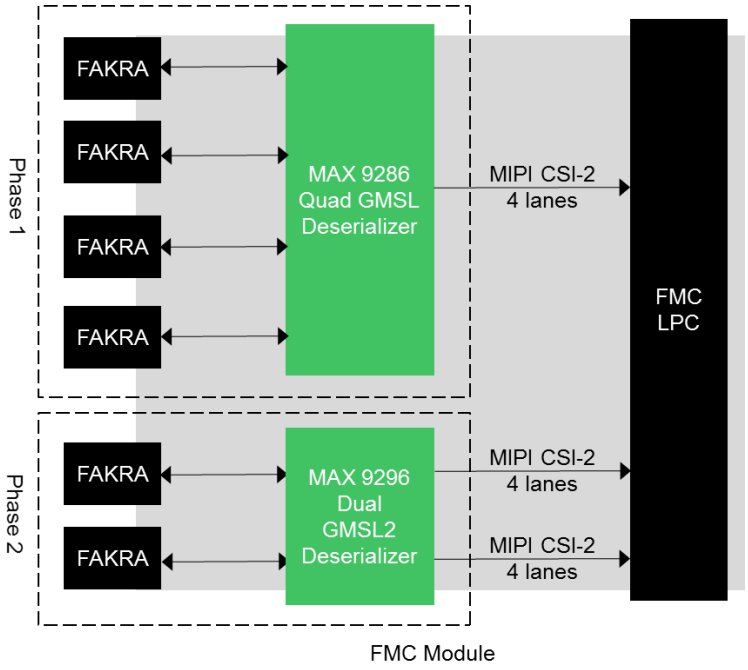


Figure 2 - Avnet Embedded Vision Multi Sensor FMC – Block Diagram

3. Functional Description

The following sections provide brief description of each feature provided on the Avnet Embedded Vision Multi-Sensor FMC module.

3.1 FMC LPC

The FMC LPC connector provides 68 single-ended I/O or 34 differential I/O as defined in the following table.

	H	G	D	C
1	VREF_A_M2C	GND	PG_C2M	GND
2	PRSNT_M2C_L	CLK1_M2C_P	GND	DP0_C2M_P
3	GND	CLK1_M2C_N	GND	DP0_C2M_N
4	CLK0_M2C_P	GND	GBTCLK0_M2C_P	GND
5	CLK0_M2C_N	GND	GBTCLK0_M2C_N	GND
6	GND	LA00_P_CC	GND	DP0_M2C_P
7	LA02_P	LA00_N_CC	GND	DP0_M2C_N
8	LA02_N	GND	LA01_P_CC	GND
9	GND	LA03_P	LA01_N_CC	GND
10	LA04_P	LA03_N	GND	LA06_P
11	LA04_N	GND	LA05_P	LA06_N
12	GND	LA08_P	LA05_N	GND
13	LA07_P	LA08_N	GND	GND
14	LA07_N	GND	LA09_P	LA10_P
15	GND	LA12_P	LA09_N	LA10_N
16	LA11_P	LA12_N	GND	GND
17	LA11_N	GND	LA13_P	GND
18	GND	LA16_P	LA13_N	LA14_P
19	LA15_P	LA16_N	GND	LA14_N
20	LA15_N	GND	LA17_P_CC	GND
21	GND	LA20_P	LA17_N_CC	GND
22	LA19_P	LA20_N	GND	LA18_P_CC
23	LA19_N	GND	LA23_P	LA18_N_CC
24	GND	LA22_P	LA23_N	GND
25	LA21_P	LA22_N	GND	GND
26	LA21_N	GND	LA26_P	LA27_P
27	GND	LA25_P	LA26_N	LA27_N
28	LA24_P	LA25_N	GND	GND
29	LA24_N	GND	TCK	GND
30	GND	LA29_P	TDI	SCL
31	LA28_P	LA29_N	TDO	SDA
32	LA28_N	GND	3P3VAUX	GND
33	GND	LA31_P	TMS	GND
34	LA30_P	LA31_N	TRST_L	GA0
35	LA30_N	GND	GA1	12P0V
36	GND	LA33_P	3P3V	GND
37	LA32_P	LA33_N	GND	12P0V
38	LA32_N	GND	3P3V	GND
39	GND	VADJ	GND	3P3V
40	VADJ	GND	3P3V	GND
	LPC Connector	LPC Connector	LPC Connector	LPC Connector

Table 1 – FMC LPC Connector Pinout

Note: For the FMC LPC, the connector columns K, J, F, E, B, and A are not used and not shown in the above table.

According to MIPI CSI-2 RX Sub-system documentation, the MIPI pin selection must respect the following requirements:

- RX CLK must be assigned to DBC / QBC / GC_QGC.
- Continuous IO pair to be used without leaving IO pairs.

Excerpt from documentation:

> The MIPI CSI-2 RX Subsystem provides an I/O planner feature for I/O selection. In the Pin Assignment tab, dedicated byte clocks (DBC) or quad byte clocks (QBC) are listed for the clock lane for the selected HP I/O bank. For the QBC clock lane, all of the I/O pins are listed for data lane I/O selection but for the DBC clock lane only the byte group I/O pins are listed for data lane I/O selection.
> Eight MIPI CSI-2 RX Subsystem IP cores can be implemented per IO bank based on BITSLICE and BITSLICE_CONTROL instances in the UltraScale+ devices.

IMPORTANT: If the RX data lane I/O pins are selected non-contiguously then an additional one, two, or three I/O pins (RX_BITSLICE) are automatically used for clock/Strobe propagation. Therefore, **it is recommended that you select adjacent I/O pins for the RX configuration to make efficient use of the I/O**. The propagation of strobes to the RX data pins follows the inter-byte and inter-nibble clocking rules given in the UltraScale Architecture SelectIO Resources User Guide (UG571).

According to the previously mentioned requirements, the following MIPI pin assignments have been found:

MIPI CSI-2 RX Interface	Signal	ZCU104 pin mapping (FMC LPC)		ZCU102 pin mapping (FMC HPC0)		ZCU102 pin mapping (FMC HPC1)		UZEV pin mapping (FMC HPC)	
1 MAX9686 Quad-GSML	**CLK**	**LA00**	F17,F16	**LA00**	Y4,Y3	**LA00**	G6,G7	**LA00**	AF16,AF17
	D0	**LA01**	H18,H17	**LA01**	AB4,AC4	**LA01**	AJ6,AJ5	**LA01**	AD17,AE17
	D1	**LA09**	H16,G16	**LA09**	W2,W1	**LA09**	AE2,AE1	**LA09**	AK17, AK18
	D2	**LA12**	G18,F18	**LA12**	W7,W6	**LA12**	AD7,AD6	**LA12**	AJ14,AK14
	D3	**LA13**	G15,F15	**LA13**	AB8,AC8	**LA13**	AG8,AH8	**LA13**	AJ15,AK15
	strobe prop.	-		*LA06 LA14*	*AC2,AC3 AC7,AC6*	*LA06 LA14*	*AH2,AJ2 AH7,AH6*	*LA10 LA16*	*AG16,AH16 AG13, AH13*
2 MAX9696 GSML2 A	**CLK**	**LA18**	D11,D10	**LA18**	N9,N8	**-**		**LA18**	AH6,AJ6
	D0	**LA23**	B11,A11	**LA23**	L16,K16	**-**		**LA23**	AJ5,AK5
	D1	**LA17**	F11,E10	**LA17**	P11,N11	**-**		**LA17**	AG6, AG5
	D2	**LA24**	B6,A6	**LA24**	L12,K12	**-**		**LA24**	AK7, AK6
	D3	**LA25**	C7,C6	**LA25**	M11,L11	**-**		**LA25**	AF6, AF5
	strobe prop.	*LA21*	*B10,A10*	*LA20*	*N13,M13*	-		-	
3 MAX9696 GMSL2 B	**CLK**	**LA31**	F7,E7	**LA31**	V8,V7	**-**		**-**	
	D0	**LA29**	K10,J10	**LA29**	U9,U8	-		-	
	D1	**LA30**	E9,D9	**LA30**	V6,U6	-		-	
	D2	**LA33**	C9,C8	**LA33**	V12,V11	-		-	
	D3	**LA32**	F8,E8	**LA32**	U11,T11	-		-	
	strobe prop.	*LA28*	*M13,L13*	*HPC1 LA29**	*W12,W11*	-		-	

Table 2 – MIPI CSI-2 RX pin mapping

The FMC pin allocation for the FMC-MULTICAM FMC Module is defined in the following table.

	H	G		D	C	
1	-	GND	1	PG_C2M	GND	1
2	PRSNT_M2C_L		2	GND	-	2
3	GND		3	GND	-	3
4		GND	4	-	GND	4
5		GND	5	-	GND	5
6	GND	MAX9286_CLK_P	6	GND	-	6
7	I2C_MUX_SCL	MAX9286_CLK_N	7	GND	-	7
8	I2C_MUX_SDA	GND	8	MAX9286_D0_P	GND	8
9	GND	I2C_MUX_RST_N	9	MAX9286_D0_N	GND	9
10	MAX9286_PWDN_N	MAX9286_FSYNC	10	GND	*strobe propagation*	10
11	POC1_INT_N	GND	11		*strobe propagation*	11
12	GND		12		GND	12
13	POC1_EN		13	GND	GND	13
14	POC2_INT_N	GND	14	MAX9286_D1_P	*strobe propagation*	14
15	GND	MAX9286_D2_P	15	MAX9286_D1_N	*strobe propagation*	15
16	POC2_EN	MAX9286_D2_N	16	GND	GND	16
17	MAX9296_PWDN_N	GND	17	MAX9286_D3_P	GND	17
18	GND	*strobe propagation*	18	MAX9286_D3_N	*strobe propagation*	18
19		*strobe propagation*	19	GND	*strobe propagation*	19
20		GND	20	MAX9296_A_D1_P	GND	20
21	GND	*strobe propagation*	21	MAX9296_A_D1_N	GND	21
22		*strobe propagation*	22	GND	MAX9296_A_CLK_P	22
23		GND	23	MAX9296_A_D0_P	MAX9296_A_CLK_N	23
24	GND		24	MAX9296_A_D0_N	GND	24
25	*strobe propagation*		25	GND	GND	25
26	*strobe propagation*	GND	26	*strobe propagation*		26
27	GND	MAX9296_A_D3_P	27	*strobe propagation*		27
28	MAX9296_A_D2_P	MAX9296_A_D3_N	28	GND	GND	28
29	MAX9296_A_D2_N	GND	29	-	GND	29
30	GND	MAX9296_B_D0_P	30	TDI	SCL	30
31	*strobe propagation*	MAX9296_B_D0_N	31	TDO[1]	SDA	31
32	*strobe propagation*	GND	32	3P3VAUX	GND	32
33	GND	MAX9296_B_CLK_P	33	-	GND	33
34	MAX9296_B_D1_P	MAX9296_B_CLK_P	34	-	GA0	34
35	MAX9296_B_D1_N	GND	35	GA1	12P0V	35
36	GND	MAX9296_B_D2_P	36	3P3V	GND	36
37	MAX9296_B_D3_P	MAX9296_B_D2_P	37	GND	12P0V	37
38	MAX9296_B_D3_N	GND	38	3P3V	GND	38
39	GND	VADJ	39	GND	3P3V	39
40	VADJ	GND	40	3P3V	GND	40

Table 3 – FMC-MULTICAM - LPC Pinout

[1] TDO is connected to TDI in order not to break the JTAG chain

Description	Single-ended	Differential	Global Clock	Total
I2C Peripheral Configuration				
	3	**0**	**0**	**3**
Quad GMSL Deserializer				
	2	**16**	**2**	**20**
Dual GMSL2 Deserializer				
	1	**22**	**4**	**27**
Power over Coax				
	4	**0**	**0**	**4**
TOTAL FMC I/O Requirements				
	10	**38**	**6**	**54**

Table 4 – FMC I/O Requirements

3.2 Power

The following table lists all the voltage sources available on the FMC-MULTICAM module.

Voltage Name	Voltage	Current	Description
supplied by **FMC connector**			
3V3AUX	3.3 V		Used by IPMI Identification prior to module power-up.
3V3	3.3 V		Used by MAX9286 (GMSL), MAX9296 (GMSL2), and MAX20087 (PoC) devices.
VADJ	1.2V		VADJ = 1.2V required for use of MIPI I/O standards on UltraScale+/ZynqUltraScale+ carriers.
12V	12.0 V		Used by MAX20087 (PoC) devices.
supplied by the FMC-MULTICAM **FMC module**			
VTERM	1.2V		Used by MAX9296 for VTERM
VDD	1.0V		Used by MAX9296 for VDD
VDD18	1.8V		Used by MAX9286 for DVDD, MVDD, MAVDD, VDDIO. Used for MAX9296A for VDD18, VDDIO

Table 5 –Voltage Sources

The following table describes the voltage requirements of the GMSL and GMSL2 circuits.

Voltage	9296A*		9286**		Total requirement
Typ	Power Rails	Max Current (mA)	Power Rails	Max Current (mA)	Current (mA)
1.0V	VDD	462	N/A	0	462
1.2V	VTERM	60	N/A	0	60
1.8V	VDD18	227	AVDD+DVDD+MAVDD	430	657
3.3V	VDDIO	9	IOVDD	1	10

Table 6 – Power Requirements

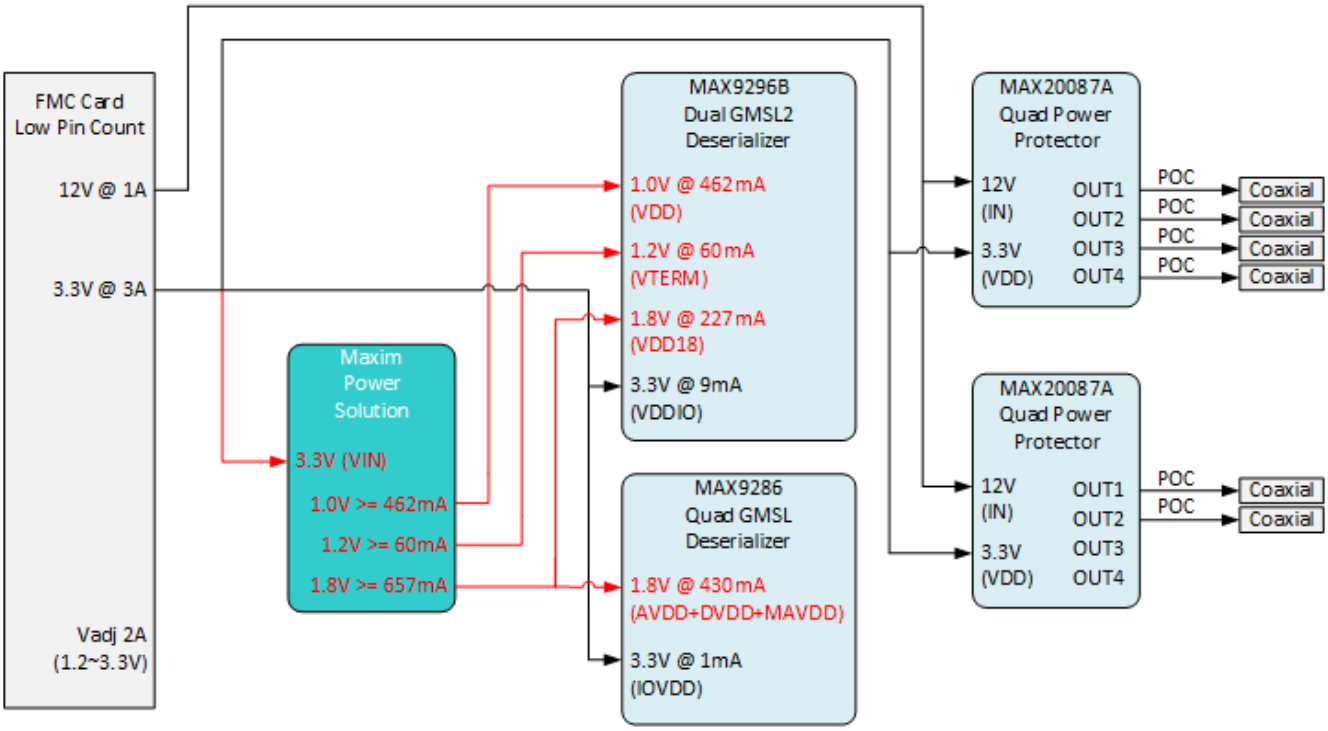


Table 7 – Power, Block Diagram

3.3 I2C Chain 1 - IPMI Identification

The following I2C section implements the IPMI identification for the FMC module.

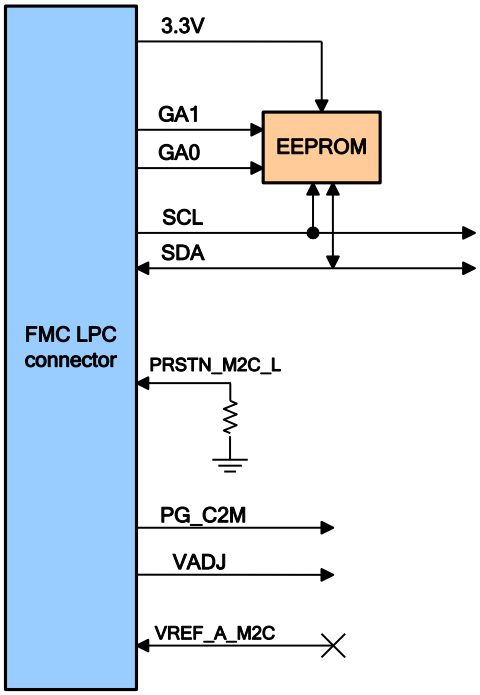


Figure 3 – IPMI Identification, Block Diagram

When the VADJ voltage is valid, the PG_C2M (ie. power good) will be asserted high. An inverted version of this signal is used to enable all the voltage level translators connected to VADJ.

The address of the I2C EEPROM will be determined by the GA[0:1] signals driven by the carrier.

Table 8 describes the EEPROM address for the FMC module.

GA[0:1]	FMC-MULTICAM I2C EEPROM Address
00	0xA0
01	0xA2
10	0xA4
11	0xA6

Table 8 – IPMI Identification, I2C EEPROM Address

The EEPROM content is defined by the Platform Management FRU Information Storage Definition V1.0.

http://download.intel.com/design/servers/ipmi/FRU1011.pdf

The EEPROM content can be generated with the following on-line utility:

https://www.opalkelly.com/tools/fmceepromgenerator/

For the FMC-MULTICAM module, the content is described in Table 9.

Content	FMC-MULTICAM
Board Information	
- Manufacturer Date/Time	-
- Manufacturer	Avnet
- Product	FMC-MULTICAM
- Serial	{programmed during factory testing}
- Part Number	AES-FMC-MULTICAM-G
- FRU File ID	-
Product Information	
- Manufacturer	Avnet
- Product	FMC-MULTICAM
- Part/Model Number	AES-FMC-MULTICAM-G
- Version	A.01.00
- Serial	{programmed during factory testing}
- Asset Tag	-
- FRU File ID	-
FMC Multi-Records	
- Module	single-width
- P1 Connector	LPC
- P2 Connector	None
- VADJ Voltage	1.2V
- VADJ load limits (mA)	min=10, max=1000
- 3.3V load limits (mA)	min=10, max=1000
- 12V load limits (mA)	min=0, max=0
- Clock direction	Mezzanine to Connector
- Max TCK Rate	10
- P1 Bank A Signals	21
- P1 Bank B Signals	0
- P2 Bank A Signals	-
- P2 Bank B Signals	-
- P1 Transceivers	-
- P2 Transceivers	-

Table 9 – IPMI Identification, EEPROM Content

3.4 I2C Chain 2 – Peripheral Configuration

The FMC-MULTICAM Module implements two I2C chains. The second I2C chain is used to configure the FMC-MULTICAM module's peripherals.

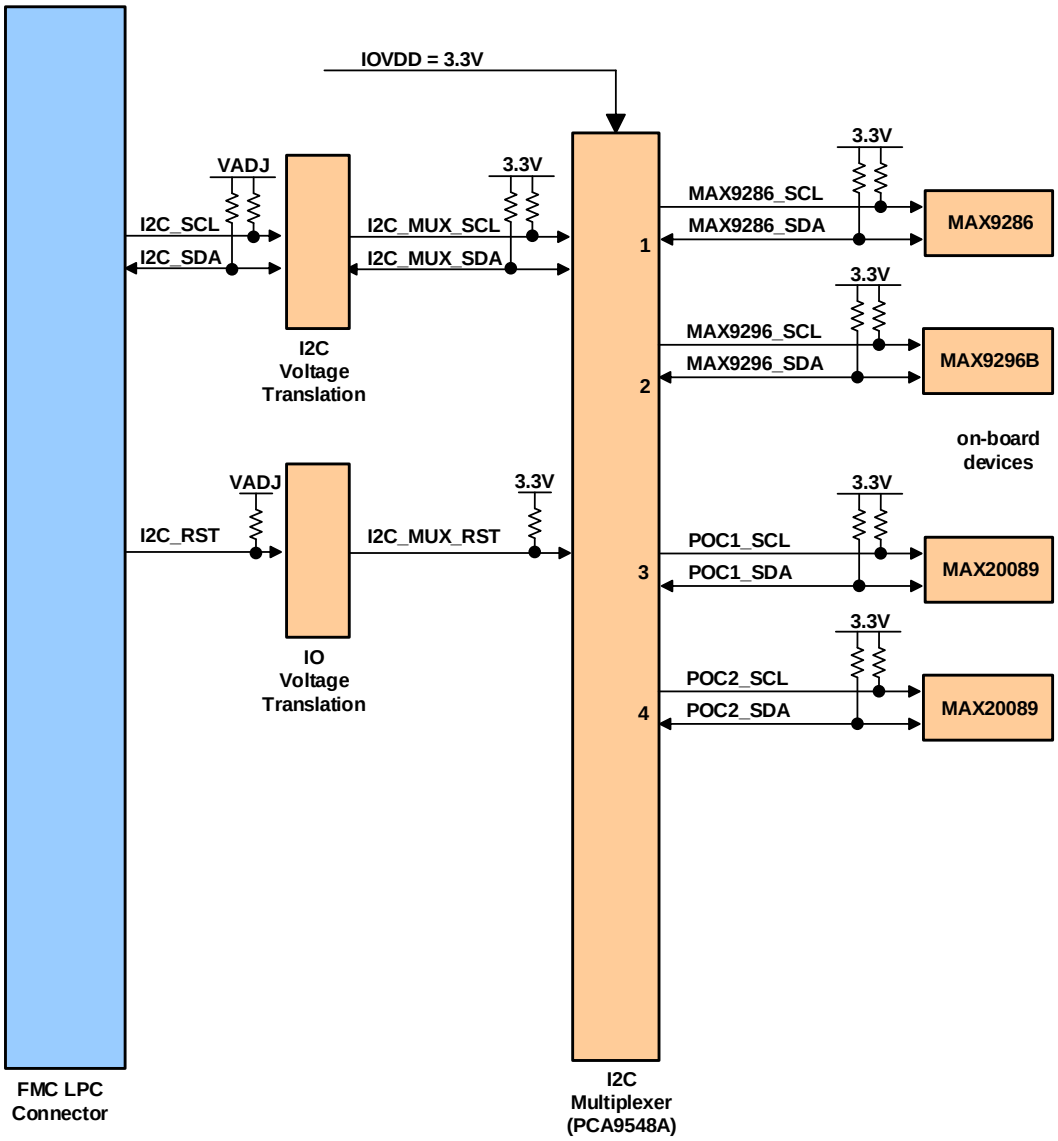


Figure 4 – I2C Peripheral Configuration, Block Diagram

The PCA9546A I2C Multiplexer provides:

- Isolation of each peripheral's I2C chain
- I2C address conflict resolution

The following table lists the I2C addresses that may be present on each of the I2C Multiplexer's ports. Notice that the I2C Multiplexer's address is always visible regardless of which port is enabled.

Device	I2C Address
I2C Multiplexer	0xE0 (PCA9548)
Mux Port 1	
Quad GMSL Deserializer + serializers (4) + image sensors (4)	0x90 (MAX9286)
Mux Port 2	
Dual GMSL2 Deserializer + serializers (2) + image sensors (2)	0x90 (MAX9296A)
Mux Port 3	
Power Over Coax 1	0x28 (MAX20087A)
Mux Port 4	
Power Over Coax 2	0x28 (MAX20087A)
Mux Port 5	
unused	
Mux Port 6	
unused	
Mux Port 7	
unused	
Mux Port 8	
unused	

Table 10 – I2C Peripheral Configuration, Device Summary

Description	Single-ended	Differential	Global Clock	Total
I2C Peripheral Configuration				
MUX_SCL, MUX_SDA, MUX_RST	3	0	0	**3**

Table 11 – Configuration – FMC I/O Requirements

3.5 Quad GMSL Deserializer

The FMC module support up to four (4) 2Mpixel cameras, connected via low cost 50Ω Coax (100Ω STP) cables. The camera modules make use of the Maxim Integrated GMSL (Gigabit Multimedia Serial Link), which includes the following features and advantages:

- compression-free alternative to Ethernet
  - 10x faster data rates
  - 50% lower cabling costs
  - better EMC
- up to 15 meters of 50Ω coax cabling
- built-in spread-spectrum capability, improving EMI performance of the link

The following figure illustrates the MAX9286 based Quad GMSL Deserializer circuit.

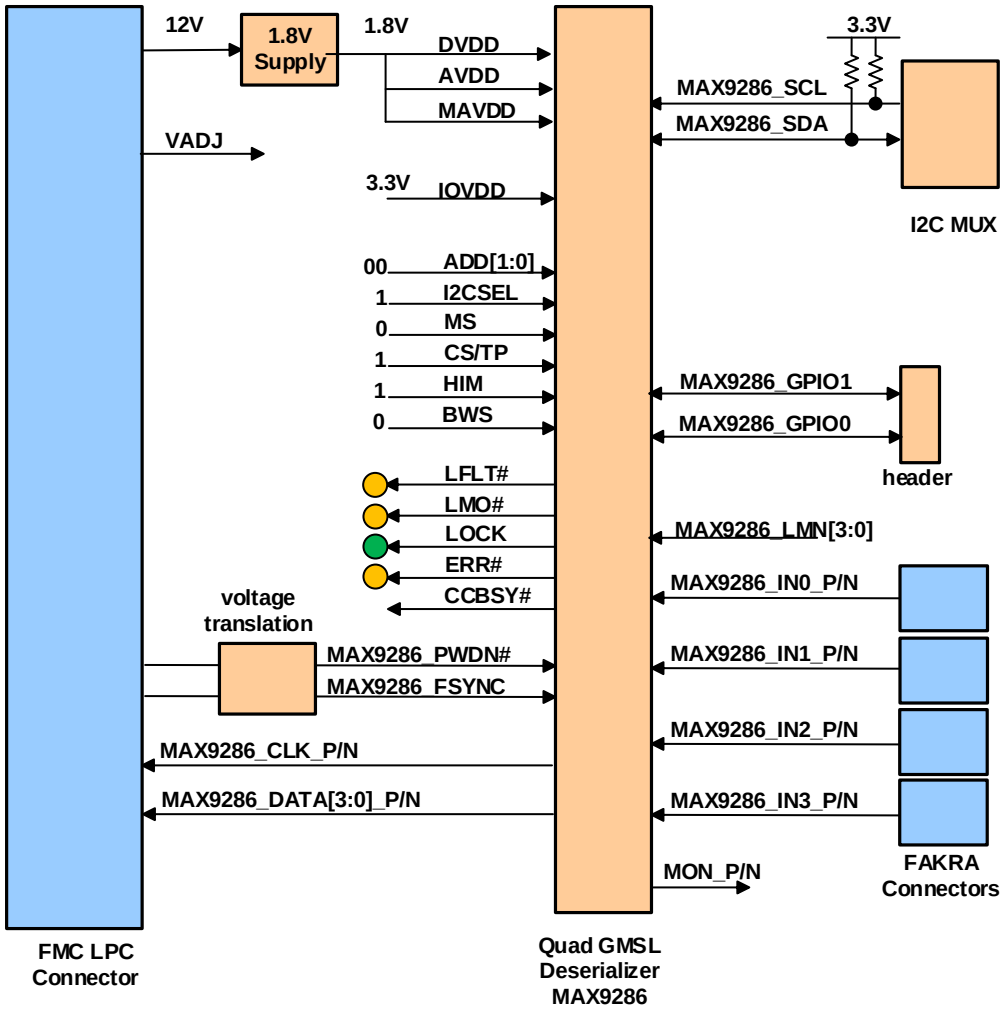


Figure 5 – Quad GMSL Deserializer – Block Diagram

The following table describes the connection of various configuration pins

Pin	Description	Value
ADD[1:0]	Three-Level Address-Selection Input. The state of ADD[1:0] latches at power-up or when resuming from power-down mode (PWDN = low). **00 = 0x90**	00
I2CSEL	I2C Select. Control-channel interface protocol select input with internal pulldown to EP. **Set I2CSEL = high to select I2C-to-I2C interface.** Set I2CSEL = low to select UART/UART or UART/I2C interface.	1
MS	Mode Select Input with Internal Pulldown to EP. Mode selection is only used in UART-to-UART and UART-to-I2C mode. Set MS = low to select base mode. Set MS = high to select bypass mode.	0
CX/TP	Coax/Twisted-Pair Select Input with Internal Pulldown to EP. **Set CX/TP high to select coax input.** Set CX/TP low for STP input. Input cable type can be programmed to a different value after power-up	1
HIM	High-Immunity Mode Input with Internal Pulldown to EP. Default HIGHIMM bit value is latched at power-up or when resuming from power-down mode (PWDN = low) and is active-high. HIGHIMM can be programmed to a different value after power-up. HIGHIMM in the serializer must be set to the same value. High-immunity mode must be supported by the serializer (MAX9275-MAX9281 only).	1
BWS	Three-Level Bus-Width Select Input. Set BWS to the same level on both sides of the serial link. **Set BWS = low for 24-bit mode.** Set BWS = high for 32-bit mode. Set BWS = open for high-bandwidth mode (MAX9275-MAX9281 only).	0

Table 12 – Quad GMSL Deserializer – Configuration Pins

The following table describes the connection of various status pins.

Pin	Description	Connection
LFLT#	Active-Low Open-Drain Line-Fault Output. LFLT has a 60kΩ pullup to IOVDD. LFLT = low indicates a line fault. LFLT is output high when PWDN is low.	YELLOW LED
LMO#	Line Memory-Overflow Output. LMO has a 60kΩ pullup to IOVDD. LMO = low when the serial data overflows the line memory.	YELLOW LED
LOCK	Open-Drain Lock Output with Internal 60kΩ Pullup to IOVDD. LOCK = high indicates that PLLs are locked with correct serial-word-boundary alignment.	GREEN LED

	LOCK = low indicates that PLLs are not locked or an incorrect serial-word-boundary alignment. LOCK is high when PWDN = low.	
ERR#	Active-Low Error Output. Open-drain data error detection and/or correction indication output with internal 60kΩ pullup to IOVDD. ERR is high when PWDN is low.	YELLOW LED
CCBSY#	Active-Low Control-Channel Busy Output. Open-drain indicator of control-channel activity with Internal 60kΩ pullup to IOVDD. CCBSY = low indicates that the control channel is currently in use.	Test Point

Table 13 – Quad GMSL Deserializer – Status Pins

Description	Single-ended	Differential	Global Clock	Total
Quad GMSL Deserializer				
MIPI-CSI2 4 lanes (CLK_P/N, DATA[3:0]_P/N)		8	2	**10**
Control signals (PDWN#, FSYNC)	2			**2**
Unuseable (strobe propagation)		8		**8**
TOTAL	**2**	**16**	**2**	**20**

Table 14 – Quad GMSL Deserializer – FMC I/O Requirements

3.6 2Mpixel Camera Module

The following figures illustrates the supported 2Mpixel Camera Module

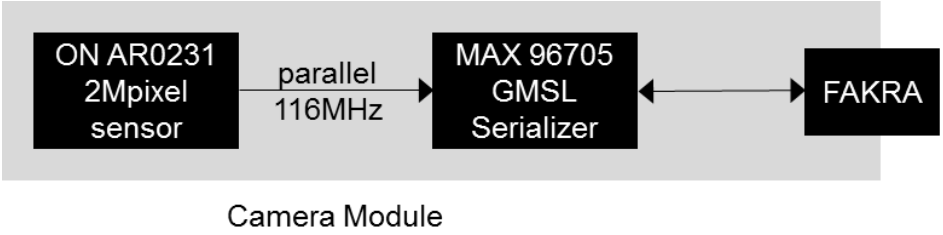


Figure 6 – 2Mpixel Camera Module – Block Diagram

The 2Mpixel Camera module is composed of existing off-the-shelf components from ON Semiconductor's Modular Automotive Reference System (MARS).

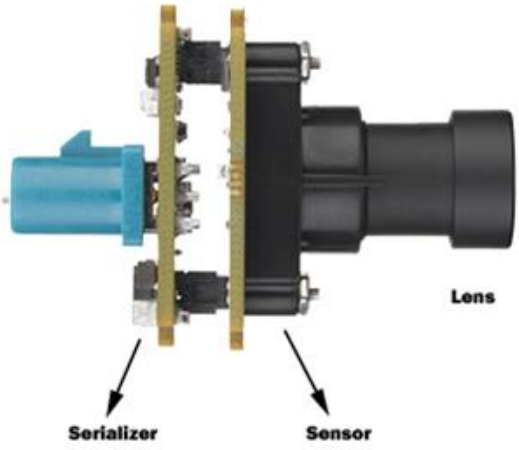


Figure 7 – 2Mpixel Camera Module – MARS Components

The following table lists the part numbers that make up the supported 2Mpixel camera module.

Part Number	Hardware
2Mpixel Camera Modules	
MARS1-AR0231AT6-GEVB MARS1-MAX96705-GEVB	On Semi MARS AR0231 camera board ON Semi MARS MAX96705 Serializer board

Table 15 – 2Mpixel Camera Module - Components

3.7 Dual GMSL2 Deserializer

The FMC module support up to two (2) 8Mpixel (4K) cameras, connected via low cost 50Ω Coax (100Ω STP) cables. The camera modules make use of the Maxim Integrated GMSL2 (Gigabit Multimedia Serial Link, V2) , which includes the following features and advantages:

- compression-free alternative to Ethernet
  - 10x faster data rates
  - 50% lower cabling costs
  - better EMC
- up to 15 meters of 50Ω coax cabling
- built-in spread-spectrum capability, improving EMI performance of the link

The following figure illustrates the MAX9296A based Dual GMSL2 Deserializer circuit.

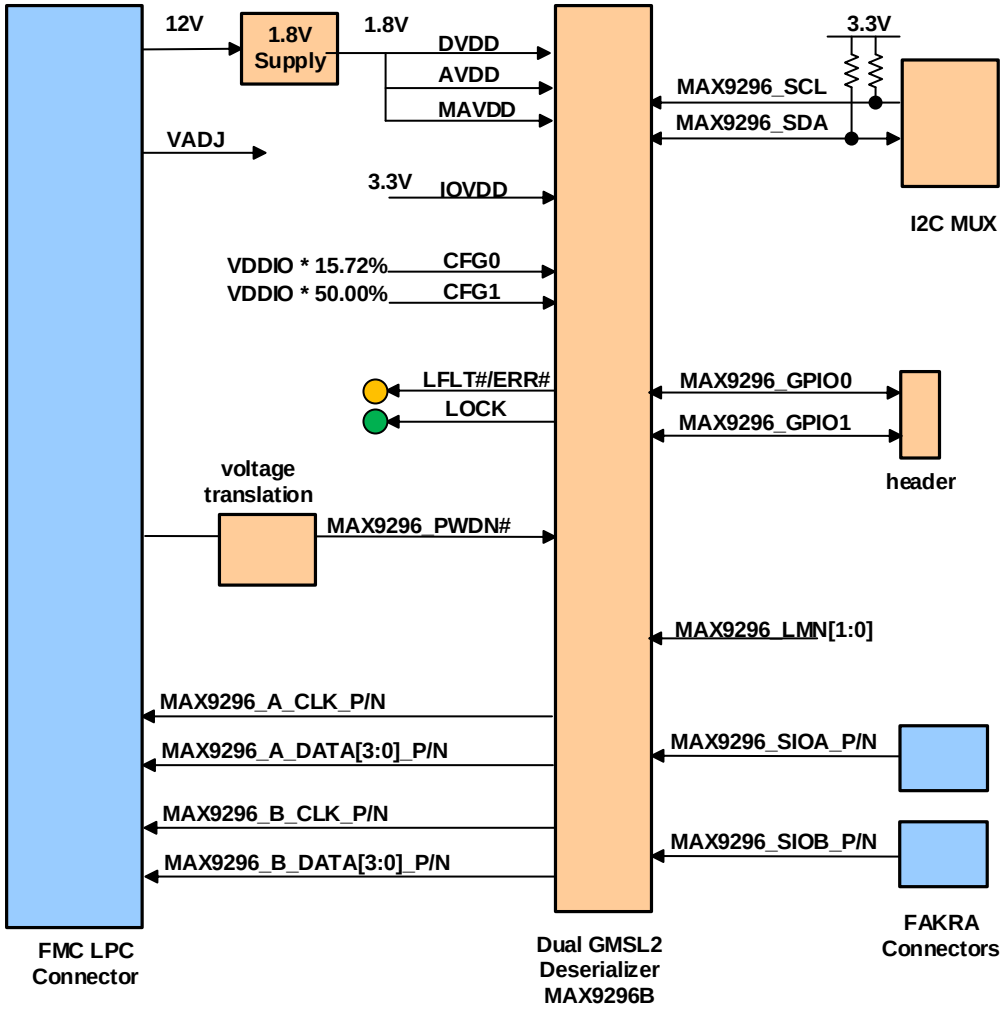


Figure 8 – Dual GMSL2 Deserializer – Block Diagram

The following table describes the connection of various configuration pins

Pin	Description	Value
CFG0	Resistor Divider for I2C/UART selection (I2CSEL) and device address selection (DEVICE_ADDRESS) **VDDIO * 15.72% = I2C 0x90** Reference : MAX9296A DataSheet – Table 1 – CFG0 Input Map	**VDDIO * 15.72%**
CFG1	Resistor Divider for CX/TP selection, GMSL1/GMSL2 selection, BWS selection, HIM selection, and GMSL2 rate. **VDDIO * 50.00% = CX/TP = coax, GMSL2, rate = 6Gbps, BWS = n/a** Reference : MAX9296A DataSheet – Table 2 – CFG1 Input Map	**VDDIO * 50.00%**

Table 16 – Dual GMSL2 Deserializer – Configuration Pins

The following table describes the connection of various status pins.

Pin	Description	Connection
LFLT#/ERR#	Active-Low Open-Drain Line-Fault Output. LFLT has a 60kΩ pullup to IOVDD. LFLT = low indicates a line fault. LFLT is output high when PWDN is low.	YELLOW LED
LOCK	Open-Drain Lock Output with Internal 60kΩ Pullup to IOVDD. LOCK = high indicates that PLLs are locked with correct serial-word-boundary alignment. LOCK = low indicates that PLLs are not locked or an incorrect serial-word-boundary alignment. LOCK is high when PWDN = low.	GREEN LED

Table 17 – Dual GMSL2 Deserializer – Status Pins

Description	Single-ended	Differential	Global Clock	Total
Dual GMSL2 Deserializer				
MIPI-CSI2 4 lanes (CLK_P/N, DATA[3:0]_P/N)		8	2	10
MIPI-CSI2 4 lanes (CLK_P/N, DATA[3:0]_P/N)		8	2	10
Control signals (PDWN#)	1			1
Unuseable (strobe propagation)		6		6
TOTAL	**1**	**22**	**4**	**27**

Table 18 – Dual GMSL2 Deserializer – FMC I/O Requirements

3.8 8Mpixel Camera Module

The following figures illustrates the supported 8Mpixel Camera Module

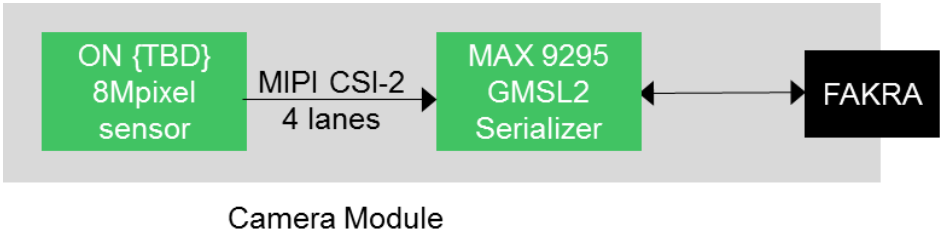


Figure 9 – 8Mpixel Camera Module – Block Diagram

… TBD …

3.9 Power Over Coax

In order to power the various cameras, the MAXIM Integrated MAX20087A delivers up to 600mA load current to each of its four output channels.

The following figure illustrates the Power Over Coax circuits.

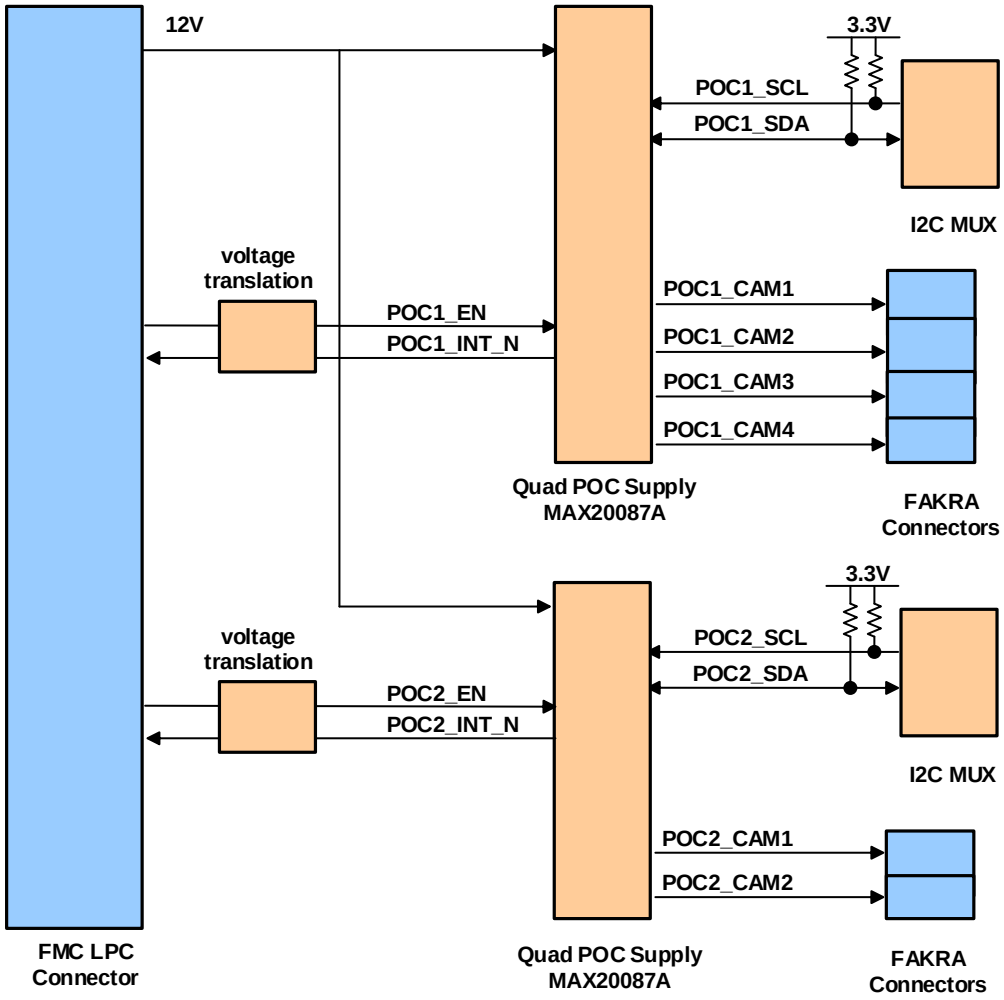


Figure 10 – Power Over Coax – Block Diagram

For the 2Mpixel camera modules, the required power per camera is:

- MAX96705 Serializer = 1.8V @ 128mA
- AR0234 Image Sensor < 350mW

For the 8Mpixel camera modules, the required power per camera is:

- TBD

Description	Single-ended	Differential	Global Clock	Total
Dual GMSL2 Deserializer				
Control signals (EN, INT_N)	4			4
TOTAL	**4**	**0**	**0**	**4**

Table 19 – Power over Coax – FMC I/O Requirements

3.10 FAKRA Connectors and Coax Cables

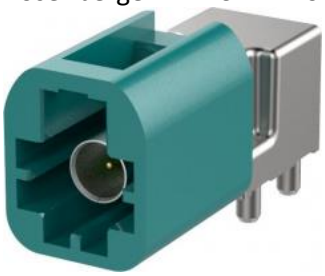
The FMC module makes use of the Rosenberger High-Speed FAKRA Mini (HFM) connectors.
www.rosenberger.com/hfm

The HFM PCB Quad Plug connector used for GMSL is

- Rosenberger : **AMS22D-40MZ5-Z**

The HFM PCB Plug connector used for GMSL2 is

- Rosenberger **: AMS22A-40MZ5-Z**



The Quad HFM to 4 x FAKRA cable assembly used for the quad GMSL cameras is:

- Rosenberger **: L02-026-1000-Z-ZZZZ_V2**

Technical Data Sheet		Rosenberger
HFM® High-Speed FAKRA Mini	CABLE ASSEMBLY	**L02-026-XXX-Y-YYYY_V2**