



UltraZed™ I/O Carrier Card

Version 1.0

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1 Introduction

The UltraZed™ I/O Carrier Card (IOCC) is a development board designed for customers to easily evaluate the Avnet UltraZed System On Module (SOM) module(s). This carrier card provides all of the necessary power, clock, reset control and SoC I/O pin accessibility through the JX1, JX2, and JX3 MicroHeaders. To reduce the product-to-market development cycle the carrier card provides the following interfaces: SATA 3, Display Port, USB 3.0, Dual UART, 12 PL-PMODs, 1 PS-PMOD, LVDS Touch Panel, Arduino UNO® R3 and microSD card.

The Carrier Card also provides two debug interfaces - SMT2 and PC-4 JTAG - to assist with SOM application development.

This document details the specific features, operation and configuration of the UltraZed IOCC board. Please visit www.ultrazed.org/product/ultrazed-EG for the latest product information.

1.1 List of Features

The UltraZed IOCC provides the following features and interfaces. Please see the associated section in this User Guide for further information.

- Supports the following SOM types:
 - XCZU3EG-SFVA625
 - XCZU2EG-SFVA625
 - XCZU2CG-SFVA625
 - XCZU3CG-SFVA625
- SOM connections:
 - 2 high density 140 pin JX connectors (JX1, JX2)
 - 1 high density 100 pin JX connector (JX3)
- Carrier Interfaces:
 - SATA3 host interface.
 - Display Port x2 connector.
 - USB 2.0/3.0 Host & OTG micro AB connector.
 - 10/100/1000 Mb/s RJ45 connector.
 - Dual USB-UART using Micro USB connector.
 - LVDS Touch Panel interface.
 - 12 PL PMOD headers (single ended).
 - 1 PS PMOD header (single ended).
 - Arduino UNO® R3 shield compatible connectors with 6 signal analog/digital select.
 - SOM +5V fan connector.
 - microSD card connector.
- User switches, pushbuttons and LEDs:
 - 8 PL user slide switches
 - 4 PL user push button switches
 - 8 PL user LEDs
 - 1 PS user push button switch
 - 1 PS user LED
 - 1 SOM reset push button switch

- Debug & Configuration
 - Digilent® SMT2 USB-JTAG module
 - PC4 JTAG header
 - Voltage monitor header
 - PG_Module LED
 - VIN_HDR LED
 - Various interface LED indicators displaying fault, link and speed.
 - Write protect jumper on microSD card interface.
 - Clock synthesizer's start-up configuration - jumper selectable.
 - 3 GTR differential refclock outputs
 - 1 Global Clock differential output for SOM fabric
 - Start-up Mode selectable via jumpers
 - Arduino Digital select function for CON4
- I2C interfaces
 - I2C programmable differential clock generator
 - I2C MAC address memory device
 - I2C PMBUS programmable IRPS5401MTRPBF Power Management IC (PMIC)
- Power
 - +VIN 11.6V up to 12.2V via six pin power connector
 - Power slide switch
 - 5 Channel I2C programmable PMIC
 - Remote rail sensing of SOM. PMIC voltage adjusts according to SOM loading.
 - Isolated Vin to +3.3V regulator
 - +VIN connections to SOM via JX connectors.
 - PMBus™ header
 - PL SYSMon header
 - PS VBATT battery connection with diode steering protection
 - LR-44 Battery slot, external jack or on board 1.8V power
 - Dual 100 mil header for user voltage input

1.2 Block Diagram

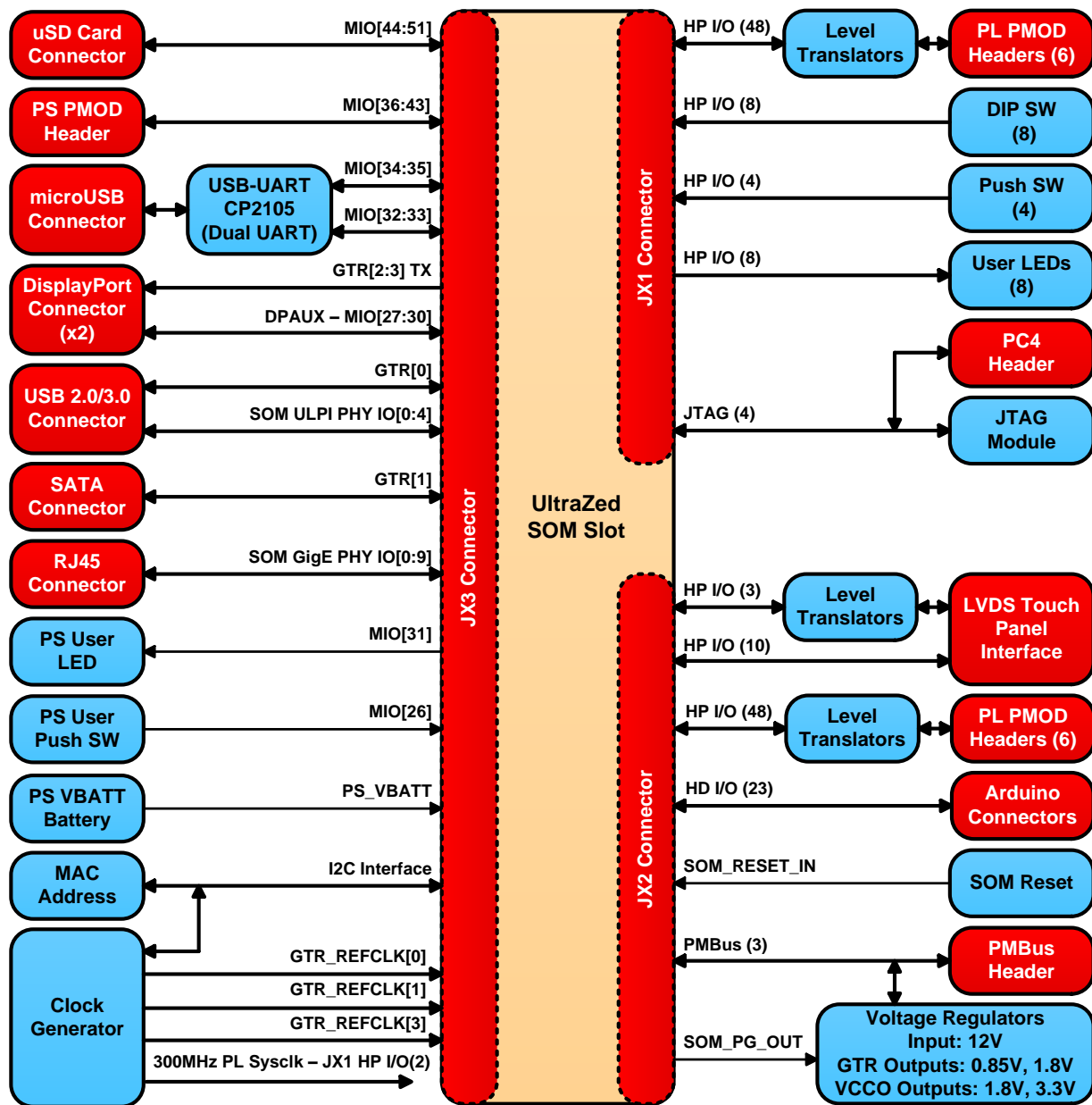


Figure 1 – UltraZed IO Carrier Card Block Diagram

Glossary

Term	Definition
IOCC	Input / Output Carrier Card. The SOM attaches to this carrier card (board) for user evaluation. The IOCC features proven high speed interfaces to the SOM as well as the necessary power, control and clocks required for the SOM to operate.
MIO	Multiplexed Input Output – the dedicated I/O available on the PS
PL	Programmable Logic – programmable fabric of the SoC.
PMIC	Power Management Integrated Circuit – voltage regulator used to create required board voltages.
POR	Power On Reset – reset asserted during power on event. Keeps board in reset until PMIC's output is stabilized.
PS	Processing System – the SoC's processor cores – Application Processing Unit (Quad core ARM Cortex-A53) and Real-Time Processing Unit (Dual core ARM Cortex-R5).
SMPS	Switch Mode Power Supply – switching power supply used to provide high current rails to the board. May be separate from the PMIC or may be the PMIC, depending application needs.
SOM	System On Module – a SoC IC placed on a PCB allowing easy access to the SoC IC's interface, power and control signals. Includes the necessary memory (RAM, storage), power and connectors to operate as a pluggable processing module.
SoC	System On Chip – Xilinx Zynq UltraScale+ IC.

Table 1: Glossary

1.2.1 Additional Documentation

- Additional information and documentation on Avnet's UltraZed product line can be found at www.ultrazed.org/product/ultrazed-EG
- Additional information and documentation on Xilinx's Zynq® UltraScale+ All Programmable Heterogenous MPSoCs can be found at <http://www.xilinx.com/products/silicon-devices/soc/zynq-ultrascale-mpsoc.html>

2 Functional Description

The following chapter details all of the IOCC interfaces, their configuration and their functional attributes. This I/O Carrier Card (IOCC or simply carrier card) provides 26 PS MIO pins and 180 user PL I/O pins (72 differential pairs and 36 single-ended) organized as follows:

- 26 PS MIO bank 501, MIO[26:51]
- 24 PL HD (High Density) I/O pins (1 bank)
- 156 PL HP (High Performance) I/O pins (3 banks)

2.1 JX Micro Connectors

The UltraZed IO Carrier Card has 3 TE 0.8mm FH (Free Height) connectors used to access the UltraZed SOM I/O pins. The carrier card to SOM connectors are designated as “JX” connectors. Two of the connectors, JX1 and JX2, are 140 pin connectors and the third connector, JX3, is a 100 pin connector.

2.1.1 JX1 Connector

- JTAG pins (JTAG_TMS, JTAG_TCK, JTAG_TDI, and JTAG_TDO)
- 42 differential HP I/O pairs (JX1_HP_DP)
- 6 single ended signals (JX1_HP_SE)
- Power and ground pins (VCCO_HP_64, VCCO_HP_65, VIN, and GND)

2.1.2 JX2 Connector

- SYSMON pins (SYSMON_VP, SYSMON_VN, SYSMON_DXP, and SYSMON_DXN)
- 30 differential HP I/O pairs (JX2_HP_DP), 30 single ended signals (JX2_HP_SE and JX2_HD_SE).
- Power and ground pins (VCCO_HP_66, VCCO_HD_26, VIN, and GND)
- SOM_RESET_IN_N input
- CC_RESET_OUT_N output
- SOM_PG_OUT_N output
- PMBus signals (PMBus_DATA, PMBus_CLK, and PMBus_ALERT#).

2.1.3 JX3 Connector

- PS GTR[0:3], PS GTR_REFCLK[0:3]
- PS MIO bank 501 pins (MIO[26:51])
- USB 2.0 connector interface (USB_OTG_P, USB_OTG_N, USB_ID, USB_OTG_VBUS, and USB_OTG_CPEN)
- Gigabit Ethernet connector interface (ETH_MD[1:4]_P, ETHMD[1:4]_N, and ETH_PHY_LED[0:1])
- Carrier Card I2C interface (CC_SDA, CC_SCL, and CC_INT_N)
- PS_VBATT input. Jack input or LR-44 battery input.
- Power and ground pins (MGTRAVCC, MGTRAVTT, and GND)
- Voltage sense feedback output pins (MGTRAVCC_Sense, MGTRAVCC_Sense, VCCO_HP_64_Sense, VCCO_HP_65_Sense, VCCO_HP_66_Sense, and VCCO_HD_26_Sense).

2.2 PS USB 2.0/3.0 Interface – J12

The UltraZed IO Carrier Card's USB 2.0/3.0 interface is implemented with a Kycon KMMX-AB10-SMT1SB30TR Micro AB connector capable of supporting OTG, Device and Host modes. The UltraZed SOM contains the USB 2.0 ULPI PHY interface (USB3320 IC) for USB 2.0. PS GTR[0] signals are used to implement the USB 3.0 interface to the same connector.

2.2.1 USB 2.0 interface:

- The USB 2.0 interface is connected via the SOM's ULPI PHY IC.
- The interface differential impedance is 90 Ω (+/- 5%), Single Ended is 45 Ω (+/- 5%)
- Power: 5V, 500mA.
- CPEN is used to enable the ACPI/USB compliant MIC2544_1YMM power control IC. When CPEN is logic high, "enabled", the +5.0V rail is passed through to the +USB_VB rail for the USB connector.
- When CPEN is low the power switch is disabled.
- R164 is used to set the current limit of the MIC2544 part. The value of 191 ohms is used to set the current to 1.23 Amps.
- When in Host or OTG mode, FB8 and FB9 along with two capacitors are used to provide filtered power to the USB connector J12.
- D25 and D26 are ESD arrays used to protect the board and attached devices against static discharge.
- LED D24 is used to indicate a current limit or thermal shutdown event with the MIC2544 IC. The output is open-drain and asserted low when a flag event has occurred which causes D24 to turn on. The output is not latched and therefore clears once the event ends thereby extinguishing D24.

2.2.2 Device, Host or OTG mode select jumpers.

- J15 selects how the USB_ID net is connected. Pin 1 to 2 allows the USB device to connect to the SOM, pin 2 to 3 forces the pin to +3.3V. No populate allows the pin to float. When floating the interface is set to Device mode but once connected the operation can be reversed via the Host Negotiation Protocol (HNP). By default the jumper is not populated.

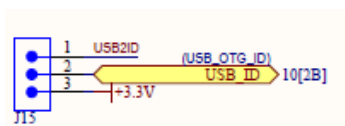


Figure 2 – J15 USB_ID select jumper

- JP6 is used to select the power for +USB_VB.
- J13 used to select the pullup resistor for the USB_OTG_VBUS net going to the SOM.
- J14 used to select the appropriate +USB_VB bus capacitance for the operating mode.
- The mode jumper positions are listed below. Default positions are USB in Host Mode.

2.2.3 USB 3.0 interface:

- USB 3.0 has a transfer data rate of up to 5Gb/s (625 MB/s) and is referred to as USB *Super Speed*. This portion of the interface is directly connected to the Zynq PS via PS GTR[0] and J12, the integrated USB micro-AB connector.
- Power capability is up to 1.23A @ 5V for non-data (charging) power delivery.
- Up to 900mA is available during data transfers.
- The differential impedance routing Zdiff is 90Ω (+/- 10%)
- The PS GTR 52 MHz clock required is derived from the IDT synthesizer.

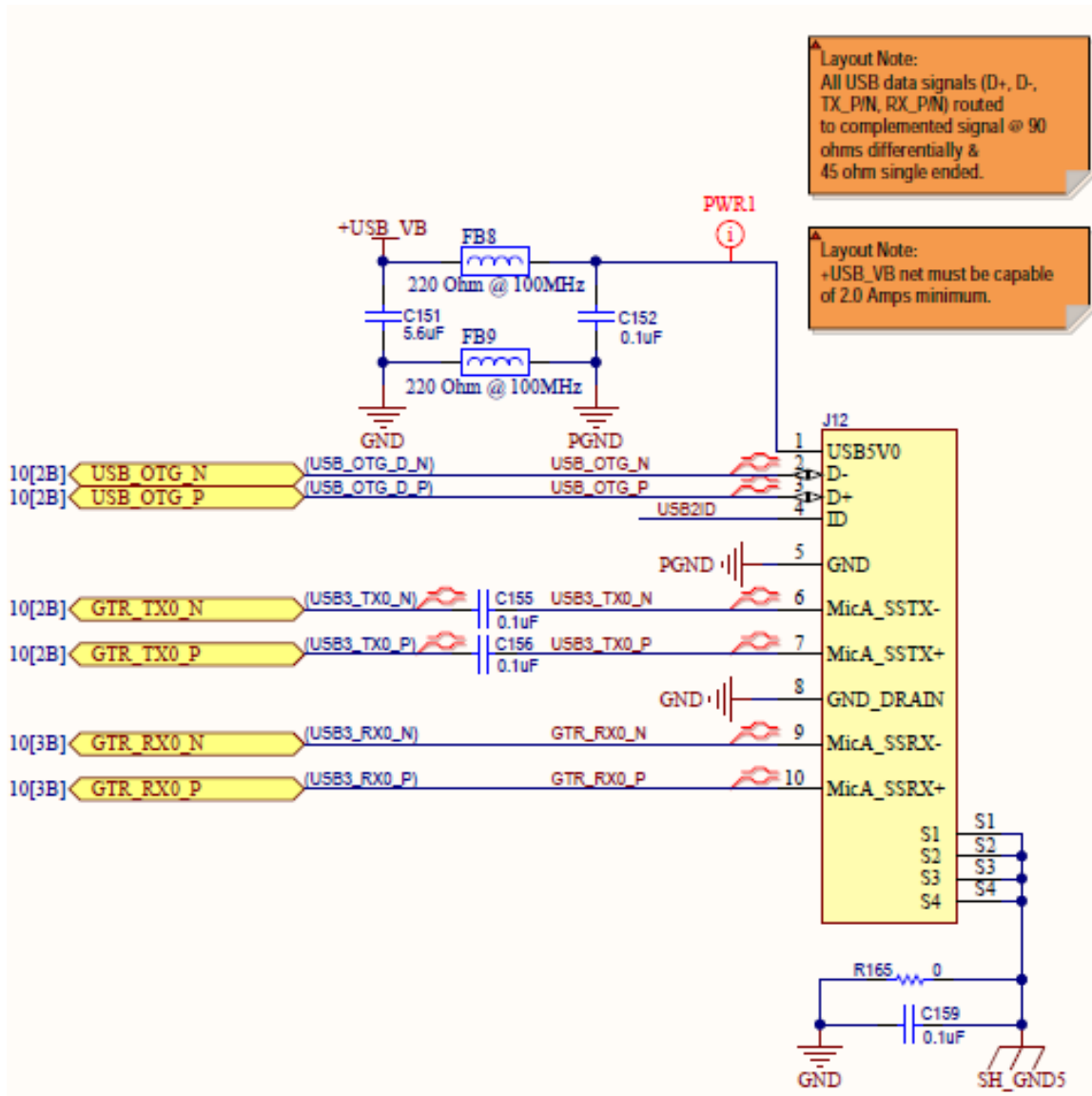


Figure 5 – USB 2.0/3.0 Port Interface

2.3 PS 1000 Mb/s Ethernet RJ45 – J5

The IOCC's 1000 Mb/s Gigabit interface uses an integrated magnetic BEL FUSE L829-1J1T-43 RJ45 connector or equivalent mounted on the IOCC. The MAC and PHY are located on the SOM and connected using the SoC's RGMII interface. The signals from the PHY are then routed to the JX3 connector where the IOCC routes them to the RJ45 connector.

- The MDI impedance is 50 Ω single ended, +/- 5% and is referenced to the positive plane (See TI AN1263) if termination resistors are used at the SOM.
- The trace lengths are matched to within 10 mils pair to pair and no more than 100 mils overall between the entire group of pairs.
- The LEDs are driven via NPN BJT inverters which also provide low cost level translation.
- Two LEDs to indicate speed and activity status:
 - ETH_PHY_LED0: Green Speed
 - ETH_PHY_LED1: Yellow Activity

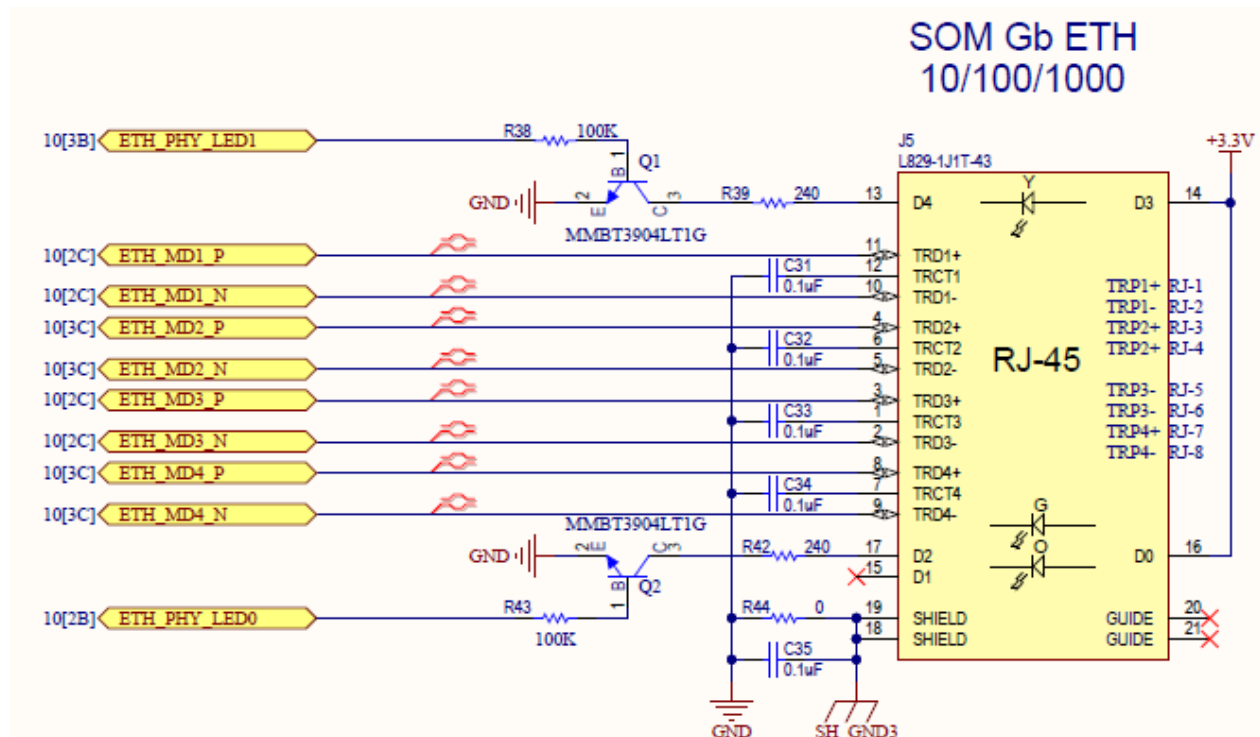


Figure 6 – Gigabit Ethernet Port

2.4 PS Display Port x2 interface – P2

The UltraZed IO Carrier Card contains a x2 Display Port connection. The PS GTR[2:3] TX ports are used to implement this interface as shown in **Figure 7**.

- The Display Port interface also uses an auxiliary interface (DPAUX) which is implemented on the IO Carrier Card using the PS MIO[27:30] signals (these are pre-defined MIO pins for the DPAUX when the display port is used).
- The DPAUX generator is used to convert single ended MIO signals to differential Display Port signals. This eliminates the need for these signals to be routed in the SoC fabric. The MIO[27:30] pins are connected to the UltraZed SOM JX3 connector and are operated at 3.3V. The MIO pin assignment and function is as follows:
 - MIO27 – DPOUT – drives DPAUX_C_P to P2
 - MIO28 – DP_HPD – active high signal from P2 indicating Hot Plug Detection.
 - MIO29 – DP_OE_N – tied to both enables of transceiver U4, enables the outputs when driven low by SoC.
 - MIO30 - DPIN – receives DPAUX_C_N from P2
- The MIO pins are routed to a differential driver (FIN1019) to create the DPAUX_P/N pair at 100Ω.
- The Vbias and 100Ω Z matching network has been implemented on the DPAUX pair.
- A separate 5V to 3.3VDP linear LDO regulator, Maxim MAX8902BATA+T, is placed to provide low noise, high precision 3.3V for the display attached to the port.
- The Display Port x2 uses ESD components (TPD8S0009DSMR, TPD4E001DRLR) placed on the data lines.

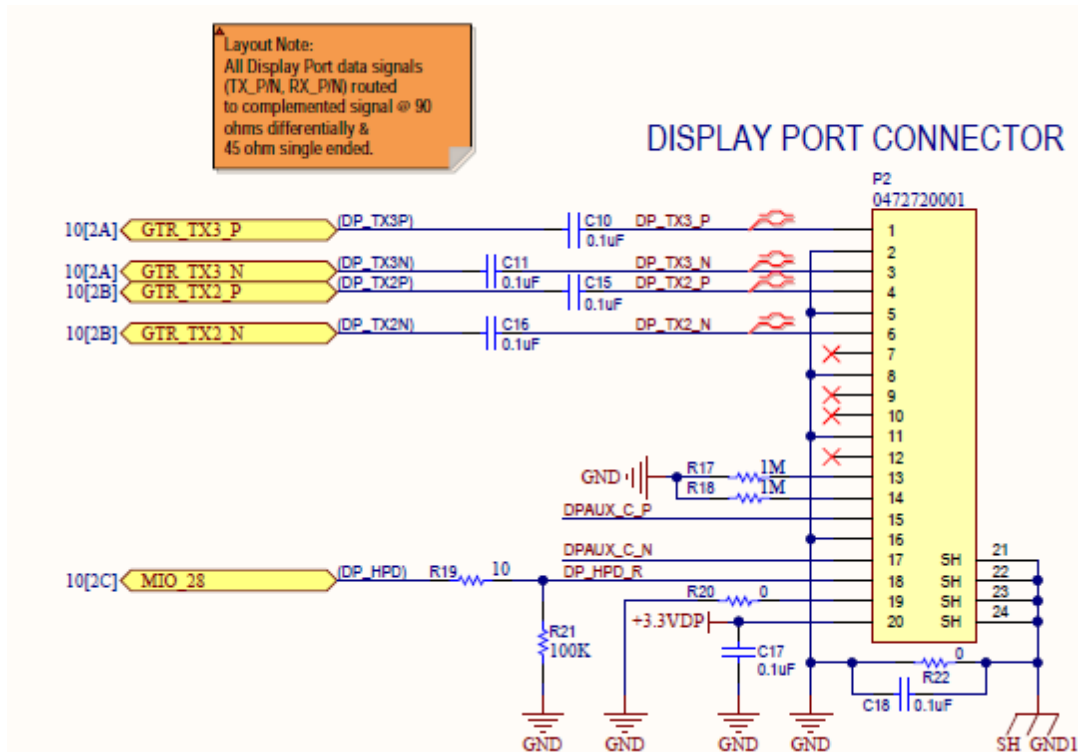


Figure 7 – Display Port Interface

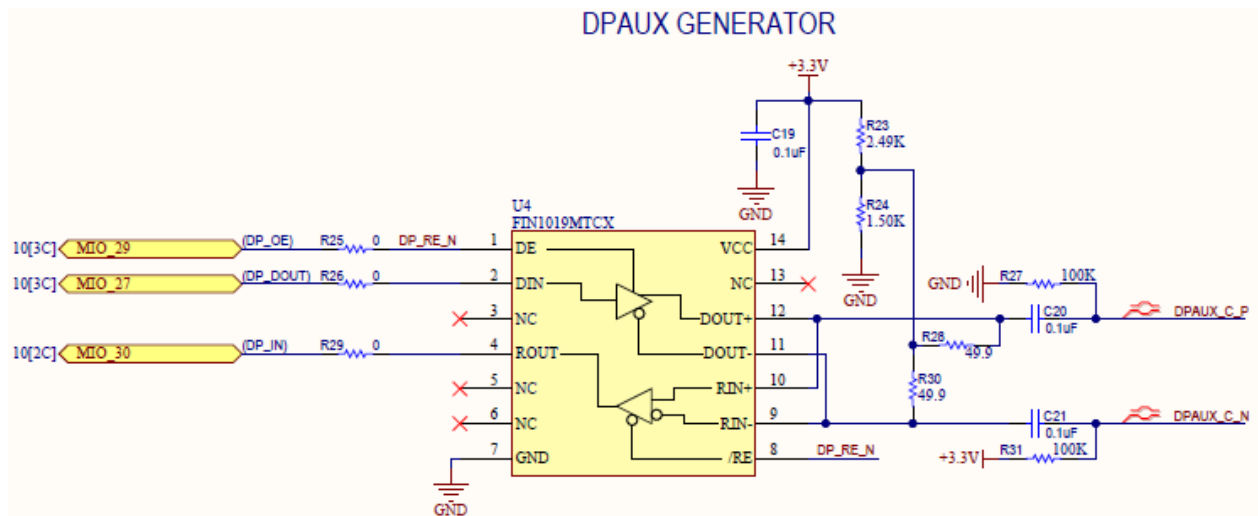


Figure 8 – Display Port DPAUX Generator including Z match and AC coupling

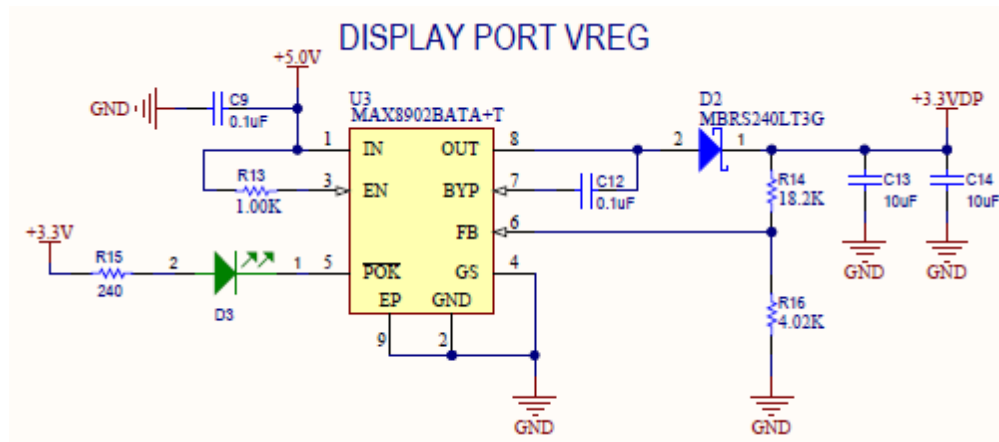


Figure 9 – Display Port 3.3V power supply

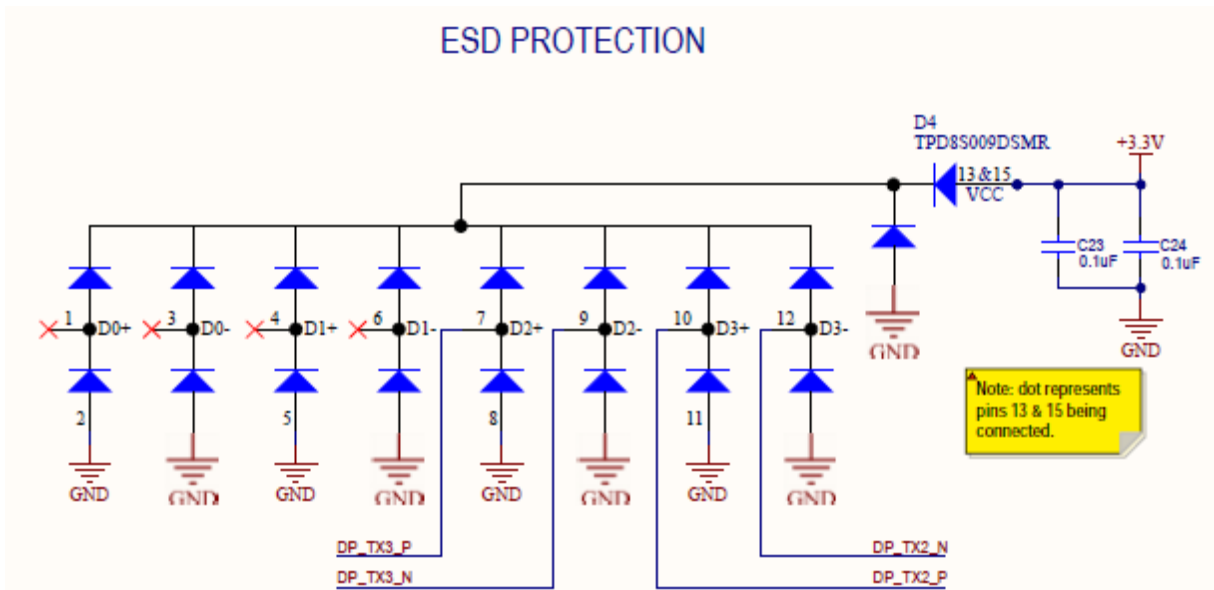


Figure 10 – Display Port GTR TX ESD protection

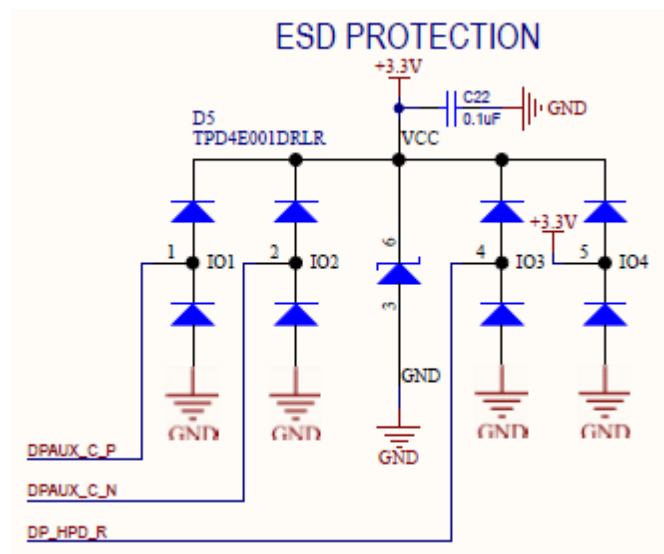


Figure 11 – Display Port DPAUX ESD protection

2.5 PS SATA 3 Host Interface – J3

The UltraZed IO Carrier Card's SATA 3 host interface uses the SoC's PS GTR[1] transceiver. The interface includes AC coupling capacitors with appropriate PCB GSSG cutouts and a maximum of 2 layer transitions per signal with no blind or buried vias. This topology is used to minimize impedance mismatches thereby improving signal integrity.

- Interface impedance: 100 ohms, +/- 15%
- Data rates up to 6 Gb/s

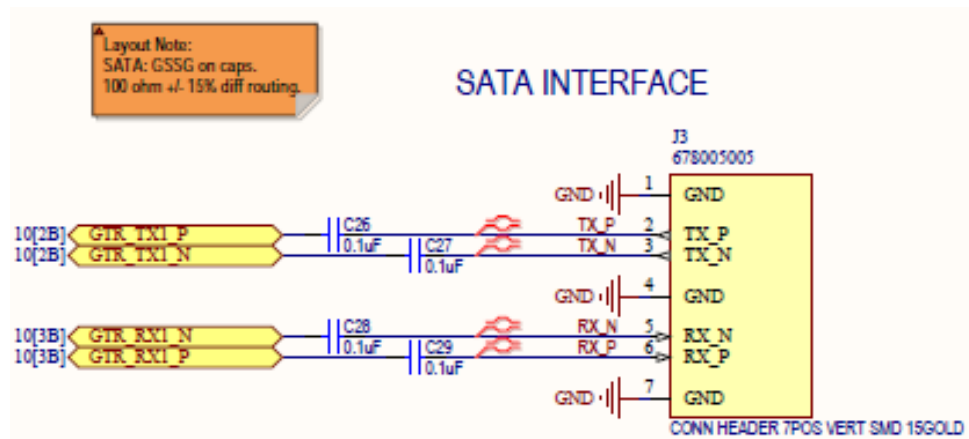


Figure 12 – SATA Port interface

2.6 PS PMOD Header – JPS1

The PS PMOD header is connected to the PS MIO[36:43] pins and operated at 3.3V I/O using the VCCO_PSIO_501 rail. The PS MIO[36:43] maps to SPI, however the UltraScale+ does not create a direct map to the UART(0 or 1) nor I2C MIO pins. Table 3: PS PMOD to MIO UltrZed SOM Table mapping shows the UART and I2C connections.

- Routed at 50Ω single ended.
- The interface follows, as close as possible, the Digilent SPI and UART/I2C pinouts.

See page 581 – 583 for TRM pin mapping:

http://www.xilinx.com/support/documentation/user_guides/ug1085-zynq-ultrascale-trm.pdf

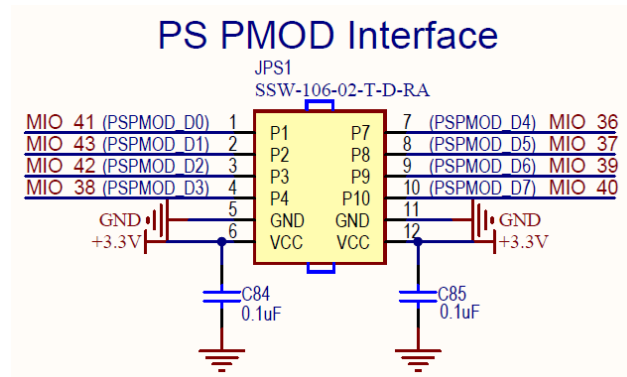


Figure 13 – PS PMOD

IO Name	TRM SPI0	TRM I2C0	TRM I2C1	TRM UART0	TRM UART1	Net Name	JX3 Connector
PS_MIO36			SCL		TXD	MIO36_PMOD	JX3.81
PS_MIO37			SDA		RXD	MIO37_PMOD	JX3.82
PS_MIO38	SCLK	SCL		RXD		MIO38_PMOD	JX3.85
PS_MIO39	N_SS[2]	SDA		TXD		MIO39_PMOD	JX3.86
PS_MIO40	N_SS[1]		SCL		TXD	MIO40_PMOD	JX3.87
PS_MIO41	N_SS[0]		SDA		RXD	MIO41_PMOD	JX3.88
PS_MIO42	MISO	SCL		RXD		MIO42_PMOD	JX3.89
PS_MIO43	MOSI	SDA		TXD		MIO43_PMOD	JX3.90

Table 3: PS PMOD to MIO UltrZed SOM Table mapping

2.7 PS microUSB Connector (Dual USB-UART Ports) – J11

The dual USB UART port is via a microUSB connector. The PHY interface IC is Silicon Labs CP2105 dual USB-UART device. The port has been configured for persistence, allowing the device to remain enumerated even when the Carrier Card's power is turned off.

- USB 2.0 compliant with royalty free drivers available for download.
- VDD and VIO are attached together to provide a persistent USB connection. When a host PC is attached, VBUS is used to generate VDD. No other board power is needed for the UART to be turned on. When the board is in the powered off state, no +3.3V is present so suspend LEDs D21 and D23 will not turn on until the board is powered on.
- Port 0 is connected to Bank 501 PS MIO[34:35], RXD, TXD and are level translated via MOSFETs. These signals are swapped on the carrier creating a null-modem connection. This allows a straight through cable connection.
- Port 1 is connected to Bank 501 PS MIO[32:33], TXD, RXD and are level translated via MOSFETs. These signals are swapped on the carrier creating a null-modem connection. This allows a straight through cable connection.
- GPIO signals or Modem control signals are not used and are brought out to a test pad for user convenience.
- LEDs: D21 and D23 indicate when the device is in suspend mode. By default the pins are active low during a suspend state. These pins are user programmable, and if desired, the polarity can be reversed allowing the LEDs to be on during normal operation and extinguish during suspend. Please refer to the Silicon Labs CP2105 datasheet for further information.
<https://products.avnet.com/shop/en/ema/uart/cp2105-f01-gmr-3074457345626208393>
- The UART reset pin has an RC time delay from power up. This pin is also be controlled by the SOM's CC_RESET_OUT_N signal.
- A Vendor ID (VID) is not programmed into the OTP ROM. The device uses the default VID provided by Silicon Labs.
- A unique PID (Product ID) can be programmed in via the USB interface by the user. To accomplish this, a 4.7uF cap is required between NC/DCD_ECI/VPP pin and ground as shown below. Upon completion of programming, the capacitor should be removed.
- ESD device D22 is used on the USB D+ and D- lines for ESD protection.
- Impedance is 45Ω single ended control, 90Ω differential.

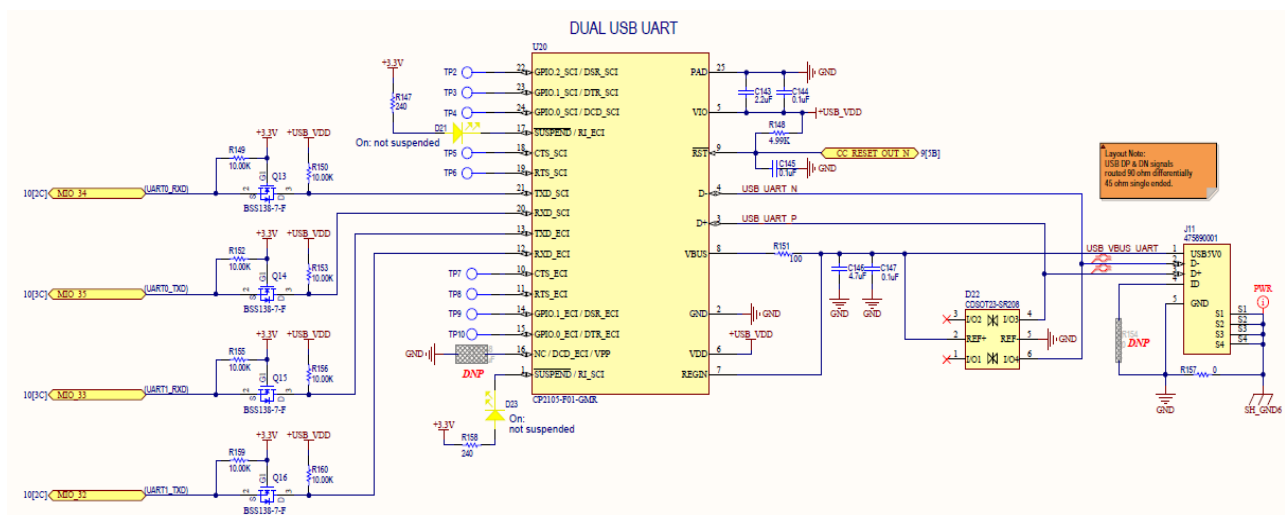


Figure 14 – Dual USB UART

IOCC Net Name:	UART Signal Name:	JX3 Pin #:
MIO_32	MIO_32.UART1_TXD	77
MIO_33	MIO_33.UART1_RXD	78
MIO_34	MIO_34.UART0_RXD	79
MIO_35	MIO_35.UART0_TXD	80

Table 4: UART Table

2.8 PS microSD Card Connector – J4

The PS MIO[44:51] pins are used to interface to a micro-SD card connector. The interface operates at 3.3V. Since microSD cards do not have a Write-Protect (WP) pin, the PS SD controller WP signal (MIO[44]) must be pulled up to the 3.3V rail and connected to ground via a jumper on the UltraZed IO Carrier Card.

- JP2 WP Jumper used to allow Write Protect emulation for microSD cards if needed. The default position for this jumper is Not Placed, thereby disabling Write Protect function.
- The interface is routed at 50 ohms single ended.

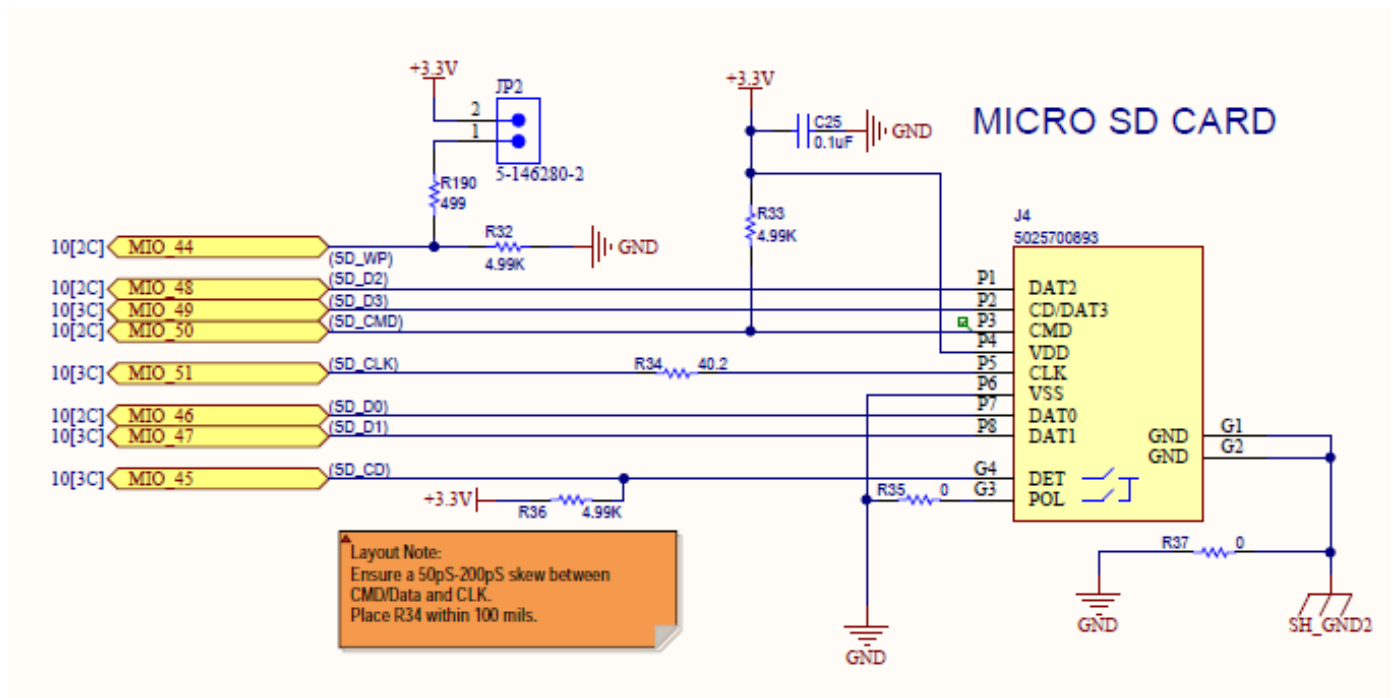


Figure 15 – Micro SD Card interface

IOCC Net Name:	J4 Signal Name:	JX3 Pin #:
MIO_44	SD_WP	93
MIO_45	SD_CD	94
MIO_46	SD_D0	95
MIO_47	SD_D1	96
MIO_48	SD_D2	97
MIO_49	SD_D3	98
MIO_50	SD_CMD	99
MIO_51	SD_CLK	100

Table 5: PS microSD card table

2.9 PS User Push Switch – SW5

The UltraZed IO Carrier Card provides a +1.8V PS active high user push button switch. The switch is connected to MIO[26] pin. When not depressed, the output is pulled low via a 10K ohm resistor. A decoupling capacitor is also added to help minimize switch bounce.

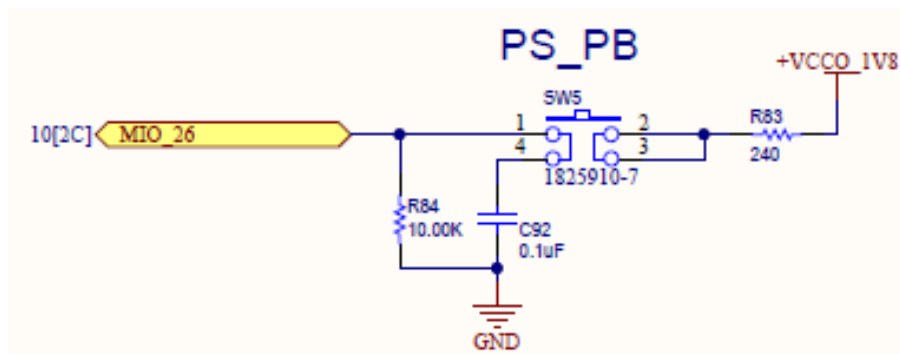


Figure 16 – User PS Push Button switch

2.10 PS User LED – D15

A red PS user LED is provided on the carrier. It is an active high LED and buffered with a NPN BJT. This LED is connected to the MIO[31] pin and operated at 3.3V I/O.

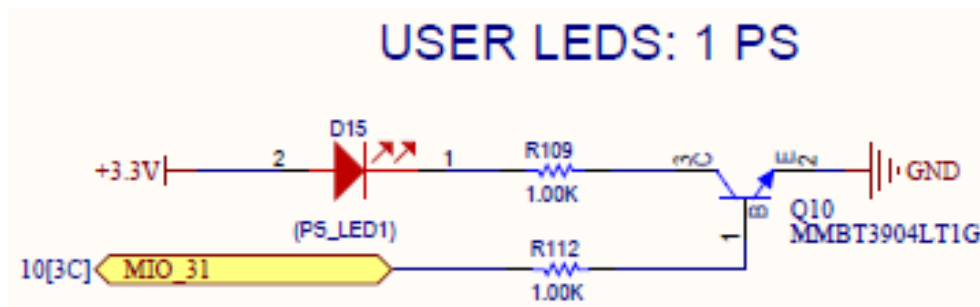


Figure 17 – PS User LED

2.11 PL User Switches, SW1 - SW4 & SW6

The Carrier Card has 12 user switches. Four pushbutton switches SW1-SW4, and an 8 pin DIP slide switch, SW6.

- SW1 – SW4 pushbutton switches are normally open when not depressed and are pulled low via RP1, a 10K resistor pack. When SW1 – SW4 are depressed, they provide a 1.8V signal. These signals are decoupled using a 0.1uF capacitor.
- When slid to the ON position (closed), SW6 outputs are pulled high to a logic level of +1.8V via a current limiting resistor pack. When in the OFF position (open), SW6 outputs are pulled low via a 4.7K resistor pack.

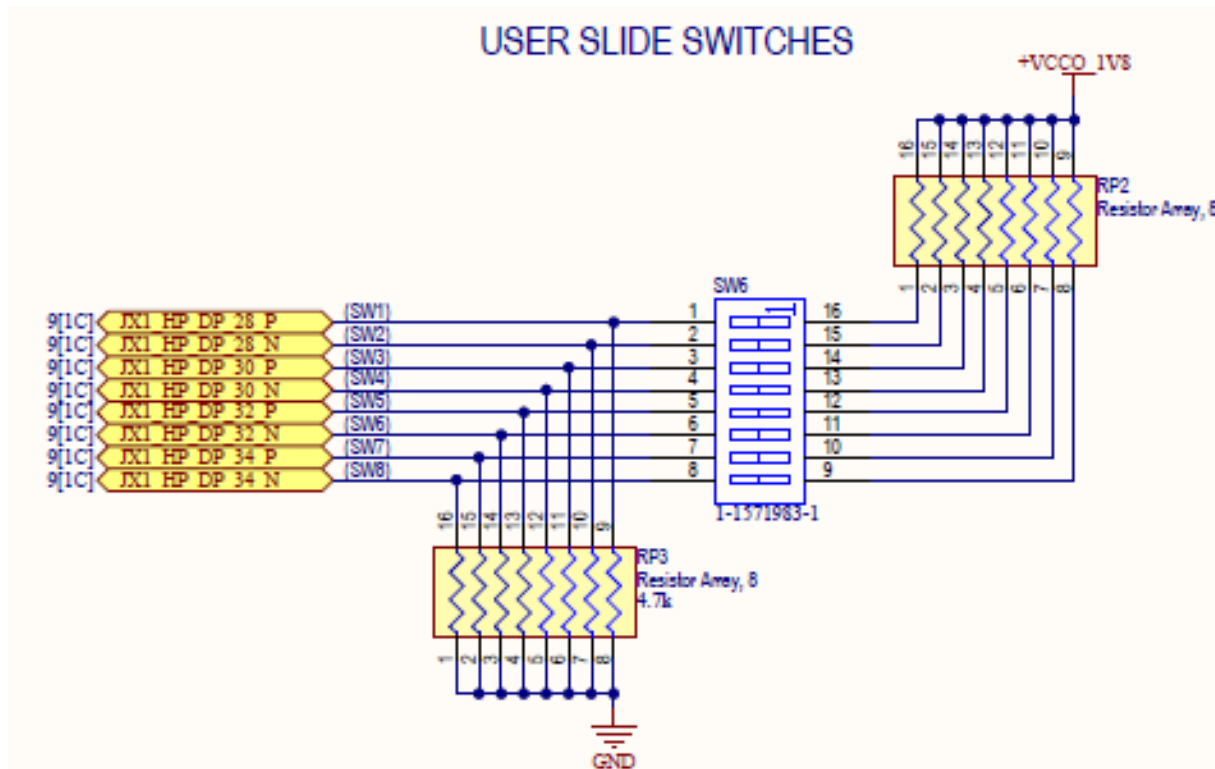


Figure 18 – PL user 8 position slide switch

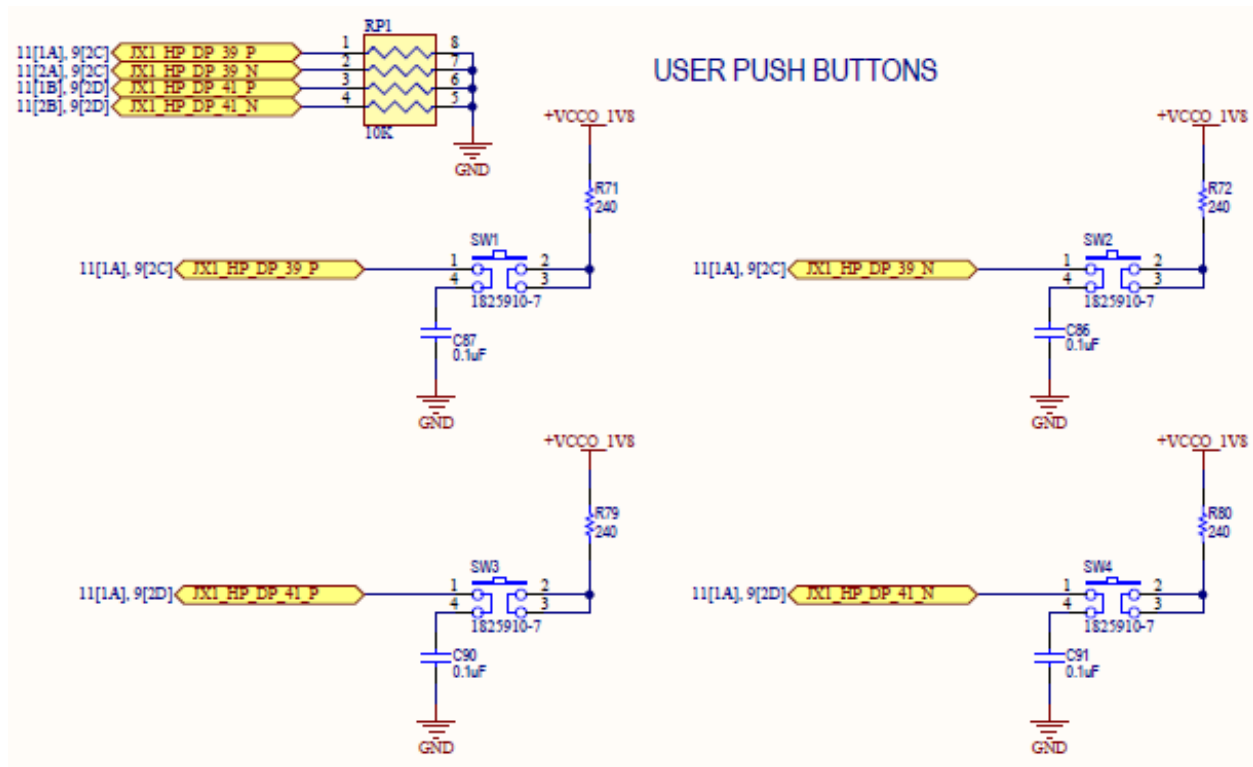


Figure 19 – PL user 4 push button switches

IOCC Net Name:	JX1 Pin #:
JX1_HP_DP_28_P	93
JX1_HP_DP_28_N	95
JX1_HP_DP_30_P	99
JX1_HP_DP_30_N	101
JX1_HP_DP_32_P	105
JX1_HP_DP_32_N	107
JX1_HP_DP_34_P	111
JX1_HP_DP_34_N	113
JX1_HP_DP_39_P	122
JX1_HP_DP_39_N	124
JX1_HP_DP_41_P	128
JX1_HP_DP_41_N	130

Table 6: PL User Switch Table

2.12 PL User LEDs – D7:D8, D11:D14, D16:D17

The UltraZed IO Carrier Card provides 8 PL user LEDs. These active high LEDs are connected to a HP bank via JX1 connector and operated at 1.8V I/O. These LEDs are buffered with NPN BJTs to minimize the current sourced by the FPGA.

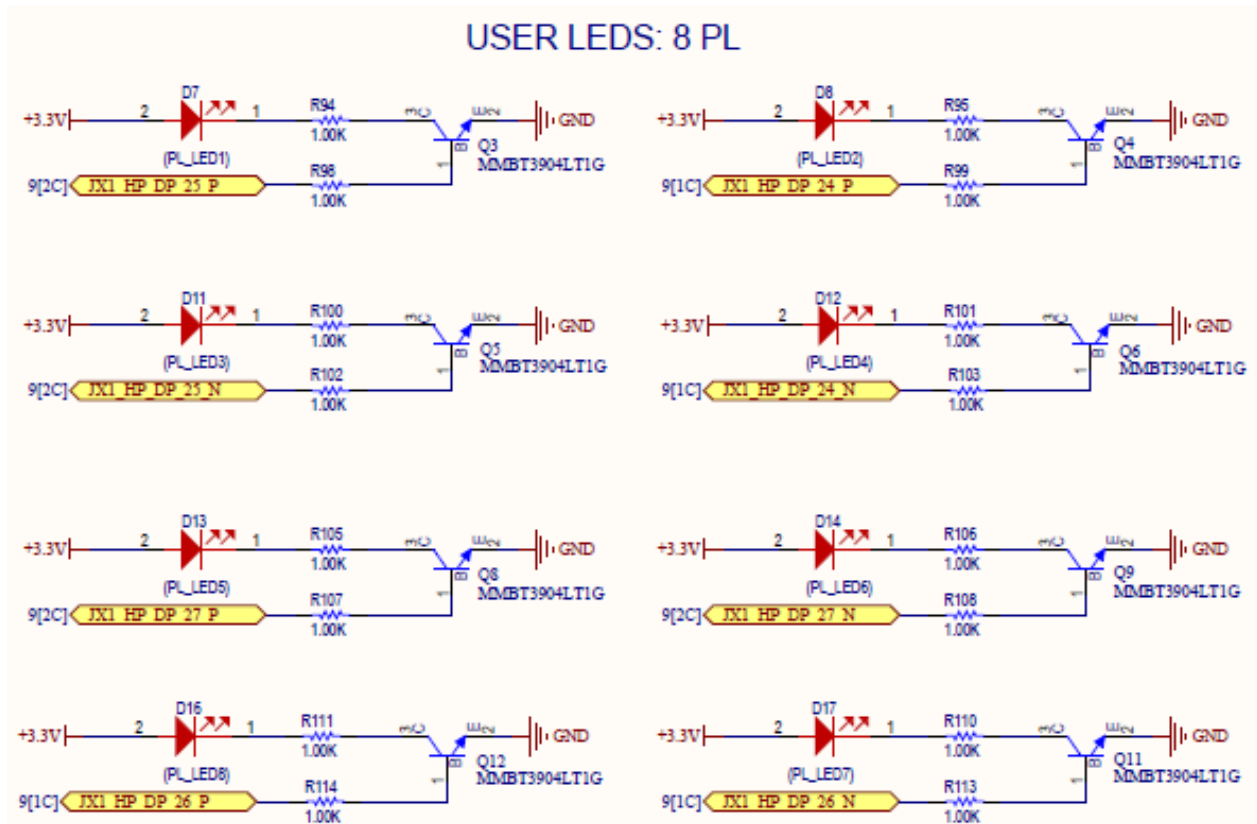


Figure 20 – PL User LEDs

IOCC Net Name:	JX1 Pin #:
JX1_HP_DP_24_P	81
JX1_HP_DP_24_N	83
JX1_HP_DP_25_P	80
JX1_HP_DP_25_N	82
JX1_HP_DP_26_P	87
JX1_HP_DP_26_N	89
JX1_HP_DP_27_P	86
JX1_HP_DP_27_N	88

Table 7: PL user LED table

2.13 PL PMOD Headers – JX1, JA1:JA6

The UltraZed IO Carrier Card has 12 PL PMOD headers with dual-PMOD connections. Six of the PMODs are attached to JX1 header, and the other six attached to the JX2 header. The PMOD interface operates at 3.3V while the SOM I/O is 1.8V. A 1.8V to 3.3V voltage translator TXS0108EPWR is used to provide high speed level translation. The signals are routed as 50 ohm single-ended signals.

- Bank 64 and 65, VCCO_HP_64/65 (1.8V)
- Uses the lower JX1_HP_DP_xx_P/N signals starting at JX1_HP_DP_00_P/N and ending at JX1_HP_DP_23_P/N.
- The PMOD connectors are paired together as follows:
 - JA1-JA2, JA3-JA4, JA5-JA6
 - This pairing allows each set of connectors to be closely routed, ensuring minimal timing skew between them.
- All JX1 PMOD signals are routed to within 10 mils within the single connector.
- All JX1 PMOD connector signals are routed within 25 mils of each other per pair.
- All JX1 PMOD signals are routed to within 3000 mils of each other throughout the entire bank of six connectors.
- All JX1 PMOD signals total route length are less than 6000 mils from the JX1 connector.
- All PMOD signals are Single Ended and routed at 50 ohms nominal impedance.

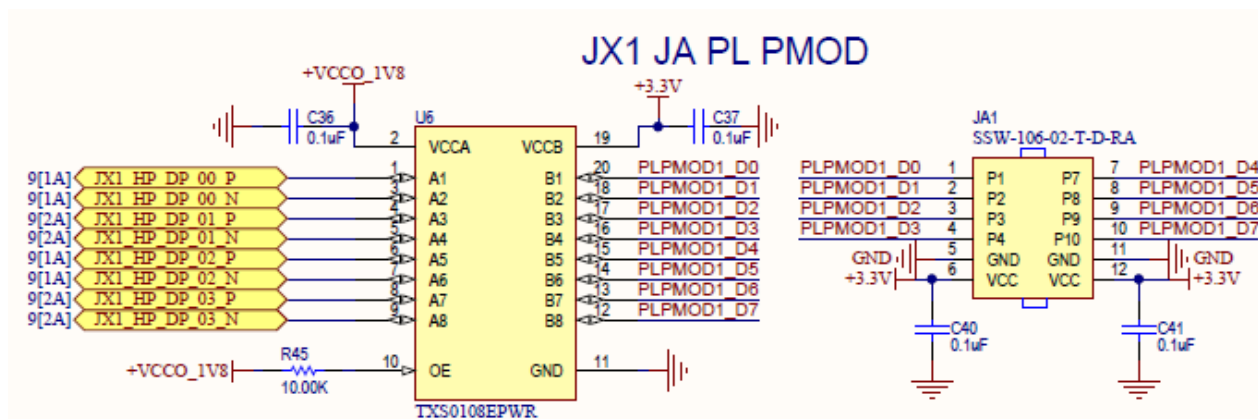


Figure 21 – JX1 PL PMOD x6

IOCC Net Name:	JX1 Pin #:	PMOD PIN #
JX1_HP_DP_00_P	9	1
JX1_HP_DP_00_N	11	2
JX1_HP_DP_01_P	8	3
JX1_HP_DP_01_N	10	4
JX1_HP_DP_02_P	15	7
JX1_HP_DP_02_N	17	8
JX1_HP_DP_03_P	14	9
JX1_HP_DP_03_N	16	10
JX1_HP_DP_04_P	21	1
JX1_HP_DP_04_N	23	2
JX1_HP_DP_05_P	20	3
JX1_HP_DP_05_N	22	4
JX1_HP_DP_06_P	27	7
JX1_HP_DP_06_N	29	8
JX1_HP_DP_07_P	26	9
JX1_HP_DP_07_N	28	10
JX1_HP_DP_08_P	33	1
JX1_HP_DP_08_N	35	2
JX1_HP_DP_09_P	32	3
JX1_HP_DP_09_N	34	4
JX1_HP_DP_10_P	39	7
JX1_HP_DP_10_N	41	8
JX1_HP_DP_11_P	38	9
JX1_HP_DP_11_N	40	10
JX1_HP_DP_12_P	45	1
JX1_HP_DP_12_N	47	2
JX1_HP_DP_13_P	44	3
JX1_HP_DP_13_N	46	4
JX1_HP_DP_14_P	51	7
JX1_HP_DP_14_N	53	8
JX1_HP_DP_15_P	50	9
JX1_HP_DP_15_N	52	10
JX1_HP_DP_16_P	57	1
JX1_HP_DP_16_N	59	2
JX1_HP_DP_17_P	56	3
JX1_HP_DP_17_N	58	4
JX1_HP_DP_18_P	63	7
JX1_HP_DP_18_N	65	8
JX1_HP_DP_19_P	62	9
JX1_HP_DP_19_N	64	10
JX1_HP_DP_20_P	69	1

IOCC Net Name:	JX1 Pin #:	PMOD PIN #
JX1_HP_DP_20_N	71	2
JX1_HP_DP_21_P	68	3
JX1_HP_DP_21_N	70	4
JX1_HP_DP_22_P	75	7
JX1_HP_DP_22_N	77	8
JX1_HP_DP_23_P	74	9
JX1_HP_DP_23_N	76	10

Table 8: JX1 PL PMOD pin table

2.14 PL PMOD Headers – JX2, JA7:JA12

The UltraZed IO Carrier Card has 12 PL PMOD headers with dual-PMOD connections. Six of the PMODs are attached to JX1 header, and the other six attached to the JX2 header. The PMOD interface operates at 3.3V while the SOM I/O is 1.8V. A 1.8V to 3.3V voltage translator TXS0108EPWR is used to provide high speed level translation. The signals are routed as 50 ohm single-ended signals.

- Bank 65 and 66, VCCO_HP_64/65 (1.8V)
- Uses the lower JX2_HP_DP_xx_P/N signals starting at JX2_HP_DP_00_P/N and ending at JX2_HP_DP_23_P/N.
- The PMOD connectors are paired together as follows:
 - JA7-JA8, JA9-JA10, JA11-JA12
 - This pairing allows each set of connectors to be closely routed, ensuring minimal timing skew between them.
- All JX2 PMOD signals are routed to within 10 mils within the single connector.
- All JX2 PMOD connector signals are routed within 25 mils of each other per pair.
- All JX2 PMOD signals are routed to within 3000 mils of each other throughout the entire bank of six connectors.
- All JX2 PMOD signals total route length are less than 6000 mils from the JX1 connector.
- All PMOD signals are Single Ended and routed at 50 ohms nominal impedance.

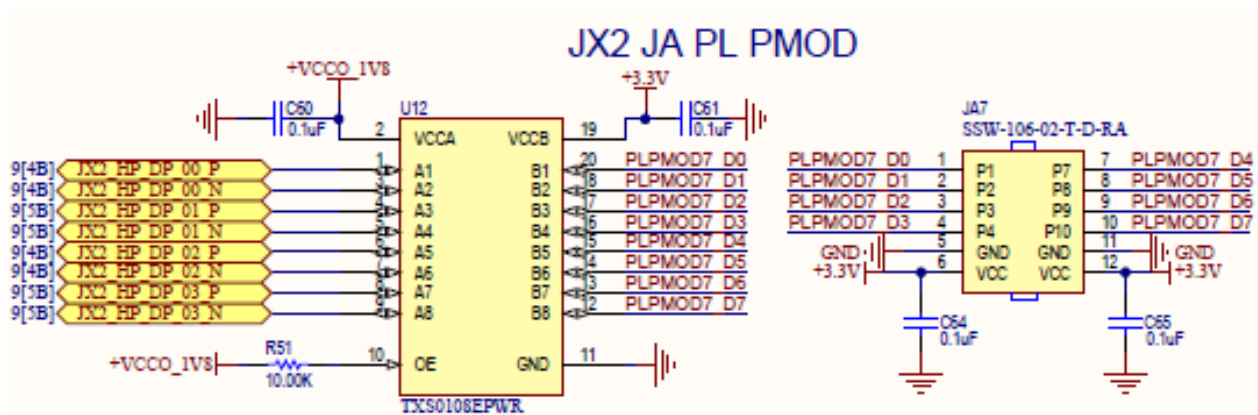


Figure 22 – JX2 PL PMOD x6

IOCC Net Name:	JX2 Pin #:	PMOD PIN #
JX2_HP_DP_00_P	45	1
JX2_HP_DP_00_N	47	2
JX2_HP_DP_01_P	44	3
JX2_HP_DP_01_N	46	4
JX2_HP_DP_02_P	51	7
JX2_HP_DP_02_N	53	8
JX2_HP_DP_03_P	50	9
JX2_HP_DP_03_N	52	10
JX2_HP_DP_04_P	57	1
JX2_HP_DP_04_N	59	2
JX2_HP_DP_05_P	56	3
JX2_HP_DP_05_N	58	4
JX2_HP_DP_06_P	63	7
JX2_HP_DP_06_N	65	8
JX2_HP_DP_07_P	62	9
JX2_HP_DP_07_N	64	10
JX2_HP_DP_08_P	69	1
JX2_HP_DP_08_N	71	2
JX2_HP_DP_09_P	68	3
JX2_HP_DP_09_N	70	4
JX2_HP_DP_10_P	75	7
JX2_HP_DP_10_N	77	8
JX2_HP_DP_11_P	74	9
JX2_HP_DP_11_N	76	10
JX2_HP_DP_12_P	81	1
JX2_HP_DP_12_N	83	2
JX2_HP_DP_13_P	80	3
JX2_HP_DP_13_N	82	4
JX2_HP_DP_14_P	87	7
JX2_HP_DP_14_N	89	8
JX2_HP_DP_15_P	86	9
JX2_HP_DP_15_N	88	10
JX2_HP_DP_16_P	93	1
JX2_HP_DP_16_N	95	2
JX2_HP_DP_17_P	92	3
JX2_HP_DP_17_N	94	4
JX2_HP_DP_18_P	99	7
JX2_HP_DP_18_N	101	8
JX2_HP_DP_19_P	98	9
JX2_HP_DP_19_N	100	10
JX2_HP_DP_20_P	105	1

IOCC Net Name:	JX2 Pin #:	PMOD PIN #
JX2_HP_DP_20_N	107	2
JX2_HP_DP_21_P	104	3
JX2_HP_DP_21_N	106	4
JX2_HP_DP_22_P	111	7
JX2_HP_DP_22_N	113	8
JX2_HP_DP_23_P	110	9
JX2_HP_DP_23_N	112	10

Table 9: JX2 PL PMOD pin table

2.15 PL Arduino Connectors, CON1:CON4

An Arduino interface has been included on the Carrier Card. This interface supports +3.3V Arduino R3 shields and includes an analog or digital select jumper for the six analog pins. The connector pin assignments are as follows (UltraZed SOM HD bank is dedicated to the Arduino shield expansion slot):

- CON1 – 8 HD I/O (3.3V) via JX2 connector
- CON2 – 8 HD I/O (3.3V) via JX2 connector, includes I2C capability on pins 9 and 10.
- CON3 – power/ground/reset pins.
- CON4 – 6 HD I/O (3.3V with analog capability) via JX2 connector.
- 1 HD I/O (3.3V) via JX2 connector for the reset pin.
- Routed at 50Ω single ended.
- A/D Vref is placed on CON2.8 for the Arduino's A/D reference voltage.
 - A/D reference pre-set to approximately 993mV via a resistor divider. This voltage is set for the SOM's maximum FSV or 1.0 volts.

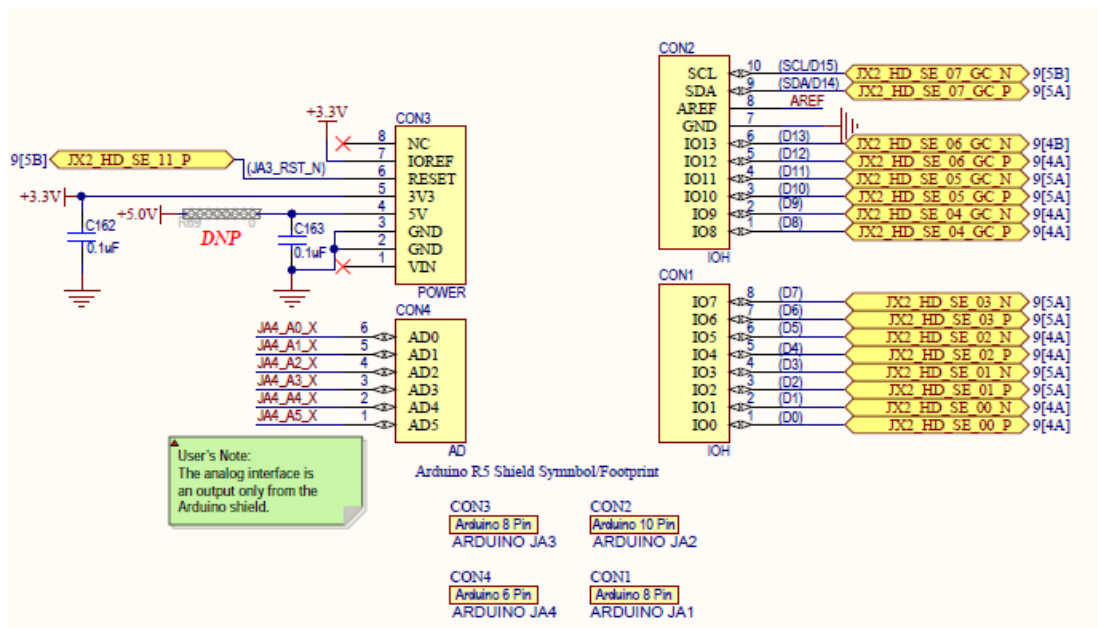


Figure 23 – Arduino Connectors

2.15.1 CON4 (JA4) Analog Switch circuit

The analog and digital switch circuits (U23, U24, U25, Q17) are used to demonstrate a method in which to control analog and digital isolation to/from the SOM & IOCC.

- Digital Mode (default): in digital mode, JP7 is not placed. This enables U25, the TXS translator and disables U23 & U26. In this mode of operation, the digital signals are passed to/from the SOM without any voltage divider scaling (which occurs in analog mode).
- Analog Mode: to use the analog capabilities of the Arduino header, JP7 must be placed. Placing this jumper pulls the 3V_DIG_EN signal low thereby disabling U25 and enabling analog switches U23 and U26.
- Placing JP7 connects CON4's analog signals JA4_A0_X through JA4_A5_X to the SOM via scaling resistors. the scaling resistors, ie R171/R172 etc... are used to divide CON4 analog output signals from +3.3V FSV to ~0.994V FSV.
- Going in the opposite direction, from the SOM to the Arduino, these resistors do not provide division, nor are they required to because the SOM digital I/O interface is at the same value as the Arduino digital interface.

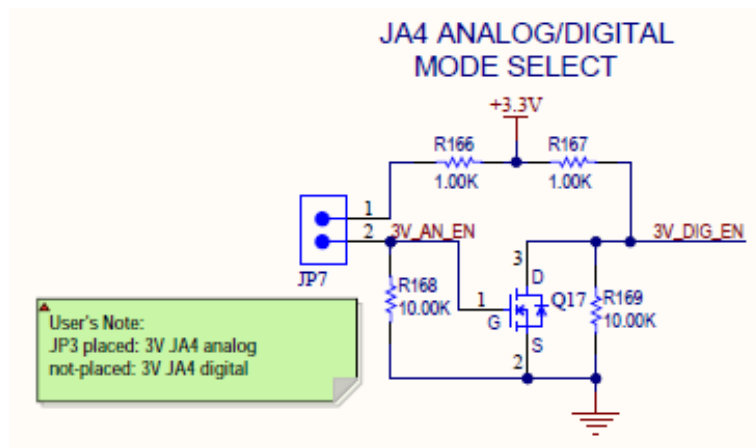


Figure 24 – CON4 (JA4) Analog/Digital select circuit

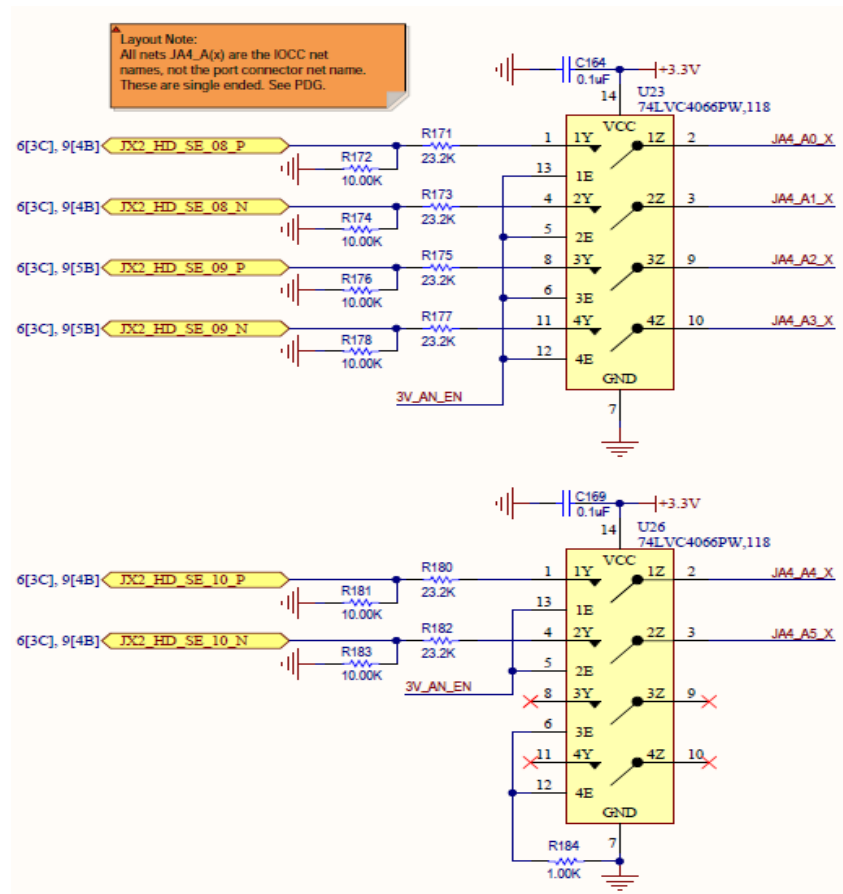


Figure 25 – Arduino Analog switches

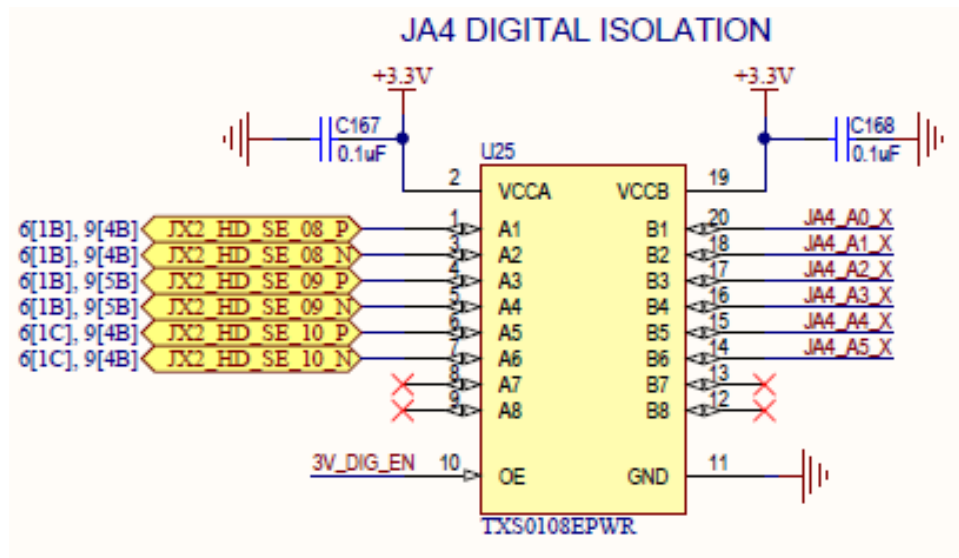


Figure 26 – Arduino Analog switches

SOM Net Name:	CONN1- 4 Signal Names:	JX2 Pin #:
JX2_HD_SE_00_P	JA1_D0	7
JX2_HD_SE_01_P	JA1_D1	8
JX2_HD_SE_00_N	JA1_D2	9
JX2_HD_SE_01_N	JA1_D3	10
JX2_HD_SE_02_P	JA1_D4	13
JX2_HD_SE_03_P	JA1_D5	14
JX2_HD_SE_02_N	JA1_D6	15
JX2_HD_SE_03_N	JA1_D7	16
JX2_HD_SE_04_P_GC	JA2_D8	19
JX2_HD_SE_05_P_GC	JA2_D9	20
JX2_HD_SE_04_N_GC	JA2_D10	21
JX2_HD_SE_05_N_GC	JA2_D11	22
JX2_HD_SE_06_P_GC	JA2_D12	25
JX2_HD_SE_07_P_GC	JA2_D13	26
JX2_HD_SE_06_N_GC	JA2_SDA_D14	27
JX2_HD_SE_07_N_GC	JA2_SCL_D15	28
JX2_HD_SE_08_P	JA4_A0	31
JX2_HD_SE_08_N	JA4_A1	33
JX2_HD_SE_09_P	JA4_A2	32
JX2_HD_SE_09_N	JA4_A3	34
JX2_HD_SE_10_P	JA4_A4	37
JX2_HD_SE_10_N	JA4_A5	39
JX2_HD_SE_11_P	JA3_RST_N	38

Table 10: JA1-JA4 Arduino interface table

2.16 Carrier Card I2C Interface

The UltraZed SOM provides a master I2C bus (CC_SDA, CC_SCL, and CC_INT_N) to the IO Carrier Card via the JX3 connector so that software can communicate with all I2C devices on the UltraZed SOM as well as the I2C devices on the IO Carrier Card using a single I2C interface.

- U1, IDT clock synthesizer, 0xD4 or 0xD0
- U5, MAC ID EEPROM, 0xA2

The CC_SDA, CC_SCL, and CC_INT_N pins are pulled up to the 1.8V rail via 1K resistors on the UltraZed IO Carrier Card. Although a Carrier Card can assert the active low CC_INT signal to interrupt the MPSoC processor, this signal is not used on the IO Carrier Card but is routed to a test point.

- The CC_INT_N pin is routed to JX3.68 attached to TP1.

The I2C interface is used to access the following Carrier Card devices:

- U1, the IDT differential clock generator at address 0xD4.
- U5, the MAC Address device at address 0xA2.

- The I2C interface pullup resistor values are 1K for 400 KHz operation. The 1K value has been proven to be necessary when I2C bus is attached to U1. While this deviates from the standard I2C pullup value of 2K value it causes no detrimental effects to the project.
- Routed impedance is 50Ω.

IOCC Net Name:	JX3 Pin #:
CC_SDA	41
CC_SCL	44
CC_INT_N	68

Table 11: I2C bus connections

2.17 Clock Generator – U1, I2C address 0xD4 (default)

The Carrier Card has a pre-programmed IDT 5P49V5935B521LTGI synthesizer on board. This clock IC generates the necessary LVDS clocks for the interfaces listed below. This part contains an internal 25 MHz crystal clock source which eliminates the need for an external clock. The part is capable of providing multiple clock frequencies, output types, spread spectrum, phase shift control and slew rate control.

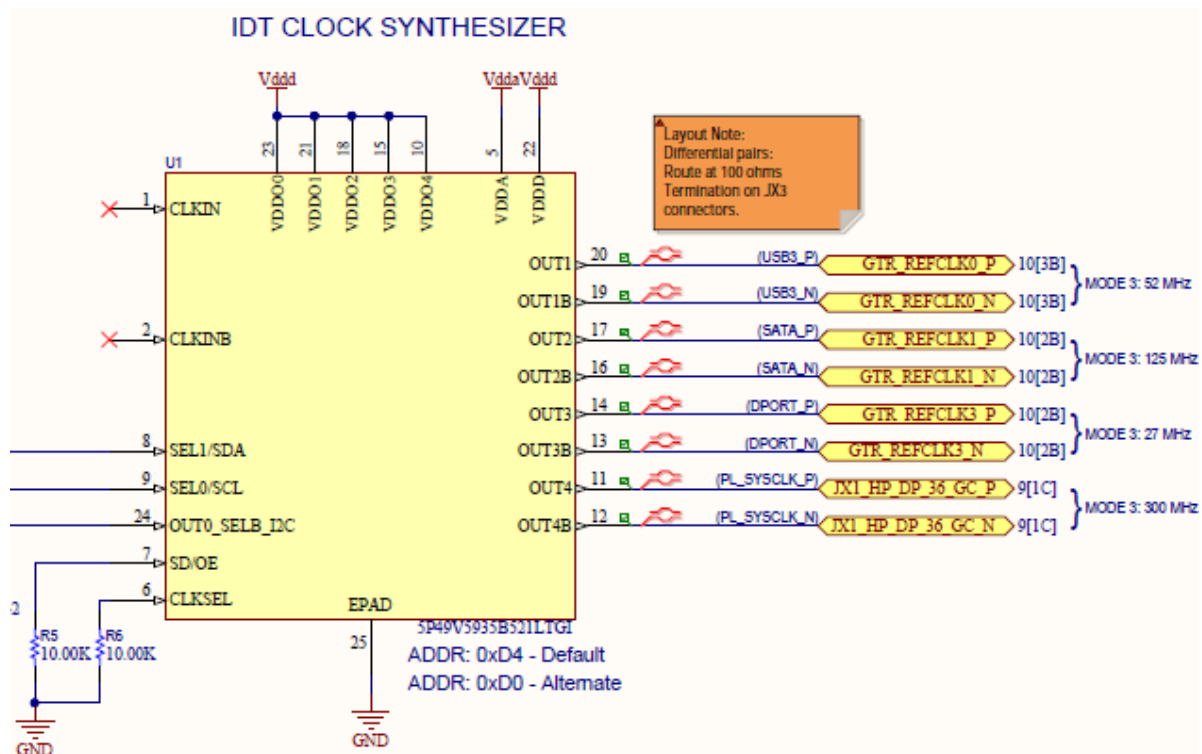
The IDT 5P49V5935B521LTGI is a custom part number with the output frequencies pre-programmed into the device via an OTP register. The device runs at 1.8V. In the default configuration (Mode 3), the clock generates the following frequencies on power up.

Default U1 configurations:

- 1.8V power
- Spread Spectrum: off
- Reference clock: 25 MHz internal
- Phase Shift: 0 degrees
- Output type: LVDS
- Slew Rate: set to 1.0x

Default (Mode 3) output frequencies:

- Output 0 – Used for configuration only.
- Output 1 – 52MHz USB 3.0 clock connected to the JX3 GTR_REFCLK[0]
- Output 2 – 125MHz GTR[1] clock connected to the JX3 GTR_REFCLK[1]
- Output 3 – 27 MHz Display Port clock connected to the JX3 GTR_REFCLK[3]
- Output 4 – 300MHz PL system clock connected to the JX1 (Global Clock Input pair).



IOCC Net Name:	JX Pin #:
GTR_REFCLK0_P	JX3.38
GTR_REFCLK0_N	JX3.40
GTR_REFCLK1_P	JX3.33
GTR_REFCLK1_N	JX3.35
GTR_REFCLK3_P	JX3.27
GTR_REFCLK3_N	JX3.29
JX1_HP_DP_36_GC_P	JX1.117
JX1_HP_DP_36_GC_N	JX1.119

Table 12: Clock outputs

2.17.1 Clock Configuration connectors JP1, J1, J2

The synthesizer has two methods of configuration: hardware and software. For hardware operation it is configured via J1, J2 and JP1. These jumpers select one of four pre-programmed OTP configuration files during power up, see Table 13: Clock boot configuration table for the other jumper configurable frequencies.

To configure using software, the device must be accessed via the I2C bus and configured each time the board is powered on.

- Mode 3 is the default frequency selection when the board is manufactured. Mode three jumper positions are as follows: J1 and J2 placed on pins 1-2 and JP1 is not placed.
- I2C software configuration mode: the user can configure the IDT part using the I2C bus. To configure the IDT part for different frequencies, J1 and J2 jumpers must be placed at positions 2 – 3 and jumper JP1 removed.

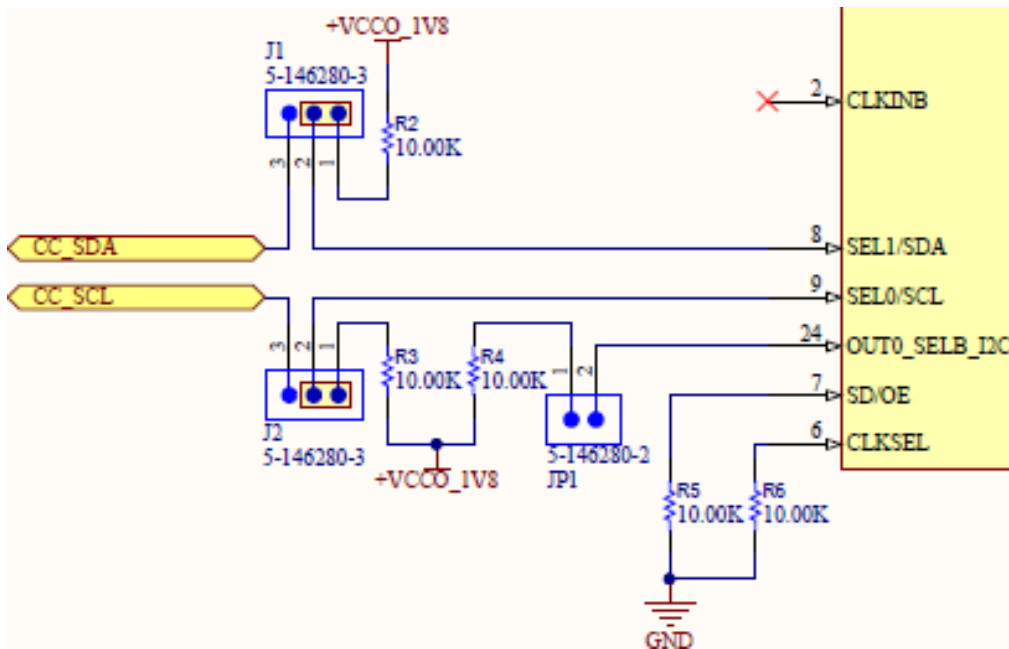


Figure 28 – IDT Clock Synthesizer configuration jumpers

Parameter	Configuration 0	Configuration 1	Configuration 2	Configuration 3	Units
Input	25	25	25	(Default Config)	MHz
Output 0	25	25	25	25	MHz
Output 1	40	48	50	52	MHz
Output 2	125	125	125	125	MHz
Output 3	27	27	27	27	MHz
Output 4	300	300	300	300	MHz

Table 13: Clock boot configuration table

2.18 MAC Address Device – I2C Device 0xA2

The UltraZed IO Carrier Card has a 1.8V MicroChip 24AA025E48T-I/OT I2C MAC Address device utilizing EUI-48™. This device is connected to the master I2C bus on the Carrier Card. The address can be configured via JT1 and JT2 (0402 SMT resistor pads). The default position is 4.7K ohm resistors placed at locations 2 – 3, yielding a default address set of 0xA2.

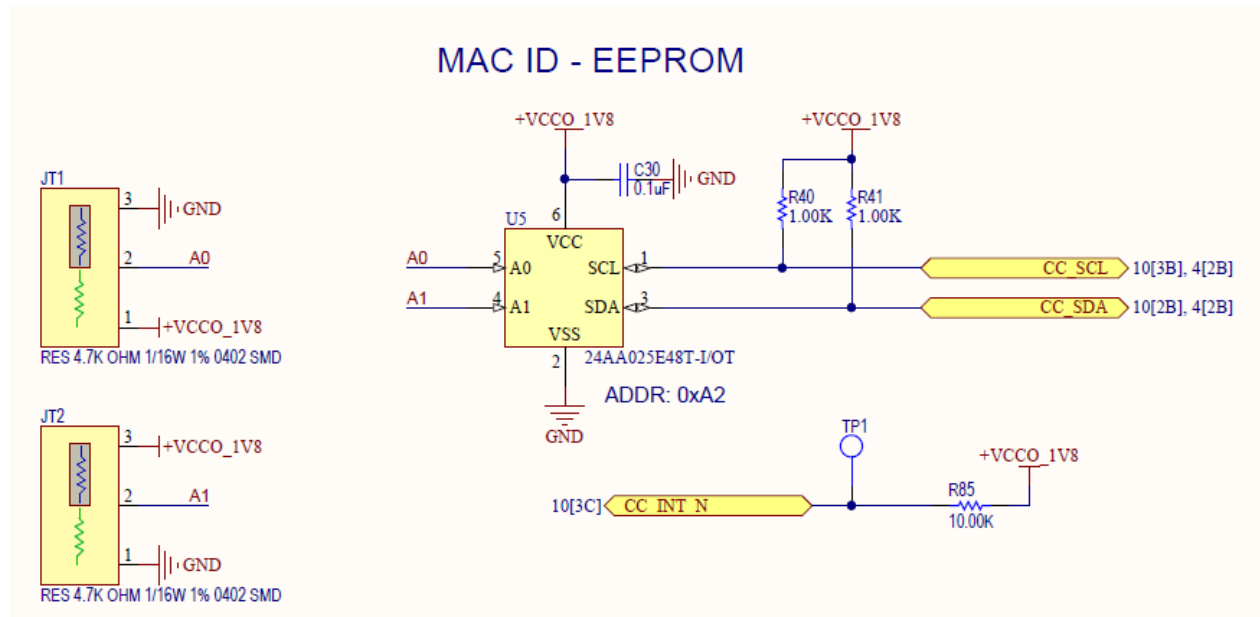


Figure 29 – 2K MAC EUI-48 EEPROM

2.19 SOM Reset Input – SW7

SW7 is a push switch used to generate an active low SOM_RST_N signal. This signal is routed to the SOM via JX2.42 and also to J6, the PC4 JTAG header for JTAG_INIT signal. This signal is floating on the IOCC and is pulled up on the SOM via the +1.8V rail.

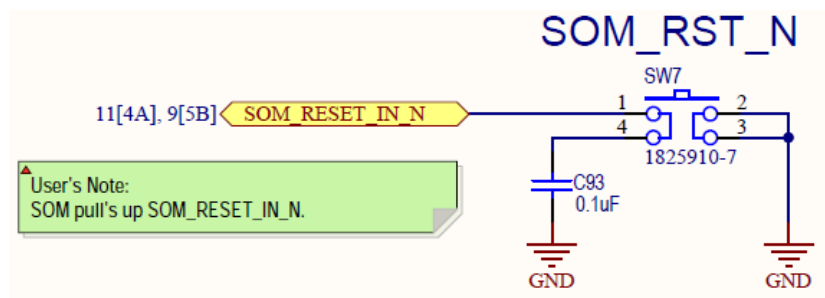


Figure 30 – SOM_RST_N circuit

2.20 SOM Reset Output – TP11

The UltraZed SOM drives an active low reset signal to the Carrier Card (CC_RESET_OUT_N) via JX2 connector at TP11. This signal is pulled up on the SOM via a 10K resistor tied to +1.8V. This signal can be monitored by the user via TP11.

2.21 JTAG Debug Interfaces

The UltraZed IO Carrier Card contains two JTAG debug interfaces to allow maximum development flexibility. One is a Digilent SMT2 JTAG module with a micro USB connection. This interface only requires a micro USB cable. No other dongles or adapters are needed. To support all development environments, including those with debuggers and dongles, a PC4 2x7 header has also been provided.

Either interface can be used for PS software debugging and UltraZed SOM PL configuration, QSPI Flash and eMMC memory programming.

2.21.1 PC4 JTAG Header – J6

The PC4 JTAG header is shown below. The PC4 header VREF pin is connected to the 1.8V rail via D6. The diode is used to prevent back drive onto the 1.8V rail from the JTAG pod.

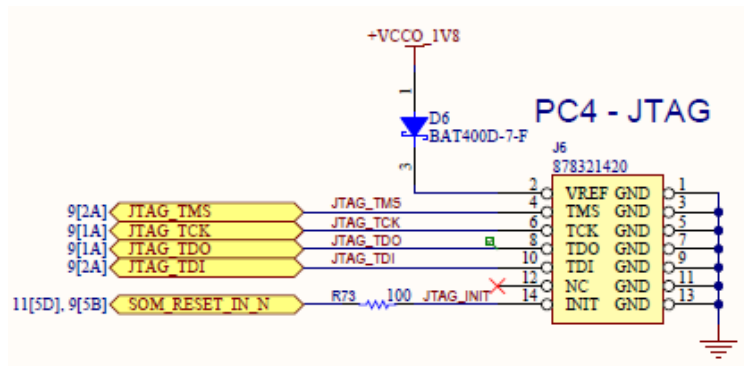


Figure 31 – PC4 JTAG Connector

2.21.2 SMT2 MicroUSB JTAG interface – U18

The SMT2 micro USB to JTAG interface is shown below. The 4.70K pullup resistors and 22.1 series termination resistors are placed as close as possible to U18 for signal integrity purposes.

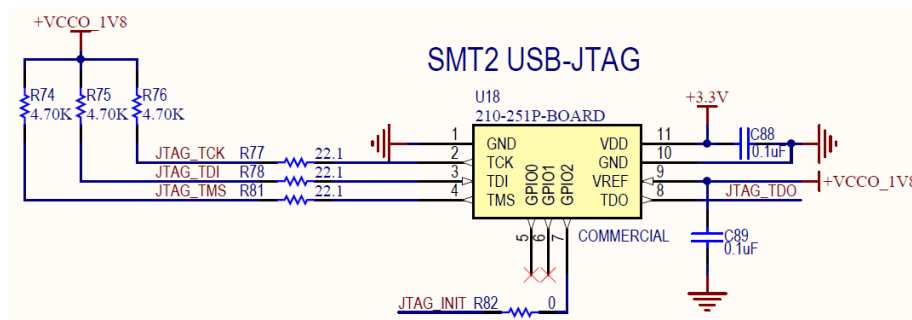


Figure 32 – PC4 JTAG Connector

IOCC Net Name:	JX1 Pin #:
JTAG_TCK	1
JTAG_TMS	2
JTAG_TDO	3
JTAG_TDI	4

Table 14: JTAG connections

2.22 LVDS Touch Panel Interface – P1

The UltraZed IO Carrier Card has an Avnet LVDS Touch Panel interface. For ease of use, software references and rapid development time, Avnet recommends the following 10 inch touch panel kit: <http://picozed.org/product/10-inch-touch-display-kit>

The touch panel's I2C interface is level translated from +3.3V I/O voltage to +1.8V VCCO voltage using a TXS0104EPWR IC.

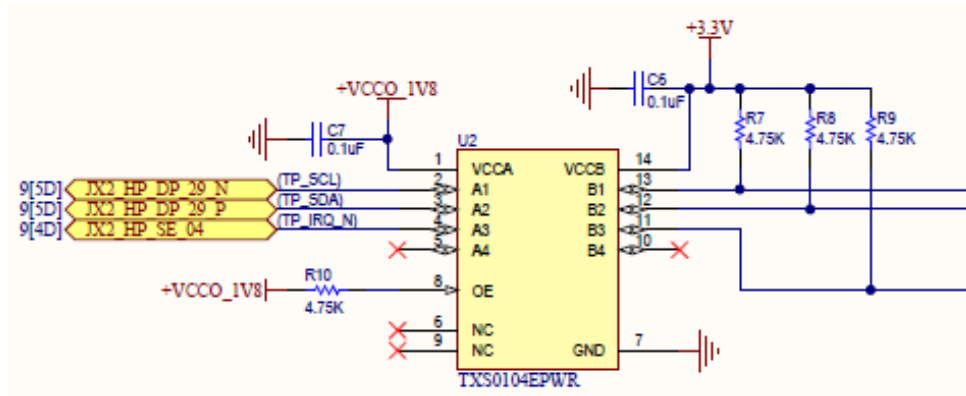


Figure 33 – Touch Panel I2C translator

- Routed at 100Ω differential.
 - Routed 50Ω single ended on control/status signals.
 - Two via transitions or less.
 - No blind or buried vias.
 - Trace length matching to within 10mils pair to pair and do not to exceed 100mils within the group.
- Diode D1 is not populated by default. If the target interface's logic is 1.8V, R11 may be removed and D1 or resistor may be placed, as necessary, to allow 1.8V reference.

IOCC Net Name:	P1 LVDS signal name:	JX2 Pin #:
JX2_HP_DP_24_P	TP_D0_P	117
JX2_HP_DP_24_N	TP_D0_N	119
JX2_HP_DP_25_P	TP_D1_P	116
JX2_HP_DP_25_N	TP_D1_N	118
JX2_HP_DP_26_P_GC	TP_D2_P	123
JX2_HP_DP_26_N_GC	TP_D2_N	125
JX2_HP_DP_27_P_GC	TP_D3_P	122
JX2_HP_DP_27_N_GC	TP_D3_N	124
JX2_HP_DP_28_P	TP_CLK_P	129
JX2_HP_DP_28_N	TP_CLK_N	131
JX2_HP_DP_29P	TP_SDA	128
JX2_HP_DP_29N	TP_SCL	130
JX2_HP_SE_04	IRQ_N	139

Table 15: LVDS Touch Panel pinout

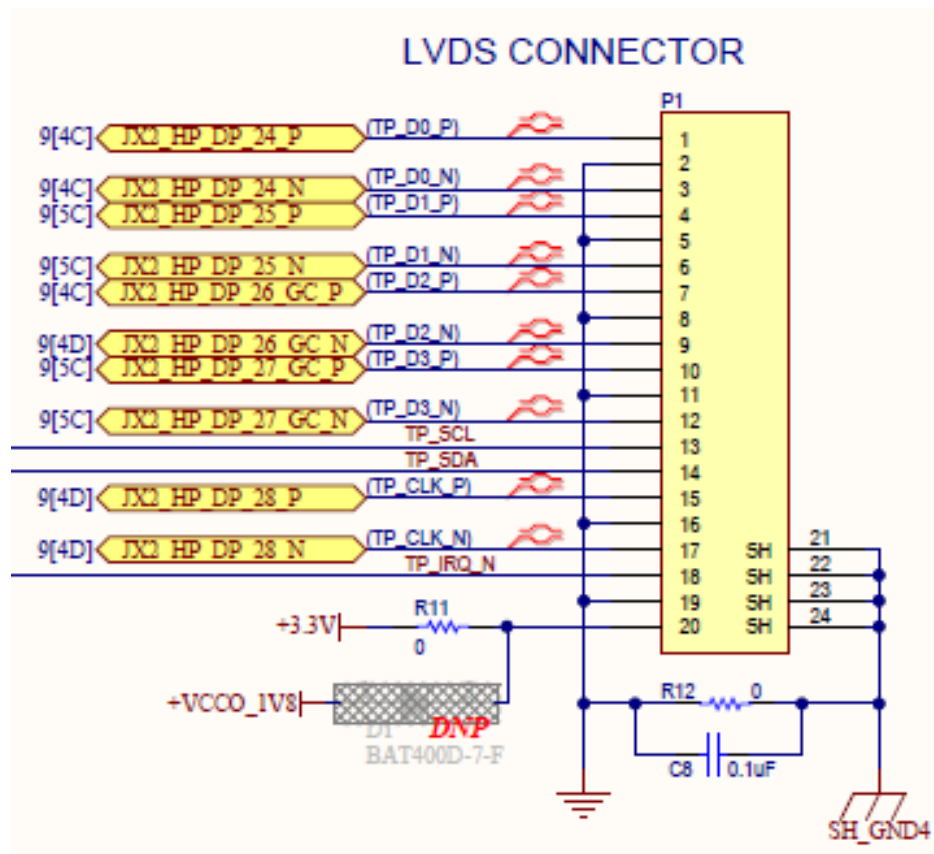


Figure 34 – LVDS Touch Panel connector, P1

2.23 LEDs – Power, Reset

Additional LEDs representing power supply status and reset status are placed on the board. LEDs include:

- Vin Header, D10, (green) – indicates 12V VIN is present.
- PG Module, D9, (green) – indicates the SOM power supply is on and within 10% nominal output.

2.24 Fan Header – JP5

The carrier card provides a dual position fan header for the SOM's cooling fan. The default configuration sources +5.0V to the SOM fan. If a 12V fan is used, FB6 and C149 need to be placed and FB7 removed. A ferrite bead and capacitor are used to minimize fan motor noise coupling to the carrier card's rails. The maximum current for the fan should not exceed 200mA.

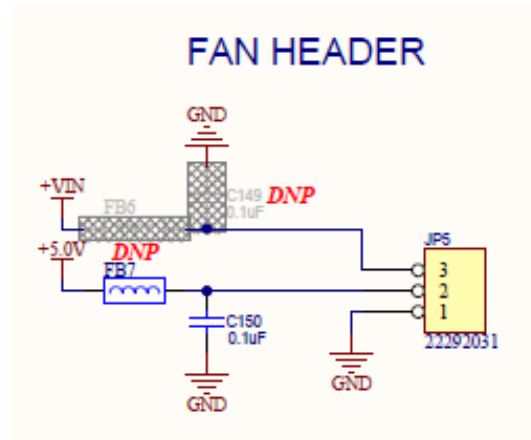


Figure 35 – JP5 Fan Header

2.25 Unused PL I/O

All unused PL I/O pins are looped back on the UltraZed IO Carrier Card PCB design using 0 Ohms resistors for testing. Nets SE 11 and SE 5 are at different voltage levels. To provide the loopback function Q18 level translator has been designed in. Please see Figure 36.

IOCC Net Name:	JX Pin Number:	Looped to via:
JX1_HP_DP_29_P	JX1.92	29 P/N via R58
JX1_HP_DP_29_N	JX1.94	" "
JX1_HP_DP_31_P	JX1.98	31 P/N via R59
JX1_HP_DP_31_N	JX1.100	" "
JX1_HP_DP_33_P	JX1.104	33 P/N via R60
JX1_HP_DP_33_N	JX1.106	" "
JX1_HP_DP_35_P	JX1.110	35 P/N via R62
JX1_HP_DP_35_N	JX1.112	" "
JX1_HP_DP_37_P	JX1.116	37 P/N via R64
JX1_HP_DP_37_N	JX1.118	" "
JX1_HP_DP_38_P	JX1.123	38 P/N via R61
JX1_HP_DP_38_N	JX1.125	" "
JX1_HP_DP_40_P	JX1.129	40 P/N via R63
JX1_HP_DP_40_N	JX1.131	" "
JX1_HP_SE_00	JX1.135	SE 02 via R65
JX1_HP_SE_02	JX1.137	SE 00 " "
JX1_HP_SE_01	JX1.134	SE 03 via R65
JX1_HP_SE_03	JX1.136	SE 01 " "
JX1_HP_SE_04	JX1.139	SE 05 via R67
JX1_HP_SE_05	JX1.138	SE 04 " "
JX2_HP_SE_00	JX2.135	
JX2_HP_SE_01	JX2.134	
JX2_HP_SE_02	JX2.137	
JX2_HP_SE_03	JX2.136	
JX2_HP_SE_05	JX2.138	SE 11 via Q18/ckts
JX2_HD_SE_11_N	JX2.40	SE 05 " "
N/A: Tied to ground	JX3.4	GND
N/A: Tied to ground	JX3.6	GND
N/A: Tied to ground	JX3.10	GND
N/A: Tied to ground	JX3.12	GND
GTR_REFCLK2_P – N.C.	JX3.32	N.C.
GTR_REFCLK2_N – N.C.	JX3.34	N.C.

Table 16: Unused pins table

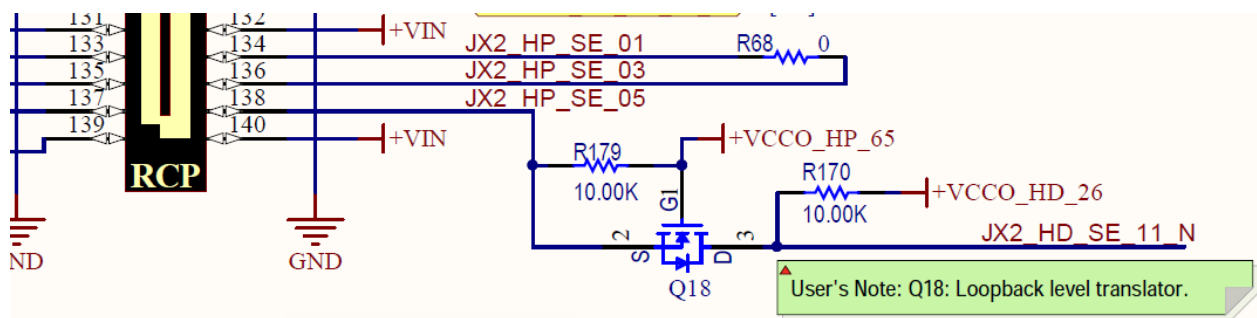


Figure 36 – Q18 loopback level translator

3 Power supplies

3.1 Power jack & switch – J7 & SW8

The Carrier Card uses a six pin ATX style (but not compatible) power jack. The jack is capable of handling in excess of 12V @ 10 Amps. The Avnet “standard” Non-ATX (NATX) power supply is recommended for use with the carrier. The power input to the board is controlled by SW8, an on/off slide switch.

- Input components C99, C101 and L1 are used to reduce spurious EMI emissions during dynamic SOM loads. These components should be used on every carrier design to reduce EMI radiation.
- R187, R188, R189 and C94/C95/C100 are used to create a low pass filter thereby smoothing the input voltage when the system is powered on. During extensive power testing Avnet has discovered some six pin power supplies may have sporadic output voltage “steps” pending the SOM loading. This LPF circuit ensures a smooth and stable power on ramp for the carrier and SOM.

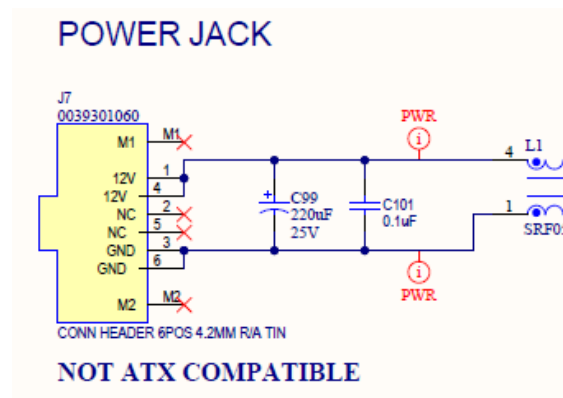


Figure 37 – Power input jack, J7

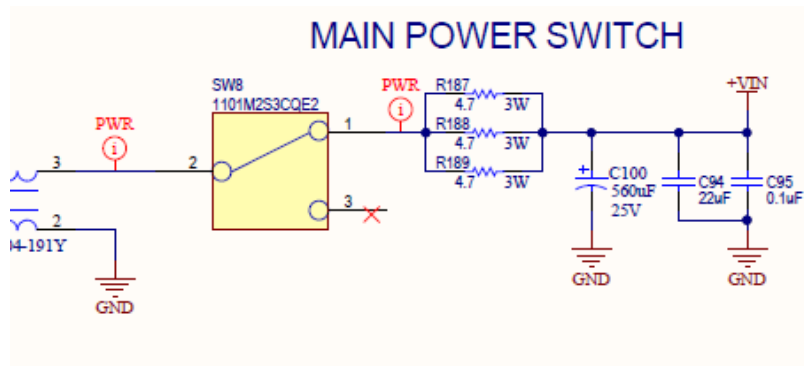


Figure 38 – Main power switch, SW8

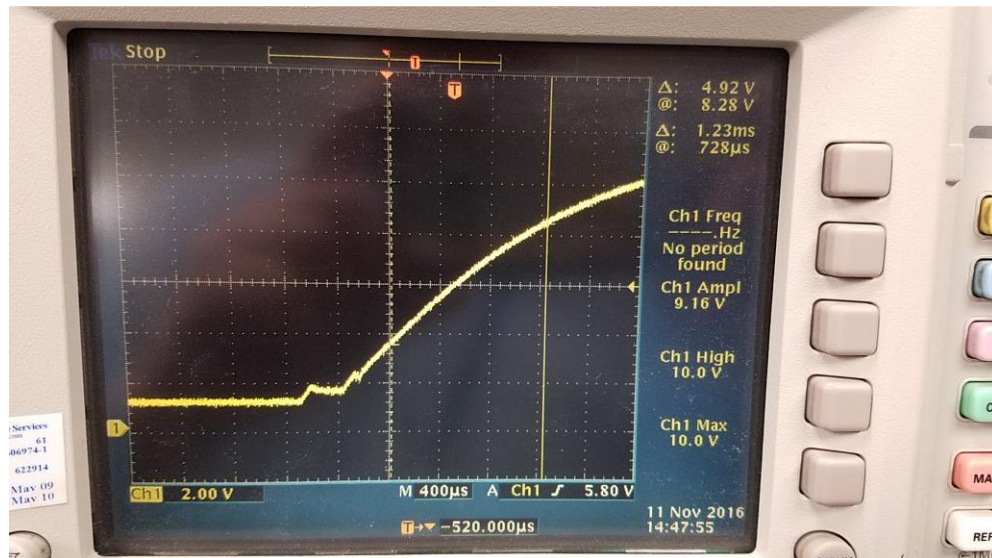


Figure 39 – +VIN LPF screenshot

3.2 Carrier Card Power Supplies

The carrier provides the below power rails for the UltraZed SOM. A PMIC, Infineon part number IRPS5401MTRPBF, is factory programmed with the necessary parameters to set the output voltages. This part number is specific to Avnet's SOM and IOCC.

The UltraZed SOM provides voltage sense feedbacks for each rail supplied by the carrier card. Please refer to Xilinx's ds925 for percent variation on the following power rails when designing the power system for a custom IO Carrier Card.

- +VIN 12V Main power in via a six pin ATX-type connector.
- PS +MGTRAVCC (0.85V)
- PS +MGTRAVTT (1.8V)
- PS MIO bank 501 VCCO (3.3V)
- PL HP bank 64/65/66 VCCO (1.8V)
- PL HD bank 26 VCCO (3.3V)

The SOM's SOM_PG_OUT signal is used to assist in power sequencing. The IO Carrier Card PMIC is not turned ON until the SOM_PG_OUT signal is asserted.

NOTE:

In normal operation, the SOM_PG_OUT signal controls the IOCC's PMIC enable pins. For this reason a SOM must be placed for the carrier to power up in normal operation. In test mode, the board can be powered up by modifying the circuit as described below.

To power up the board without a SOM, the user can place R123 with a 49.9K ohm resistor. This weak pull turns on the carrier card's PMIC. While it is recommended a SOM not be placed when R123 is placed, the resistor value is high enough to allow the SOM to maintain control of the IOCC's PMIC.

Voltage Level:	Rail/Connector/Interface:
12V	+VIN
5V	+VUSB
0.85V	JX3, GTR AVCC
1.8V	JX3, GTR AVTT
1.8V	JX1, JX2, PL HP banks (Vcco_HP_64/65)
3.3V	JX2, JX3, PL HD & PS MIO bank 501

Table 17: Voltage levels by connector, rail, interface & bank

3.3 +3.3V Primary Regulator – U19

The carrier card uses an always-on ON Semiconductor NCP565D2T33R4G +3.3V Low Drop Out linear regulator. This part is used to provide logic power to the main board regulator, the Infineon IRPS5401MTRPBF PMIC.

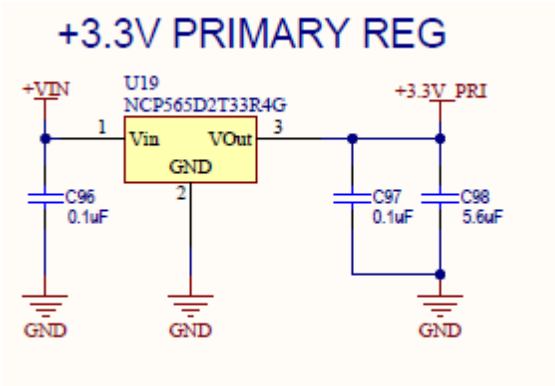


Figure 40 – +3.3V primary regulator, U19

3.4 Main Regulator - Infineon IRPS5401MTRPBF PMIC – U27

A five channel, high current programmable PMIC is required to source the SOM with high accuracy rails. The Infineon IRPS5401MTRPBF PMIC was chosen due to it's small size, high efficiency, and programmable features. This part is on the PMBUS and is accessible via J10, the PMBus header. The part has been factory programmed with 3 selectable output profiles. One profile is used for the carrier card, while the remaining two are used for the SOM.

NOTE: The IRPS5401 PMIC has been set as follows:

- Turn off outputs if PMIC input voltage is less than 10.5V
- Turn on outputs if PMIC input voltage is equal or greater than 11.0V

In practice, the minimum +VIN on J7 (power jack) must be 11.6 volts or greater. This minimum value accounts for the voltage drop on the input filter circuit at maximum current draw. In a custom carrier design, pending the +VIN source, the input-low threshold of the PMIC can be adjusted to user preferences.

- +VIN range is +11.6V to +12.2V
- The carrier card PMIC I2C address is: 0x12
- The carrier card PMBus address is: 0x42

Power Rail Name:	Source, Channel:	Volts, Amps:	Purpose:	JX Pins:
+VIN	Wall adapter, N/A	+12V, 5.0 A	Main board power	JX1 & JX2: 132, 133, 140
+3.3VDP	U3 LDO, N/A	+3.3V, 500 mA	Display Port power	N/A
+3.3V PRIMARY	U19 LDO, N/A	+3.3V, 1.5 A	PMIC core power	N/A
+5.0V	PMIC, CHB	+5.0V, 2.0 A	Main board power	N/A
+MGTRAVCC	PMIC, CHA	+0.85V, 2.0 A	SOM VCCIO power	JX3: 31, 37, 39
+3.3V, +VCCO_HD_26, VCCO_PSIO_501	PMIC, CHC	+3.3V, 3.0 A	Main board power, SOM VCCIO power	JX2: 18, 24, 30 JX3.67
+VCCO_1V8, +VCCO_HP_64/65/66	PMIC, CHD	+1.8V, 4.0 A	SOM VCCIO power	JX1: 5, 6, 7, 12, 13, 18 JX2: 17, 23, 29
+MGTRAVTT	PMIC, LDO	+1.8V, 0.3 A	SOM VCCIO power	JX3: 36, 42
+USB_VB	U21, LDO	+5.0V, 1.5 A	USB interface	N/A
+PS_VBATT	JP3, LR44, +VCCO_1V8	+ <2.0V, < 10mA	FPGA key memory	JX3.46

Table 18 – Carrier Card power rails

3.4.1 Power supply net ties

There are several rails that are tied together on the carrier card through the use of PCB net ties. PCB net ties are two separate signal planes tied to each through a piece of PCB copper. This technique is used to illustrate schematic/electrical connectivity

- +VCCO_1V8 → VCCO_HP_64/65/66
- +3.3V → VCCO_HD_26 & VCCO_PSIO_501

NOTE: These rails are not tied together on the SOM. They are not tied together at the SOM because a user may want different I/O voltages on each bank. They are tied together on the carrier card because these are the voltages required for our specific application.

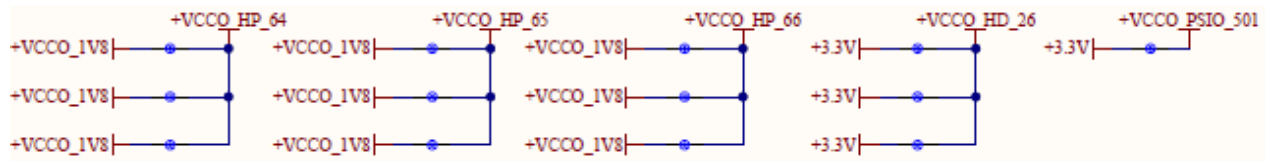


Figure 41 – Net Tie rail bonds

Component	PMBus 0x	Node Text
I2C 0x	12	IRPS5401R2
Switcher A	42	Switcher A
Switcher B	42	Switcher B
Switcher C	42	Switcher C
Switcher D	42	Switcher D
LDO	42	LDO

Figure 42 – Carrier Card PMIC Address window via IR PowIRCenter

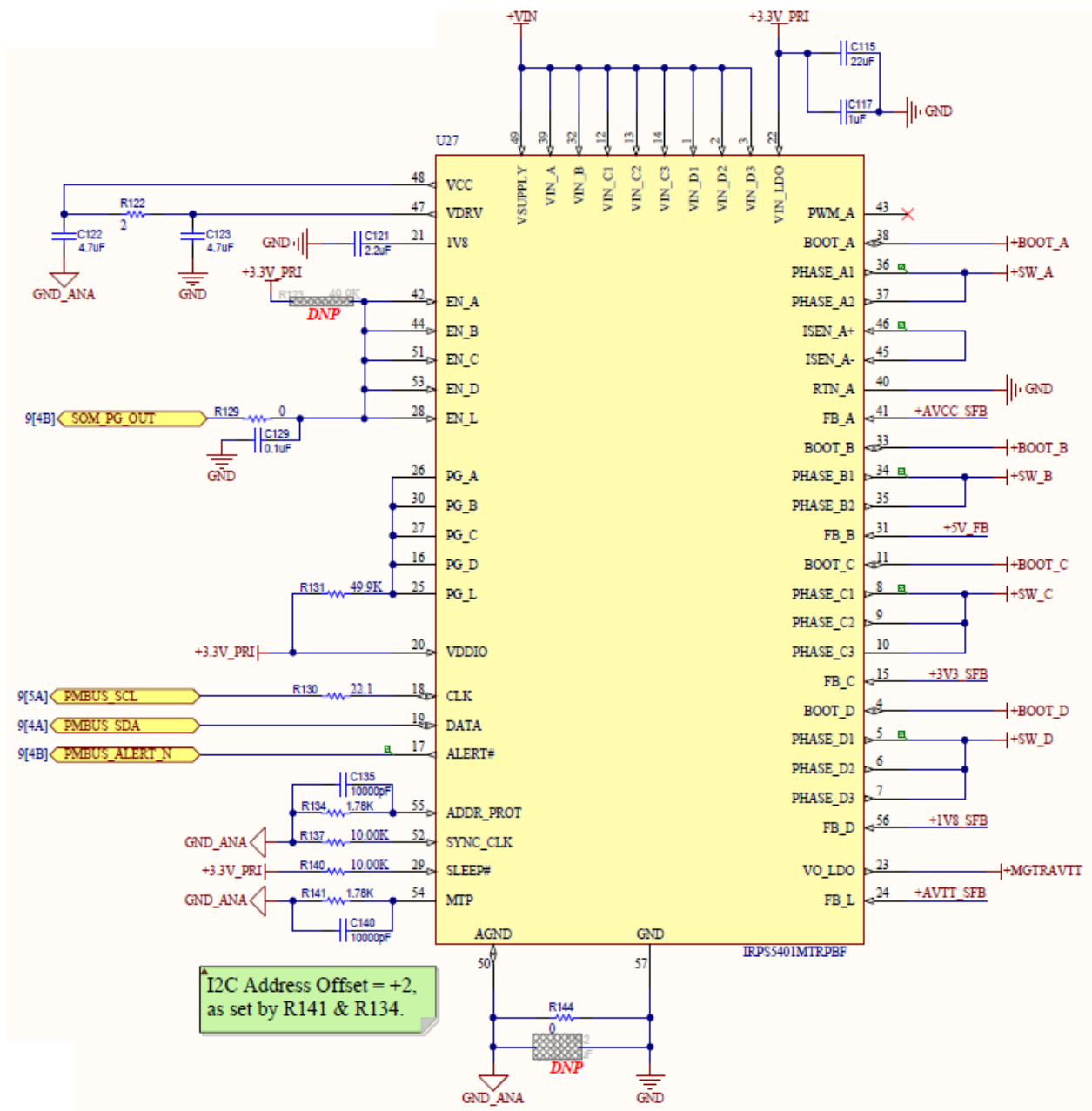


Figure 43 – Infineon PMIC IRPS5401MTRPBF 5 Channel regulator

3.4.2 PMIC Feedback resistors

Feedback resistors are placed on each PMIC output channel. However, these resistors may not be placed, are labeled as “DNP” and are hash-marked out in the schematic. These parts are removed to allow SOM remote sensing to occur. If the user desires, however, these components can be placed for power supply evaluation, but should NOT be placed when a SOM is used.

More information on the Infineon PMIC may be obtained by contacting your local Avnet FAE.

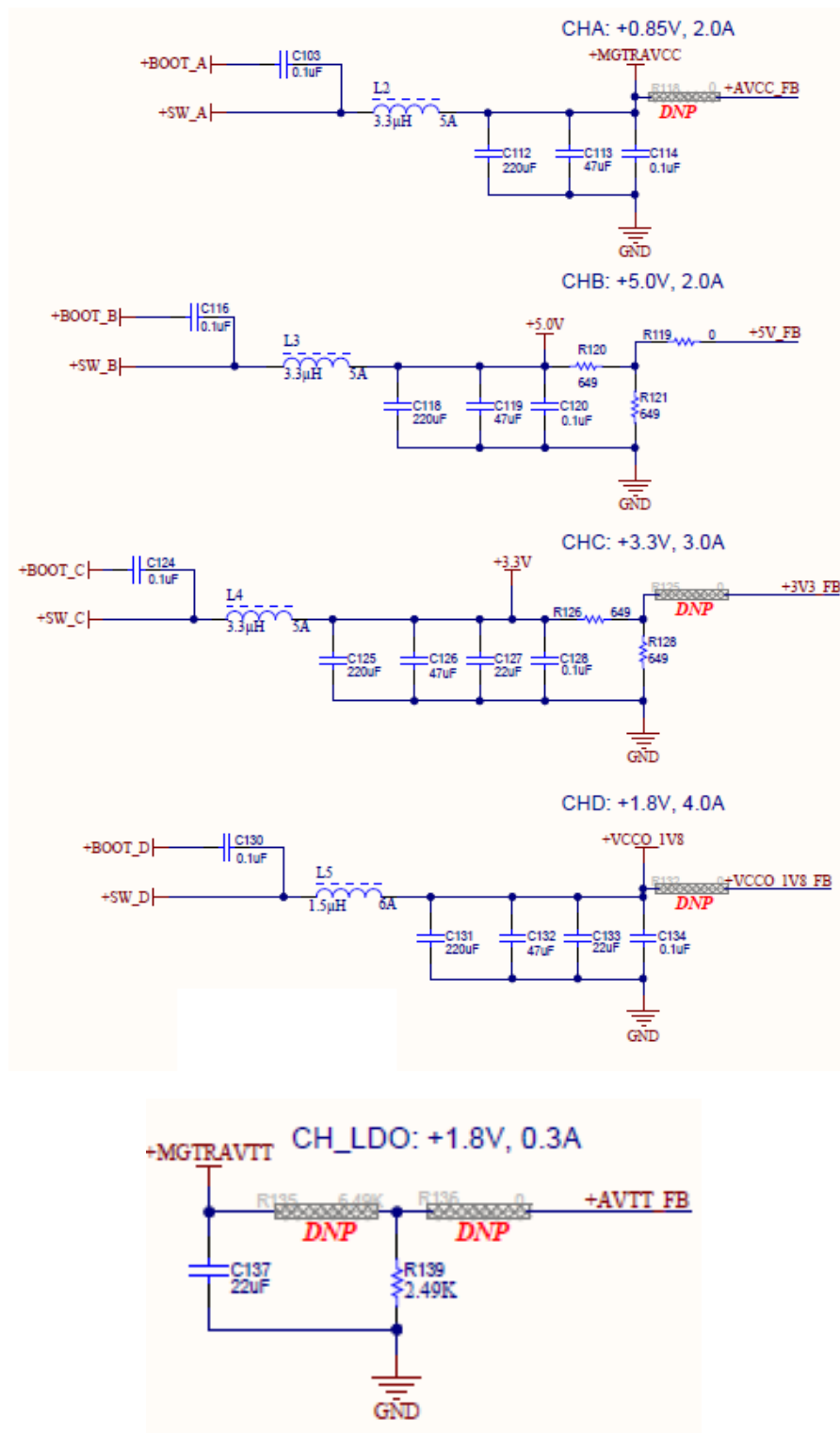


Figure 44 – PMIC power outputs with DNP feedback components

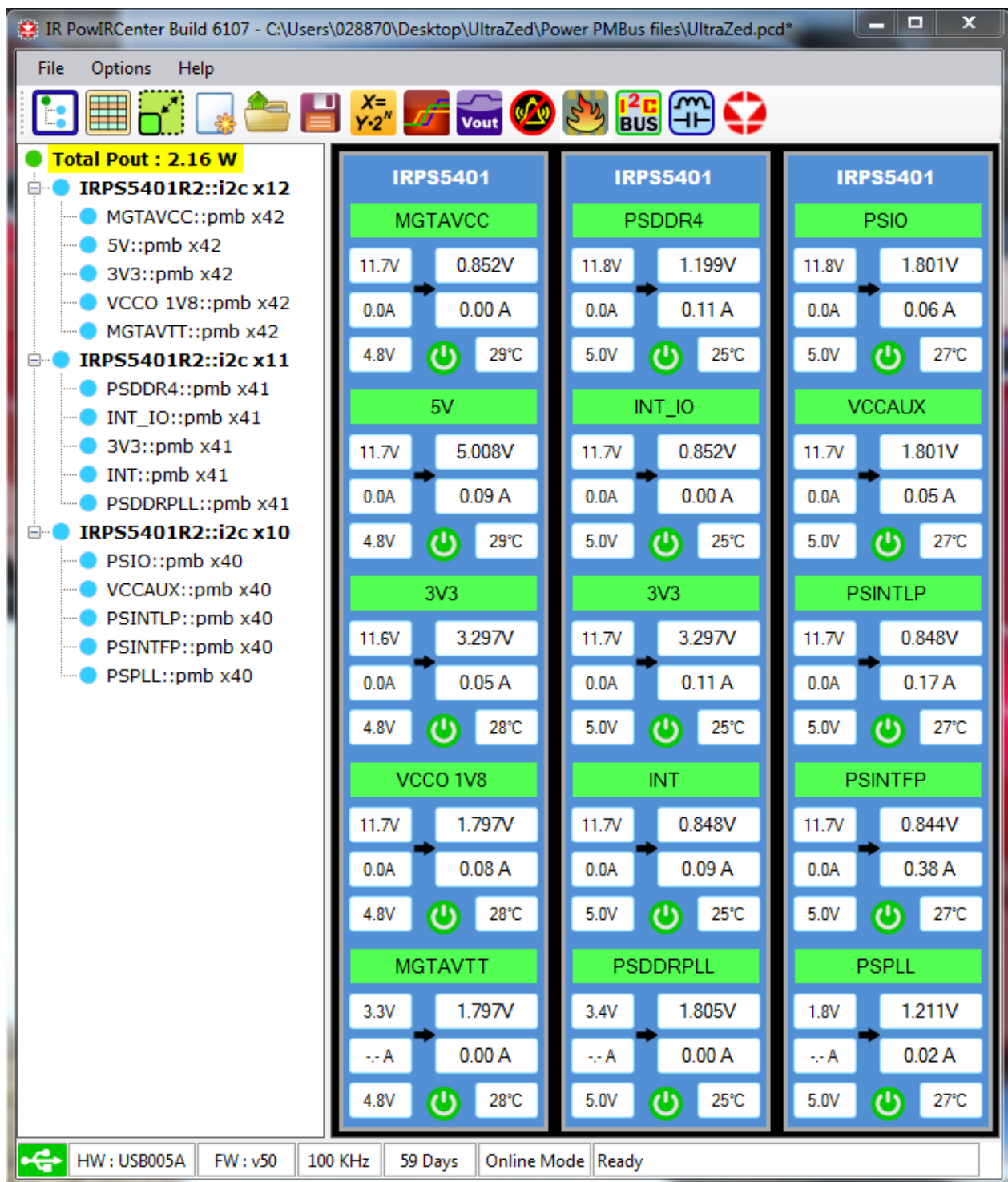


Figure 45 – PMIC Interface window via IR PowIRCenter

3.5 Power Sense signals

The UltraZed SOM provides low current power sense signals for the below carrier rails. These feedback signals are used to adjust the output voltage for each rail. This method of feedback ensures the load (SOM) is provided stable power during dynamic power loading conditions. This method of sensing also nulls out all current and resistance drops across both boards and connectors.

IOCC Net Name:	JX3 Pin:
VCCO_HP_66_SENSE	83
VCCO_HP_65_SENSE	91
VCCO_HP_64_SENSE	92
VCCO_HD_26_SENSE	84
MGTRAVCC_SENSE	75
MGTRAVTT_SENSE	76

Table 19 – SOM power rail sense connections

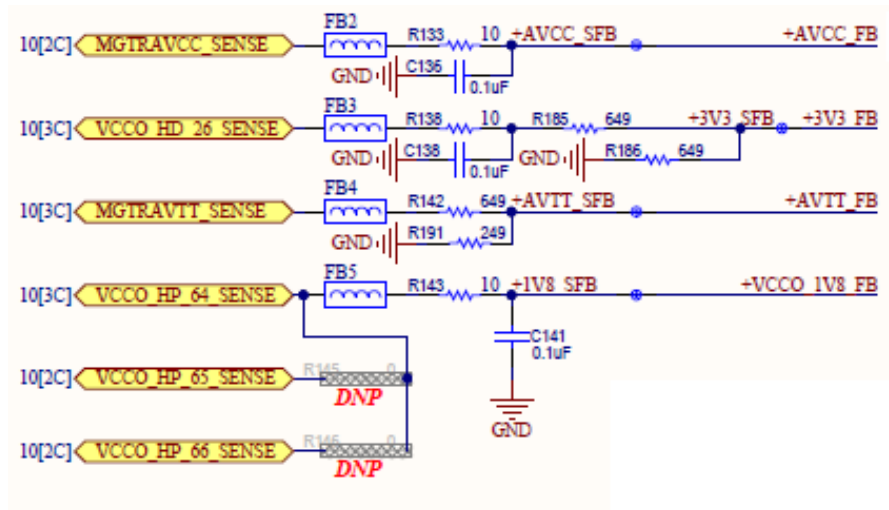


Figure 46 – Power supply sense rail filters

3.6 PMIC PMBus Interface – J10

The UltraZed IOCC and SOM's Power Management ICs can be accessed by attaching to the PMBus header, J10. This header can be used for monitoring and programming all PMBus voltage regulators on the IO Carrier Card SOM. To attach to this interface the customer may use a generic I2C dongle or an Infinion USB005 dongle.

NOTE:

After the initial programming of all PMBus voltage regulators, the UltraZed SOM can drive the PMBus in order to control/monitor the PMBus voltage regulators on the UltraZed SOM as well as the IO Carrier Card for the purpose of power management and/or measurements.

The SOM contains the I2C pullup resistors to allow the board to read/write the PMBus regulators.

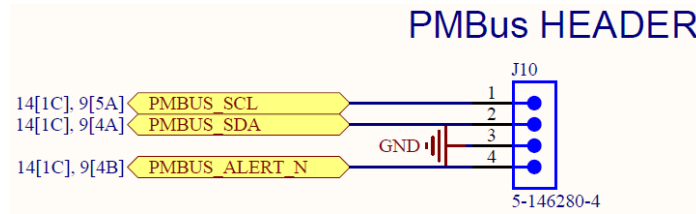


Figure 47 – PMBus header

IOCC Net Name:	JX2 Pin #:
PMBus_SDA	11
PMBus_SCL	12
PMBus_ALERT#	35
SOM_PG_OUT	41

Table 20: PMBus connections and PG connection

Rail Name, voltage:	JX1 Pin #	JX1 Pin #	Rail Name, voltage:
VCCO_HP_65, 1.8V	5	6	VCCO_HP_64, 1.8V
VCCO_HP_65, 1.8V	7	12	VCCO_HP_64, 1.8V
VCCO_HP_65, 1.8V	13	18	VCCO_HP_64, 1.8V
GND	19	24	GND
GND	25	30	GND
GND	31	36	GND
GND	37	42	GND
GND	43	48	GND
GND	49	54	GND
GND	55	60	GND
GND	61	66	GND
GND	67	72	GND
GND	73	78	GND
GND	79	84	GND
GND	85	90	GND
GND	91	96	GND
GND	97	102	GND
GND	103	108	GND
GND	109	114	GND
GND	115	120	GND
GND	121	126	GND
GND	127	132	VIN
VIN	133	140	VIN

Table 21: JX1 Power and Ground connections

Signal Name	JX2 Pin #	JX2 Pin #	Signal Name
GND	5	6	GND
VCCO_HP_66	17	18	VCCO_HD_26
VCCO HP 66	23	24	VCCO HD 26
VCCO HP 66	29	30	VCCO HD 26
GND	43	48	GND
GND	49	54	GND
GND	55	60	GND
GND	61	66	GND
GND	67	72	GND
GND	73	78	GND
GND	79	84	GND
GND	85	90	GND
GND	91	96	GND
GND	97	102	GND
GND	103	108	GND
GND	109	114	GND
GND	115	120	GND
GND	121	126	GND
GND	127	132	VIN
VIN	133	140	VIN

Table 22: JX2 Power and Ground connections

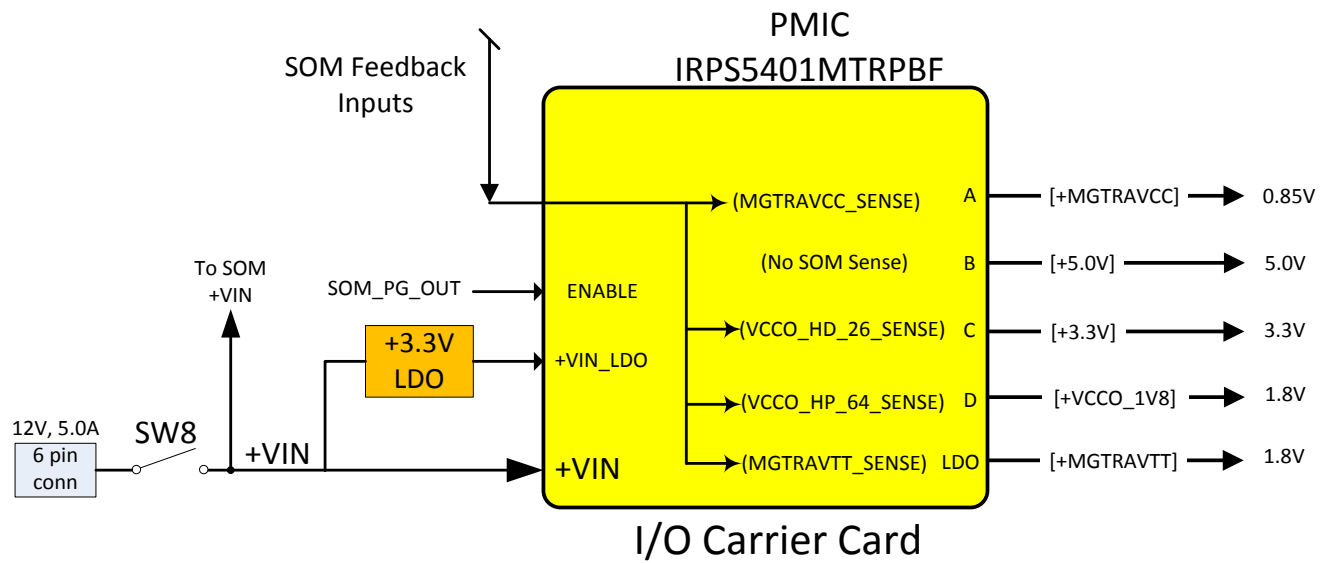


Figure 48 – Infineon/IR power topology example

3.7 Display Port Regulator – U3

The Display Port requires a high precision power supply, +3.3VDP. The Maxim Part MAX8902BATA+T creates this rail. Features include:

- Vout is high precision, ($<1.5\%$ Vout) & low noise (16uVRMS)
- 500mA source in normal operation
- 700mA source in short mode
- Auto thermal shutdown and protect
- POK output
- 2mm X 2mm package

LED D3 is used to indicate the regulator is on. It illuminates when the regulator is within 88% of nominal output voltage.

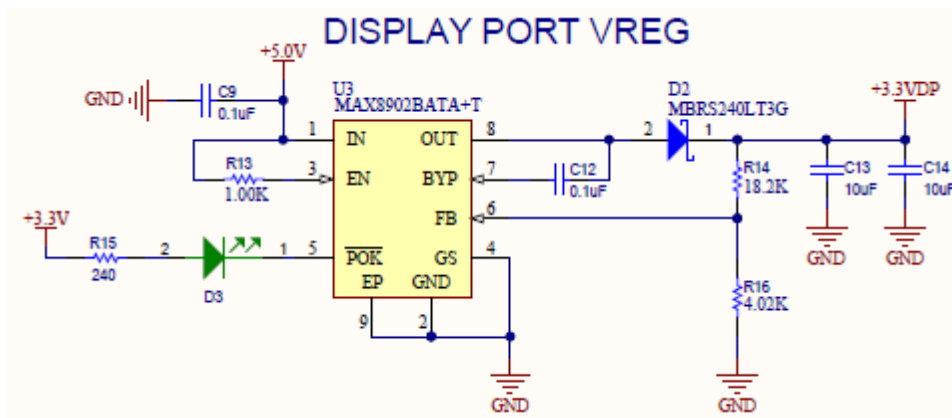


Figure 49 – +3.3V Display Port regulator

3.8 Power Monitor interfaces: SYSMON (J9) and PSU (J8)

The UltraZed SOM SYSMON interface is available on the carrier card. The pins are routed to a 0.1" SIP header for access to the SYSMON interface pins.

- The signals are routed differentially at 100 ohms.
- Termination resistors R115 and R116 are placed within 100 mils of J9.
- The signals are routed to within 10 mils across both pairs.

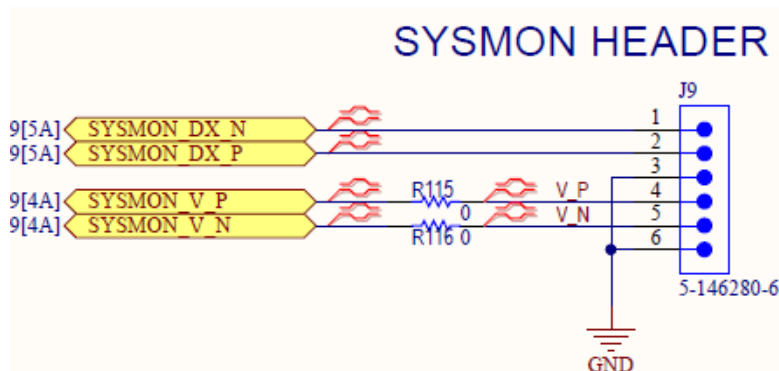


Figure 50 – SYSMON header

IOCC Net Name:	JX2 Pin #:	SYSMON Jack Pin #:
SYSMON_V_N	1	1
SYSMON_V_P	3	2
SYSMON_DX_N	2	3
SYSMON_DX_P	4	4

Table 23: SYSMON connection table

3.8.1 Power Supply monitor header – J8

A non-populated dual row 100 mil pitch 8 pin header is used for measuring the carrier card's voltage rails. The below figure shows the available voltage monitor points.

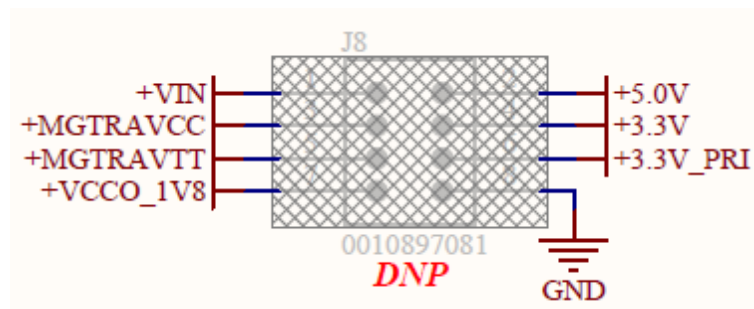


Figure 51 – J8 Voltage Monitor Header

3.9 PS VBATT LR44 Battery – JP3/BTH-1

The Carrier Card provides two methods of maintaining the SOM's Zynq device volatile AES decryptor keys when the carrier is turned off. A 1.5V LR44 battery or a customer connection through JP3. Either connection provides power to the SOM's +PS_VBATT signal via the JX3 pin 46 connector. When the carrier card is turned on, neither method is required as +VCCO_1V8 is diode OR'd with +PS_VBATT signal.

- The +PS_VBATT pin is pulled up via +VCCO_1V8 & D18 when the board is powered on, no battery or external power source needed to maintain decryptor keys.
- Place a LR44 battery to maintain the AES decryption keys on the SOM when board is power off.
- Diode D18 and D20 provide back source isolation for +VCCO_1V8 & LR44 battery.
- In lieu of placing a LR44 battery, the user may decide to use an external power supply or battery connected via JP3. In doing so, **the input voltage on JP3 MUST NOT EXCEED 2.0 volts otherwise the SOM's FPGA may be damaged.** Diode D19 and resistor R117 are placed to help prevent this, but this is by no means intended to encourage a voltage higher than 2.0V to be applied!

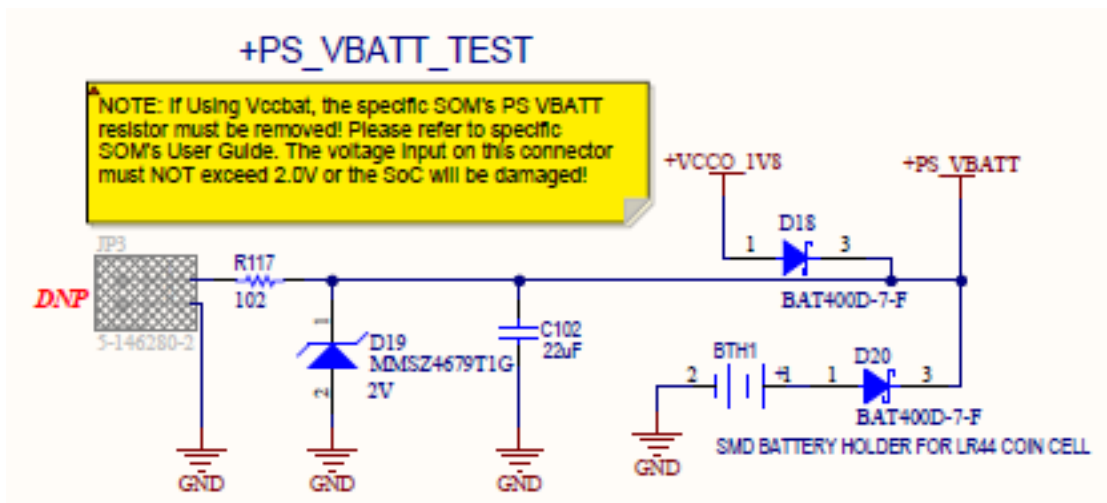


Figure 52 – +PS_VBATT circuit

3.10 PS VBATT placement

LR44 Battery installation instructions:

The LR44 battery is required to be installed in a sleeve, part number BHX1-LR44 and firmly inserted into the carrier's socket. The coin cell's positive terminal is placed into the opening of the sleeve facing up.

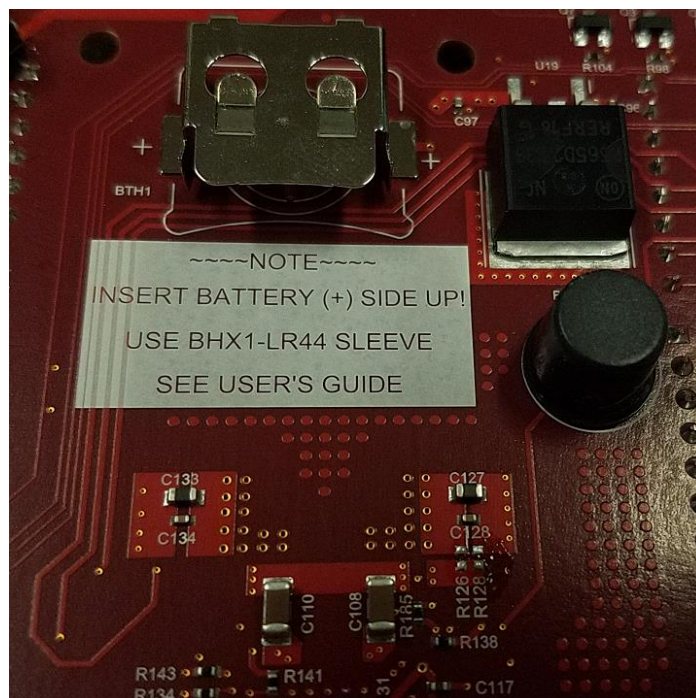


Figure 53 – BTH1 LR44 battery cage

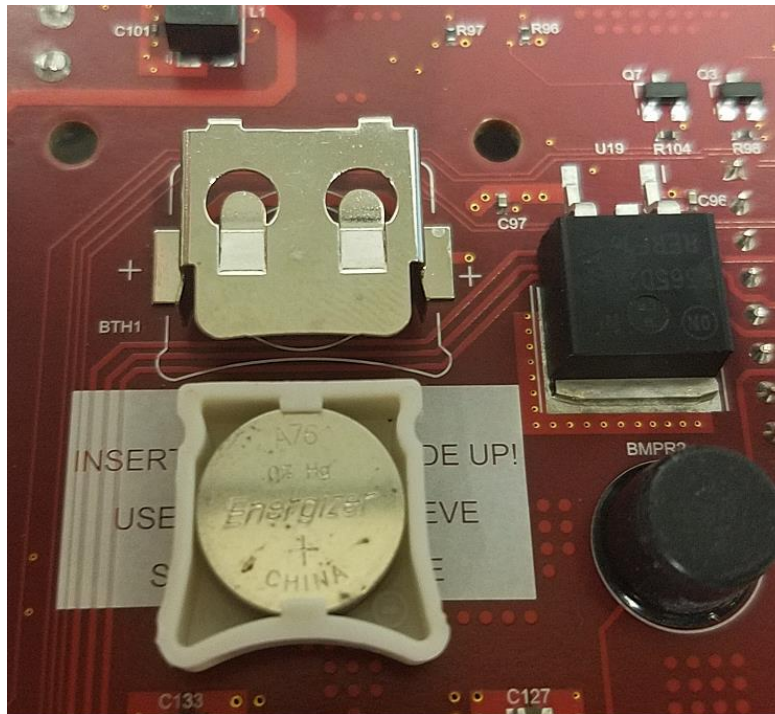


Figure 54 – Battery & sleeve orientation prior to insertion

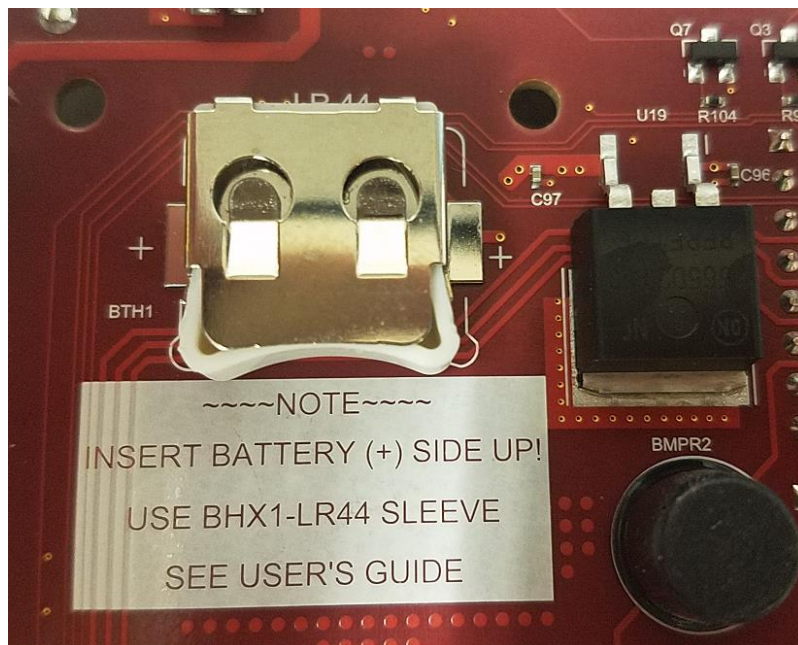


Figure 55 – Final battery placement. Push battery back as far as possible.

3.10.1 Sequencing

- The SOM must provide an active high SOM_PG_OUT for the carrier card's PMIC to turn on.
- The below image shows the power sequencing using the IR PowlRCenter software. The Ton time delays are set to 10 ms on CHA – CHD with a rise time of 6 ms. The LDO is set for a delay of 20 ms and no rise time delay.

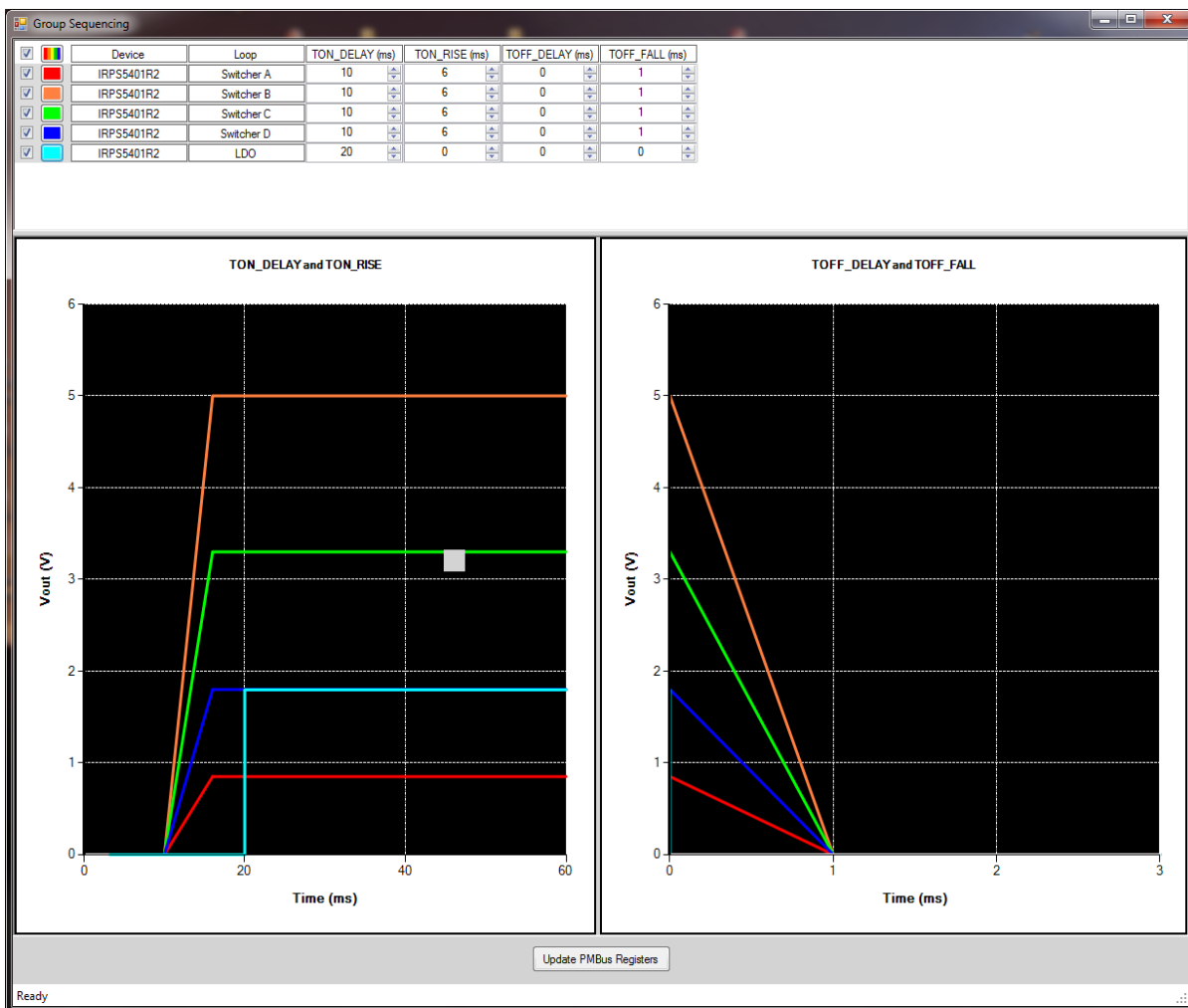


Figure 56 – Power Sequencing

3.10.2 Bypassing/Decoupling/Filtering

The PZCC-FMC-V2 follows the recommended decoupling and layout techniques per each manufacturer's datasheet.

3.10.3 PG Module Power Good LED

- A green status LED, D9, illuminates when PG_CARRIER signal is high (good).
- A green status LED, D10, illuminates when +VIN is present.

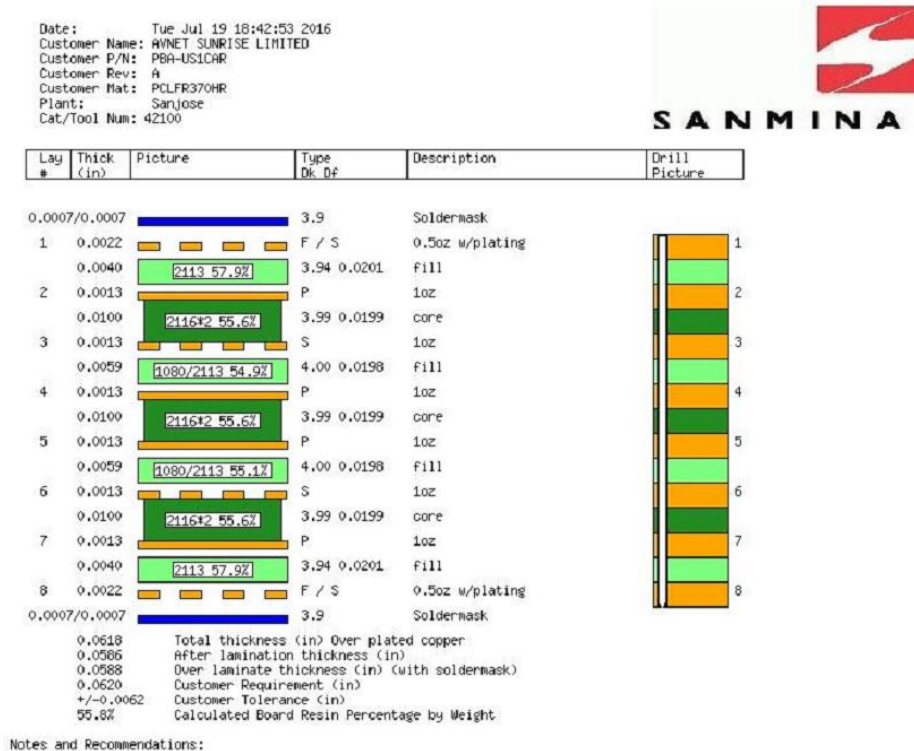


Figure 57 – PG_MODULE LED

4 Mechanical

4.1 Layer stackup

Below is the as-built to layer stackup of the UltraZed IOCC.



Impedance Constraint Information

Imp #	Impedance Type	Affect (1)	Lur (2)	Cust L/W	Line Width (1)	CenterToCenter (2)	Ref Plane Top	Ref Plane Bot	Targ ohms	Tol ohms	Predicted ohms@2GHz
1	EC MS	1	None	0.0049	0.005	0.0099	None	2	90	9	92.13
2	EC MS	1	None	0.00375	0.0038	0.009	None	2	100	10	102.64
3	Surf MS	1	None	0.0065	0.0061		None	2	50	5	51.66
4	EC SL	3	None	0.0035	0.0041	0.0091	4	2	100	10	97.79
5	Stripline	3	None	0.007	0.0067		4	2	50	5	48.67
6	Stripline	6	None	0.007	0.0067		5	7	50	5	48.75
7	EC MS	8	None	0.0049	0.005	0.0099	None	7	90	9	92.13
8	EC MS	8	None	0.00375	0.0038	0.009	None	7	100	10	102.64
9	Surf MS	8	None	0.0065	0.0061		None	7	50	5	51.66

Trace widths measured at base of trace
All dimensions in inches (unless otherwise noted)
All values are calculated using a frequency of 2.00GHz

Products built using these specified nominal dimensions will have variation in physical and electrical results based on acceptable manufacturing materials and process tolerance.
This data is intended to provide one possible solution to meet a particular set of impedance and thickness requirements.
If any of these values are attached to fabrication prints, they should be marked as 'reference'.

This is proprietary Sanmina-SCI Corporation information. All rights are reserved.

Figure 58 – UltraZed IOCC PCB Stackup

4.2 Diagram and Model

A mechanical diagram and a 3D Model for the US1CAR are available for download at www.ultrazed.org/product/ultrazed-EG

4.3 Weight

The weight of the UltraZed-IOCC with rubber feet, SD card, and jumpers populated without the SOM attached is 161 grams (5.68 ounces).