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UltraZed™ PCIe Carrier Card Hardware User Guide

Version 1.1

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1.1	1/30/2017	1st release
1.1	3/20/2017	Updated GTR Reference for USB & DP.

Contents

1 Introduction

The UltraZed™ PCIe Carrier Card is a development board designed for customers to easily evaluate the Avnet UltraZed System On Module (SOM) module(s) and accelerate the design cycle of product-to-market. This carrier card provides all of the necessary power, clock, reset control and SoC I/O pin accessibility through the JX1, JX2, and JX3 MicroHeaders and includes multiple industry standard interfaces listed in section 1.1, List of Features.

In addition to industry interfaces, the card also provides two debug interfaces - SMT2 and PC-4 JTAG. Both interfaces are provided to assist with SOM application development.

This document details the specific features, operation and configuration of the UltraZed PCIe board. Please visit www.ultrazed.org/product/ultrazed-EG for the latest product information.

1.1 List of Features

The UltraZed PCIe provides the following features and interfaces. Please see the associated section in this User Guide for further information.

- Supports the following SOM types:
  - XCZU3EG-SFVA625
  - XCZU2EG-SFVA625
  - XCZU2CG-SFVA625
  - XCZU3CG-SFVA625

- SOM connections:
  - 2 high density 140 pin JX connectors (JX1, JX2)
  - 1 high density 100 pin JX connector (JX3)

- Interfaces:
  - SATA3 host interface.
  - Display Port x1 connector.
  - USB 2.0/3.0 Host & OTG micro AB connector.
  - 10/100/1000 Mb/s RJ45 connector.
  - Dual USB-UART using Micro USB connector.
  - LVDS Touch Panel interface.
  - PL PMOD headers (single ended).
  - 1 PS PMOD header (single ended).
  - FMC LPC connector.
  - PCIe x1 endpoint interface.
  - SOM +5V fan connector.
  - microSD card connector.

- User switches, pushbuttons and LEDs:
  - 8 PL user slide switches
  - 4 PL user push button switches
  - 8 PL user LEDs
  - 1 PS user LED
  - 1 SOM reset push button switch

- Debug & Configuration
  - Digilent® SMT2 USB-JTAG module
  - PC4 JTAG header
  - Voltage monitor header
  - PG_Module LED
  - VIN_HDR LED
  - Various interface LED indicators displaying fault, link and speed.
  - Write protect jumper on microSD card interface.
  - Clock synthesizer's start-up configuration - jumper selectable.
    - 1 PS GTR differential refclock outputs
    - 1 Global Clock differential output for SOM fabric
    - Start-up Mode selectable via jumpers

- I2C interfaces
  - I2C programmable IDT differential clock generator
  - I2C EUI48 MAC address memory device
  - I2C PMBUS programmable IRPS5401MTRPBF Power Management IC (PMIC)

- Power
  - +VIN 11.6V up to 12.2V via six pin power connector
  - Power slide switch
  - 5 Channel I2C programmable PMIC
  - Remote rail sensing of SOM. PMIC voltage adjusts according to SOM loading.
  - Isolated Vin to +3.3V regulator
  - +VIN connections to SOM via JX connectors.
  - PMBus™ header
  - PL SYSMon header
  - PS VBATT battery connection with diode steering protection
    - LR-44 Battery slot, external jack or on board 1.8V power.
    - Dual 100 mil header for user voltage input

1.2 Block Diagram

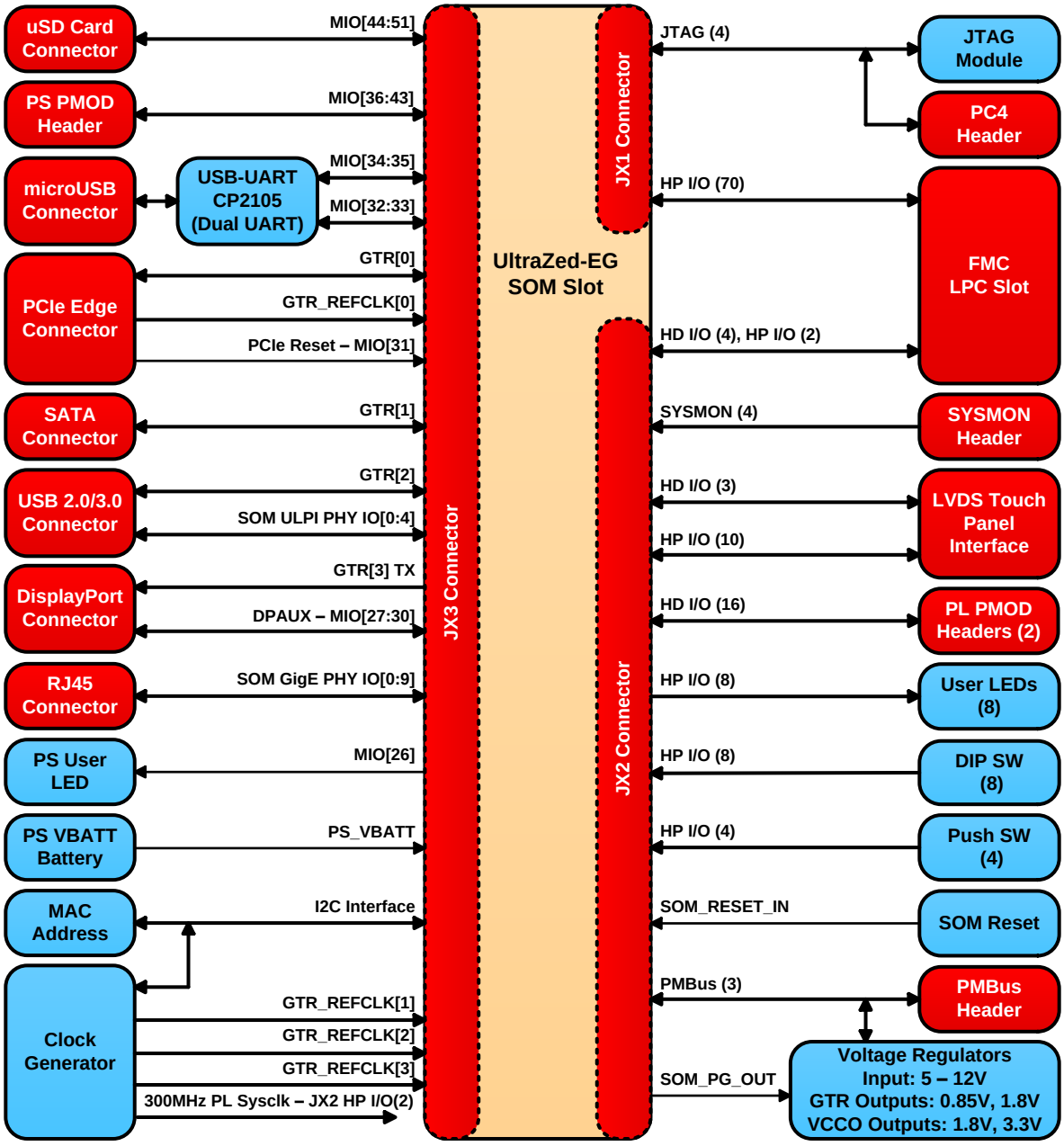

Figure 1 – UltraZed PCIe Carrier Card Block Diagram

Glossary

Term	Definition
PCIe	Input / Output Carrier Card. The SOM attaches to this carrier card (board) for user evaluation. The PCIe features proven high speed interfaces to the SOM as well as the necessary power, control and clocks required for the SOM to operate.
MIO	Multiplexed Input Output – the dedicated I/O available on the PS
PL	Programmable Logic – programmable fabric of the SOM's SoC.
PMIC	Power Management Integrated Circuit – voltage regulator used to create required board voltages.
POR	Power On Reset – reset asserted during power on event. Keeps board in reset until PMIC's output is stabilized.
Port IO Name	The name of the IO port signal with respect to the JX connectors and the SOM. It is not the name of the signal wire in the design netlist. This allows the customer to name each signal a specific name if so chosen without losing the port reference.
PS	Processing System – the SoC's processor cores – Application Processing Unit (Quad core ARM Cortex-A53) and Real-Time Processing Unit (Dual core ARM Cortex-R5).
SMPS	Switch Mode Power Supply – switching power supply used to provide high current rails to the board. May be separate from the PMIC or may be the PMIC, depending application needs.
SOM	System On Module – a SoC IC placed on a PCB allowing easy access to the SoC IC's interface, power and control signals. Includes the necessary memory (RAM, storage), power and connectors to operate as a pluggable processing module.
SoC	System On Chip – Xilinx Zynq UltraScale+ IC.

Table 1 – Glossary

1.3 Additional Documentation

- Additional information and documentation on Avnet's UltraZed product line can be found at www.ultrazed.org/product/ultrazed-EG
- Additional information and documentation on Xilinx's Zynq® UltraScale+ All Programmable Heterogenous MPSoCs can be found at http://www.xilinx.com/products/silicon-devices/soc/zynq-ultrascale-mpsoc.html

2 Functional Description

The following chapter details all of the PCIe interfaces, their configuration and their functional attributes.

2.1 JX Micro Connectors (SOM slot):

The UltraZed PCIe Carrier Card has 3 TE 0.8mm FH (Free Height) connectors used to access the UltraZed SOM I/O pins. The carrier card to SOM connectors are designated as “JX” connectors. Two of the connectors, JX1 and JX2, are 140 pin connectors and the third connector, JX3, is a 100 pin connector.

2.1.1 JX1 Connector

- JTAG pins (JTAG_TMS, JTAG_TCK, JTAG_TDI, and JTAG_TDO)
- 35 differential HP I/O pairs (JX1_HP_DP)
- Power and ground pins (+VIN, VCCO_HP_64, VCCO_HP_65 and GND)

2.1.2 JX2 Connector

- SYSMON pins (SYSMON_VP, SYSMON_VN, SYSMON_DXP, and SYSMON_DXN)
- 15 differential HP I/O pairs (JX2_HP_DP)
- 13 single ended signals (JX2_HP_SE and JX2_HD_SE).
- Power and ground pins (+VIN, VCCO_HP_66, VCCO_HD_26 and GND)
- SOM_RESET_IN_N input
- CC_RESET_OUT_N output
- SOM_PG_OUT_N output
- PMBus signals (PMBus_DATA, PMBus_CLK, and PMBus_ALERT_N).

2.1.3 JX3 Connector

- PS GTR[0:3] Note: GTR_RX3_P/N tied to ground.
- PS GTR_REFCLK[0:3]
- PS MIO bank 501 pins (MIO[26:51])
- USB 2.0 connector interface (USB_OTG_P, USB_OTG_N, USB_ID, USB_OTG_VBUS, and USB_OTG_CPEN)
- Gigabit Ethernet connector interface (ETH_MD[1:4]_P, ETHMD[1:4]_N, and ETH_PHY_LED[0:1])
- Carrier Card I2C interface (CC_SDA, CC_SCL, and CC_INT_N)
- SD Card interface
- PS_VBATT input. Jack input or LR-44 battery input.
- Power and ground pins (MGTRAVCC, MGTRAVTT, +VCCO_PSIO_501 and GND)
- Voltage sense feedback output pins (MGTRAVCC_Sense, MGTRAVTT_Sense, VCCO_HP_64_Sense, VCCO_HP_65_Sense, VCCO_HP_66_Sense, and VCCO_HD_26_Sense).

2.2 PS USB 2.0/3.0 Interface – J4

The UltraZed PCIe Carrier Card's USB 2.0/3.0 interface is implemented with a Kycon KMMX-AB10-SMT1SB30TR Micro AB connector capable of supporting OTG, Device and Host modes. The UltraZed SOM contains the USB 2.0 ULPI PHY interface (USB3320 IC) for USB 2.0. PS GTR[2] signals are used to implement the USB 3.0 interface to the same connector.

2.2.1 USB 2.0 interface:

a. The USB 2.0 interface is connected via the SOM's ULPI PHY IC.
b. The USB 2.0 interface differential impedance is 90 Ω (+/- 5%), Single Ended is 45 Ω (+/- 5%).
c. The USB 3.0 GTR interface differential impedance is 100 Ω (+/- 5%), Single Ended is 50 Ω (+/- 5%).
d. Power: 5V, 500mA.
e. CPEN is used to enable the ACPI/USB compliant MIC2544_1YMM power control IC. When CPEN is logic high, "enabled", the +5.0V rail is passed through to the +USB_VB rail for the USB connector.
f. When CPEN is low the power switch is disabled.
g. R28 is used to set the current limit of the MIC2544 part. The value of 191 ohms is used to set the current to 1.23 Amps.
h. When in Host or OTG mode, FB1 and FB2 along with two capacitors are used to provide filtered power to the USB connector J4.
i. D5 and D7 are ESD arrays used to protect the board and attached devices against static discharge.
j. LED D6 is used to indicate a current limit or thermal shutdown event with the MIC2544 IC. The output is open-drain and asserted low when a flag event has occurred which causes D6 to turn on. The output is not latched and therefore clears once the event ends thereby extinguishing D6.

2.2.2 Device, Host or OTG mode select jumpers.

a. JP4 selects how the USB_ID net is connected. Pin 1 to 2 allows the USB device to connect to the SOM, pin 2 to 3 forces the pin to +3.3V. No populate allows the pin to float. When floating the interface is set to Device mode but once connected the operation can be reversed via the Host Negotiation Protocol (HNP). By default the jumper is not populated.

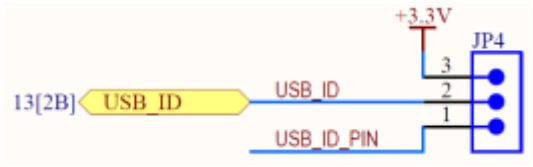

Figure 2 – JP4, USB_ID select jumper

b. JP2 is used to select +5.0V power for +VBUS_SEL.
c. JP3 used to select the appropriate +VBUS_SEL bus capacitance for the operating mode.
d. JP5 used to select the pullup resistor for the USB_OTG_VBUS net going to the SOM.
e. The mode jumper positions are listed below. Default positions are USB in Host Mode.

Jumper Number:	Jumper Position:	Mode select:
JP2	On	Host or OTG (default)
JP2	Off	Device
JP3	Pin 1 – 2	Device or OTG
JP3	Pin 2 – 3	Host (default)
JP5	Pin 1 – 2	Device or Host (default)
JP5	Pin 2 – 3	OTG

Table 2 – USB Mode Select jumpers

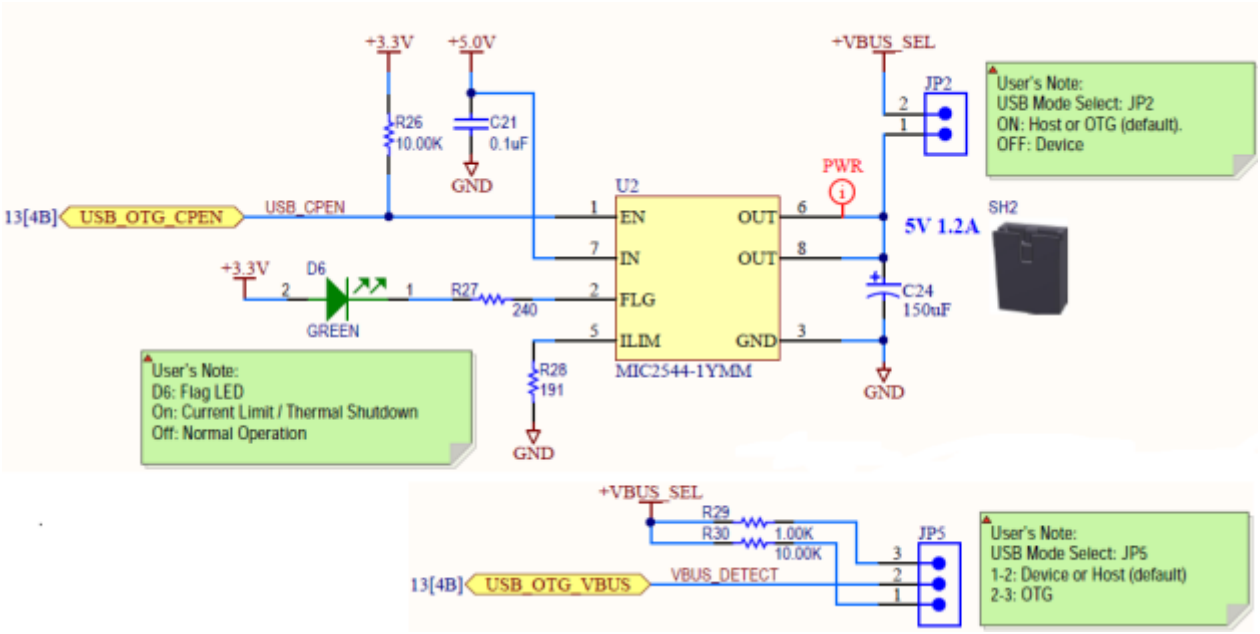

Figure 3 – JP2 & JP5, USB Device, OTG and Host select

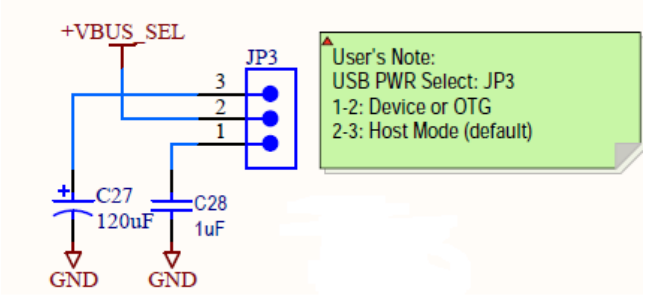

Figure 4 – JP3, USB Device, OTG and Host select

2.2.3 USB 3.0 interface:

a. USB 3.0 has a transfer data rate of up to 5Gb/s (625 MB/s) and is referred to as USB Super Speed. This portion of the interface is directly connected to the Zynq PS via PS GTR[2] and J4, the integrated USB micro-AB connector.
b. Power capability is up to 1.23A @ 5V for non-data (charging) power delivery.
c. Up to 900mA is available during data transfers.
d. The differential impedance routing Zdiff is 100Ω (+/- 10%)
e. The PS GTR 52 MHz clock required is derived from the IDT synthesizer.

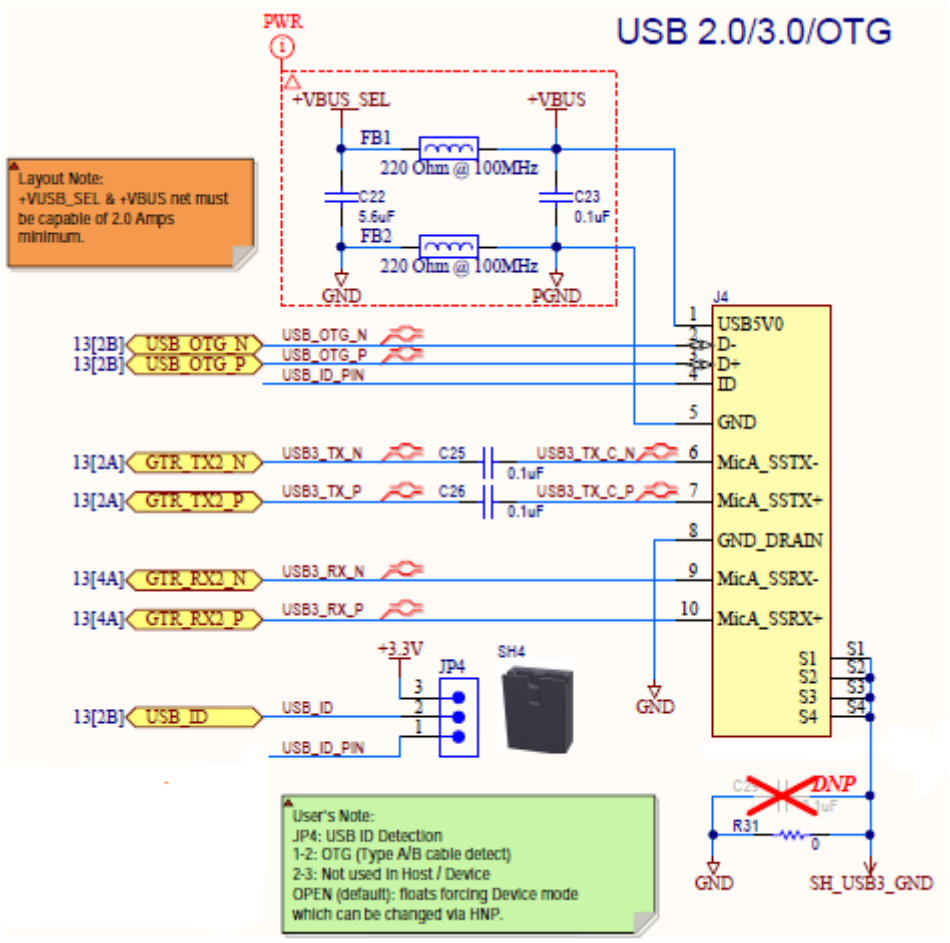

Figure 5 – J4, USB 2.0/3.0 Port Interface

2.3 PS 1000 Mb/s Ethernet RJ45 – J5

The PCIe's 1000 Mb/s Gigabit interface uses an integrated magnetic BEL FUSE L829-1J1T-43 RJ45 connector or equivalent mounted on the PCIe. The MAC and PHY are located on the SOM and connected using the SoC's RGMII interface. The SOM's PHY signals are routed to the JX3 connector where the PCIe Carrier routes them to the RJ45 connector.

- The MDI impedance is 50 Ω single ended, +/- 5% and is referenced to the positive plane (See TI AN1263) if termination resistors are used at the SOM.
- The trace lengths are matched to within 10 mils pair to pair and no more than 100 mils overall between the entire group of pairs.
- The LEDs are driven via NPN BJT inverters which allow the 1.8V drive signal to control the 3.3V LEDs.
- Two LEDs to indicate speed and activity status:
  - ETH_PHY_LED0: Green Speed
  - ETH_PHY_LED1: Yellow Activity

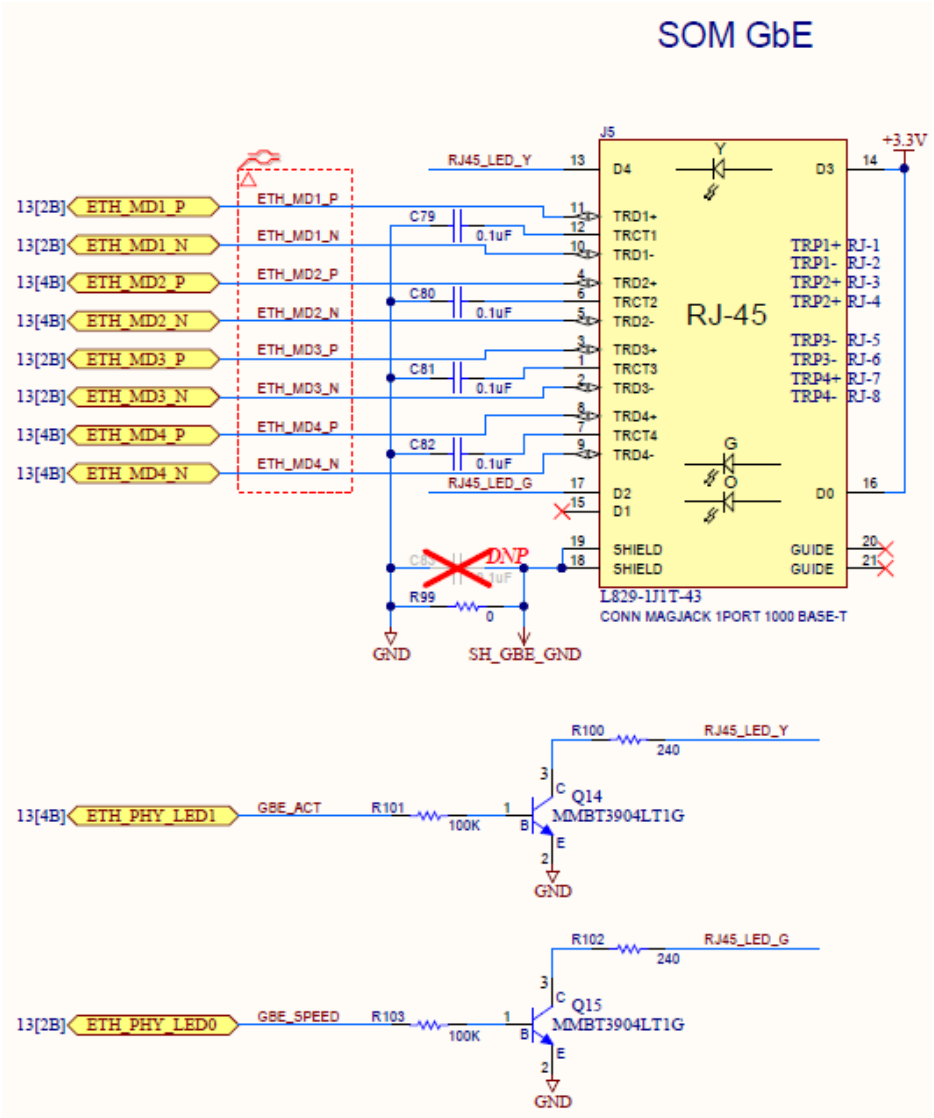

Figure 6 – J5, Gigabit Ethernet Port

2.4 PS Display Port x1 interface – P2

The UltraZed PCIe Carrier Card features a x1 Display Port connection. The PS GTR[3] TX port is used to implement DP interface as shown in Figure 7 – P2, Display Port Interface.

- The Display Port interface also uses an auxiliary interface (DPAUX) which is implemented on the PCIe Carrier Card using the PS MIO[27:30] signals (these are pre-defined MIO pins for the DPAUX when the display port is used).
- The DPAUX generator is used to convert single ended MIO signals to differential Display Port signals. This eliminates the need for these signals to be routed in the SoC fabric. The MIO[27:30] pins are connected to the UltraZed SOM JX3 connector and are operated at 3.3V. The MIO pin assignment and function is as follows:
  - MIO27 – DPOUT – drives DPAUX_C_P to P2
  - MIO28 – DP_HPD – active high signal from P2 indicating Hot Plug Detection.
  - MIO29 – DP_OE_N – tied to both enables of transceiver U3, enables the outputs when driven low by SoC.
  - MIO30 – DPIN – receives DPAUX_C_N from P2
- The MIO pins are routed to a differential driver (FIN1019) to create the DPAUX_P/N pair at 100Ω.
- The Vbias and 100Ω Z matching network has been implemented on the DPAUX pair.
- A separate 5V to 3.3VDP linear LDO regulator, Maxim MAX8902BATA+T, is placed to provide low noise, high precision 3.3V for the display attached to the port.
- The Display Port x1 uses ESD components (TPD8S0009DSMR, TPD4E001DRLR) placed on the data lines.

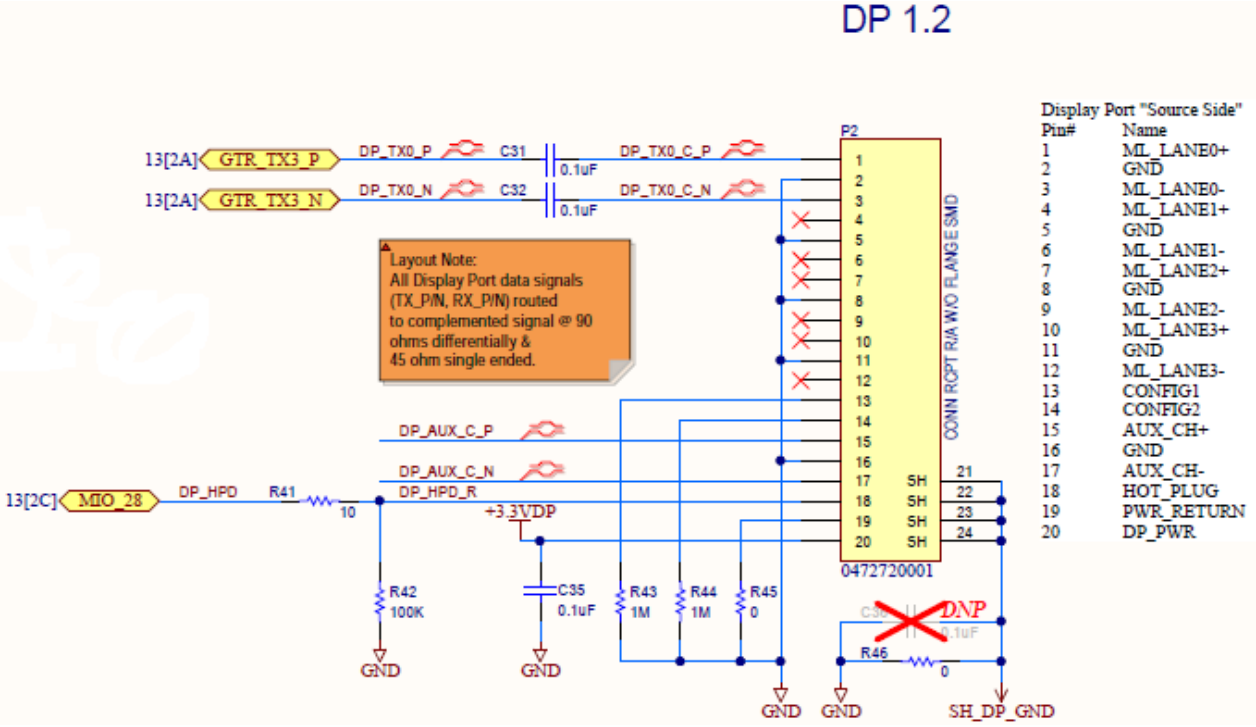

Figure 7 – P2, Display Port Interface

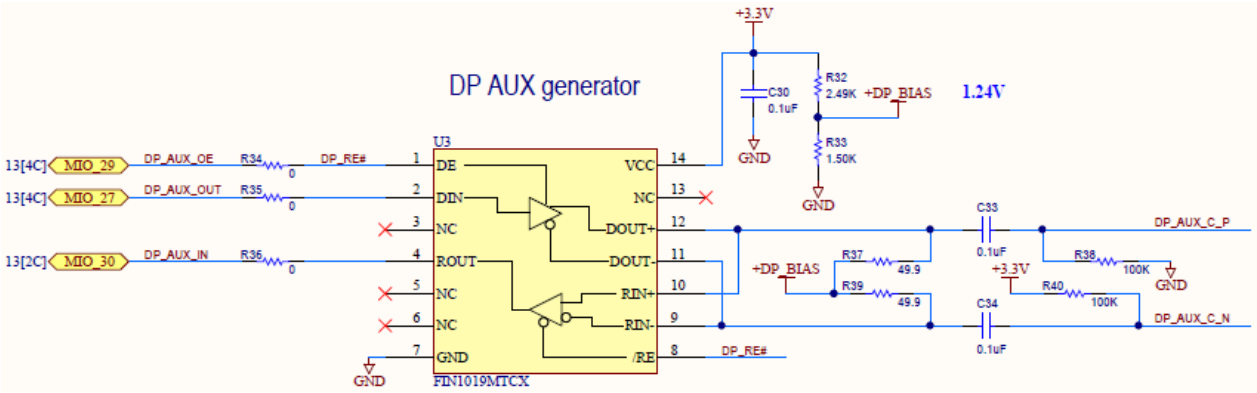

Figure 8 – U3, Display Port DPAUX Generator including Z match and AC coupling

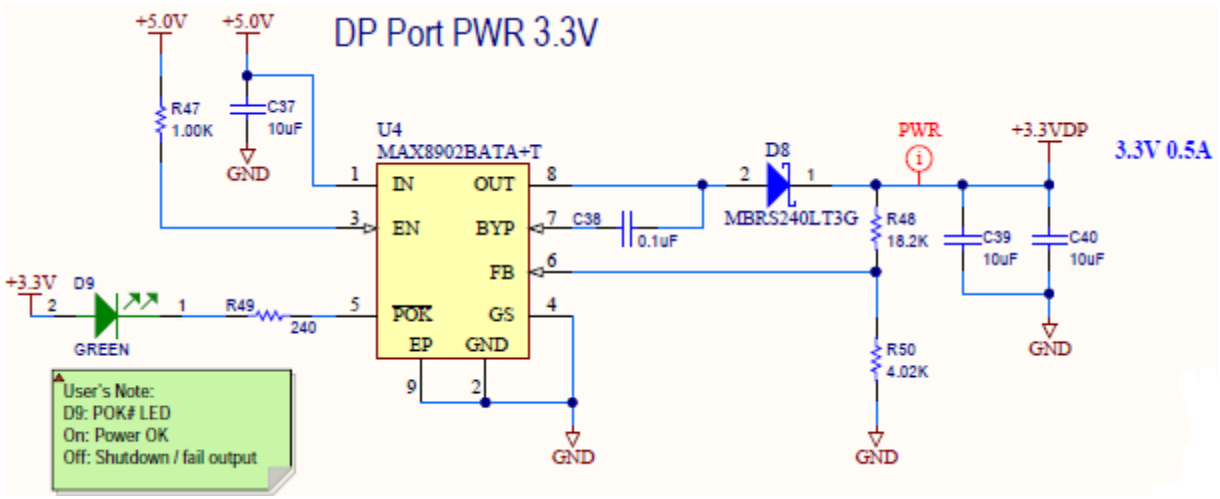

Figure 9 – U4, Display Port 3.3V power supply

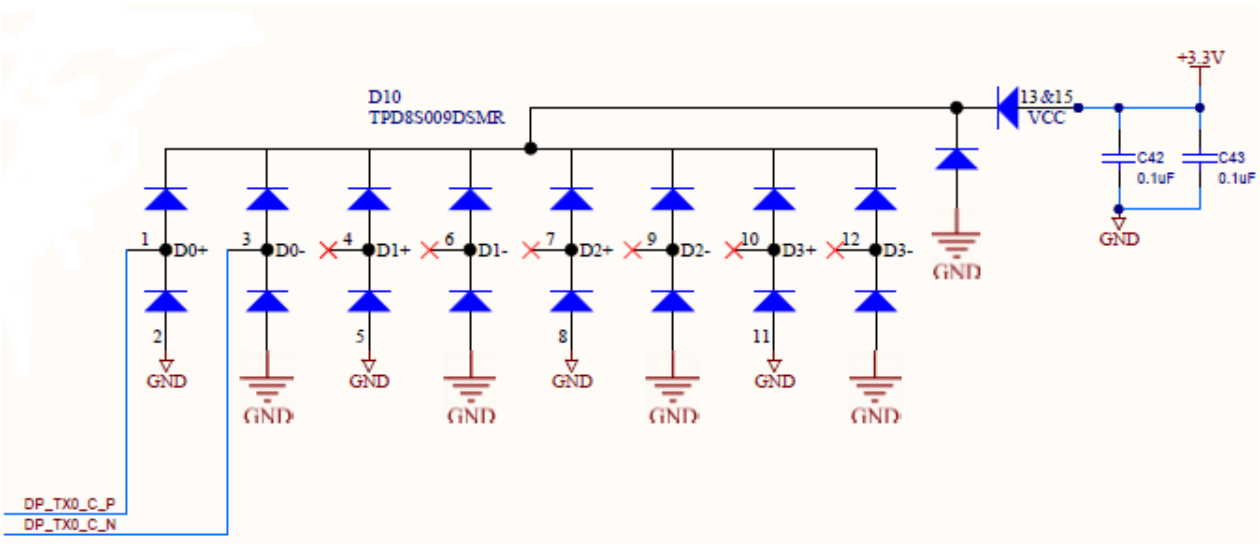

Figure 10 – D10, Display Port GTR TX ESD protection

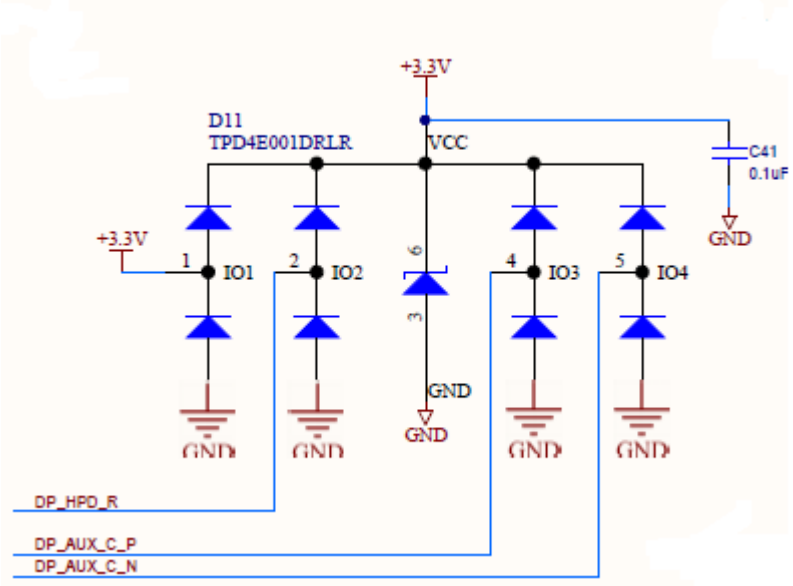

Figure 11 – D11, Display Port DPAUX ESD protection

2.5 PS SATA 3 Host Interface – J3

The UltraZed PCIe Carrier Card's SATA 3 host interface uses the SoC's PS GTR[1] transceiver. The interface includes AC coupling capacitors with appropriate PCB GSSG cutouts and a maximum of 2 layer transitions per signal with no blind or buried vias. This topology is used to minimize impedance mismatches thereby improving signal integrity.

- Interface impedance: 100 ohms, +/- 15%
- Data rates up to 6 Gb/s

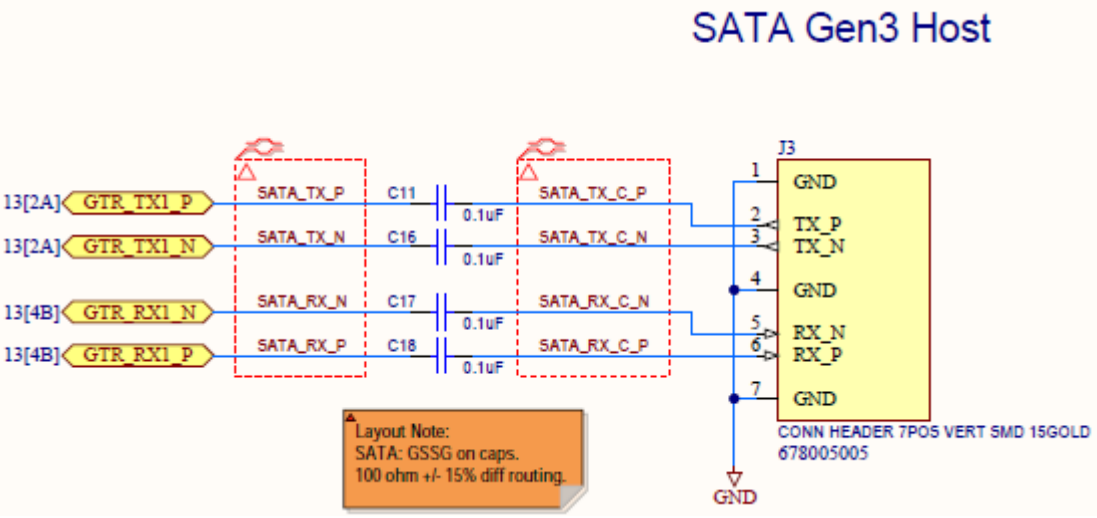

Figure 12 – J3, SATA Port interface

2.6 PS PMOD Header – JP5

The PS PMOD header is connected to the PS MIO[36:43] pins and operated at 3.3V I/O using the VCCO_PSIO_501 rail. The PS MIO[36:43] maps to SPI, however the UltraScale+ does not create a direct map to the UART(0 or 1) nor I2C MIO pins. Table 3 – PS PMOD to MIO UltrZed SOM Table mapping shows the UART and I2C connections.

- Routed at 50Ω single ended.
- The interface follows, as close as possible, the Digilent SPI and UART/I2C pinouts. See page 581 – 583 for TRM pin mapping: http://www.xilinx.com/support/documentation/user_guides/ug1085-zynq-ultrascale-trm.pdf

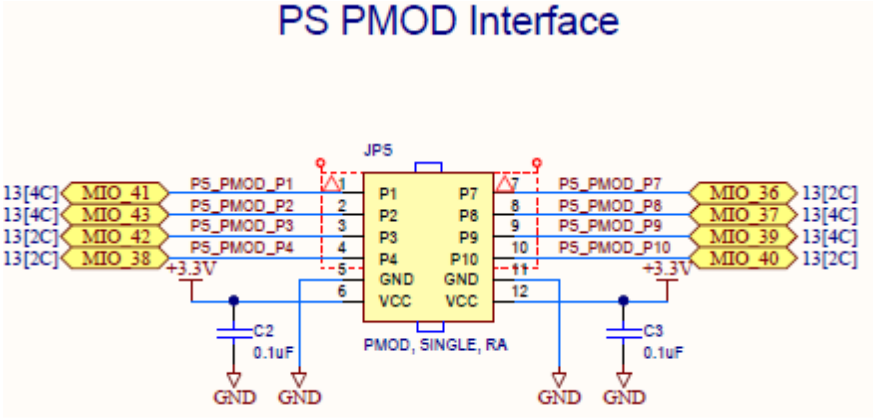

Figure 13 – JP5, PS PMOD

Port IO NAME	TRM SPI0	TRM I2C0	TRM I2C1	TRM UART0	TRM UART1	JX3 CONNECTOR
MIO36			SCL		TXD	JX3.81
MIO37			SDA		RXD	JX3.82
MIO38	SCLK	SCL		RXD		JX3.85
MIO39	N_SS[2]	SDA		TXD		JX3.86
MIO40	N_SS[1]		SCL		TXD	JX3.87
MIO41	N_SS[0]		SDA		RXD	JX3.88
MIO42	MISO	SCL		RXD		JX3.89
MIO43	MOSI	SDA		TXD		JX3.90

Table 3 – PS PMOD to MIO UltrZed SOM Table mapping

2.7 Dual USB-UART Ports – J2

A micro USB connector provides the connection to the dual USB UART. The PHY interface IC is Silicon Labs CP2105 dual USB-UART device. The port has been configured for persistence, allowing the device to remain enumerated even when the Carrier Card's power is turned off.

- USB 2.0 compliant with royalty free drivers available for download.
- VDD and VIO are attached together to provide a persistent USB connection. When a host PC is attached, VBUS is used to generate VDD. No other board power is needed for the UART to be turned on. However, note that LEDs D2 & D4 are not operational until the board is powered on.
- LEDs: D2 and D4 indicate when the device is in suspend mode. By default the pins are active low during a suspend state. These pins are user programmable, and if desired, the polarity can be reversed allowing the LEDs to be on during normal operation and extinguish during suspend. Please refer to the Silicon Labs CP2105 datasheet for further information. https://products.avnet.com/shop/en/ema/uart/cp2105-f01-gmr-3074457345626208393
- Port 0 is connected to Bank 501 PS MIO[34:35], RXD, TXD and are level translated via MOSFETs. These signals are swapped on the carrier creating a null-modem connection.
- Port 1 is connected to Bank 501 PS MIO[32:33], TXD, RXD and are level translated via MOSFETs. These signals are swapped on the carrier creating a null-modem connection.
- GPIO signals or Modem control signals are not used and are brought out to a test pad for user convenience.
- The UART reset pin has an RC time delay from power up. This pin is also be controlled by the SOM's CC_RESET_OUT_N signal when R13 is placed.
- A Vendor ID (VID) is not programmed into the OTP ROM. The device uses the default VID provided by Silicon Labs.
- A unique PID (Product ID) can be programmed in via the USB interface by the user. To accomplish this, a 4.7uF cap is required between NC/DCD_ECI/VPP pin and ground as shown below. Upon completion of programming, the capacitor should be removed.
- ESD device D3 is used on the USB D+ and D- lines for ESD protection.
- Impedance is 45Ω single ended and 90Ω differential (USB_UART_P/N).

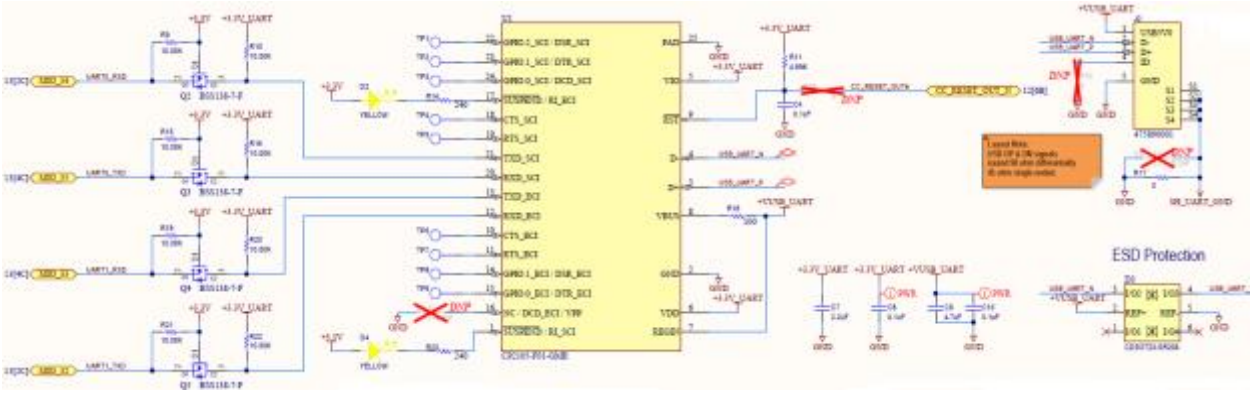

Figure 14 – U1, Dual USB UART

Port IO Name:	UART Signal Name:	JX3 Pin #:
MIO_32	MIO_32.UART1_TXD	77
MIO_33	MIO_33.UART1_RXD	78
MIO_34	MIO_34.UART0_RXD	79
MIO_35	MIO_35.UART0_TXD	80

Table 4 – UART Table

2.8 PS microSD Card Connector – J1

The PS MIO[44:51] pins are used to interface to a micro-SD card connector. The interface operates at 3.3V. Since microSD cards do not have a Write-Protect (WP) pin, the PS SD controller WP signal (MIO[44]) must be pulled down to ground during normal operation (allowing read and writes to the SD card). If the user wants to invoke a Write Protect, place JP1 which will prevent the SD card from being written to.

- JP1 WP Jumper used to allow Write Protect emulation for microSD cards if needed. The default position for this jumper is Not Placed, thereby disabling Write Protect function.
- The interface is routed at 50 ohms single ended.
- The interface speed is rated as Class 10 (10 MB/s) which does not support the latest SD 3.01 specification of up to 50 MB/s.

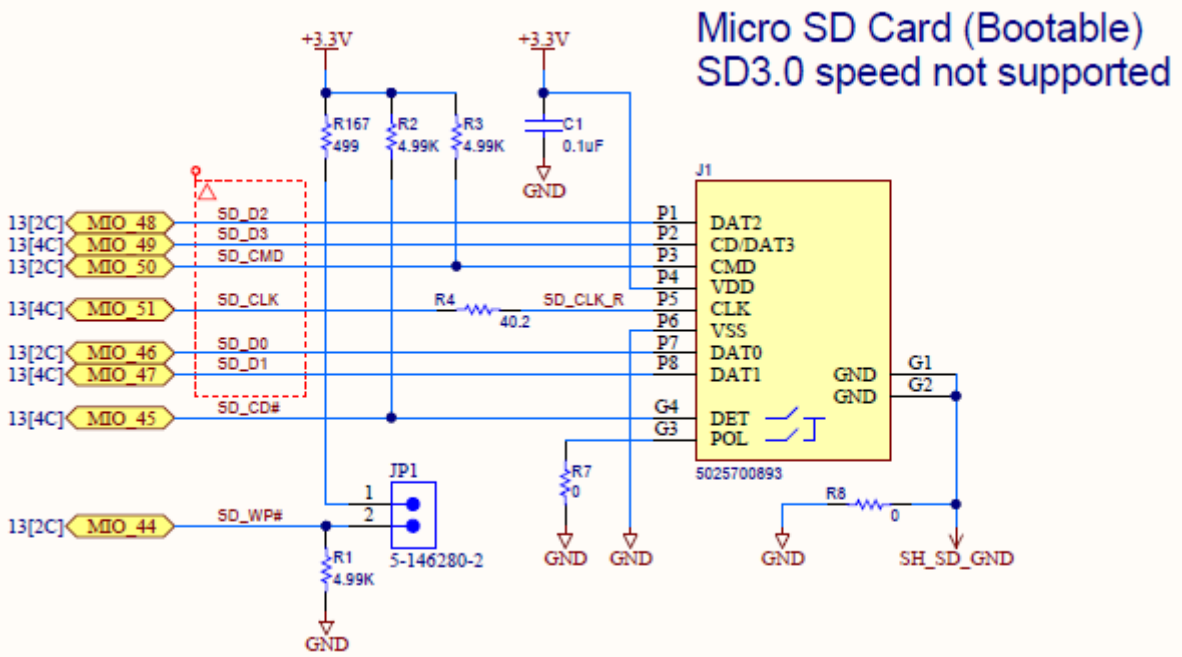

Figure 15 – J1, Micro SD Card interface

Port IO Name:	J4 Signal Name:	JX3 Pin #:
MIO_44	SD_WP	93
MIO_45	SD_CD	94
MIO_46	SD_D0	95
MIO_47	SD_D1	96
MIO_48	SD_D2	97
MIO_49	SD_D3	98
MIO_50	SD_CMD	99
MIO_51	SD_CLK	100

Table 5 – PS microSD card table

2.9 PS User LED – D1

A red PS user LED is provided on the carrier. It is an active high LED and buffered with a NPN BJT. This LED is connected to the MIO[26] pin and operated at 3.3V I/O.

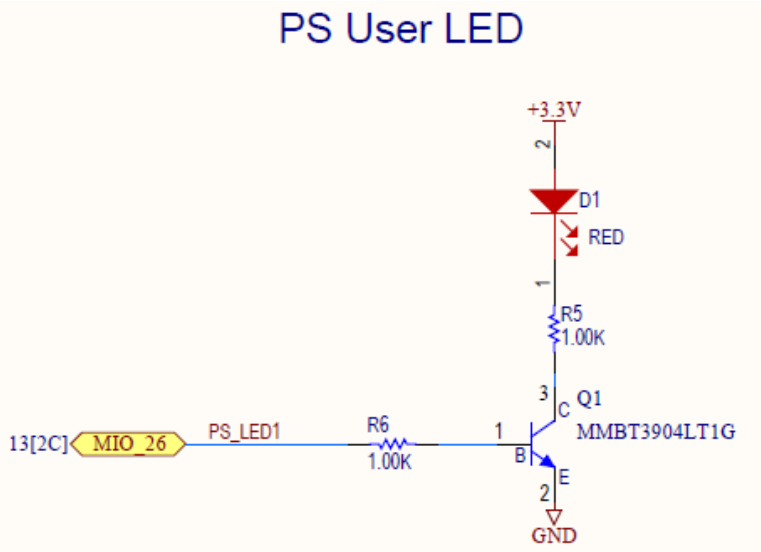

Figure 16 – D1, PS User LED

2.10 PL User Switches, SW1 - SW4 & SW5

The Carrier Card has 12 user switches. Four pushbutton switches SW1-SW4, and an 8 pin DIP slide switch, SW5.

- SW5 provides 8 user slide switches. When slid to the ON position (closed), SW5 outputs are pulled high to a level of +1.6V via a 240 ohm current limiting resistor pack. When in the OFF position (open), SW5 outputs are pulled low via a 4.7K resistor pack.
- SW1 – SW4 pushbutton switches are normally open when not depressed and are pulled low via a 10K resistor. When SW1 – SW4 are depressed they provide a high level of +1.6V via the current limiting 240 ohm resistors. These signals are decoupled using a 0.1uF capacitor.

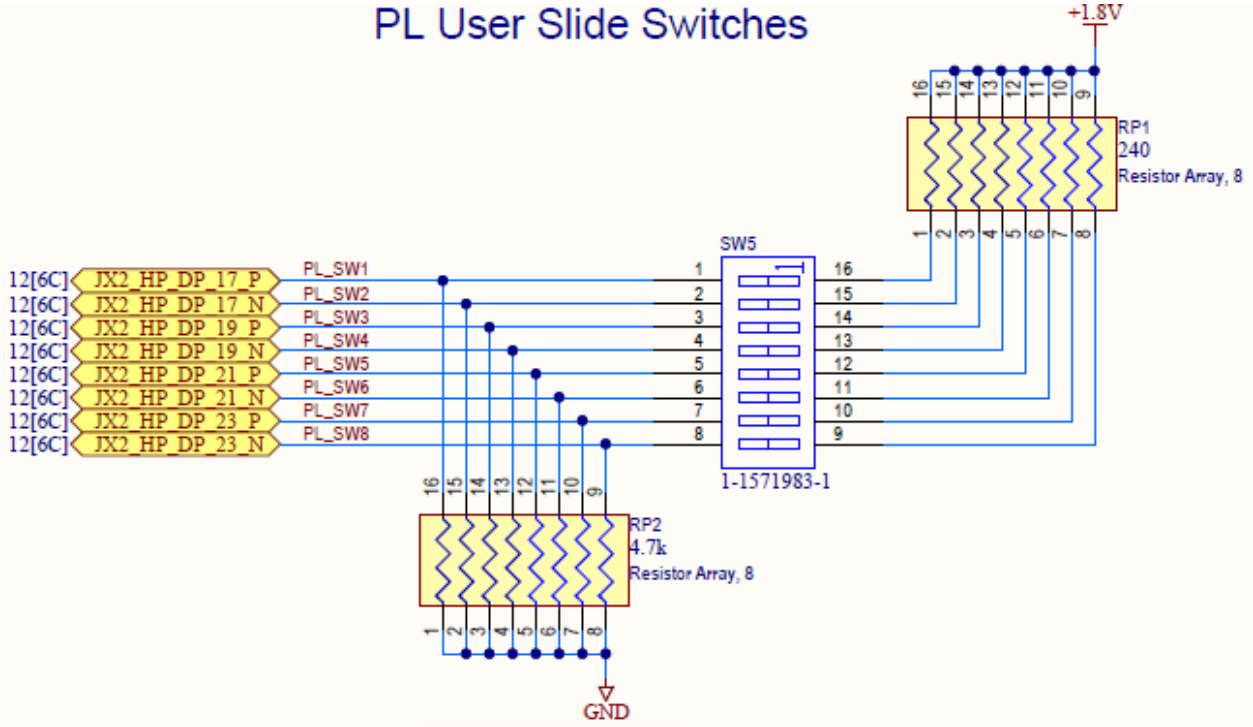

Figure 17 – SW5, PL user 8 position slide switch

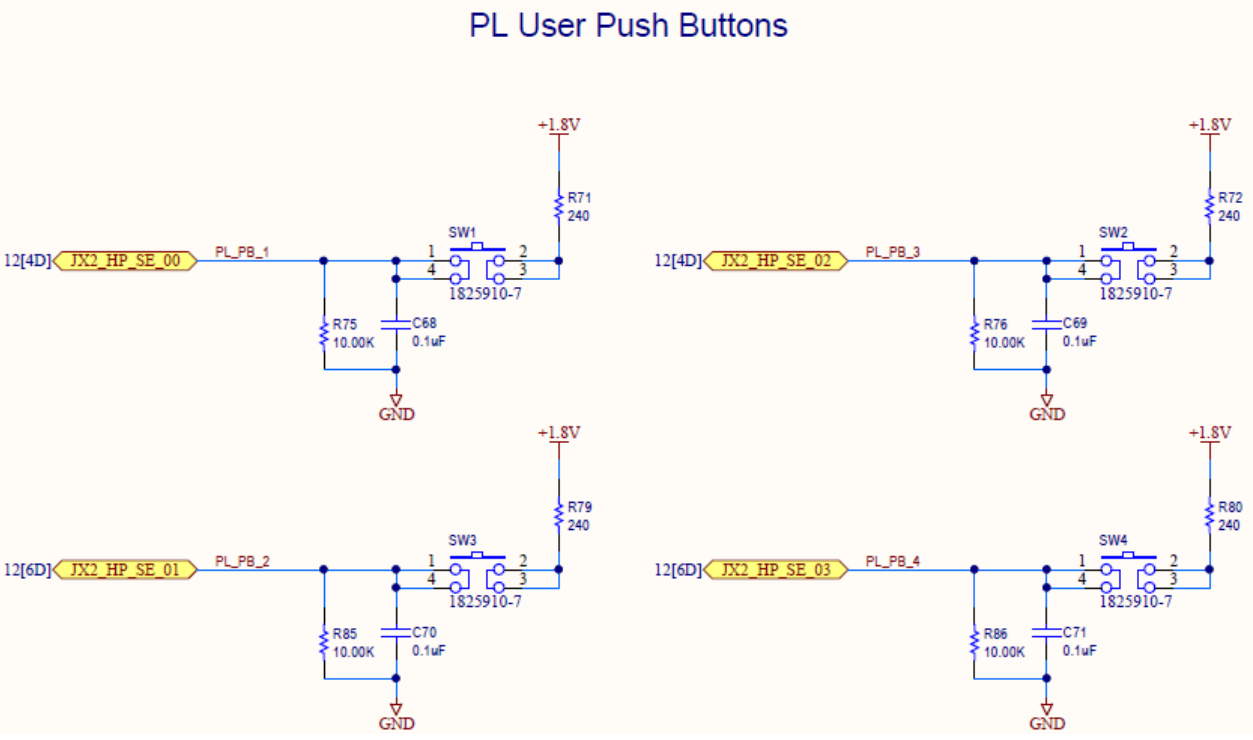

Figure 18 – SW1-SW4, PL user 4 push button switches

Port IO Name:	JX1 Pin #:
JX2_HP_SE_00	135
JX2_HP_SE_01	134
JX2_HP_SE_02	137
JX2_HP_SE_03	136
JX2_HP_DP_17_P	92
JX2_HP_DP_17_N	94
JX2_HP_DP_19_P	98
JX2_HP_DP_19_N	100
JX2_HP_DP_21_P	104
JX2_HP_DP_21_N	106
JX2_HP_DP_23_P	110
JX2_HP_DP_23_N	112

Table 6 – PL User Switch Table

2.11 PL User LEDs – D12:D19

The UltraZed PCIe Carrier Card provides 8 PL user LEDs. These active high LEDs are connected to a HP bank via JX2 connector and operated at 1.8V I/O. These LEDs are buffered with NPN BJTs to minimize the current sourced by the SoC and to provided adequate LED Vf bias.

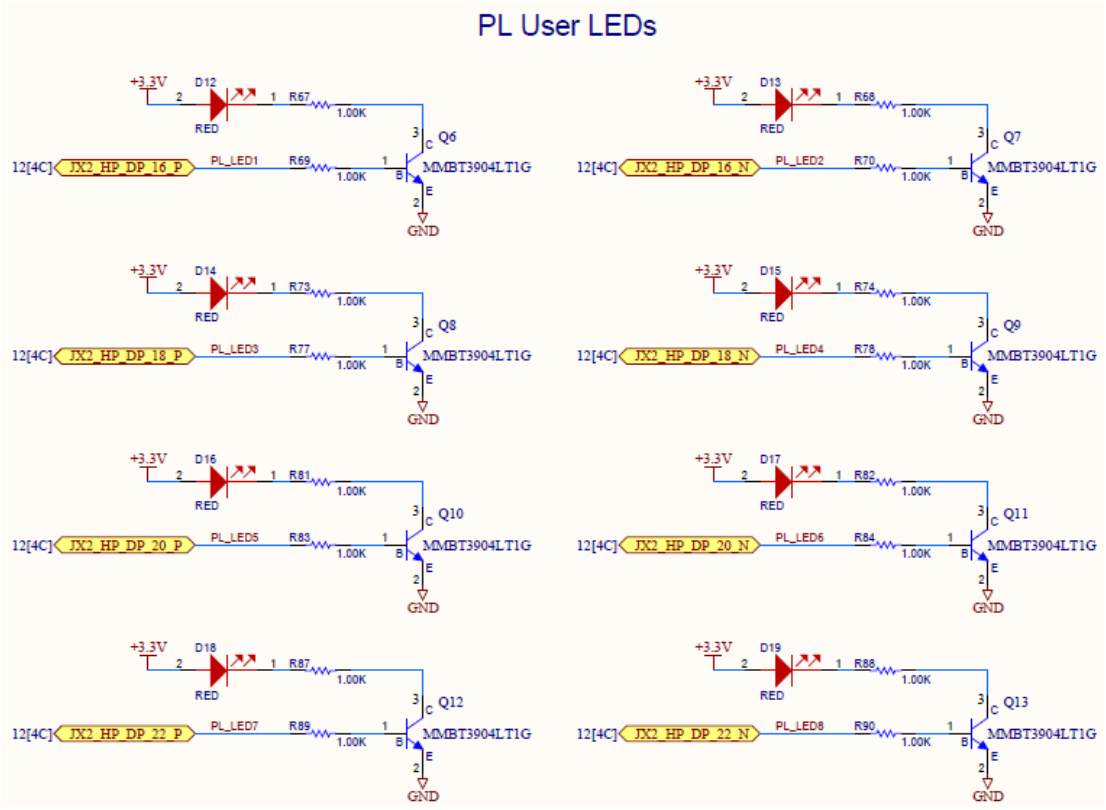

Figure 19 – PL User LEDs

Port IO Name:	JX1 Pin #:
JX2_HP_DP_16_P	93
JX2_HP_DP_16_N	95
JX2_HP_DP_18_P	99
JX2_HP_DP_18_N	101
JX2_HP_DP_20_P	105
JX2_HP_DP_20_N	107
JX2_HP_DP_22_P	111
JX2_HP_DP_22_N	113

Table 7 – PL user LED table

2.12 PL PMOD Headers – JX2, JA & JB

The UltraZed PCIe Carrier Card has 2 +3.3V PL PMOD headers configured in a dual-PMOD connection and routed to the JX2 connector.

- JA and JB PMOD signals are routed to within 10 mils within the single connector.
- JA and JB PMOD connector signals are routed within 25 mils of each other per pair.
- JA and JB PMOD signals are routed to within 50 mils of each other throughout both connectors with reference to JX2.
- The PMOD signals total route length do not exceed 4500 mils from the JX2 connector.
- All PMOD signals are Single Ended and routed at 50 ohms nominal impedance.

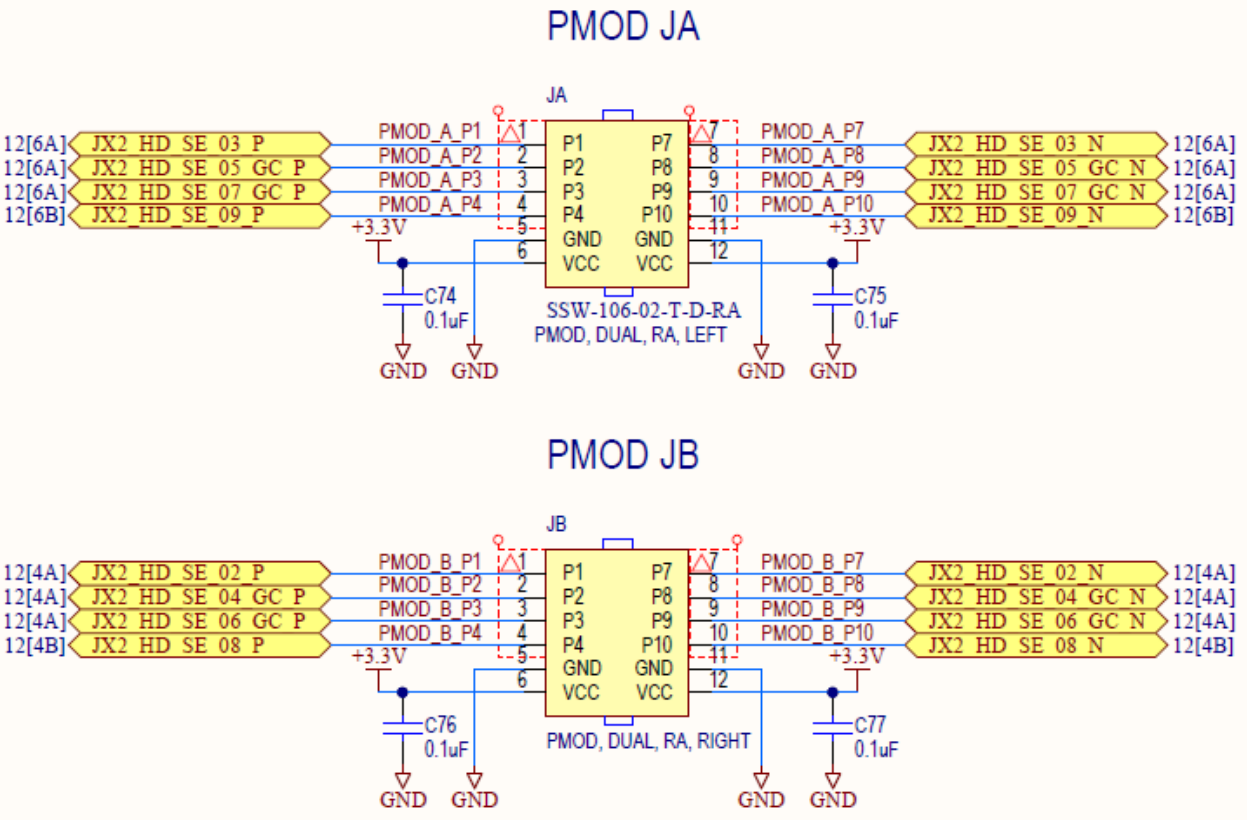

Figure 20 – JA & JB, JX2 PL PMODs

Port IO Name:	JX2 Pin #:	PMOD PIN #
JX2_HD_SE_03_P	14	JA-1
JX2_HD_SE_03_N	16	JA-7
JX2_HD_SE_05_GC_P	20	JA-2
JX2_HD_SE_05_GC_N	22	JA-8
JX2_HD_SE_07_GC_P	26	JA-3
JX2_HD_SE_07_GC_N	28	JA-9
JX2_HD_SE_09_P	32	JA-4
JX2_HD_SE_09_N	34	JA-10
JX2_HD_SE_02_P	13	JB-1
JX2_HD_SE_02_N	15	JB-7
JX2_HD_SE_04_GC_P	19	JB-2
JX2_HD_SE_04_GC_N	21	JB-8
JX2_HD_SE_06_GC_P	25	JB-3
JX2_HD_SE_06_GC_N	27	JB-9
JX2_HD_SE_08_P	31	JB-4
JX2_HD_SE_08_N	33	JB-10

Table 8 – JX2 PL PMOD signal pin table

2.13 FMC Header – JX1, 2 CON1A-E

The PCIe Carrier Card features a LPC FMC header for FMC development use. The Geographical Address of the FMC slot can be configured via the use of JP10 and JP11. In the default configuration JP10 and JP11 are set using jumpers at location pins 2-3. This sets GA[0:1] low, setting the FMC geographical address to 00. When the jumpers are placed at location 1-2 the respective line is pulled up to 3.3V, setting a logic high.

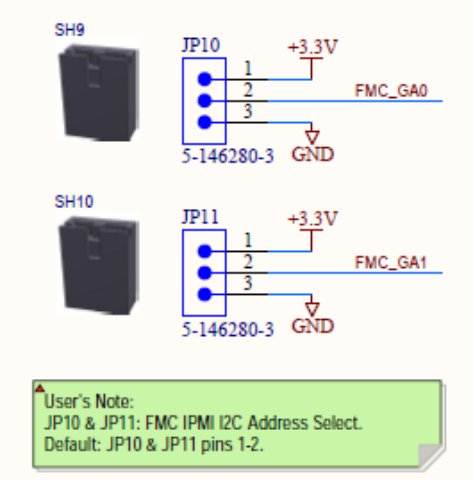

Figure 21 – JP10 & JP11, FMC Geographical Address jumpers

	K	J	H	G	F	E	D	C	B	A
1	NC	NC	VREF_A_M2C	GND	NC	NC	PG_C2M	GND	NC	NC
2	NC	NC	PRSNT_M2C_L	CLK1_M2C_P	NC	NC	GND	DP0_C2M_P	NC	NC
3	NC	NC	GND	CLK1_M2C_N	NC	NC	GND	DP0_C2M_N	NC	NC
4	NC	NC	CLK0_M2C_P	GND	NC	NC	GBTCLK0_M2C_P	GND	NC	NC
5	NC	NC	CLK0_M2C_N	GND	NC	NC	GBTCLK0_M2C_N	GND	NC	NC
6	NC	NC	GND	LA00_P_CC	NC	NC	GND	DP0_M2C_P	NC	NC
7	NC	NC	LA02_P	LA00_N_CC	NC	NC	GND	DP0_M2C_N	NC	NC
8	NC	NC	LA02_N	GND	NC	NC	LA01_P_CC	GND	NC	NC
9	NC	NC	GND	LA03_P	NC	NC	LA01_N_CC	GND	NC	NC
10	NC	NC	LA04_P	LA03_N	NC	NC	GND	LA06_P	NC	NC
11	NC	NC	LA04_N	GND	NC	NC	LA05_P	LA06_N	NC	NC
12	NC	NC	GND	LA08_P	NC	NC	LA05_N	GND	NC	NC
13	NC	NC	LA07_P	LA08_N	NC	NC	GND	GND	NC	NC
14	NC	NC	LA07_N	GND	NC	NC	LA09_P	LA10_P	NC	NC
15	NC	NC	GND	LA12_P	NC	NC	LA09_N	LA10_N	NC	NC
16	NC	NC	LA11_P	LA12_N	NC	NC	GND	GND	NC	NC
17	NC	NC	LA11_N	GND	NC	NC	LA13_P	GND	NC	NC
18	NC	NC	GND	LA16_P	NC	NC	LA13_N	LA14_P	NC	NC
19	NC	NC	LA15_P	LA16_N	NC	NC	GND	LA14_N	NC	NC
20	NC	NC	LA15_N	GND	NC	NC	LA17_P_CC	GND	NC	NC
21	NC	NC	GND	LA20_P	NC	NC	LA17_N_CC	GND	NC	NC
22	NC	NC	LA19_P	LA20_N	NC	NC	GND	LA18_P_CC	NC	NC
23	NC	NC	LA19_N	GND	NC	NC	LA23_P	LA18_N_CC	NC	NC
24	NC	NC	GND	LA22_P	NC	NC	LA23_N	GND	NC	NC
25	NC	NC	LA21_P	LA22_N	NC	NC	GND	GND	NC	NC
26	NC	NC	LA21_N	GND	NC	NC	LA26_P	LA27_P	NC	NC
27	NC	NC	GND	LA25_P	NC	NC	LA26_N	LA27_N	NC	NC
28	NC	NC	LA24_P	LA25_N	NC	NC	GND	GND	NC	NC
29	NC	NC	LA24_N	GND	NC	NC	TCK	GND	NC	NC
30	NC	NC	GND	LA29_P	NC	NC	TDI	SCL	NC	NC
31	NC	NC	LA28_P	LA29_N	NC	NC	TDO	SDA	NC	NC
32	NC	NC	LA28_N	GND	NC	NC	3P3VAUX	GND	NC	NC
33	NC	NC	GND	LA31_P	NC	NC	TMS	GND	NC	NC
34	NC	NC	LA30_P	LA31_N	NC	NC	TRST_L	GA0	NC	NC
35	NC	NC	LA30_N	GND	NC	NC	GA1	12P0V	NC	NC
36	NC	NC	GND	LA33_P	NC	NC	3P3V	GND	NC	NC
37	NC	NC	LA32_P	LA33_N	NC	NC	GND	12P0V	NC	NC
38	NC	NC	LA32_N	GND	NC	NC	3P3V	GND	NC	NC
39	NC	NC	GND	VADJ	NC	NC	GND	3P3V	NC	NC
40	NC	NC	VADJ	GND	NC	NC	3P3V	GND	NC	NC
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

Table 9 – CON1 FMC connector pinout table

FMC Signal Net Name:	CON1 A Port IO Name:	JX1 Pin #:
N.C.	C2 – N.C.	N.C.
N.C.	C3 – N.C.	N.C.
N.C.	C6 – N.C.	N.C.
N.C.	C7 – N.C.	N.C.
FMC_LA06_P	JX1_HP_DP_40_P	129
FMC_LA06_N	JX1_HP_DP_40_N	131
FMC_LA10_P	JX1_HP_DP_34_P	111
FMC_LA10_N	JX1_HP_DP_34_N	113
FMC_LA14_P	JX1_HP_DP_28_P	93
FMC_LA14_N	JX1_HP_DP_28_N	95
FMC_LA18_CC_P	JX1_HP_DP_19_GC_P	62
FMC_LA18_CC_N	JX1_HP_DP_19_GC_N	64
FMC_LA27_P	JX1_HP_DP_14_P	51
FMC_LA27_N	JX1_HP_DP_14_N	53

Table 10 – JX1 FMC CON1 A Signals

FMC Signal Net Name:	CON1 B Port IO Name:	JX1 Pin #:
FMC_LA01_CC_P	JX1_HP_DP_36_GC_P	117
FMC_LA01_CC_N	JX1_HP_DP_36_GC_N	119
FMC_LA05_P	JX1_HP_DP_38_P	123
FMC_LA05_N	JX1_HP_DP_38_N	125
FMC_LA09_P	JX1_HP_DP_32_P	105
FMC_LA09_N	JX1_HP_DP_32_N	107
FMC_LA13_P	JX1_HP_DP_30_P	99
FMC_LA13_N	JX1_HP_DP_30_N	101
FMC_LA17_CC_P	JX1_HP_DP_18_GC_P	63
FMC_LA17_CC_N	JX1_HP_DP_18_GC_N	65
FMC_LA23_P	JX1_HP_DP_16_P	57
FMC_LA23_N	JX1_HP_DP_16_N	59
FMC_LA26_P	JX1_HP_DP_12_P	45
FMC_LA26_N	JX1_HP_DP_12_N	47

Table 11 – JX1 FMC CON1 B Signals

FMC Signal Net Name:	CON1 C Port IO Name:	JX1 Pin #:
FMC_CLK1_M2C_P	JX1_HP_DP_20_GC_P	69
FMC_CLK1_M2C_N	JX1_HP_DP_20_GC_N	71
FMC_LA00_CC_P	JX1_HP_DP_37_GC_P	116
FMC_LA00_CC_N	JX1_HP_DP_37_GC_N	118
FMC_LA03_P	JX1_HP_DP_39_P	122
FMC_LA03_N	JX1_HP_DP_39_N	124
FMC_LA08_P	JX1_HP_DP_33_P	104
FMC_LA08_N	JX1_HP_DP_33_N	106
FMC_LA12_P	JX1_HP_DP_29_P	92
FMC_LA12_N	JX1_HP_DP_29_N	94
FMC_LA16_P	JX1_HP_DP_25_P	80
FMC_LA16_N	JX1_HP_DP_25_N	82
FMC_LA20_P	JX1_HP_DP_17_P	56
FMC_LA20_N	JX1_HP_DP_17_N	58
FMC_LA22_P	JX1_HP_DP_13_P	44
FMC_LA22_N	JX1_HP_DP_13_N	46
FMC_LA25_P	JX1_HP_DP_09_P	32
FMC_LA25_N	JX1_HP_DP_09_N	34
FMC_LA29_P	JX1_HP_DP_10_P	39
FMC_LA29_N	JX1_HP_DP_10_N	41
FMC_LA31_P	JX1_HP_DP_06_P	27
FMC_LA31_N	JX1_HP_DP_06_N	29
FMC_LA33_P	JX1_HP_DP_02_P	15
FMC_LA33_N	JX1_HP_DP_02_N	17

Table 12 – JX1 FMC CON1 C Signals

FMC Signal Net Name:	CON1 D Port IO Name:	JX(n) Pin #:
FMC_CLK0_M2C_P	JX2_HP_DP_27_GC_P	122
FMC_CLK0_M2C_N	JX2_HP_DP_27_GC_N	124
FMC_LA02_P	JX1_HP_DP_41_P	128
FMC_LA02_N	JX1_HP_DP_41_N	130
FMC_LA04_P	JX1_HP_DP_35_P	110
FMC_LA04_N	JX1_HP_DP_35_N	112
FMC_LA07_P	JX1_HP_DP_31_P	98
FMC_LA07_N	JX1_HP_DP_31_N	100
FMC_LA11_P	JX1_HP_DP_27_P	86
FMC_LA11_N	JX1_HP_DP_27_N	88
FMC_LA15_P	JX1_HP_DP_23_P	74
FMC_LA15_N	JX1_HP_DP_23_N	76
FMC_LA19_P	JX1_HP_DP_15_P	50
FMC_LA19_N	JX1_HP_DP_15_N	52
FMC_LA21_P	JX1_HP_DP_11_P	38
FMC_LA21_N	JX1_HP_DP_11_N	40
FMC_LA24_P	JX1_HP_DP_07_P	26
FMC_LA24_N	JX1_HP_DP_07_N	28
FMC_LA28_P	JX1_HP_DP_08_P	33
FMC_LA28_N	JX1_HP_DP_08_N	35
FMC_LA30_P	JX1_HP_DP_04_P	21
FMC_LA30_N	JX1_HP_DP_04_N	23
FMC_LA32_P	JX1_HP_DP_00_P	9
FMC_LA32_N	JX1_HP_DP_00_N	11

Table 13 – JX(n) FMC CON1 D Signals

FMC Signal Net Name:	CON1 E Port IO Name:	JX2 Pin #:
FMC_PG_C2M	FMC_PG_C2M	N/A
FMC_PRSNT_M2C#	JX2_HD_SE_00_N	9
FMC_GA0	FMC_GA0	N/A
FMC_GA1	FMC_GA1	N/A
FMC_IPM_SCL	JX2_HD_SE_01_P	8
FMC_IPMI_SDA	JX2_HD_SE_01_N	10
FMC_TCK	FMC_TCK	N/A
FMC_TDI	FMC_TDI	N/A
FMC_TDO	FMC_TDO	N/A
FMC_TMS	FMC_TMS	N/A
FMC_TRST#	JX2_HD_SE_00_P	7
+12.0V	12P0V	N/A
+3.3V	3P3V	N/A
+3.3V	3P3VAUX	N/A
+1.8V	VADJ	N/A

Table 14 – FMC CON1 E Signals

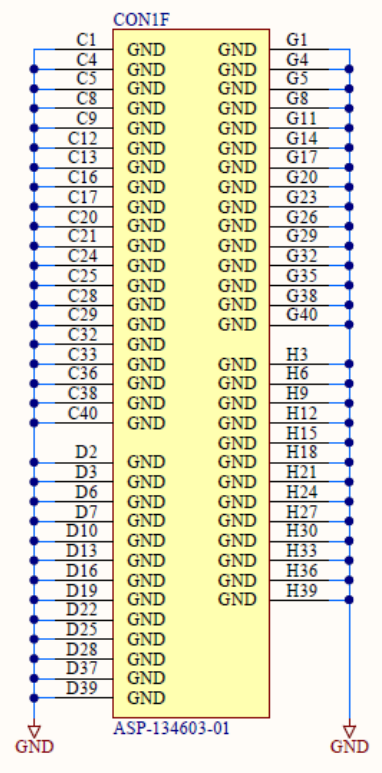

Table 15 – JX1 FMC CON1 F Grounds

2.14 Carrier Card I2C Interface

The UltraZed SOM provides a master I2C bus (CC_SDA, CC_SCL, and CC_INT_N) to the PCIe Carrier Card via the JX3 connector so that software can communicate with all I2C devices on the UltraZed SOM as well as the I2C devices on the PCIe Carrier Card using a single I2C interface.

- U5, IDT clock synthesizer, 0xD4 or 0xD0
- U6, MAC ID EEPROM, 0xA2

The CC_SDA and CC_SCL pins are pulled up to the 1.8V rail via 1K resistors on the UltraZed PCIe Carrier Card. Although a Carrier Card can assert the active low CC_INT signal to interrupt the MPSoC processor, this signal is not used on the PCIe Carrier Card and is pulled up to +1.8V via a 10K resistor, R98.

The I2C interface is used to access the following Carrier Card devices:

- U5, the IDT differential clock generator at address 0xD4.
- U6, the MAC Address device at address 0xA2.
- The I2C interface pullup resistor values are 1K for 400 KHz operation. The 1K value has been proven to be necessary when I2C bus is attached to U5. While this deviates from the standard I2C pullup value of 2K value it causes no detrimental effects to the project.
- Routed impedance is 50Ω.

PCIe Net Name:	JX3 Pin #:
CC_SDA	41
CC_SCL	44
CC_INT_N	68

Table 16 – I2C bus connections

2.15 Clock Generator – U5, I2C address 0xD4 (default)

The PCIe Carrier Card has a pre-programmed IDT 5P49V5935B521LTGI clock synthesizer on board. This clock IC generates the necessary LVDS clocks for the interfaces listed below. This part contains an internal 25 MHz crystal clock source which eliminates the need for an external clock. The part is capable of providing multiple clock frequencies, output types, spread spectrum, phase shift control and slew rate control.

The IDT 5P49V5935B521LTGI is a custom part number with the output frequencies pre-programmed into the device via an OTP register. The device runs at 1.8V. In the default configuration (Mode 3), the clock generates the following frequencies on power up.

- Default configuration settings:
  - 1.8V power
  - Spread Spectrum: off
  - Reference clock: 25 MHz internal
  - Phase Shift: 0 degrees
  - Output type: LVDS
  - Slew Rate: set to 1.0x

- Default (Mode 3) output frequencies:
  - Output 0 – Used for configuration only.
  - Output 1 – 52MHz USB 3.0 clock connected to the JX3 GTR_REFCLK[2]
  - Output 2 – 125MHz SATA GTR[1] clock connected to the JX3 GTR_REFCLK[1]
  - Output 3 – 27 MHz DP Display Port clock connected to the JX3 GTR_REFCLK[3]
  - Output 4 – 300MHz PL system clock connected to the JX2 JX2_HP_DP_GC_P/N (Global Clock Input pair). Note R51 placed close to JX2 connector for termination.

NOTE: The PCIe edge clock (PCIE_REFCLK_P/N) is routed from PCIe edge connector to JX3 GTR_REFCLK0_P/N, pins 38 & 40. See PCIe interface section for more information.

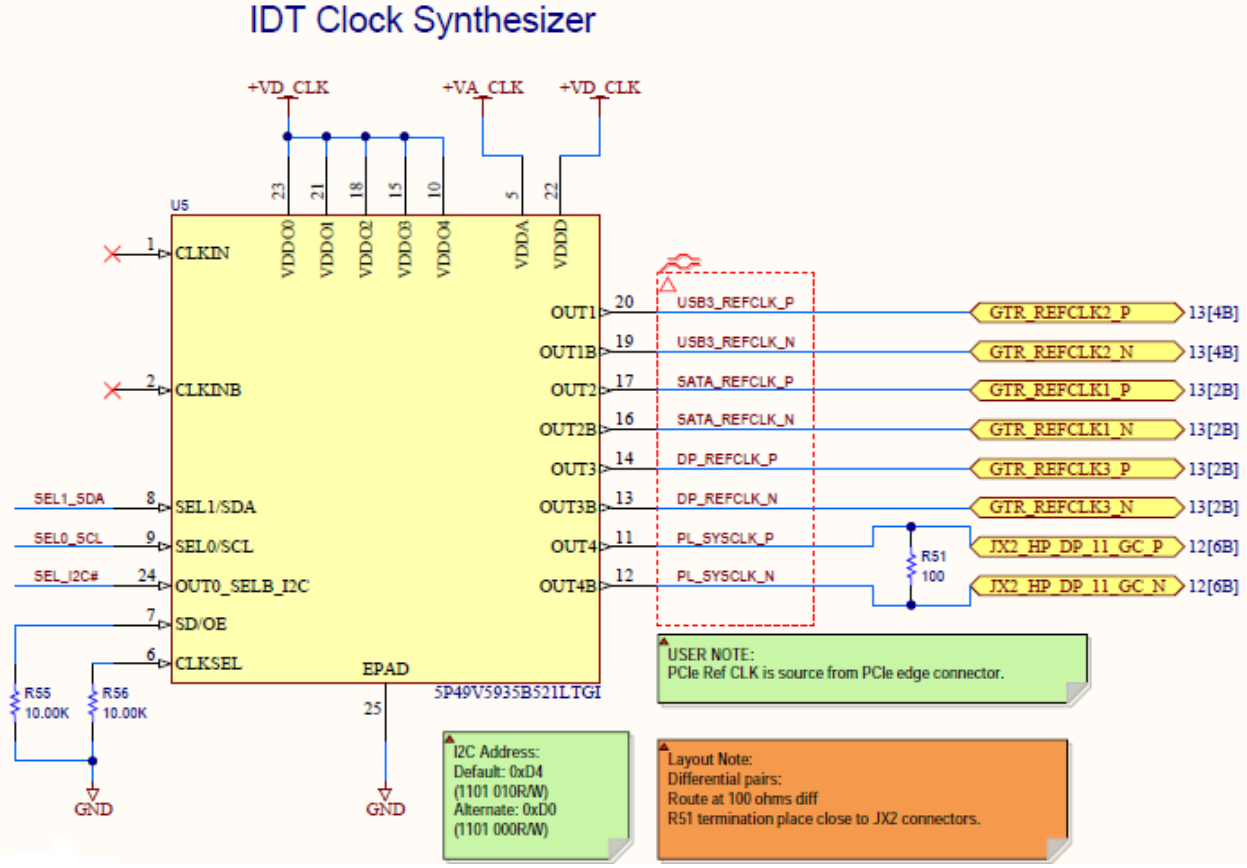

Figure 22 – U5, IDT Clock Synthesizer

Port IO Name:	PCIe Signal Net Name:	JX Pin #:
GTR_REFCLK0_P	PCIE_REFCLK_P	JX3.38
GTR_REFCLK0_N	PCIE_REFCLK_N	JX3.40
GTR_REFCLK1_P	SATA_REFCLK_P	JX3.33
GTR_REFCLK1_N	SATA_REFCLK_N	JX3.35
GTR_REFCLK2_P	USB3_REFCLK_P	JX3.32
GTR_REFCLK2_N	USB3_REFCLK_N	JX3.34
GTR_REFCLK3_P	DP_REFCLK_P	JX3.27
GTR_REFCLK3_N	DP_REFCLK_N	JX3.29
JX2_HP_DP_11_GC_P	PL_SYSCLK_P	JX2.74
JX2_HP_DP_11_GC_N	PL_SYSCLK_N	JX2.76

Table 17 – PCIe Carrier Card clock table

2.15.1 Clock Configuration jumpers JP6, JP7, JP8

The synthesizer has two methods of configuration: hardware and software. For hardware operation it is configured via JP6, JP7 and JP8. These jumpers select one of four pre-programmed OTP configuration files during power up, see Table 18 – Clock boot configuration table for the other jumper configurable frequencies.

To configure using software, the device must be accessed via the I2C bus and configured each time the board is powered on.

- Mode 3 is the default frequency selection when the board is manufactured. The IDT part has internal weak pull down resistors on SEL0 and SEL1 pins. JP6 is used to select what configuration mode is used when the IC is powered up. JP6 floating (open) boots device into I2C mode. JP6 placed sets the hardware SEL0/1 pin mode. Default mode is JP6 closed to set hardware configuration.
- By default the PCIe Carrier Card uses Mode Three, which has the following jumper positions: JP7 & JP8 placed on pins 1-2 and JP6 closed.
- I2C software configuration mode: the user can configure the IDT part using the I2C bus. To configure the IDT part for different frequencies, JP7 and JP8 jumpers must be placed at positions 2 – 3 and jumper JP6 removed.

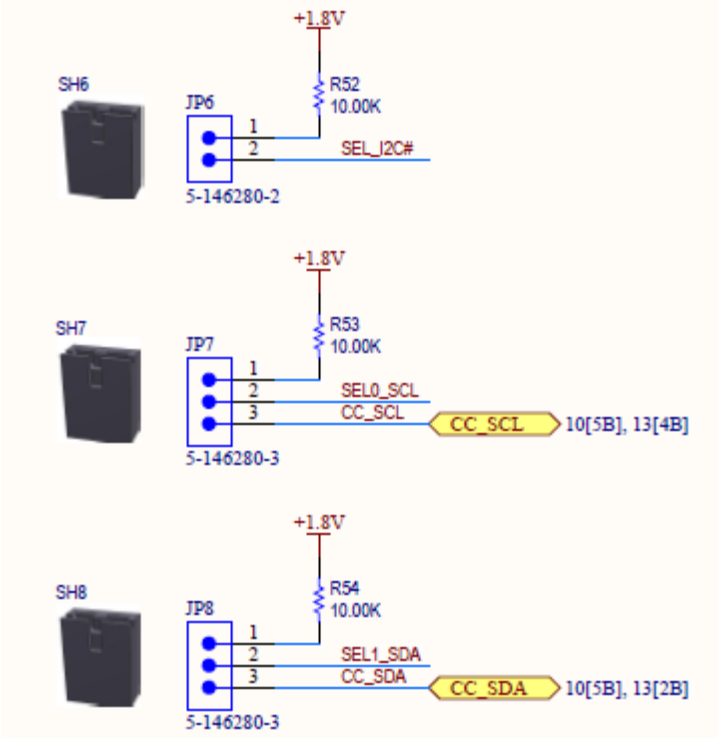

Figure 23 – JP6-JP8 Clock configuration jumpers

Frequency Overview

Parameter	Configuration 0	Configuration 1	Configuration 2	Configuration 3	Units
Input	25	25	25	(default configuration)	MHz
Output 0	25	25	25	25	MHz
Output 1	40	48	50	52	MHz
Output 2	125	125	125	125	MHz
Output 3	27	27	27	27	MHz
Output 4	300	300	300	300	MHz

Table 18 – Clock boot configuration table

Configuration 3 Parameters: SEL[1:0] = 11

Parameter	Output 0	Output 1	Output 2	Output 3	Output 4	Units
Input Frequency	25	25	25	25	25	MHz
Default Output Status	(Unused Output)	On	On	On	On	
VDDO Voltage	1.8	1.8	1.8	1.8	1.8	V
Output Type	LVCMOS	LVDS	LVDS	LVDS	LVDS	
Frequency	25	52	125	27	300	MHz
Spread Spectrum	Off	Off	Off	Off	Off	
Spread Spectrum Modulation						%
Slew Rate	1.0x	1.0x	1.0x	1.0x	1.0x	V/s
Phase Shift	0	0	0	0	0	Degrees

Table 19 – Mode 3 clock parameters

2.16 PCIe Edge Connector, P1

The UltraZed-EG PCIe Carrier Card uses the UltraZed-EG SOM PS GTR[0] transceiver for the PCIe x1 Endpoint interface with a maximum data rate of 5.0 GT/s. The GTR_REFCLK[0] of the UltraZed-EG SOM is connected to the PCIe edge connector 100 MHz clock output, see Table 17 – PCIe Carrier Card clock table. The PCIe edge connector reset (PERST#) is connected to the MIO[31] of the UltraZed-EG SOM JX3 connector. See Figure 24 – P1, PCIe Gen 2 x1 Endpoint interface.

- The carrier is not required to be plugged into a PCIe slot for normal operation. However, it has been provided to assist in the development of PCIe based SOM products. When the carrier is inserted into a PCIe slot, 12V power from the host PCIe slot can be used for low power applications (10 Watts or less per the PCIe specification Version 1.1, unless the user configures the PCIe to 25W via motherboard BIOS or Software). The PCIe interface includes a 12V power circuit, control signals and a single data lane (differential TX and RX) and one differential PCIe clock.
- The PRSNT signals are used to identify the lane width (x1) of the PCIe bus for the host motherboard. The carrier ties the PRSNT1# and PRSNT2# signals together to accomplish this. The host motherboard has pull-up and pull-down resistors on these signals so the carrier does not require any other special configurations to enumerate as a single lane PCIe device when plugged into a host PC.

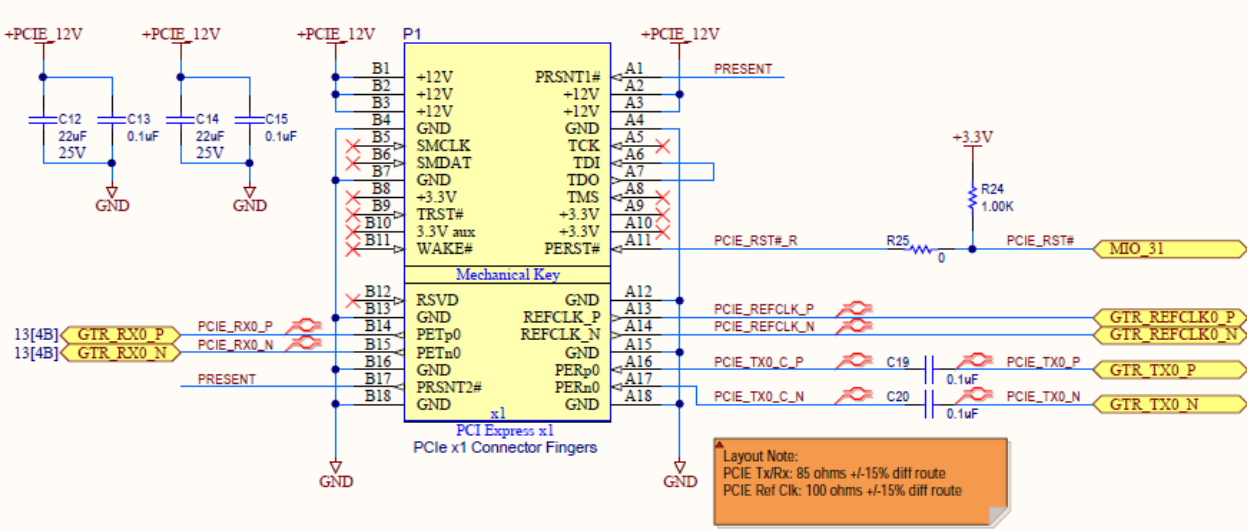

Figure 24 – P1, PCIe Gen 2 x1 Endpoint interface

2.17 EUI-48 MAC Address Device – U6, I2C address 0xA2 (default)

The carrier has a 1.8V MicroChip 24AA025E48T-I/OT I2C MAC Address device with the Global Identifier EUI-48™. This device is connected to the master I2C bus on the Carrier Card. The address can be configured via JT1 and JT2 (0402 SMT resistor pads). The default position is 4.7K ohm resistors placed at locations 1-2, yielding a default address set of 0xA2.

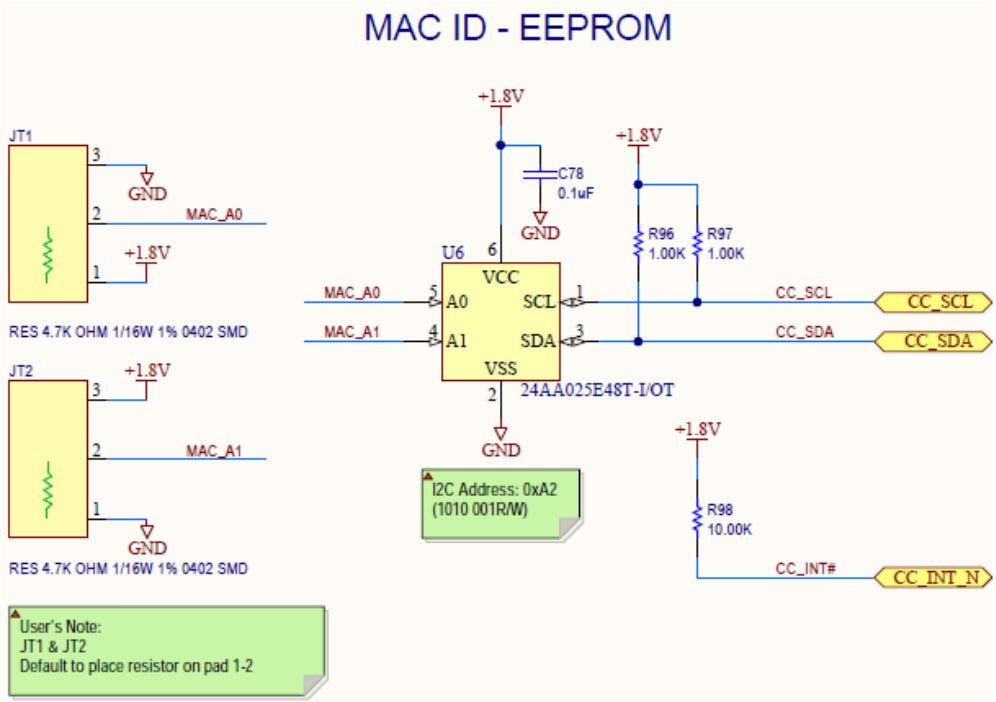

Figure 25 – U6, 2K MAC EUI-48 EEPROM

2.18 SOM Reset Input – SW6

SW6 is a push switch used to generate an active low SOM_RST_N signal. This signal is routed to the SOM via JX2.42 and is pulled up on the SOM via the +1.8V rail.

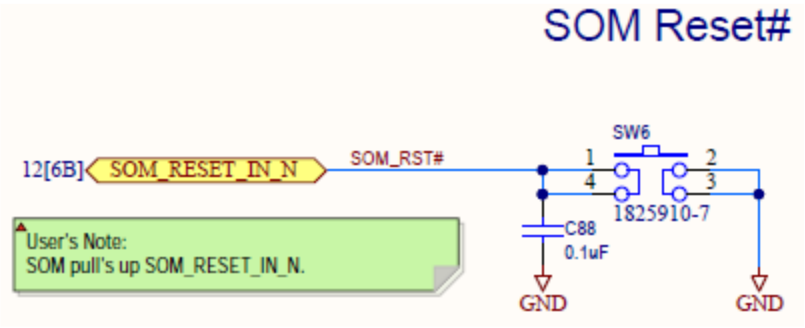

Figure 26 – SW6, SOM_RST_N circuit

2.19 SOM Reset Output

The UltraZed SOM drives an active low reset signal to the Carrier Card (CC_RESET_OUT_N) via JX2 pin 36. The signal is pulled up on the SOM via a 10K resistor tied to +1.8V. This signal can be connected to the dual USB UART for UART reset control via R13.

2.20 JTAG Debug Interfaces

The UltraZed PCIe Carrier Card contains two JTAG debug interfaces to facilitate maximum development flexibility. One is a Digilent SMT2 JTAG module with a micro USB connection. This interface requires a micro USB cable to attach to the host PC. To support all development environments, including those with debuggers and dongles, a PC4 2x7 header has also been provided.

Either interface can be used for PS software debugging and UltraZed SOM PL configuration, QSPI Flash and eMMC memory programming. Below is the JTAG chain diagram.

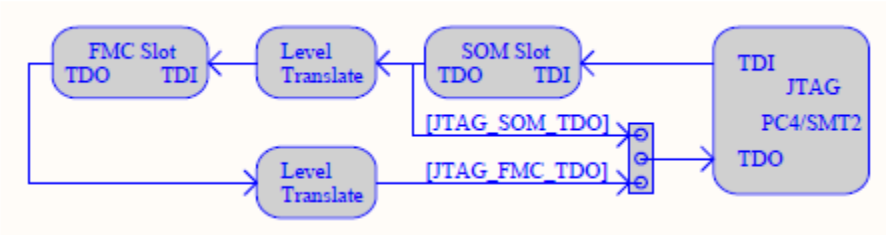

Figure 27 – JTAG Chain diagram

2.20.1 PC4 JTAG Header – J6

The PC4 JTAG header is shown below. The PC4 header VREF pin is connected to the 1.8V rail via D21. The diode is used to prevent back drive onto the 1.8V rail from the JTAG pod.

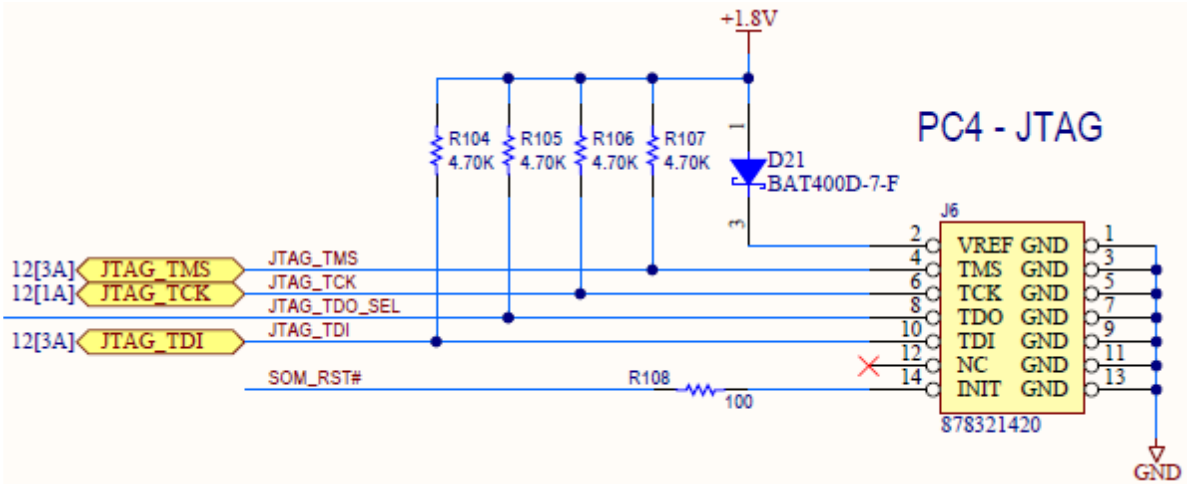

Figure 28 – J6, PC4 JTAG Connector

2.20.2 SMT2 Micro USB JTAG interface – U8

The SMT2 micro USB to JTAG interface is shown below. The 4.70K pullup resistors and 22.1 series termination resistors are placed as close as possible to U8 for signal integrity purposes.

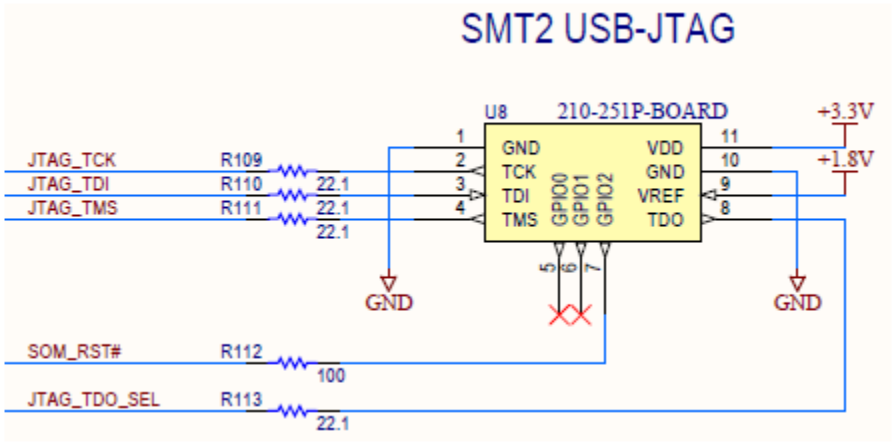

Figure 29 – U8, SMT2 USB-JTAG Connector

PCIe Net Name:	JX1 Pin #:
JTAG_TCK	1
JTAG_TMS	2
JTAG_TDO	3
JTAT_TDI	4

Table 20 – JTAG connections

2.20.3 FMC JTAG Level Translator, U7

The FMC JTAG interface operates at 3.3V, but the SOM JTAG interface is 1.8V. U7 has been placed for bidirectional 1.8V to 3.3V translation.

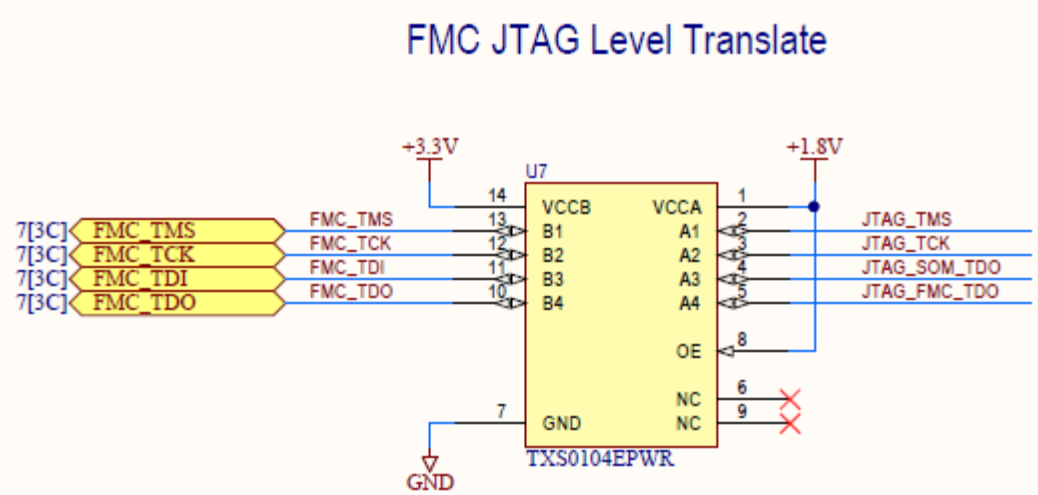

Figure 30 – U7, FMC JTAG Level Translator

2.20.4 JTAG SOM or SOM+FMC chain select, JP12

The JTAG on the PCIe Carrier Card allows the user to access either the SOM via the JTAG or the SOM and FMC board via the JTAG chain. JP12 placed on location 2-3 is for SOM only JTAG. JP12 placed at location 1-2 allows JTAG access to the SOM and the FMC board. By default JP12 is placed at location 2-3 thereby allowing SOM JTAG access while a FMC board is not present on the carrier.

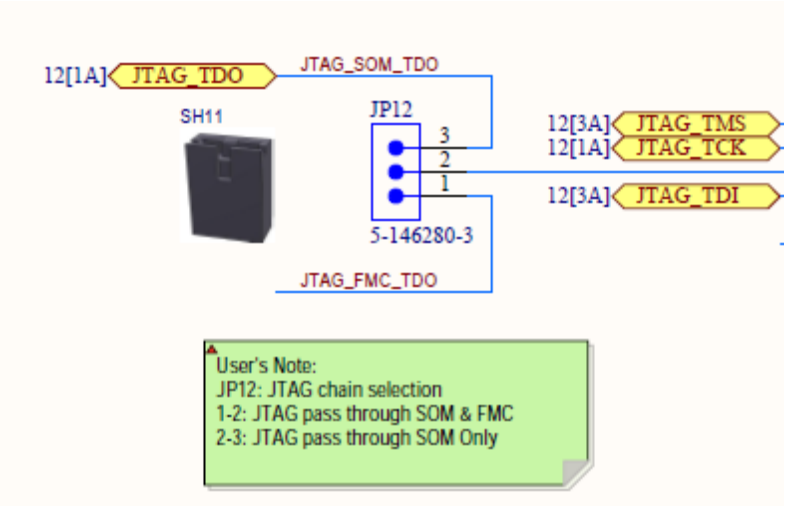

Figure 31 – JP12, JTAG Select (SOM or SOM+FMC)

2.21 LVDS Touch Panel Interface – P3

The UltraZed PCIe Carrier Card has an Avnet LVDS Touch Panel interface. This interface uses a Display Port form factor connection, P3. For ease of use, software references and rapid development time, Avnet recommends the following 10 inch touch panel kit: http://picozed.org/product/10-inch-touch-display-kit

- Routed at 100Ω differential.
- Routed 50Ω single ended on control/status signals.
- Two via transitions or less.
- No blind or buried vias.
- Trace length matching to within 10mils pair to pair and do not to exceed 100mils within the group. Diode D20 is not populated by default. If the target interface's logic is 1.8V, R94 may be removed and D20 or resistor may be placed, as necessary, to allow 1.8V reference.

Port IO Name:	P3 LVDS signal name:	JX2 Pin #:
JX2_HP_DP_00_P	TP_D0_P	45
JX2_HP_DP_00_N	TP_D0_N	47
JX2_HP_DP_01_P	TP_D1_P	44
JX2_HP_DP_01_N	TP_D1_N	46
JX2_HP_DP_02_P	TP_D2_P	51
JX2_HP_DP_02_N	TP_D2_N	53
JX2_HP_DP_03_P	TP_D3_P	50
JX2_HP_DP_03_N	TP_D3_N	52
JX2_HP_DP_04_P	TP_CLK_P	57
JX2_HP_DP_04_N	TP_CLK_N	59
JX2_HD_SE_10_P	TP_SCL	37
JX2_HD_SE_10_N	TP_SDA	39
JX2_HD_SE_11_P	TP_INT#	38

Table 21 – LVDS Touch Panel pinout

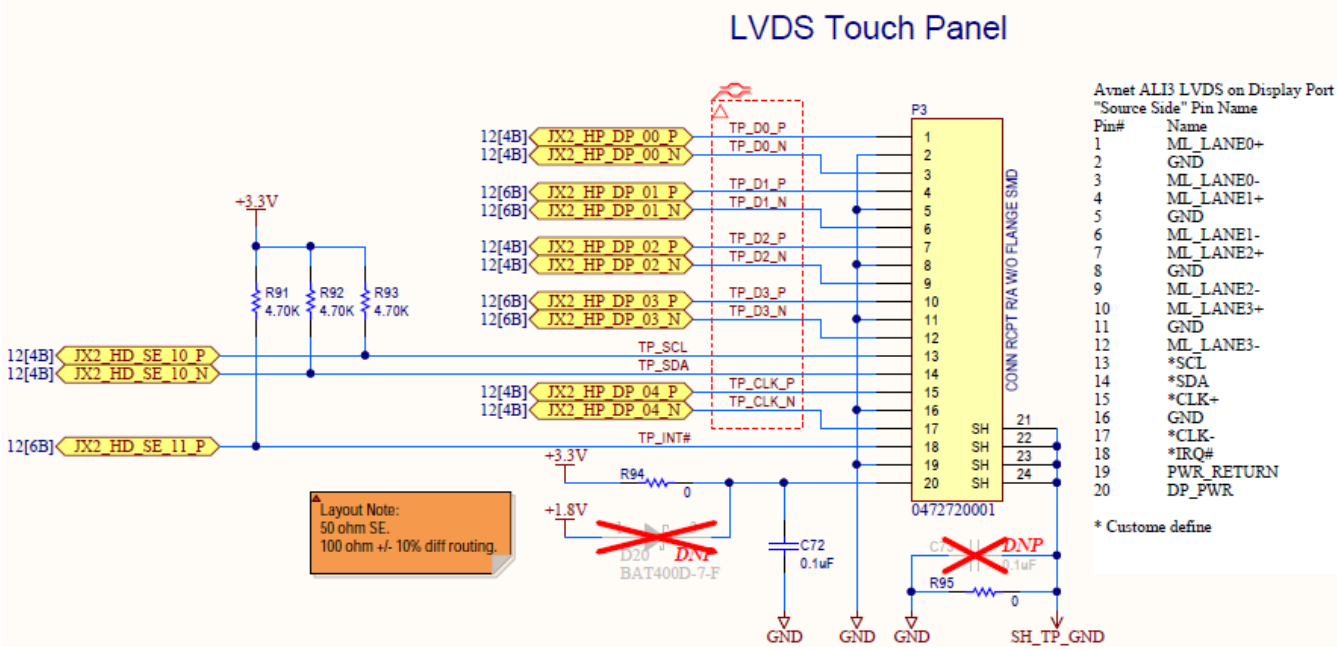

Figure 32 – P3, LVDS Touch Panel connector

2.22 LEDs – Power Status LEDs (green)

Additional LEDs representing power supply status and reset status are placed on the board. LEDs include:

- +12V Main Input, D26 – Indicates 12V VIN is present.
- SOM Module PG, D25 – Pulled up on the SOM. SOM drives a low until the SOM power supply is within 10% nominal output. When SOM is within 10% regulation, LED turns on.
- Carrier Card PG, D27 – Pulled low (off) until IRPS PMIC IC is within regulation on all output rails. When PMIC within regulation, LED turns on. The CC_PG signal is pulled up to +3.3V_PRI via a 10K resistor, R131.
- FMC PG C2M, D28 – Pulled low by FMC module until FMC power supplies stabilized. Once FMC supply stabilized, the signal is pulled up on the PCIe to +3.3V via a 10K resistor, R62, turning on LED D28.

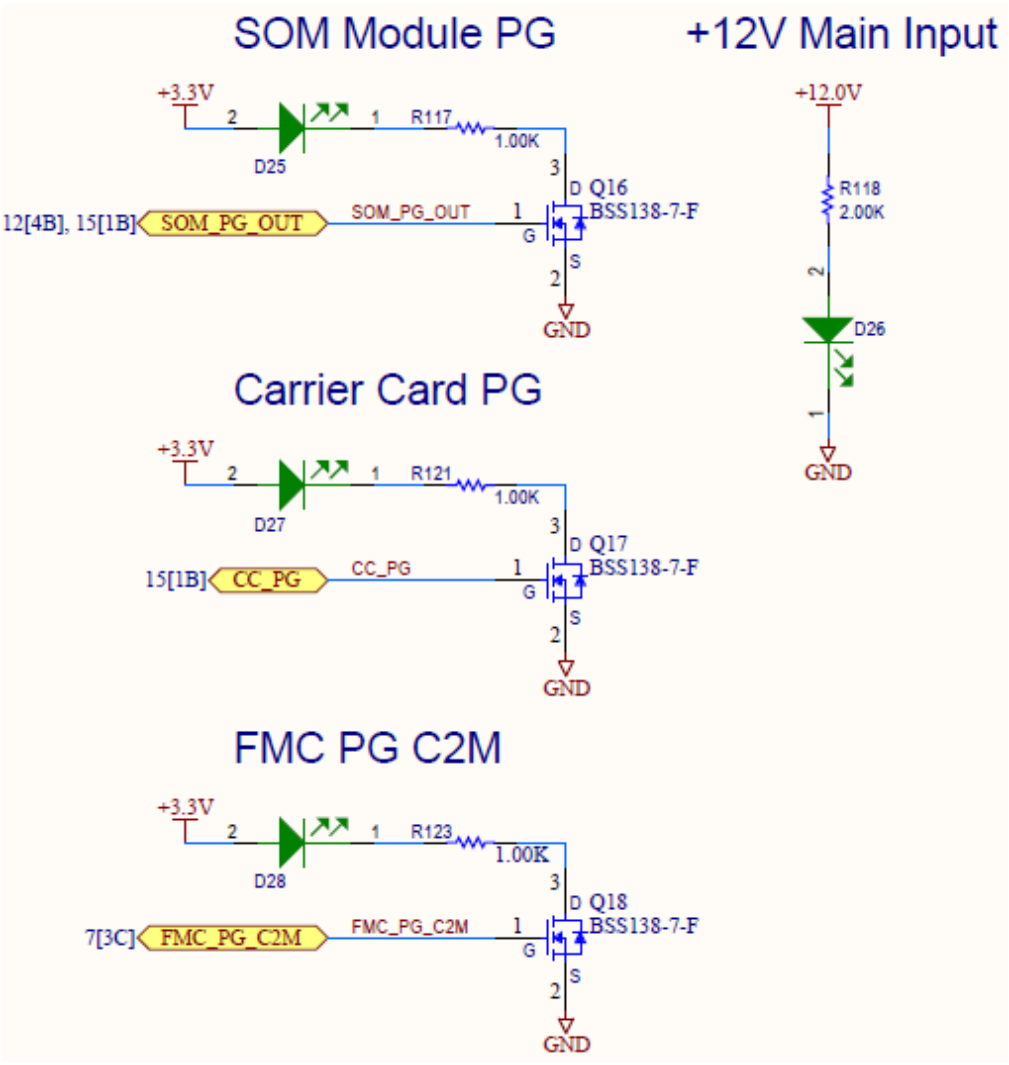

Figure 33 – Power status LEDs

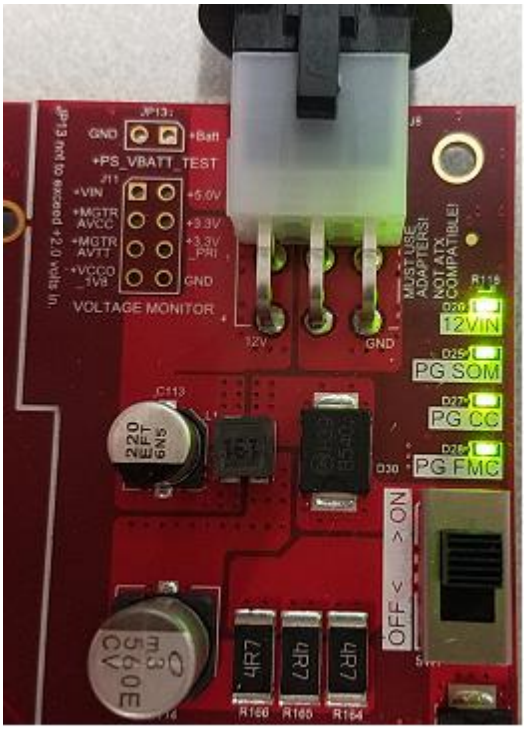

Figure 34 – Power Status LEDs

2.23 Fan Header – J10

The carrier card provides a dual position fan header for the SOM's cooling fan. The default configuration sources +5.0V to the SOM fan. If a 12V fan is used, FB4 and C117 need to be placed and FB5 removed. A ferrite bead and capacitor are used to minimize fan motor noise coupling to the carrier card's rails. The maximum current for the fan should not exceed 200mA.

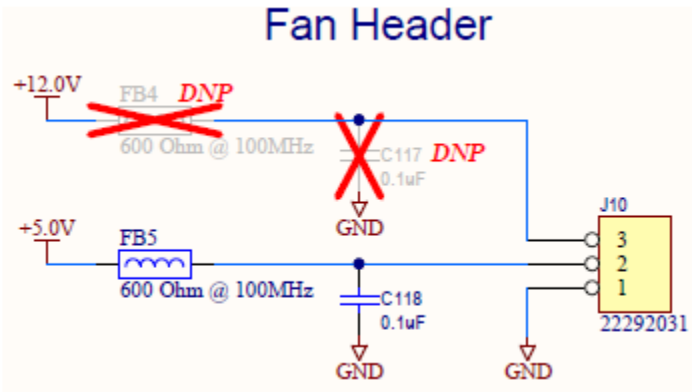

Figure 35 – J10, Fan Header

2.24 Unused PL I/O Pins

All unused JX PL I/O pins are terminated at the JX connector. They are not routed out to test points or looped back.

Port IO Name:	JX1 Pin Number:
JX1_HP_DP_01_P	8
JX1_HP_DP_01_N	10
JX1_HP_DP_03_P	14
JX1_HP_DP_03_N	16
JX1_HP_DP_05_P	20
JX1_HP_DP_05_N	22
JX1_HP_DP_21_GC_P	68
JX1_HP_DP_21_GC_N	70
JX1_HP_DP_22_P	75
JX1_HP_DP_22_N	77
JX1_HP_DP_24_P	81
JX1_HP_DP_24_N	83
JX1_HP_DP_26_P	87
JX1_HP_DP_26_N	89
JX1_HP_SE_00	135
JX1_HP_SE_02	137
JX1_HP_SE_04	139
JX1_HP_SE_01	134
JX1_HP_SE_03	136
JX1_HP_SE_05	138

Table 22 – Unused JX1 pin table

Port IO Name:	JX2 Pin Number:
JX2_HD_SE_11_N	40
JX2_HP_DP_05_P	56
JX2_HP_DP_05_N	58
JX2_HP_DP_06_P	63
JX2_HP_DP_06_N	65
JX2_HP_DP_07_P	62
JX2_HP_DP_07_N	64
JX2_HP_DP_08_P	69
JX2_HP_DP_08_N	71
JX2_HP_DP_09_P	68
JX2_HP_DP_09_N	70
JX2_HP_DP_10_P	75
JX2_HP_DP_10_N	77
JX2_HP_DP_12_P	81
JX2_HP_DP_12_N	83
JX2_HP_DP_13_P	80
JX2_HP_DP_13_N	82
JX2_HP_DP_14_P	87
JX2_HP_DP_14_N	89
JX2_HP_DP_15_P	86
JX2_HP_DP_15_N	88
JX2_HP_DP_24_P	117
JX2_HP_DP_24_N	119
JX2_HP_DP_25_P	116
JX2_HP_DP_25_N	118
JX2_HP_DP_26_P	123
JX2_HP_DP_26_N	125
JX2_HP_DP_28_P	129
JX2_HP_DP_28_N	131
JX2_HP_DP_29_P	128
JX2_HP_DP_29_N	130
JX2_HP_SE_04	139
JX2_HP_SE_05	138

Table 23 – Unused JX2 pin table

Port IO Name (pins tied to ground):	JX3 Pin Number:
GTR_RX3_P	4
GTR_RX3_N	6

Table 24 – Unused JX3 pin table

3 Power

3.1 Power Input – J8, SW7, P1

The PCIe Carrier Card has two input power connections, J8 and P1. J8 is a six pin power jack and P1 is the PCIe edge connector. J8 is capable of handling in excess of 12V @ 5 Amps, while the PCIe slot is capable of providing a minimum of 10 watts. The maximum PCIe current varies by the motherboard manufacturer. Some PCIe slots can be configured via the PC for higher current. The Avnet "standard" Non-ATX (NATX), AES-SLP-12V5A-G, power supply is recommended for use with this carrier. The power input to the board is controlled by SW7, an on/off slide switch.

- Input components C113, C115 and L1 are used to reduce spurious EMI emissions during dynamic interface and SOM loads. These components should be used on every carrier design to reduce EMI radiation.
- R164, R165, R166 and C114/C111/C112 are used to create a low pass filter to minimize any VIN voltage dips during power up when high current demands are placed on certain six pin wall adapters. The LPF circuit ensures a smooth and stable power on ramp for the carrier and SOM. This or an appropriate circuit is highly recommended if the customer is designing their own Carrier Card.
- Diodes D29 and D30 are used for power steering in the event the user wants to insert the board into a PCIe x1 slot for development purposes. **Please Note:** While the PCIe slot can source 10 watts of power (up to 25W via PC configuration) it is recommended the carrier card also be plugged in using J8 to eliminate potential under-power scenarios.
- If the customer choses to power the PCIe carrier in an enclosed PC chassis and does not want to attach the external power adapter, a Molex to Non-ATX adapter is available from Avnet under part number AES-ACC-PWR-ADPT. This adapter allows the user to attach to their PC's internal power supply unit (PSU) using a Molex 4 pin connector to the PCIe Carrier Card's power jack.
- Below is a link to the AES-ACC-PWR-ADPT: http://avnetexpress.avnet.com/store/em/EMController?term=AES-ACC-PWR-ADPT&x=0&y=0&action=products&langId=-1&storeId=500201&catalogId=500201&hbxSType=&N=0&filterButton=true

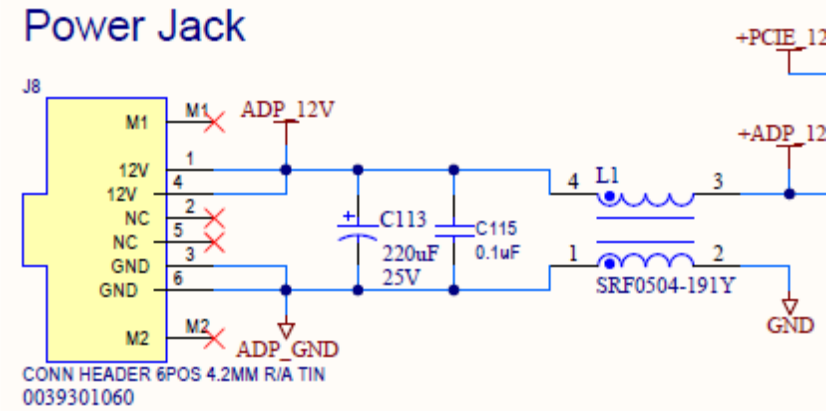

Figure 36 – J8, Power input jack

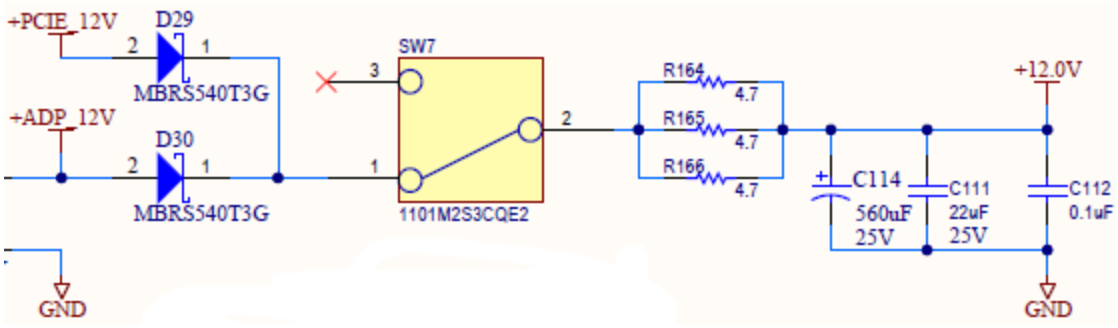

Figure 37 – SW7, Power switch and Low Pass Filter

3.2 PCIe Carrier Card Power Supplies

The carrier card provides the below listed power rails for the UltraZed SOM. A PMIC, Infineon part number IRPS5401MTRPBF, is factory programmed with the necessary parameters to set the output voltages. This part number is specific to Avnet's SOM, IOCC and PCIe Carrier Cards.

- +VIN 12V Main power in via a six pin ATX-type connector
- +PCIE_12V PCIe from PCIe socket (when plugged into a PCIe slot)
- +3.3V_PRI – always on +3.3V LDO regulator used to provide the PMIC with voltage.
- +3.3VDP – Display port power LDO. Ultra low noise rail for Display Port connection. See Figure 9 – U4, Display Port 3.3V power supply
- PS +MGTRAVCC (0.85V)
- PS +MGTRAVTT (1.8V)
- PS MIO bank 501 VCCO (3.3V)
- PL HP bank 64/65/66 VCCO (1.8V)
- PL HD bank 26 VCCO (3.3V)
- +PS_VBATT, 1.5V

- SOM rail feedback. The UltraZed SOM provides voltage sense feedbacks for each power rail supplied by the carrier card. Please refer to Xilinx's ds925 for percent variation on the following power rails when designing the power system for a custom PCIe Carrier Card.
- The SOM's SOM_PG_OUT signal is used to assist in power sequencing. The PCIe Carrier Card PMIC is not turned ON until the SOM_PG_OUT signal is asserted. The SOMs PG signal is asserted when the SOMs PMICs have successfully powered up and are within operating voltage tolerance.

NOTE:
In normal operation, the SOM_PG_OUT signal controls the PCIe's PMIC enable pins. For this reason a SOM must be placed for the carrier to power up in normal operation. In test mode, the board can be powered up by modifying the circuit as described below.

- To power up the board without a SOM, the user can place R125 with a 49.9K ohm resistor. This weak pull turns on the carrier card's PMIC. While it is recommended a SOM not be placed when R123 is placed, the resistor value is high enough to allow the SOM to maintain control of the PCIe's PMIC in the event a SOM is placed.

Voltage Level:	Rail/Connector/Interface:
12V	+VIN
12V	+PCIE_12V to +VIN
3.3V_PRI	+3.3V_PRI for PMIC
3.3VDP	+3.3V Display Port LDO
5V	+VUSB
0.85V	JX3, GTR AVCC
1.8V	JX3, GTR AVTT
1.8V	JX1, JX2, PL HP banks (Vcco_HP_64/65)
3.3V	JX2, JX3, PL HD & PS MIO bank 501

Table 25 – Voltage levels by connector, rail, interface & bank

3.3 Sequencing

- The SOM must provide an active high SOM_PG_OUT for the carrier card's PMIC to turn on.
- The below image shows the power sequencing using the IR PowIRCenter software. The Ton time delays are set to 10 ms on CHA – CHD with a rise time of 6 ms. The LDO is set for a delay of 20 ms and no rise time delay.

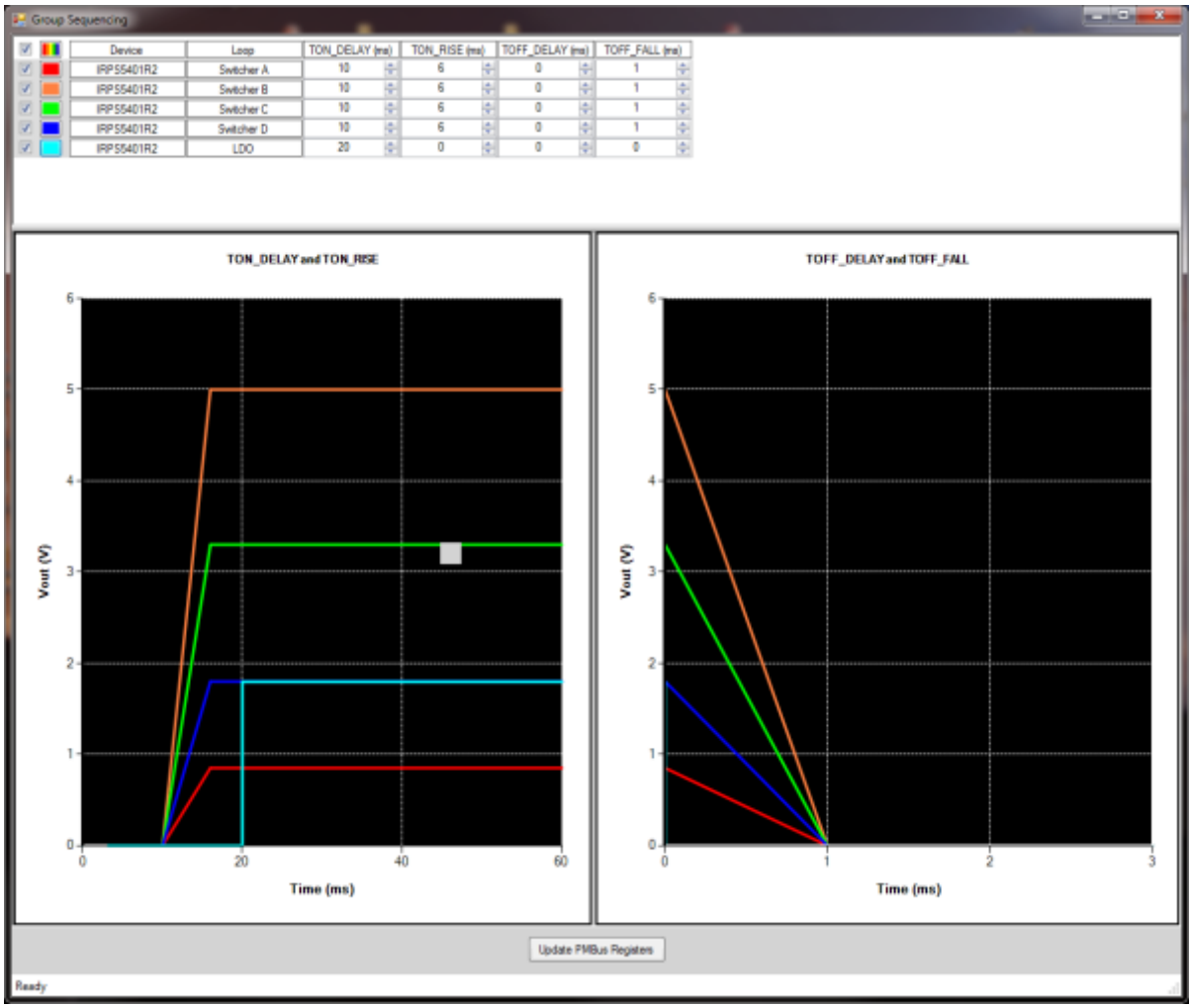

Figure 38 – Power Sequencing

3.4 Bypassing/Decoupling/Filtering

The PCIe Carrier Card follows the recommended decoupling and layout techniques per each IC manufacturer's datasheet.

3.5 +3.3V Primary Regulator – U11

The carrier card uses an always-on ON Semiconductor NCP565D2T33R4G +3.3V Low Drop Out linear regulator. This part is used to provide LDO power to the Infineon IRPS5401MTRPBF PMIC.

- U9 is an additional footprint in the event a customer chooses to use an alternate LDO. It is DNP'd by default as is R159 and R160.

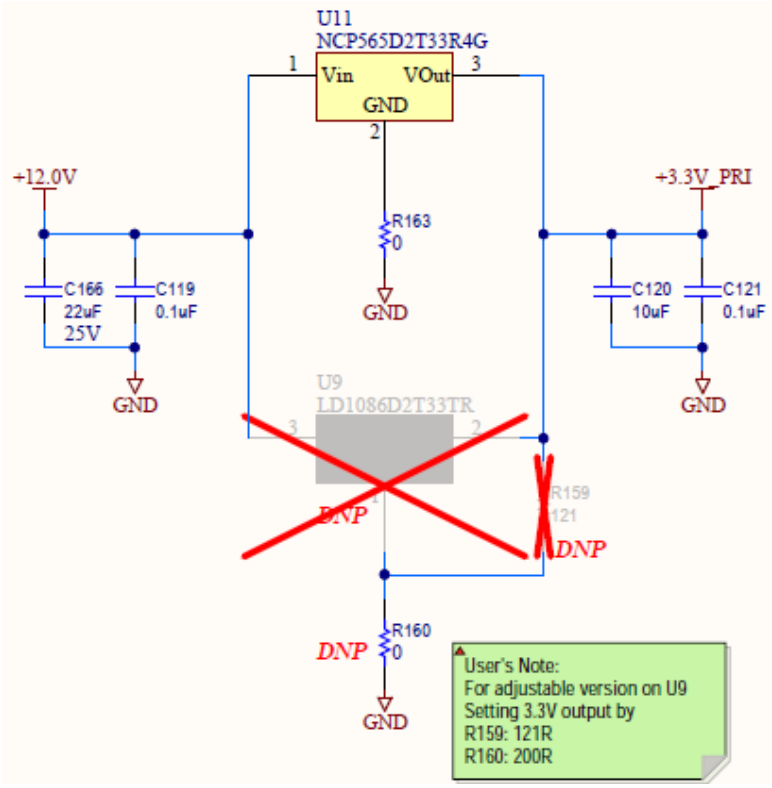

Figure 39 – U11, +3.3V primary regulator

3.6 Main Regulator - Infineon IRPS5401MTRPBF PMIC – U10

A five channel, high current programmable PMIC is required to source the SOM with high accuracy rails. The Infineon IRPS5401MTRPBF PMIC was chosen due to it's small size, high efficiency, and programmable features. This part is on the PMBUS and is accessible via J9, the PMBus header. The PMIC has been factory programmed with 3 selectable output profiles. One profile is used for the carrier card, while the remaining two are used for the SOM.

NOTE: The IRPS5401 PMIC has been set as follows:

- Turn off outputs if PMIC input voltage is less than 10.5V
- Turn on outputs if PMIC input voltage is equal or greater than 11.0V

In practice, the minimum +VIN on J8 (power jack) must be 11.6 volts or greater. This minimum value accounts for the voltage drop on the input filter circuit at maximum current draw. In a custom carrier design, pending the +VIN source, the input-low threshold of the PMIC can be adjusted to user preferences via software configuration using the PMBus.

- +VIN range is +11.6V to +12.2V
- The carrier card PMIC I2C address is: 0x12
- The carrier card PMBus address is: 0x42
- Please contact your local Avnet FAE for further PMIC design or ordering information.

Power Rail Name:	Source, Channel:	Volts, Amps:	Purpose:	JX Pins:
+VIN	Wall adapter, N/A	+12V, 5.0 A	Main board power	JX1 & JX2: 132, 133, 140
+PCIE_12V	PCIE	+12V, 833 mA or 2083 mA	All power	JX1 & JX2: 132, 133, 140
+3.3VDP	U3 LDO, N/A	+3.3V, 500 mA	Display Port power	N/A
+3.3V PRIMARY	U19 LDO, N/A	+3.3V, 1.5 A	PMIC core power	N/A
+5.0V	PMIC, CHB	+5.0V, 2.0 A	Main board power	N/A
+MGTRAVCC	PMIC, CHA	+0.85V, 2.0 A	SOM VCCIO power	JX3: 31, 37, 39
+3.3V, +VCCO_HD_26, VCCO_PSIO_501	PMIC, CHC	+3.3V, 3.0 A	Main board power, SOM VCCIO power	JX2: 18, 24, 30 JX3.67
+VCCO_1V8, +VCCO_HP_64/65/66	PMIC, CHD	+1.8V, 4.0 A	SOM VCCIO power	JX1: 5, 6, 7, 12, 13, 18 JX2: 17, 23, 29
+MGTRAVTT	PMIC, LDO	+1.8V, 0.3 A	SOM VCCIO power	JX3: 36, 42
+USB_VB	U21, LDO	+5.0V, 1.5 A	USB interface	N/A
+PS_VBATT	JP3, LR44, +VCCO_1V8	+ <2.0V, < 10mA	FPGA key memory	JX3.46

Table 26 – PCIe Carrier Card power rails

3.6.1 Power supply net ties

Several rails are tied together on the Carrier Card using PCB net ties. PCB net ties are two separate signal planes tied to each through a piece of PCB copper. This technique is used to illustrate schematic/electrical connectivity

- +VCCO_1V8 →VCCO_HP_64/65/66
- +3.3V → VCCO_HD_26 & VCCO_PSIO_501

NOTE: These rails are not tied together on the SOM. They are not tied together at the SOM because a user may want different I/O voltages on each bank. They are tied together on the carrier card because these are the voltages required for Avnet's specific application.

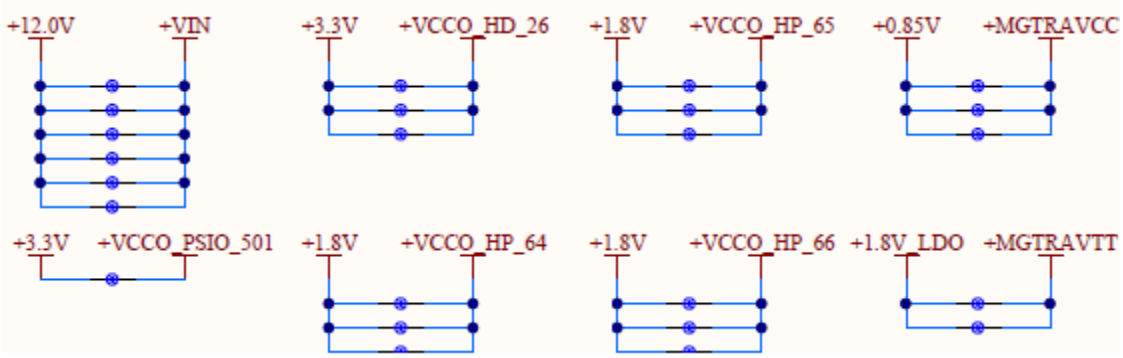

Figure 40 – Net Tie rail bonds

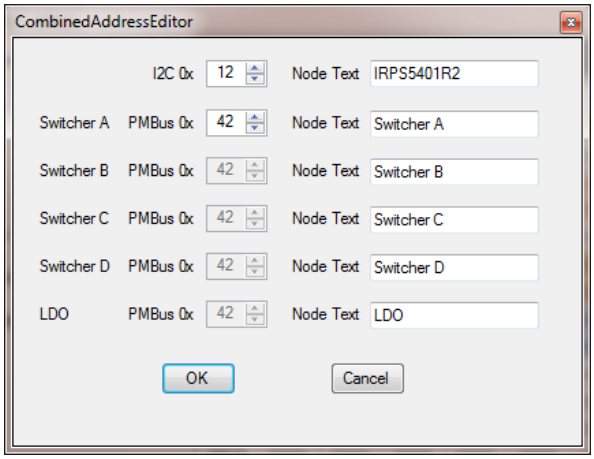

Figure 41 – Carrier Card PMIC Address window via IR PowIRCenter

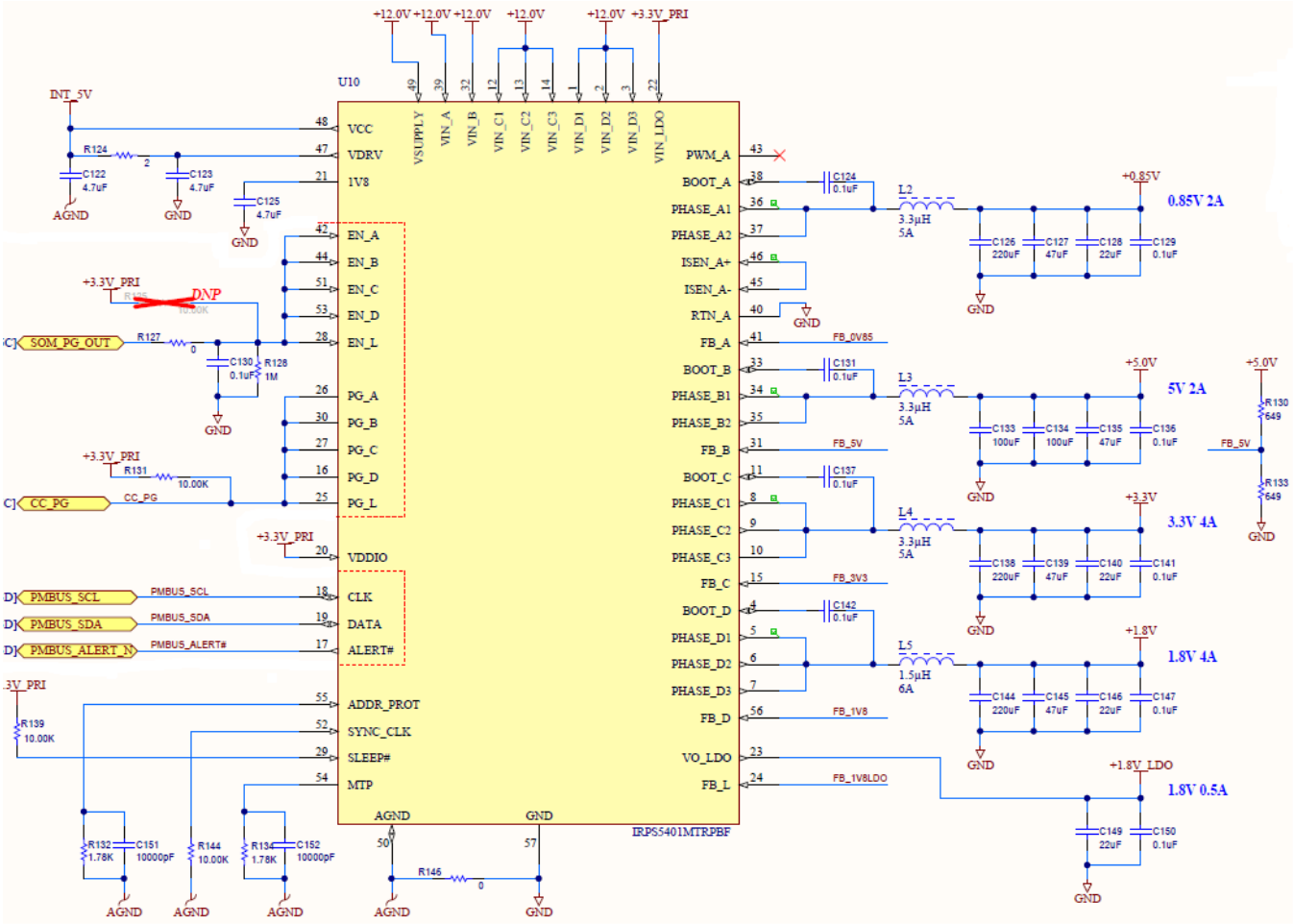

Figure 42 – U10, Infineon PMIC IRPS5401MTRPBF 5 Channel regulator

3.6.2 PMIC Feedback resistors

The SOM provides remote sensing signals for the PCIe carrier's PMIC feedback loop (see section 3.7). This eliminates the need for the carrier to have on-board feedback resistors when a SOM is plugged in. However, to aid in power supply development for custom carrier designs, Avnet put non-populated feedback resistors on the board. These resistors are **Not Populated** by default as listed in the BOM and marked out with a red X in the schematic.

IMPORTANT! The Not Populated (DNP) resistors may be placed **by the user** for carrier card power supply evaluation and configuration **without** a SOM. **These resistors should be removed prior to a SOM being placed. Failure to remove these parts will cause the PMIC to create incorrect and potentially SOM damaging voltages.**

– For Revision 1 of the PCIe CC, the following resistors are Not Populated by default: R126, R135, R140, R143, R145, R147.

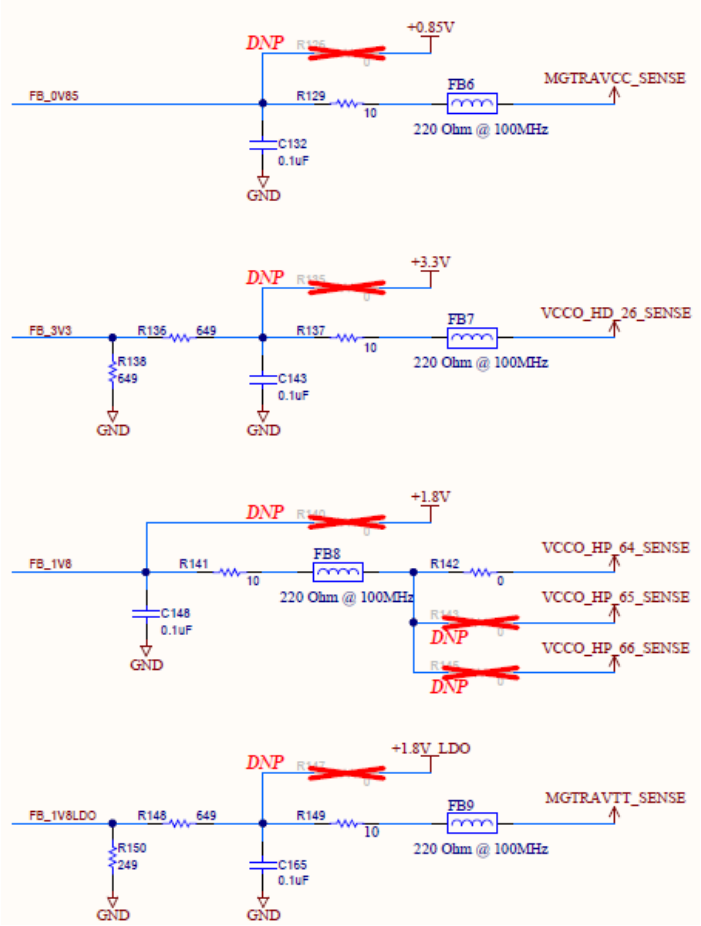

Figure 43 – PMIC feedback resistors Not Populated (red X)

3.7 Power Sense signals

The UltraZed SOM provides low current power sense signals for the below carrier rails. The power sense feedback signals are used to adjust the output voltage for each rail based on the SOMs rail loading. This method of feedback ensures the SOM is provided stable power during dynamic power loading conditions. This method of sensing also nulls out all current and resistance drops across both boards and connectors.

PCIe Net Name:	JX3 Pin:
VCCO_HP_66_SENSE	83
VCCO_HP_65_SENSE	91
VCCO_HP_64_SENSE	92
VCCO_HD_26_SENSE	84
MGTRAVCC_SENSE	75
MGTRAVTT_SENSE	76

Table 27 – SOM power rail sense connections

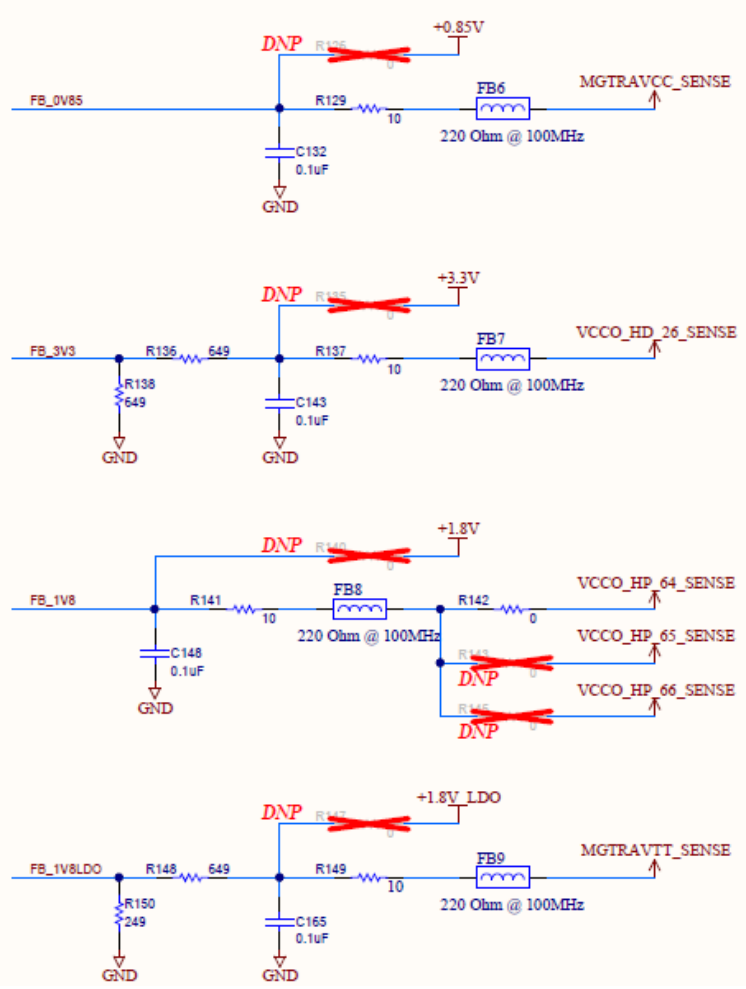

Figure 44 – Power supply sense rail filters

3.8 PMBus Interface – J9

The UltraZed PCIe and SOM's Power Management ICs can be accessed by attaching to the PMBus header, J9. This header can be used for monitoring and programming all PMBus voltage regulators on the PCIe Carrier Card and the UZ-SOM. To attach to this interface the customer may use a generic I2C dongle or an Infinion USB005 dongle with the Infineon IR PowIRCenter Software. Use this URL for the software:
http://www.infineon.com/cms/en/product/promopages/power-center-software/

NOTE:
After the initial programming of all PMBus voltage regulators, the UltraZed SOM can control the PMBus in order to control/monitor the PMBus voltage regulators on the UltraZed SOM as well as the PCIe Carrier Card for the purpose of power management and/or measurements.

- The SOM contains the I2C pullup resistors to allow the board to read/write the PMBus regulators.

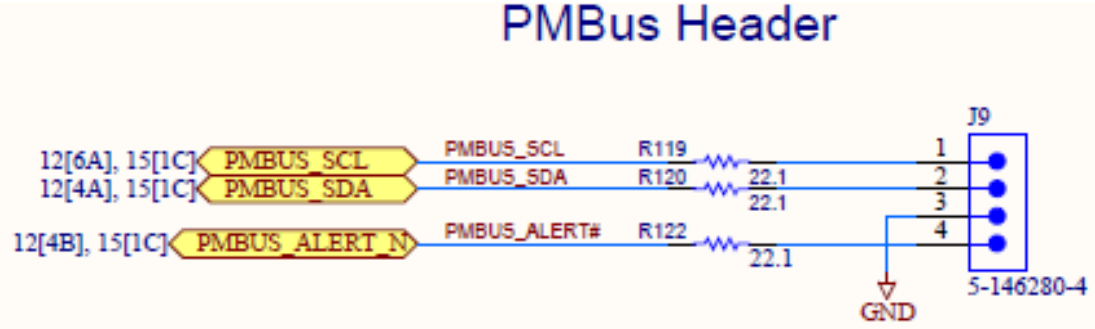

Figure 45 – J9, PMBus header

PCIe Net Name:	JX2 Pin #:
PMBus_SDA	11
PMBus_SCL	12
PMBus_ALERT#	35
SOM_PG_OUT	41

Table 28 – PMBus connections

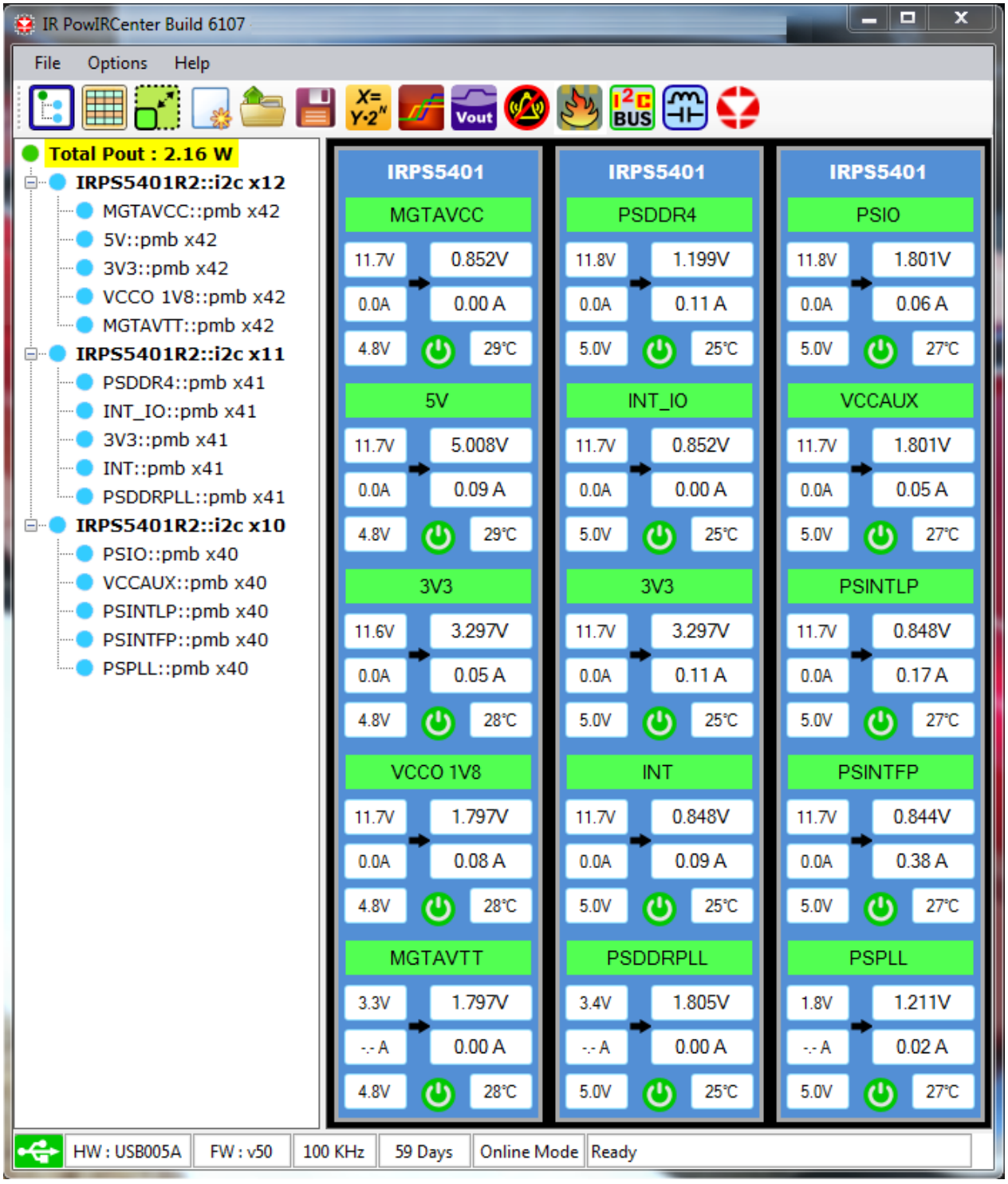

Figure 46 – PMIC Interface window via IR PowIRCenter

3.9 JX connectors power pins

Rail Name, voltage:	JX1 Pin #	JX1 Pin #	Rail Name, voltage:
VCCO_HP_65, 1.8V	5	6	VCCO_HP_64, 1.8V
VCCO_HP_65, 1.8V	7	12	VCCO_HP_64, 1.8V
VCCO_HP_65, 1.8V	13	18	VCCO_HP_64, 1.8V
GND	19	24	GND
GND	25	30	GND
GND	31	36	GND
GND	37	42	GND
GND	43	48	GND
GND	49	54	GND
GND	55	60	GND
GND	61	66	GND
GND	67	72	GND
GND	73	78	GND
GND	79	84	GND
GND	85	90	GND
GND	91	96	GND
GND	97	102	GND
GND	103	108	GND
GND	109	114	GND
GND	115	120	GND
GND	121	126	GND
GND	127	132	+VIN
+VIN	133	140	+VIN

Table 29 – JX1 Power and Ground connections

Signal Name	JX2 Pin #	JX2 Pin #	Signal Name
GND	5	6	GND
VCCO_HP_66	17	18	VCCO_HD_26
VCCO_HP_66	23	24	VCCO_HD_26
VCCO_HP_66	29	30	VCCO_HD_26
GND	43	48	GND
GND	49	54	GND
GND	55	60	GND
GND	61	66	GND
GND	67	72	GND
GND	73	78	GND
GND	79	84	GND
GND	85	90	GND
GND	91	96	GND
GND	97	102	GND
GND	103	108	GND
GND	109	114	GND
GND	115	120	GND
GND	121	126	GND
GND	127	132	+VIN
+VIN	133	140	+VIN

Table 30 – JX2 Power and Ground connections

Signal Name	JX3 Pin #	JX3 Pin #	Signal Name
GND	5	2	GND
GND	11	4	GND
GND	17	6	GND
GND	19	8	GND
GND	25	14	GND
+MGTRAVCC	31	16	GND
+MGTRAVCC	37	22	GND
+MGTRAVCC	39	24	GND
GND	43	30	GND
GND	49	36	+MGTRAVTT
GND	55	42	+MGTRAVTT
GND	61	46	+PS_VBATT
+VCCO_PSIO_501	67	54	GND
		60	GND
		66	GND

Table 31 – JX3 Power and Ground connections

3.10 Display Port Regulator – U3

The Display Port requires a high precision power supply, +3.3VDP. The Maxim Part MAX8902BATA+T creates this rail. Features include:

- Vout is high precision, (<1.5% Vout) & low noise (16uVRMS)
- 500mA source in normal operation
- 700mA source in short mode
- Auto thermal shutdown and protect
- POK output
- 2mm X 2mm package

LED D3 is used to indicate the regulator is on. It illuminates when the regulator is within 88% of nominal output voltage.

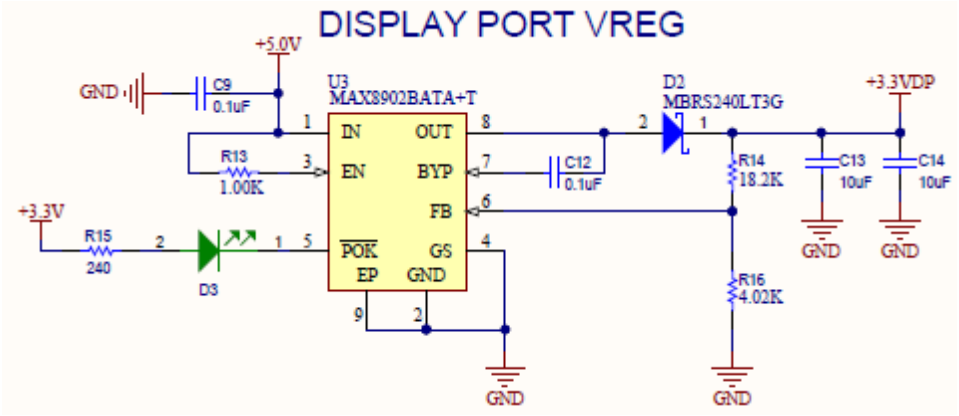

Figure 47 – U3, +3.3V Display Port regulator

3.11 Power Monitor interfaces – J7 & J11

The UltraZed SOM SYSMON interface is available on the carrier card. The pins are routed to a 0.1" SIP header for access to the SYSMON interface pins.

- The signals are routed differentially at 100 ohms.
- Termination resistors R114 and R115 are placed within 100 mils of J7.
- The signals are routed to within 10 mils across both pairs.

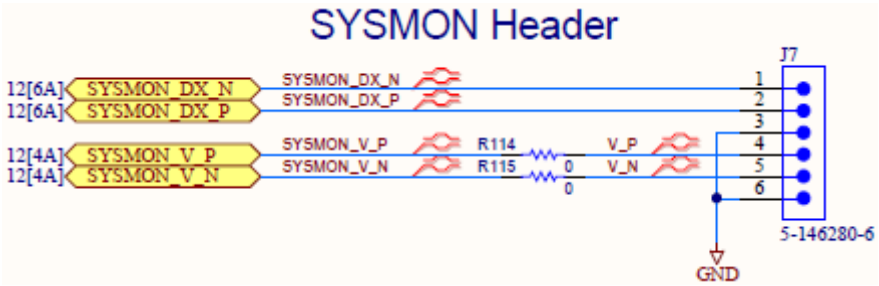

Figure 48 –J7, SYSMON header

PCIe Net Name:	JX2 Pin #:	SYSMON Jack Pin #:
SYSMON_V_N	1	1
SYSMON_V_P	3	2
SYSMON_DX_N	2	3
SYSMON_DX_P	4	4

Table 32 – SYSMON connection table

3.11.1 Power Supply monitor header – J11

A non-populated dual row 100 mil pitch 8 pin header is used for measuring the carrier card's voltage rails. The below figure shows the available voltage monitor points.

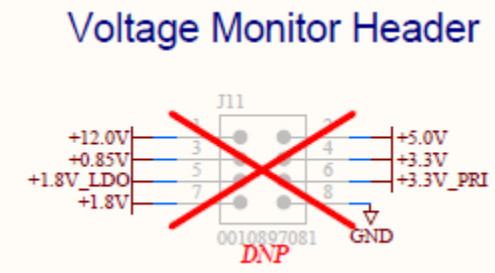

Figure 49 – J11, Voltage Monitor Header

3.12 PS VBATT LR44 Battery – BTH1 & JP13

The Carrier Card provides two methods of maintaining the SOM's Zynq device volatile AES decryptor keys when the carrier is turned off. A 1.5V LR44 battery or a customer's power connection through JP13. Either connection provides power to the SOM's +PS_VBATT signal via the JX3 pin 46 connector. When the carrier card is turned on, neither method is required as +VCCO_1V8 is diode OR'd with +PS_VBATT signal.

- The +PS_VBATT pin is pulled up via +VCCO_1V8 & D22 when the board is powered on, no battery or external power source needed to maintain decryptor keys.
- Place a LR44 battery to maintain the AES decryption keys on the SOM when board is power off.
- Diode D22 and D23 provide back source isolation for +VCCO_1V8 & LR44 battery.
- In lieu of placing a LR44 battery, the user may decide to use an external power supply or battery connected via JP13. In doing so, *the input voltage on JP13 MUST NOT EXCEED 2.0 volts otherwise the SOM's FPGA may be damaged.* Diode D24 and resistor R116 are placed to help prevent this, but this is by no means intended to encourage a voltage higher than 2.0V to be applied!

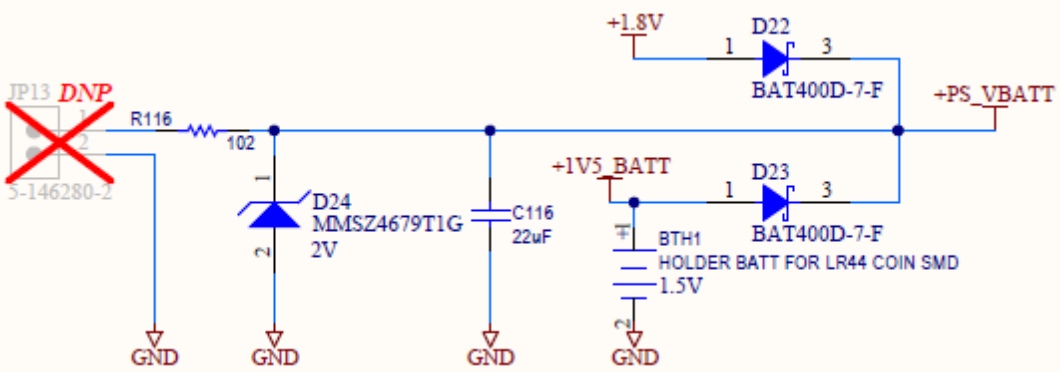

Figure 50 – JP13 & BTH1, +PS_VBATT circuit

3.12.1 PS VBATT placement

LR44 Battery installation instructions:

The LR44 battery is required to be installed in a sleeve, part number BHX1-LR44 and firmly inserted into the carrier's socket. The coin cell's positive terminal is placed into the opening of the sleeve facing up.

Figure 51 – BTH1 LR44 battery cage

Figure 52 – Battery & sleeve orientation prior to insertion

Figure 53 – Final battery placement. Push battery in as far as possible.

4 Mechanical

4.1 Layer stackup

Below is the as-built to layer stackup of the UltraZed PCIe.

Form # ENF-005

LAZER - TECH LIMITED

Customer: Dynamic Source
Part Num: PRJ-US2CAR
Part Rev: A1.00

Job Name: T14040
User Name: Steve Calvert
Req. Thick: 0.0630

Layer	Base CU / Plt	Thick	Type	Stackup	Subs	Material
Soldermask		0.0010				Taiyo - PSR-4000 BN - RED
Lyr1	1/4oz / Std	0.0017	S			
Prepreg		0.0035				FR4 Hi-Tg - 1x2113
Lyr2	1oz	0.0013	P			
Core		0.0050				FR4 Hi-Tg - 0.0050
Lyr3	1oz	0.0013	S			
Prepreg		0.0079				FR4 Hi-Tg - 2x2116
Lyr4	1oz	0.0013	P			
Core		0.0160				FR4 Hi-Tg - 0.0160
Lyr5	1oz	0.0013	P			
Prepreg		0.0079				FR4 Hi-Tg - 2x2116
Lyr6	1oz	0.0013	S			
Core		0.0050				FR4 Hi-Tg - 0.0050
Lyr7	1oz	0.0013	P			
Prepreg		0.0035				FR4 Hi-Tg - 1x2113
Lyr8	1/4oz / Std	0.0017	S			
Soldermask		0.0010				Taiyo - PSR-4000 BN - RED

Required Thickness

Type	Req. Thick	Tol% +	Tol% -	Act. Thick	Measured
Overall	0.0630	10.0	10.0	0.0620	
Over lamination	0.0581	10.0	10.0	0.0569	
Over laminate	0.0568	10.0	10.0	0.0563	
Over metal	0.0610	10.0	10.0	0.0597	

Impedance Constraints

#	Type	Layer	Design Line	Actual Line	Pitch (traces)	Space (ground)	Ref Lyrs	Target (ohms)	Tolerance (ohms)	Predicted (ohms)
1	Single Ended	Lyr1	0.0050	0.0053			0 / 2	50.0	5.0	50.6
2	Single Ended	Lyr6	0.0056	0.0053			5 / 7	50.0	5.0	49.7
3	Single Ended	Lyr8	0.0050	0.0053			7 / 0	50.0	5.0	50.6
4	Differential	Lyr1	0.0044	0.0046	0.0099		0 / 2	90.0	9.0	90.5
5	Differential	Lyr1	0.0034	0.0035	0.0090		0 / 2	100.0	10.0	100.8
6	Differential	Lyr3	0.0036	0.0038	0.0091		2 / 4	100.0	10.0	100.3
7	Differential	Lyr6	0.0036	0.0038	0.0091		5 / 7	100.0	10.0	100.3
8	Differential	Lyr8	0.0044	0.0046	0.0099		7 / 0	90.0	9.0	90.5
9	Differential	Lyr8	0.0034	0.0035	0.0090		7 / 0	100.0	10.0	100.8

Updated: May 15/13 Arkeo Stack 11/4/2016 2:09:44 PM

Figure 54 – UltraZed PCIe PCB Stackup

4.2 Diagram and Model

A mechanical diagram and a 3D Model for the US1CAR are available for download at www.ultrazed.org/product/ultrazed-EG.

4.3 Weight

The weight of the UltraZed-PCIe with rubber feet, SD card, and jumpers populated without the SOM attached is 149 grams (5.20 ounces).