Xilinx® Zynq® Mini-ITX Development Kit User Guide

Version 1.1

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Version	Date	Comment
1.0	3/3/2014	Initial release for production board (AES-MMP-7Zxxx-G Revision D)
1.1	1/12/2015	Corrected table 17

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1 Introduction

The purpose of this manual is to describe the functionality and contents of the Zynq Mini-ITX Development Kit from Avnet Electronics Marketing.This document includes instructions for operating the board, descriptions of the hardware features and explains out-of-the- box design code programmed in the on-board QSPI flash and microSD card.

1.1 Description

The Zynq Mini-ITX Development Kit provides a complete hardware environment for designers to accelerate their time to market. The kit delivers a stable platform to develop and test designs targeted to the advanced Xilinx Zynq AP SoC family. The installed Zynq 7Z045 or 7Z100 device offers a prototyping environment to effectively demonstrate the enhanced benefits of leading edge Xilinx AP SoC solutions.Reference designs are included with the kit to exercise standard peripherals on the evaluation board for a quick start to device familiarization.

1.2 Board Features

- **Zynq AP SoC**
  - Xilinx XC7Z045-2FFG900 or XC7Z100-2FFG900
- **I/O Connectors**
  - One (1) FMC HPC connector
- **Multi-gigabit Serial transceivers (GTX)**
  - Fourteen (14) GTX ports
    - SATA x1
    - SFP x1
    - PCIe x4 Root Port
    - FMC x8
- **Memory**
  - 1 GB DDR3 SDRAM (PS)
  - 1 GB DDR3 SDRAM (PL)
  - 32 MB QSPI Flash
  - 8 KB I2C EEPROM
  - MicroSD Card
- **Communication**
  - USB-UART
  - USB 2.0 4 Port Hub
  - 10/100/1000 Ethernet
- **Configuration**
  - 32 MB QSPI Flash
  - MicroSD Card
  - JTAG
  - Digilent USB JTAG Module
- **Video**
  - HDMI Interface
  - LVDS Touch Panel Interface

- **Audio**
  - Audio Codec
    - Headphone Output
    - Stereo Output
    - Differential Input
    - Stereo Input
- **Other**
  - Programmable LVDS clock source
  - Processor PJTAG port
  - Real-time clock (I2C)
  - User LEDs and Switches

1.3 Reference Designs

Reference designs that demonstrate some of the potential applications of the Zynq Mini-ITX Development Kit can be downloaded from ZedBoard.org (www.zedboard.org/products/mini-itx). The reference designs include all of the source code and project files necessary to implement the designs. See the PDF document included with each reference design for a complete description of the design and detailed instructions for running a demonstration on the development board. Check the DRC periodically for updates and new designs.

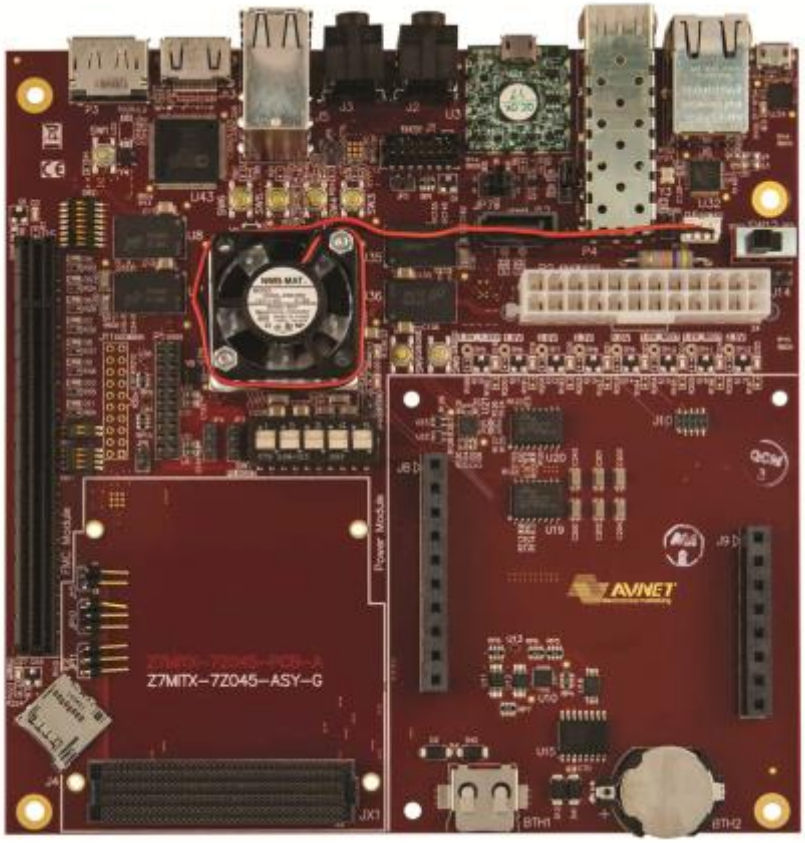

Figure 1 – Zynq Mini-ITX Development Board Picture

1.4 Ordering Information

The following table lists the development kit part numbers.
Internet link at http://avnet.com/us/Mini-ITX-7Z-G

Part Number	Hardware
AES-MINI-ITX-7Z045-BAS-G	– Xilinx Zynq 7Z045 Mini-ITX Development Board populated with an XC7Z045 FFG900 -2 speed grade device. – Kit includes ATX power supply.
AES-MINI-ITX-7Z045-G	– Xilinx Zynq 7Z045 Mini-ITX Development Board populated with an XC7Z045 FFG900 -2 speed grade device.
AES-MINI-ITX-7Z045-SYS-G	– Xilinx Zynq 7Z045 Mini-ITX Development Board populated with an XC7Z045 FFG900 -2 speed grade device. – 8GB microSD Card included. – Kit includes Mini-ITX Chassis and ATX power supply. – Kit includes 500GB SATA-III HDD.
AES-MINI-ITX-7Z100-BAS-G	– Xilinx Zynq 7Z100 Mini-ITX Development Board populated with an XC7Z100 FFG900 -2 speed grade device. – 8GB microSD Card included. – Kit includes ATX power supply.
AES-MINI-ITX-7Z100-G	– Xilinx Zynq 7Z100 Mini-ITX Development Board populated with an XC7Z100 FFG900 -2 speed grade device. – 8GB microSD Card included.
AES-MINI-ITX-7Z100-SYS-G	– Xilinx Zynq 7Z100 Mini-ITX Development Board populated with an XC7Z100 FFG900 -2 speed grade device. – 8GB microSD Card included. – Kit includes Mini-ITX Chassis and ATX power supply. – Kit includes 500GB SATA-III HDD.

Table 1 - Ordering Information

2 Functional Description

A high-level block diagram of the Zynq Mini-ITX Development Board is shown below followed by a brief description of each sub-section.

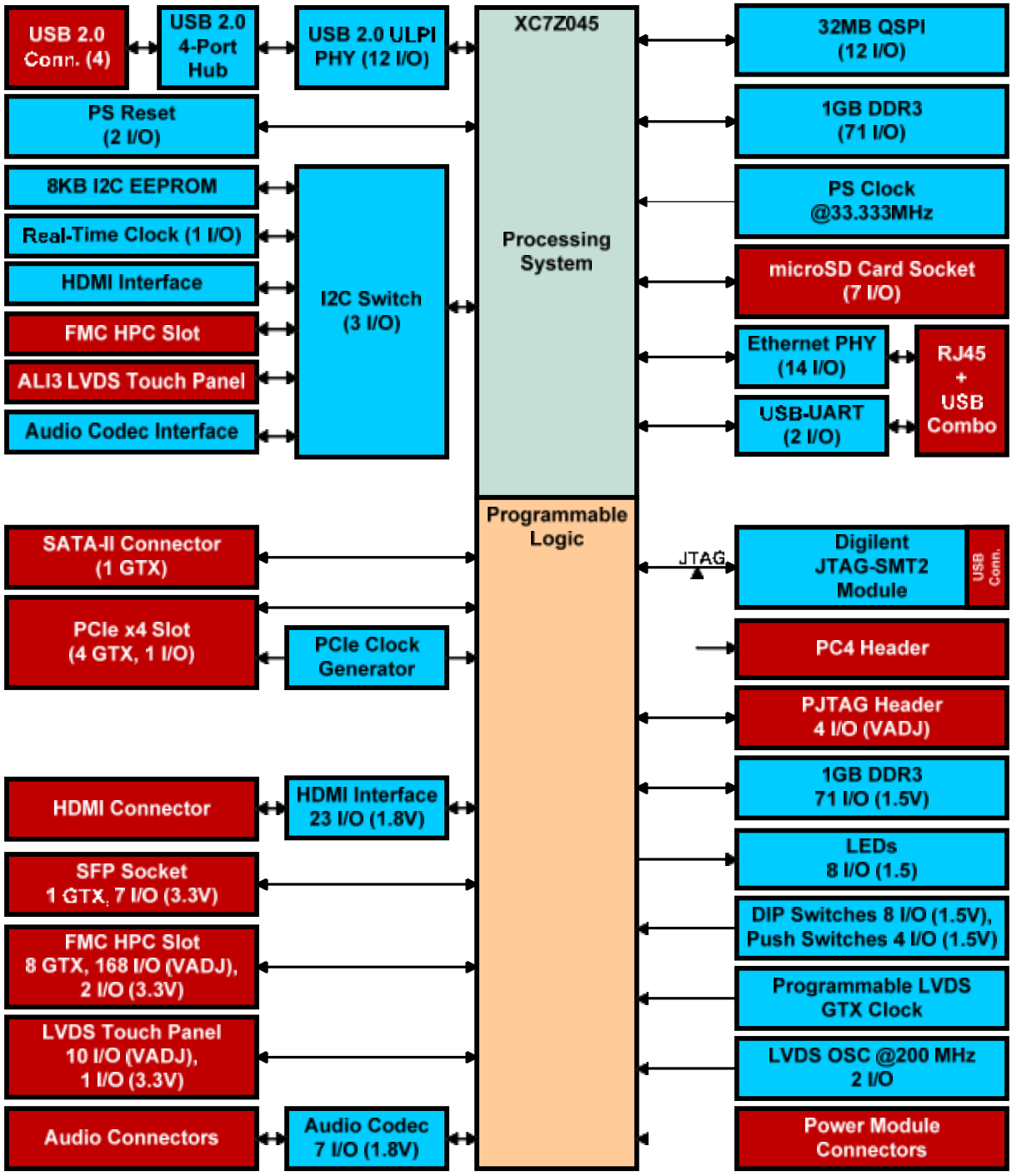

Figure 2 – Zynq Mini-ITX Development Kit Block Diagram

2.1 Xilinx Zynq 7Z045 and 7Z100 AP SoC

The Zynq 7Z045 and 7Z100 AP SoC devices available in the FFG900 package have an impressive list of features. The devices are made up of two main systems one of which is the Processing System (PS) and the other Programmable Logic (PL). The tables below list some of the 7Z045 and 7Z100 features.

Processing System	
Processor Core	Dual ARM Cortex-A9 MPCore
Processor Extensions	NEON and Single/Double Precision Floating Point for each processor
Max Frequency	800MHz (-2)
L1 cache	32 KB Instruction, 32 KB Data per processor
L2 cache	512KB
On-Chip Memory	256KB
External Memory Controllers	DDR3, DDR3L, DDR2, LPDDR2
External Static Memory Controllers	2X Quad SPI, NAND, NOR
DMA Channels	8 (4 dedicated to PL)
Peripherals	2x UART, 2x CAN, 2x SPI, 2x I2C, 4x 32b GPIO
Security	RSA, AES, SHA 256b
Programmable Logic	
Programmable Logic Cells	350K
LUTs	218,600
Flip-Flops	437,200
Block RAM	900
DSP Slices	2,180 KB
PCI Express (Root Complex or Endpoint)	Gen2 x8
Analog Mixed Signal	2x 12-bit, MSPS ADCs with up to 17 differential inputs
Security	AES, SHA 256b

Table 2 – Zynq 7Z045 AP SoC Features

Processing System	
Processor Core	Dual ARM Cortex-A9 MPCore
Processor Extensions	NEON and Single/Double Precision Floating Point for each processor
Max Frequency	800MHz (-2)
L1 cache	32 KB Instruction, 32 KB Data per processor
L2 cache	512KB
On-Chip Memory	256KB
External Memory Controllers	DDR3, DDR3L, DDR2, LPDDR2
External Static Memory Controllers	2X Quad SPI, NAND, NOR
DMA Channels	8 (4 dedicated to PL)
Peripherals	2x UART, 2x CAN, 2x SPI, 2x I2C, 4x 32b GPIO
Security	RSA, AES, SHA 256b
Programmable Logic	
Programmable Logic Cells	350K
LUTs	277,400
Flip-Flops	554,800
Block RAM	3,020 KB
DSP Slices	2,020
PCI Express (Root Complex or Endpoint)	Gen2 x8
Analog Mixed Signal	2x 12-bit, MSPS ADCs with up to 17 differential inputs
Security	AES, SHA 256b

Table 3 - Zynq 7Z100 AP SoC Features

2.2 GTX Interfaces

The GTX transceiver is a full-duplex serial transceiver for point-to-point transmission applications. Up to 16 transceivers are available on a single 7Z045 and 7Z100 FFG900 devices. The transceiver block is designed to operate at up to 10.3125Gbps for the populated -2 speed grade part.

The -3 speed grade part is capable of 12.5 Gb/s. The -1 speed grade part is capable of 8.0 Gbps in the FF package.

The Zynq-7000 AP SoC GTX transceivers are grouped into four transceivers per bank. Banks 109, 110, 111, and 112 are the GTX banks. Each GTX bank has two inputs for reference clocks.

The table below shows the GTX interface connections on the Zynq Mini-ITX Development Board.

GTX Bank	GTX Interface	Lane	Number
			7Z045
109	FMC DP0	1	GTX0_109
109	FMC DP1	1	GTX1_109
109	FMC DP2	1	GTX2_109
109	FMC DP3	1	GTX3_109
110	FMC DP4	1	GTX0_110
110	FMC DP5	1	GTX1_110
110	FMC DP6	1	GTX2_110
110	FMC DP7	1	GTX3_110
111	SFP	1	GTX0_111
111	SATA	1	GTX1_111
111	Unused	-	GTX2_111
111	Unused	-	GTX3_111
112	PCI Express x4	0	GTX3_112
112		1	GTX2_112
112		2	GTX1_112
112		3	GTX0_112

Table 4 - GTX Interface Pin Assignments

2.2.1 GTX Reference Clock Inputs

Each GTX bank has reference clock inputs. These reference clock inputs are supplied by a variety of on and off-board clock sources.

Two clock sources are used to provide reference clock frequencies to GTX bank 111 (SATA and SFP). One source is an LVDS clock synthesizer that can provide variable frequencies and the other is a fixed frequency clock chip. The synthesizer provides reference clock frequencies that support the full range of line rates for the SFP interface. The fixed frequency clock chip provides a 150MHz reference clock to bank 111 for the SATA-III interface.

Two other fixed frequency clocks supply the reference clock to the other GTX banks. Banks 109 and 110 are connected to the FMC HPC gigabit lanes and the reference clock inputs for those GTX lanes are sourced by the FMC connector. The following figure shows the clock sources provided to the dedicated GTX clock inputs.

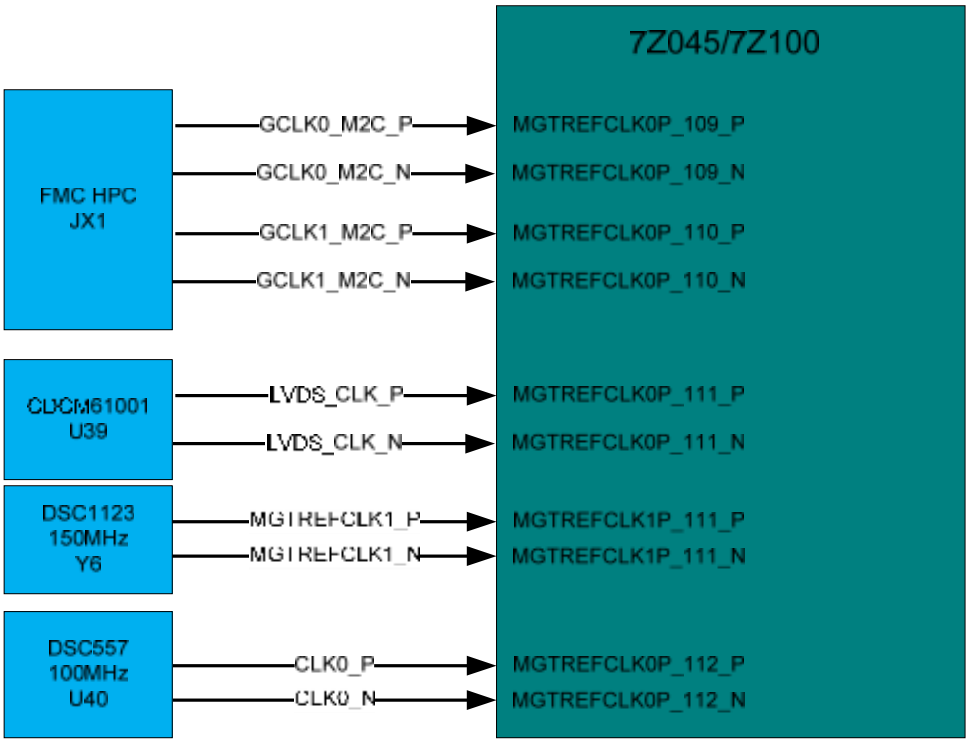

Figure 3 - GTX Clock Sources on the Zynq Mini-ITX Development Board

2.2.2 PCI Express x4 Interface

GTX transceiver bank 112 is connected to the PCI Express x4 card slot on the Zynq Mini-ITX Development Kit. PCI Express is an enhancement to the PCI architecture where the parallel bus has been replaced with a scalable, fully serial interface. The differences in the electrical interface are transparent to the software so existing PCI software implementations are compatible. Use of the Zynq Mini-ITX Development Kit in a PCI Express application requires the implementation of the PCI Express protocol in the Zynq-7000 AP SoC PL.

Zynq-7000 All Programmable System on Chip (SoC) with transceivers includes an Integrated Block for PCI Express technology that can be configured as an Endpoint or Root Port, compliant to the PCI Express Base Specification Revision 2.1. The Root Port can be used to build the basis for a compatible Root Complex, to allow custom communication between the Zynq-7000 AP SoC and other devices via the PCI Express protocol, and to attach ASSP Endpoint devices such as Ethernet Controllers or Wireless Adapters to the Zynq-7000 All Programmable SoC.

The PCI Express electrical interface on the Zynq Mini-ITX Development Kit consists of 4 lanes, having unidirectional transmit and receive differential pairs. It supports second generation PCI Express data rates of 5.0Gbps. In addition to the data lanes there is a 100MHz reference clock that is provided to the system slot. In order to work in open systems, add-in cards must use the reference clock provided over the PCI Express card edge to be frequency locked with the host system. The 100MHz clock is sourced from an on-board clock (U40) and forwarded to whatever add-in card is plugged into the Zynq Mini-ITX Development Board.

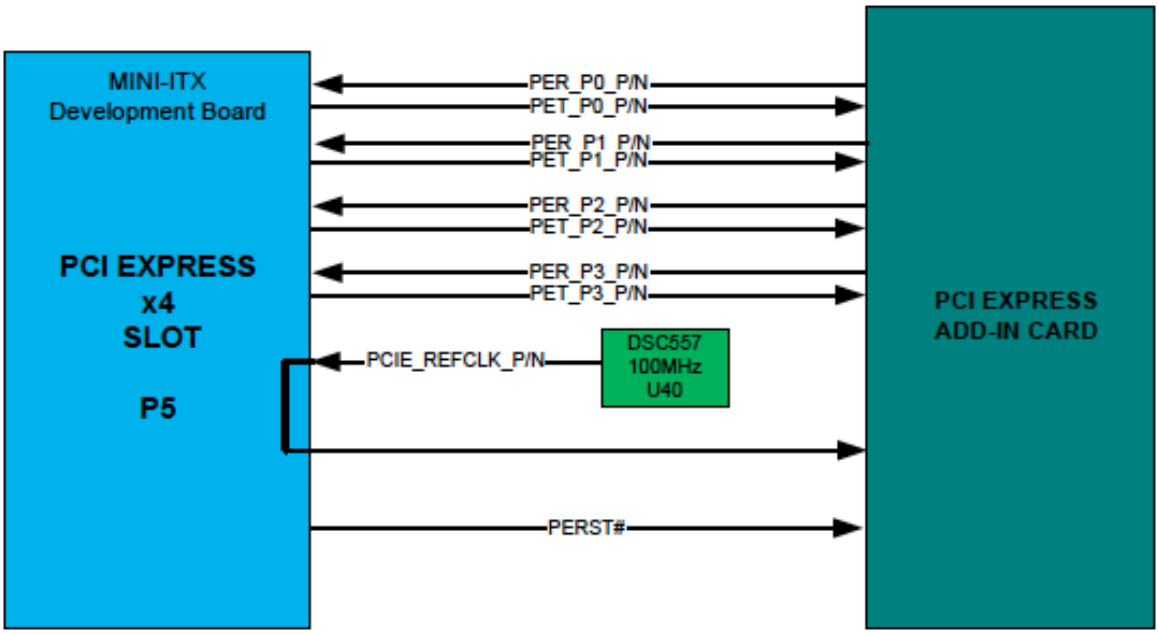

Figure 4 - PCI Express x4 Interface

The PCI Express transmit lanes are AC coupled (DC blocking capacitors are included in the signal path) as required by the PCI Express specification.

Bank 112	Net Name	7Z045/7Z100 Pin #
PCIE LANE 0	PET0_P	N4
	PET0_N	N3
	PER0_P	P6
	PER0_N	P5
PCIE LANE 1	PET1_P	P2
	PET1_N	P1
	PER1_P	T6
	PER1_N	T5
PCIE LANE 2	PET2_P	R4
	PET2_N	R3
	PER2_P	U4
	PER2_N	U3
PCIE LANE 3	PET3_P	T2
	PET3_N	T1
	PER3_P	V6
	PER3_N	V5

Table 5 - GTX Pin Assignments for PCI Express

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2.2.3 GTX for FMC Expansion Connector, SFP, and SATA

Three other high-speed gigabit interfaces are connected to the Zynq-7000 AP SoC. The SATA and SFP interfaces are one lane wide and reside on bank 111 of the Zynq-7000 AP SoC. Two transceiver lanes are not used in Bank 111.

Eight GTX transceiver ports are connected to the FMC HPC connector. The interface can be configured from one up to eight lanes depending on the FMC modules that is attached.

Bank 109	Net Name	7Z045/7Z100 Pin #
FMC DP0	DP0_C2M_P	AK10
	DP0_C2M_N	AK9
	DP0_M2C_P	AH10
	DP0_M2C_N	AH9
FMC DP1	DP1_C2M_P	AK6
	DP1_C2M_N	AK5
	DP1_M2C_P	AJ8
	DP1_M2C_N	AJ7
FMC DP2	DP2_C2M_P	AJ4
	DP2_C2M_N	AJ3
	DP2_M2C_P	AG8
	DP2_M2C_N	AG7
FMC DP3	DP3_C2M_P	AK2
	DP3_C2M_N	AK1
	DP2_M2C_P	AE8
	DP3_M2C_N	AE7
Bank 110	**Net Name**	**7Z045/7Z100 Pin #**
FMC DP4	DP4_C2M_P	AH2
	DP4_C2M_N	AH1
	DP4_M2C_P	AH5
	DP4_M2C_N	AH5
FMC DP5	DP5_C2M_P	AF2
	DP5_C2M_N	AF1
	DP5_M2C_P	AG4
	DP5_M2C_N	AG3
FMC DP6	DP6_C2M_P	AE4
	DP6_C2M_N	AE3
	DP6_M2C_P	AF6
	DP6_M2C_N	AF5
FMC DP7	DP7_C2M_P	AD2
	DP7_C2M_N	AD1
	DP7_M2C_P	AD6
	DP7_M2C_N	AD5

Bank 111	Net Name	7Z045/7Z100 Pin #
SFP	SFP_TX_P	AB2
	SFP_TX_N	AB1
	SFP_RX_P	AC4
	SFP_RX_N	AC3
SATA	SATA_TX_P	Y2
	SATA _TX_N	Y1
	SATA _RX_P	AB6
	SATA _RX_N	AB5
UNUSED		
UNUSED		

Table 6 - GTX Pin Assignments for FMC, SFP, and SATA

2.3 Memory

The Zynq Mini-ITX Development Kit is populated with both high-speed RAM and non-volatile ROM to support various types of applications. Each development board has five memory interfaces:

1. DDR3: 256GB x32 DDR3 SDRAM (PS)
2. DDR3: 256GB x32 DDR3 SDRAM (PL)
3. 32MB QSPI Flash
4. 8KB I2C EEPROM
5. SD Micro Card

2.3.1 DDR3 SDRAM Interface

The Zynq Mini-ITX Development Board utilizes two 1GB banks of DDR3 memory. One bank resides on the PS side of the Zynq-7000 AP SoC and the other on the PL side. The PL bank pin out is generated by MIG.

Each bank consists of two **Micron** DDR3 SDRAM devices, part number **MT41K256M16HA-125E:E**. Each bank is configured as a 1GB x32 SDRAM memory interface. Each device provides 512 MB of memory on a single IC and is organized as 32 Megabits x 16 x 8 banks. The device has an operating voltage of 1.5V and the interface is JEDEC Standard SSTL_15 (Class I for unidirectional signals, Class II for bidirectional signals). The -125E speed grade supports 1.25ns cycle times with 11 clock read latency (DDR3-1600).

The following figures show high-level block diagrams of the DDR3 SDRAM interfaces on the development board.

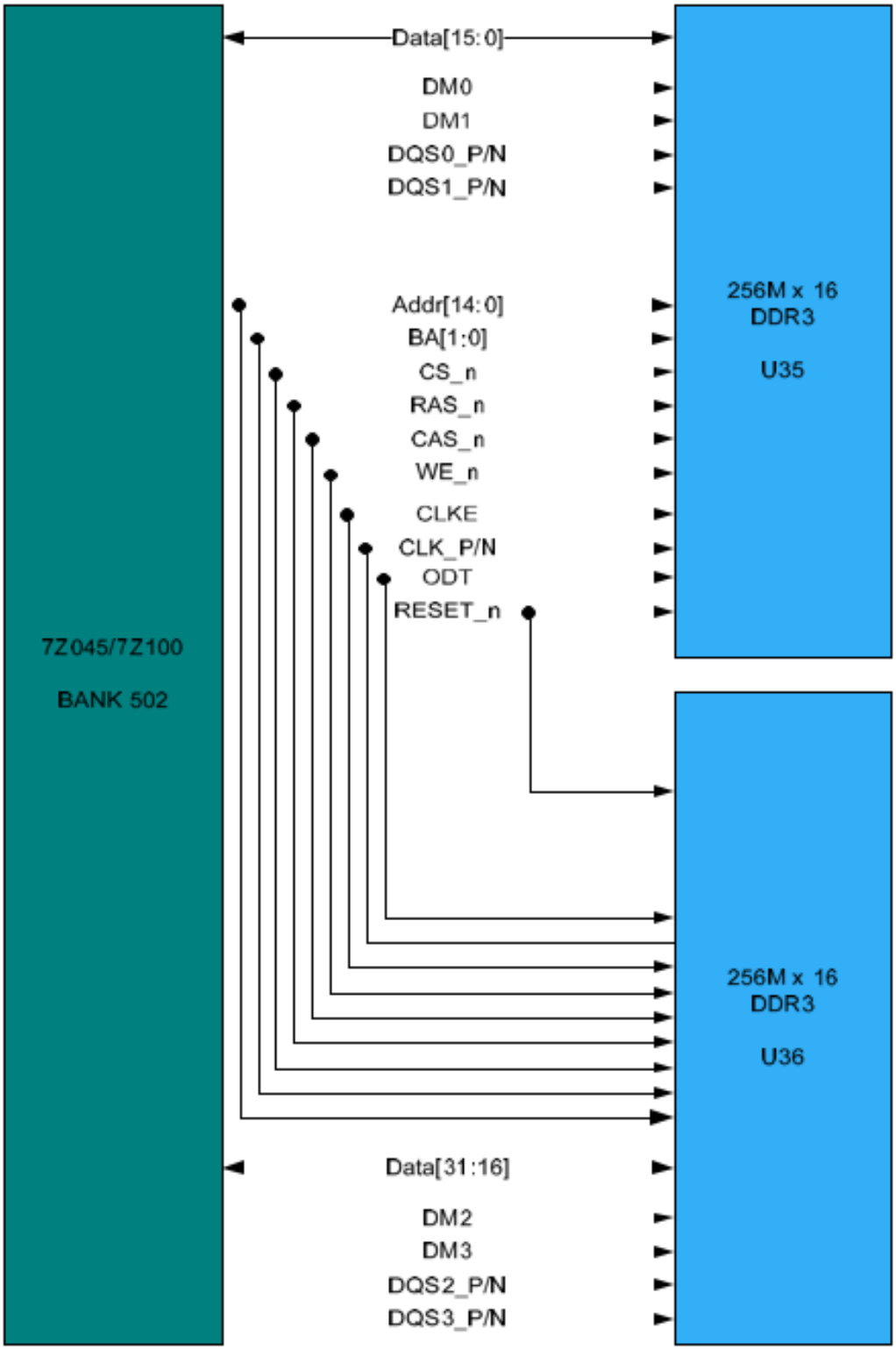

Figure 5 – PS DDR3 SDRAM Interface

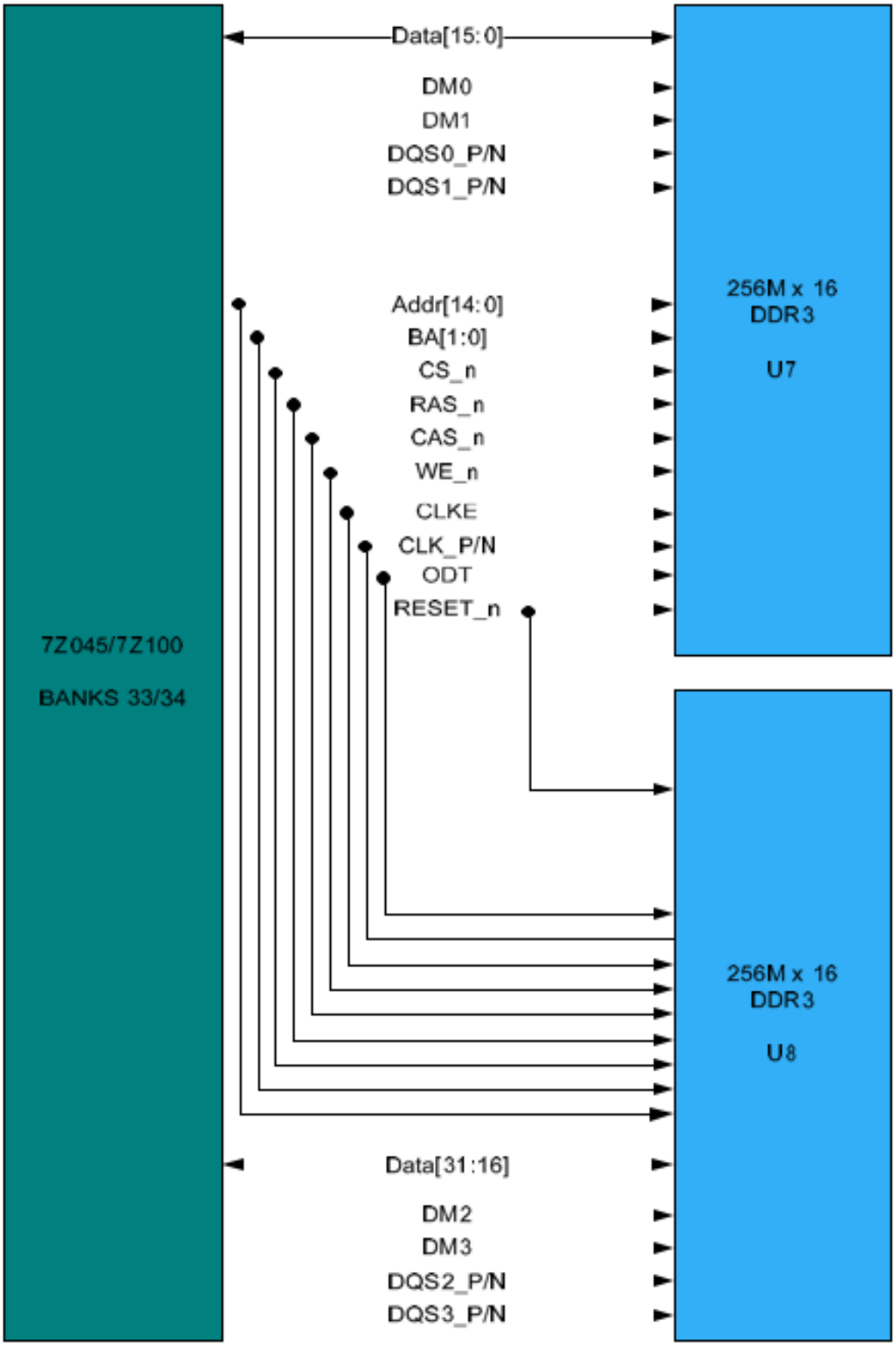

Figure 6 - PL DDR3 SDRAM Interface

The Zynq-7000 AP SoC VCCO pins for the bank 502, 33 and 34 are connected to 1.5V. This supply rail can be measured at the test point labeled 1.5_1.35V located just above the power module next to the power LEDs. The reference voltage pins (VREF) for the DDR3 banks are connected to the reference outputs of the Texas Instruments TPS51200. This device provides the termination voltage and reference voltage necessary for the DDR3 and Zynq-7000 AP SoC devices. The termination and reference voltage is 0.75V.

The following guidelines were used in the design of the DDR3 interface to the 7Z045. These guidelines are based on Micron recommendations and board level simulation.

- DDR3 devices routed with daisy-chain topology for shared signals of the two devices (clock, address, control).
- 40 ohm* controlled trace impedance for single ended signals. 80 ohm* differential impedance for differential signals.
- Dedicated data bus with matched trace lengths (+/- 50 mils).
- Memory clocks and data strobes routed differentially.
- Series termination following the memory device connection on shared signals (control, address).
- Termination supply that can both source and sink current.
- Ideal impedance values. Actual may vary.

All DDR3 signals are compliant to the Xilinx recommended and MIG generated pin out.

The following table contains the Zynq-7000 AP SoC PS pin assignments used for the DDR3 SDRAM interface.

NET NAME	7Z045/7Z100 PIN	NET NAME	7Z045/7Z100 PIN
DDR3_A0	L25	DDR3_D0	A25
DDR3_A1	K26	DDR3_D1	E25
DDR3_A2	L27	DDR3_D2	B27
DDR3_A3	G25	DDR3_D3	D25
DDR3_A4	J26	DDR3_D4	B25
DDR3_A5	G24	DDR3_D5	E26
DDR3_A6	H26	DDR3_D6	D26
DDR3_A7	K22	DDR3_D7	E27
DDR3_A8	F27	DDR3_D8	A29
DDR3_A9	J23	DDR3_D9	A27
DDR3_A10	G26	DDR3_D10	A30
DDR3_A11	H24	DDR3_D11	A28
DDR3_A12	K23	DDR3_D12	C28
DDR3_A13	H23	DDR3_D13	D30
DDR3_A14	J24	DDR3_D14	D28
		DDR3_D15	D29
DDR3_BA0	M27	DDR3_D16	H27
DDR3_BA1	M26	DDR3_D17	G27
DDR3_BA2	M25	DDR3_D18	H28
		DDR3_D19	E28
DDR3_WE#	N23	DDR3_D20	E30

DDR3_RAS#	N24	DDR3_D21	F28
DDR3_CAS#	M24	DDR3_D22	G30
DDR3_RST#	F25	DDR3_D23	F30
DDR3_ODT	L23	DDR3_D24	J29
DDR3_CKE	M22	DDR3_D25	K27
		DDR3_D26	J30
DDR3_CK0_P	K25	DDR3_D27	J28
DDR3_CK0_N	J25	DDR3_D28	K30
		DDR3_D29	M29
DDR3_DQS0_P	C26	DDR3_D30	L30
DDR3_DQS0_N	B26	DDR3_D31	M30
DDR3_DQS1_P	C29		
DDR3_DQS1_N	B29	DDR3_DM0	C27
DDR3_DQS2_P	G29	DDR3_DM1	B30
DDR3_DQS2_N	F29	DDR3_DM2	H29
DDR3_DQS3_P	L28	DDR3_DM3	K28
DDR3_DQS3_N	L29	DDR3_CS#	N22

Table 7 –Pin Assignments for PS DDR3

The following table contains the Zynq-7000 AP SoC PL pin assignments used for the DDR3 SDRAM interface.

NET NAME	7Z045/7Z100 PIN	NET NAME	7Z045/7Z100 PIN
DDR3_A0	J8	DDR3_D0	J3
DDR3_A1	E8	DDR3_D1	A1
DDR3_A2	F9	DDR3_D2	K1
DDR3_A3	D8	DDR3_D3	L3
DDR3_A4	D9	DDR3_D4	L2
DDR3_A5	F10	DDR3_D5	K5
DDR3_A6	G10	DDR3_D6	J5
DDR3_A7	D10	DDR3_D7	K6
DDR3_A8	E10	DDR3_D8	F2
DDR3_A9	G11	DDR3_D9	H6
DDR3_A10	H12	DDR3_D10	G6
DDR3_A11	D11	DDR3_D11	H2
DDR3_A12	E11	DDR3_D12	G1
DDR3_A13	H11	DDR3_D13	H4
DDR3_A14	J11	DDR3_D14	H3
		DDR3_D15	G5
DDR3_BA0	F7	DDR3_D16	F5
DDR3_BA1	F8	DDR3_D17	E5
DDR3_BA2	H8	DDR3_D18	F4
		DDR3_D19	F3

DDR3_WE#	H7	DDR3_D20	D3
DDR3_RAS#	E7	DDR3_D21	E3
DDR3_CAS#	D6	DDR3_D22	E2
DDR3_RST#	G4	DDR3_D23	E1
DDR3_ODT	J10	DDR3_D24	B5
DDR3_CKE	L7	DDR3_D25	B4
		DDR3_D26	C2
DDR3_CK0_P	L8	DDR3_D27	C1
DDR3_CK0_N	K8	DDR3_D28	B2
		DDR3_D29	B1
DDR3_DQS0_P	K3	DDR3_D30	A3
DDR3_DQS0_N	K2	DDR3_D31	A2
DDR3_DQS1_P	J1		
DDR3_DQS1_N	H1	DDR3_DM0	J4
DDR3_DQS2_P	E6	DDR3_DM1	G2
DDR3_DQS2_N	D5	DDR3_DM2	D4
DDR3_DQS3_P	A5	DDR3_DM3	C4
DDR3_DQS3_N	A4	DDR3_CS#	G7

Table 8 - Pin Assignments for PL DDR3

2.3.2 QSPI Flash Interface

The Zynq Mini-ITX Development Kit utilizes two on-board Spansion multi-bit (x4) SPI flash devices, part number **S25FL128SAGMFIR0** to configure the Zynq-7000 AP SoC PL quickly using the QSPI configuration mode. The QSPI devices are connected to bank 500 of the Zynq-7000 AP SoC.

The figure below shows the interface between the SPI flash and the Zynq-7000 AP SoC.

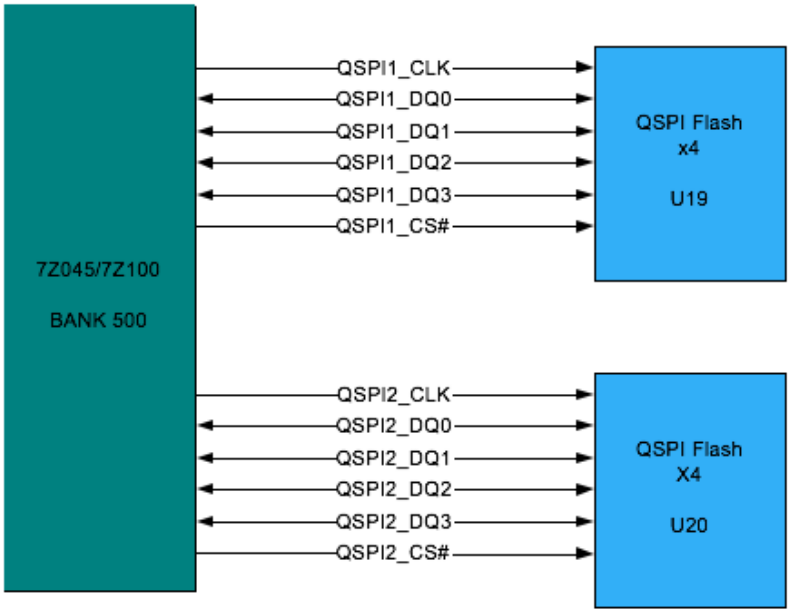

Figure 7 – QSPI Flash Interface

To configure the Zynq Mini-ITX Development Kit using the QSPI flash interface the configuration mode must be set to QSPI mode. This is accomplished by setting the configuration mode switch to the proper setting. The configuration mode switch is SW7. It is a five position slide switch. Setting SW7 to SW7[1:5] = x001x will put the Zynq Mini-ITX Development Kit in QSPI configuration mode at power-on. See Section 2.9 for more details on the various Zynq-7000 AP SoC configuration modes.

2.3.3 I2C EEPROM Interface

The Zynq Mini-ITX Development Kit has an on-board 8KB I2C EEPROM for additional data storage. A Micron M24C08-R is the device used. The I2C EEPROM is on the shared I2C bus. Refer to section 2.8 for more information on the Zynq Mini-ITX Development Board I2C bus.

2.3.4 MicroSD Card Interface

The Zynq Mini-ITX Development Kit implements a microSD card interface that can be used for boot configuration as well as additional data storage. The board ships with an 8 GB microSD card. The microSD card will be installed by the user at J4 for use with the Zynq Mini-ITX Development Board. The SD card that is shipped with the Zynq Mini-ITX Development Kit is pre- programmed with a Linux LED reference design. Refer to section 3.2 for more information on the Linux LED reference design.

When boot code is stored on the microSD card, configuration of the PS can be done by setting the configuration mode switch SW7 to the proper setting. The proper setting for configuring from the microSD card is **SW7[1:5]=x011x.** See Section 2.17 for more details on the various Zynq-7000 AP SoC configuration modes.

2.4 PL Global Clock Sources

The Zynq Mini-ITX Development Kit includes all of the necessary clocks to implement high-speed logic and GTX transceiver designs. All of these clocks are tied to the Zynq-7000 AP SoC MRCC pins giving access to the Zynq-7000 AP SoC global clock tree. The clock sources described in this section are used to derive the required clocks for the memory and communications devices, and the general system clocks for the logic design. For a description of the GTX reference clock sources, see Section 2.2.1**.**

The following figure shows the clock nets connected to the I/O banks of the Zynq-7000 AP SoC.

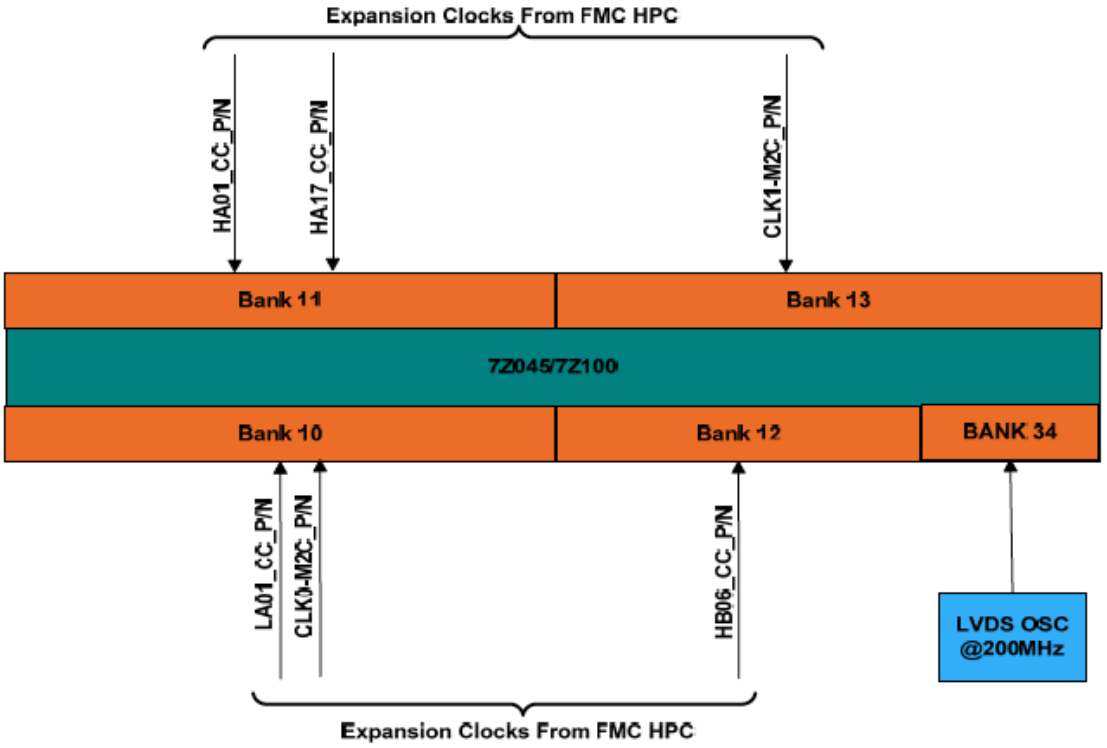

Figure 8 - Clock Nets Connected to PL Global Clock Inputs

The on-board 200MHz LVDS oscillator provides the system clock input to the global clock tree. This 200MHz clock can be used in conjunction with the Zynq-7000 AP SoC internal clock generators to generate the various logic clocks and the clocks forwarded to the DDR3 SDRAM devices.

Additionally, there is an on-board 33MHz LVTTL clock source connected to bank 500 and serves as the PS system clock.

2.4.1 CDCM61001 Programmable LVDS Clock Synthesizer

The Zynq Mini-ITX Development Kit design uses the **TI CDCM61001** LVDS frequency synthesizer for generating various clock frequencies as an input reference clock for GTX bank 111. A list of features included in the CDCM61001 device is shown below.

- Output frequency range: 43.75 MHz to 683.264 MHz
- RMS period jitter: 0.509ps @ 625 MHz
- Output rise and fall time: 255ps (maximum)
- Output duty cycle: varies dependent on output frequency

The following figure shows a high-level block diagram of the CDCM61001 programmable clock synthesizer. Inputs OS0 and OS1 are hard wired to use the LVDS mode of the CDCM61001 device.

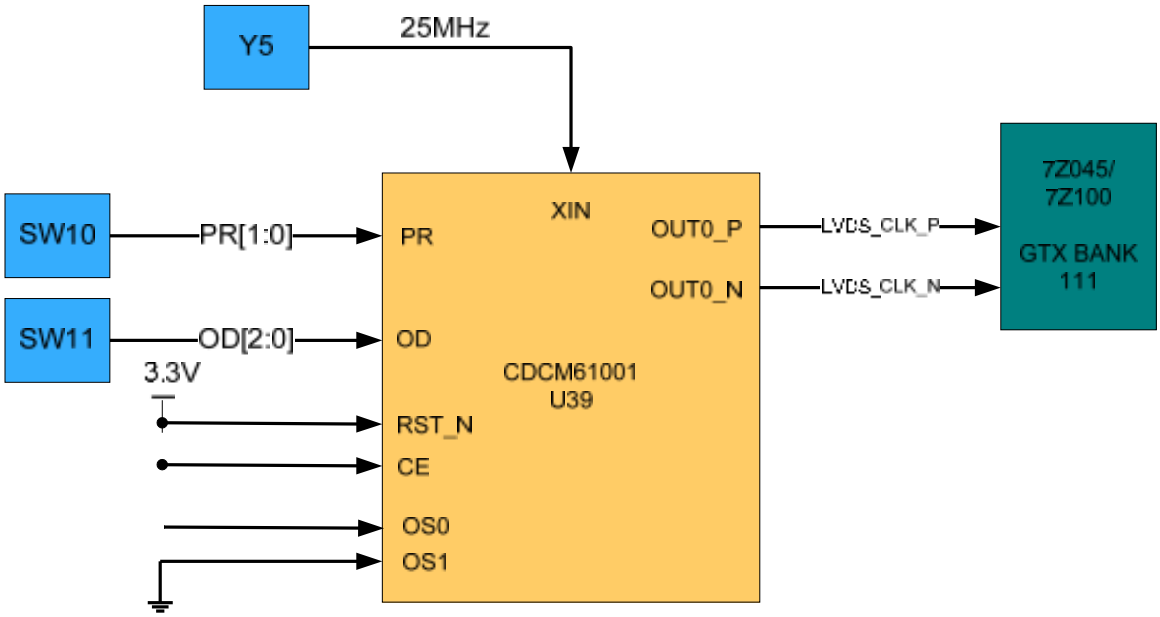

Figure 9 - CDCM61001 Clock Synthesizer

Signal Name	Direction	Pull up/Pull down	Description
PR[1:0]	Input	Pull up	Prescaler and Feedback divider control pins.
OD[2:0]	Input	Pull up	Output divider control pins.
OS[1:0]	Input	Pull up	Output type select control pins.
CE	Input	Pull up	Chip enable.
RST_N	Input	Pull up	Device reset (active low).
XIN	Input	Pull up	Parallel resonant crystal/LVCMOS input.
OUT0 P/N	Input		Differential output pair.

Table 9 - CDCM61001 Clock Synthesizer Pin Description

2.4.1.1 CDCM61001 Clock Generation

The CDCM61001 output clocks are generated based on the following formula (assuming the crystal clock input is 25 MHz):

FOUT = (FIN) (FD) / OD

Equation Variables:
FOUT = Output Frequency
FIN = Clock Input Frequency
FD = Feedback Divider Value
OD = Output Divider Value

Please refer to the CDCM61001 datasheet for detailed tables regarding the Feedback Divider and Output Divider values. The CDCM61001 FD and OD values are programmed via dipswitches **SW10** and **SW11**. These dipswitches should be configured prior to powering up the board.

The following table shows how to set the dipswitches for a common application. All the values are based on a 25 MHz crystal clock input to the CDCM61001 device.

Interconnect Technology	OUT0 and OUT1 (MHz)	PR1	PR0	OD2	OD1	OD0
SATA	150	0	0	0	1	1
GigE	125	1	1	0	1	1
10 GigE	156.25	1	0	0	1	1
12 GigE	187.5	0	1	0	0	1

Table 10 - CDCM61001 Common Application Settings

2.4.1.2 CDCM61001 Programming Mode

The Zynq Mini-ITX Development Board allows programming of the PR and OD values in parallel mode. This is the only mode supported by the device. In parallel mode, PR and OD values are programmed into the device upon the release of the master reset signal (rising edge of the MR_N signal). The switches should be set into the correct position prior to turning on power to the board. Should the switch settings change after power up the board will have to be power cycled to reset the device.

2.5 Communication

The Zynq Mini-ITX Development Kit utilizes Ethernet, USB 2.0 (Host mode only) and USB UART physical layer transceivers for communication purposes. Network access is provided by a single 10/100/1000 Mb/s Ethernet PHY device, which is connected to the Zynq-7000 AP SoC via a standard RGMII interface. The PHY device connects to the outside world with a standard RJ45 connector.

Serial port communication to the embedded ARM processor or Zynq-7000 AP SoC PL fabric is provided through a Silicon Labs USB-RS232 transceiver.

2.5.1 10/100/1000 Ethernet PHY

The PHY device is a **Marvel 88E1518**. The PHY is connected to a Tyco Electronics RJ-45 jack with integrated magnetics (part number: **1840808-7**). The jack also integrates two LEDs that indicate a valid link and traffic over the interface. The PHY clock is generated from a 25 MHz crystal. The following figure shows a high-level block diagram of the interface to the Ethernet PHY.

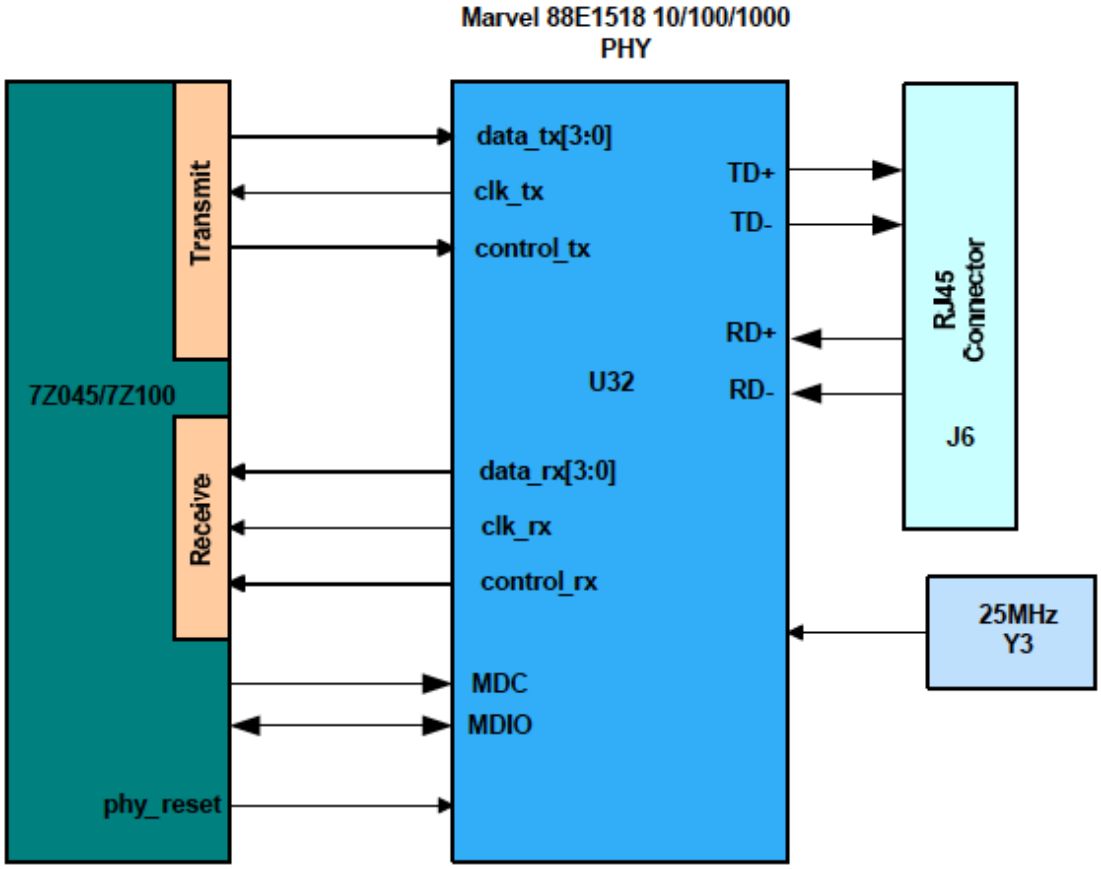

Figure 10 - 10/100/1000 Ethernet Interface

The PHY has two methods that can be used to reset the device. The PHY reset signal is ANDed (active low) with the on- board power-on reset circuit and one of the I/O pins in bank 500. If having the Zynq-7000 AP SoC reset the Ethernet PHY is desired toggle pin A18 LOW. To manually reset the PHY SW8 can be pressed. See section 2.7 for details about the power-on reset circuit.

The following tables provide the Zynq-7000 AP SoC pin assignments for the Ethernet PHY interface.

Net Name	7Z045 Pin #		Net Name	7Z045 Pin #
ETH_MDC	D19		ETH _RST#	A18 or SW8
ETH _MDIO	C18			
ETH _TX_CTRL			ETH _RX_CTRL	G20
ETH_TX_CLK	L19		ETH_RX_CLK	L20
ETH _TX_D0	K21		ETH _RX_D0	J21
ETH _TX_D1	K20		ETH _RX_D1	M19
ETH _TX_D2	J20		ETH _RX_D2	G19
ETH _TX_D3	M20		ETH _RX_D3	M17

Table 11 - Ethernet PHY Pin Assignments

2.5.2 USB UART

The Zynq Mini-ITX Development Kit implements a **Silicon Labs CP2103** device that provides a USB-to-RS232 bridge. The USB physical interface is brought out on a USB Micro-AB connector labeled “J7”.

The USB UART interface connects to the Zynq-7000 AP SoC at the following pins:

Net Name	7Z045 Pin #
USB_UART_RXD	C19
USB_UART_TXD	D18

Table 12 – USB UART Pin Assignments

2.5.3 USB 2.0

The Zynq Mini-ITX Development Kit implements a **SMSC USB3320** USB 2.0 PHY configured to operate in host mode. The USB3320 device is interfaced to the outside world via a 4-port USB hub (**Cypress CY7C65632)** and the 4-port USB type A connector “J5” on the board. In addition to the built-in ESD protection the USB3320 offers there are added ESD protection diodes on-board to protect against electrostatic discharge when plugging in a USB cable.

The USB3320 device is powered from 1.8V (VDDIO) and is clocked at 12MHz via “Y4”.

Resetting the USB 2.0 PHY can be done two ways. The USB_RESET# signal is wire ANDed (active low) by an I/O pin on the Zynq-7000 AP SoC and the power-on reset circuit. To reset the USB PHY via the Zynq-7000 AP SoC I/O pin toggle pin B24 LOW. To reset the USB PHY via the power-on reset circuit press SW9. See section 2.7 for details about the power-on reset circuit.

The table below shows the pin assignments of the USB 2.0 PHY to the Zynq-7000 AP SoC.

Net Name	7Z045 Pin #
USB_D0	K17
USB_D1	G22
USB_D2	K18
USB_D3	G21
USB_D4	L17
USB_D5	B21
USB_D6	A20
USB_D7	F18
USB_STP	L18
USB_NXT	H21
USB_DIR	H22
USB_CLK	H17
USB_RESET#	B24 or SW9

Table 13 – USB 2.0 Pin Assignments

When operating in host mode, the Zynq Mini-ITX Development Kit supplies 5V to the endpoint devices.

2.6 Real-Time Clock (RTC)

The Zynq Mini-ITX Development Kit has a real-time clock circuit that can be accessed via the I2C interface. The **Maxim DS1337** device is used for this purpose. The DS1337 can count seconds, minutes, hours, days, date, month and year with leap year compensation up to the year 2100.

The Real-Time Clock is on the shared I2C bus. Refer to section 2.8 for more information on the Zynq Mini-ITX Development Board I2C bus.

2.7 Power-on Reset

The Zynq Mini-ITX Development Kit utilizes a power-on reset IC and circuit to insure the Zynq-7000 AP SoC PS_POR# and PS_SRST# signals de-assert in the correct sequence at power-up. To accomplish this, the **Maxim MAX16025TE** device is used and is referenced on the board as “U21”. As shipped, the delay sequence is programmed to release the PS_SRST# signal before the PS_POR# signal. The delay for PS_POR# is adjustable and set by C106, which as shipped is a 3300pf capacitor.

Please also note that the PS_POR# signal also gates the reset signal of the Ethernet and USB 2.0 PHY devices.

The power-on reset circuit also allows for the reset outputs of the MAX16025TE device to be controlled manually by way of two push button switches. SW8 when depressed will assert the PS_POR# signal which will completely reset the processor and all of the Zynq-7000 AP SoC PS

registers. Depressing SW9 will assert the PS_SRST# signal which will send a soft reset to the Zynq-7000 AP SoC PS block. This reset signal will reset the processor but retain register data.

Both reset outputs can be asserted low together by placing a jumper on JP6 which is a master reset for the MAX16025TE device.

2.8 I2C Bus

The Zynq Mini-ITX Development Kit interfaces to several on-board I2C compatible devices and interfaces. These devices and interfaces include the 8KB EEPROM, real-time clock, FMC HPC, LVDS Touch Panel port, HDMI PHY and the Audio Codec. Communication between the Zynq-7000 AP SoC and end-point devices is done through a **Texas Instruments PCA9548A** 8- chanel I2C switch. Only six of the channels are used.

The I2C switch is driven by an I2C Master that can reside in either the PS or PL of the Zynq-7000 AP SoC. Only one Master can control the end-point devices at any given time. PL or PS Master control of the bus is determined by setting the jumper position on JP12. JP12 controls the enable signals on voltage translators between the Zynq-7000 AP SoC which operates at 1.8V (PL Bank 35 and PS Bank 501) and the I2C switch which operates at 3.3V. Setting **JP12:1-2** enables a PL master, while setting **JP12:2-3** enables a PS master.

The figure below shows a high level diagram of the I2C circuit on the Zynq Mini-ITX Development Kit.

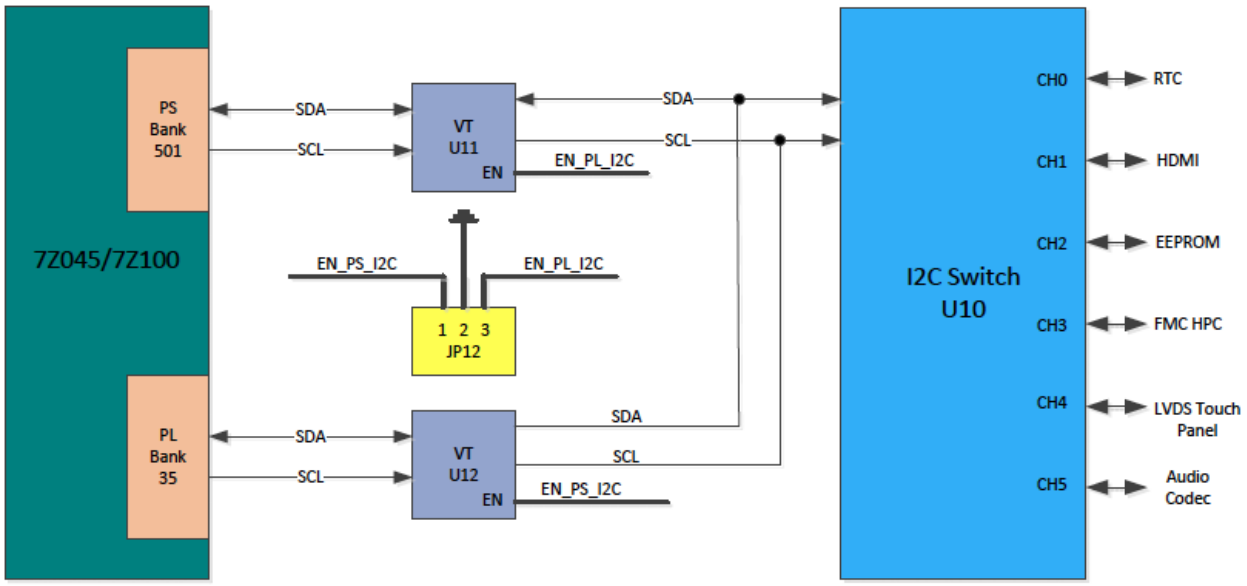

Figure 11 – Mini-ITX I2C Bus

2.9 Configuration

The Zynq Mini-ITX Development Kit supports several methods of configuring the Zynq-7000 AP SoC. The possible configuration sources include Boundary-scan (JTAG cable), QSPI and MicroSD card. The blue LED D3 labeled “DONE” on the baseboard illuminates to indicate when the Zynq-7000 AP SoC has been successfully configured.

2.9.1 Boot Mode Settings

Upon power-up the Zynq-7000 AP SoC will be enabled in a boot mode defined by the position of the switches on the five position slide switch “SW7”.

SW7 also controls the JTAG mode and whether the PS PLL is enabled or disabled.

SW7 position 0 controls the JTAG mode. The JTAG mode options are “cascaded” and “independent”. In cascaded mode, the PS and the PL systems of the Zynq-7000 AP SoC are included in the JTAG chain while in independent mode only the PL system is included. While in independent mode the ARM DAP is accessible but the user must use a separate JTAG cable via the 20-pin PJTAG connector J5.

SW7 position 4 controls the PLL.

The following table shows the two configuration modes and settings and the proper SW7 position settings:

Config Mode/Setting	SW7[1]	SW7[2]	SW7[3]	SW7[4]	SW7[5]
JTAG Cascaded	0	x	x	x	x
JTAG Independent	1	x	x	x	x
JTAG Config Mode	x	0	0	0	x
QSPI Config Mode	x	0	0	1	x
SD Card Config Mode	x	0	1	1	x
Disable PLL	x	x	x	x	0
Enable PLL	x	x	x	x	1

Table 14 - Setting the Configuration Mode “SW7”

2.9.2 JTAG Interface (PL TAP and ARM DAP)

A Xilinx parallel programmer or USB cable is required to configure the Zynq-7000 AP SoC in JTAG mode. The JTAG connector is referenced as J1.

Alternately, a simple USB type A-micro B cable can be used to access the JTAG chain by plugging into U3 (Digilent SMT2).

The Zynq-7000 AP SoC PROGRAM_B signal is asserted via push button SW1. The following figure shows a block diagram of the JTAG interface.

The JTAG chain also allows for the user to access the JTAG chain of the FMC HPC interface. Only one chain can be active at any given time (Zynq-7000 AP SoC or FMC HPC) by way of setting JP1 to the proper position.

The diagram below shows the Zynq Mini-ITX Development Kit JTAG circuit

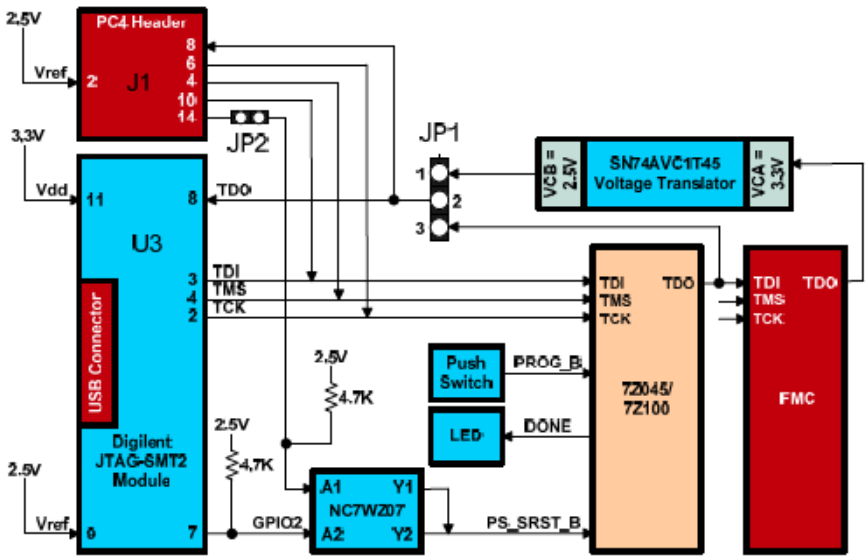

Figure 12 - JTAG Interface

Programming the Zynq-7000 AP SoC via boundary-scan mode requires a JTAG download cable if using the JTAG connector J1. For more information about JTAG download cables, perform a search on the Xilinx web page http://www.xilinx.com using the key words “Programming Cables”.

JP2 can be used to allow the JTAG programmer’s reset pin to assert the Zynq-7000 AP SoC PS_SRST# signal.

If using the Xilinx PC4 JTAG module (14-pin connector) the reset output on the cable is pin 14. If using the JTAG-SMT2 module pin 7 is the reset output.

2.9.3 PJTAG Interface (ARM DAP)

The Zynq Mini-ITX Development Kit has a dedicated JTAG connector that can be used to debug/trace the PS ARM processor via third party debugger/trace modules. This 20-pin connector is referenced on the board as J11. This JTAG connector cannot be used for Zynq-7000 AP SoC configuration. The PJTAG signals are connected to pins on the Zynq-7000 AP SoC at bank 13. The table below shows the connections between J11 and the Zynq-7000 AP SoC.

J11 pin	Signal Name	7Z045/7Z100 Pin
5	PJTAG_TDI	N26
7	PJTAG_TMS	T27
9	PJTAG_TCK	R27
13	PJTAG_TDO	N27

Table 15 – PJTAG Pin Assignments

JP8 gives the user an option to provide a reference voltage to the third party debugger module if required.

2.10 FMC HPC (High Pin Count) Expansion Connector

The FMC specification defines the HPC interface to be a 400-pin connector arranged in a 10x40 array. The FMC HPC configuration implemented on the Zynq Mini-ITX Development Kit uses one HPC connector (SAMTEC part number ASP- 134604-01), for a total of 160 user I/Os. The FMC HPC I/O is connected to the Zynq-7000 AP SoC at banks 10, 11, 12 and 13.

The FMC specification defines five user signal types: Differential I/O, Differential Clock Inputs, Differential Clock Outputs, MGT I/O, and MGT Clock Inputs. Because the FPGA I/Os can be configured for either single-ended or differential use, the differential I/Os defined in the FMC specification can serve a dual role. All the differential I/O signals can be configured as either differential pairs or single-ended signals, as required by the end application. In providing differential signaling, higher performance LVDS interfaces can be implemented between the Zynq Mini-ITX Development Kit and an FMC LPC or HPC module. Connection to high speed A/Ds, D/As, and flat panel displays are possible with this signaling configuration. Applications that require single-ended signals only can use each differential pair as two single-ended signals, for a total of 160 single-ended I/O on the connector.

Net Names	Signal Description	Pins per Connector
FMC_LA**_P/N	Differential I/O Pairs – LPC and HPC	68
FMC_HA**_P/N	Differential I/O Pairs – HPC Only	48
FMC_HB**_P/N	Differential I/O Pairs – HPC Only	44
Total	**User I/O**	**160**
FMC_CLK*_BIDIR_P/N	Differential BIDIR Clock Pair	4
FMC_CLK_DIR	BIDIR Clock Direction Pin	1
FMC_CLK*_M2C_P/N	Differential Input Clock Pair	4
Total	**Clock I/O**	**9**
FMC_DP*_M2C_P/N	4 Lane MGT Receive Differential Pairs	8
FMC_DP*_C2M_P/N	4 Lane MGT Transmit Differential Pairs	8
FMC_GBTCLK*_M2C_P/N	MGT Differential Clock Input Pairs	4
Total	**MGT I/O**	**20**

Table 16 - FMC HPC Connector Signals

The Zynq Mini-ITX Development Kit evaluation kit user I/O pins that connects to the FMC HPC connector is shown in the following table. The SAMTEC connector plug on the kit (CC-HPC-10 part number: ASP-134486-01) mates with the SAMTEC high pin count receptacle (MC-HPC-10 part number: ASP-134488-01) or low pin count receptacle (MC-LPC-10 part number: ASP-134604-01), located on FMC modules.

7Z045/7Z100 Pin Location	Schematic Net Name	FMC Connector Pin Location (JX1)	FMC Connector Symbol Name
-	GND	A1	GND
AJ8	DP1_M2C_P	A2	DP1_M2C_P
AJ7	DP1_M2C_N	A3	DP1_M2C_N
-	GND	A4	GND
-	GND	A5	GND
AG8	DP2_M2C_P	A6	DP2_M2C_P
AG7	DP2_M2C_N	A7	DP2_M2C_N
-	GND	A8	GND
-	GND	A9	GND

AE8	DP3_M2C_P	A10	DP3_M2C_P
AE7	DP3_M2C_N	A11	DP3_M2C_N
-	GND	A12	GND
-	GND	A13	GND
AH6	DP4_M2C_P	A14	DP4_M2C_P
AH5	DP4_M2C_N	A15	DP4_M2C_N
-	GND	A16	GND
-	GND	A17	GND
AG4	DP5_M2C_P	A18	DP5_M2C_P
AG3	DP5_M2C_N	A19	DP5_M2C_N
-	GND	A20	GND
-	GND	A21	GND
AK6	DP1_C2M_P	A22	DP1_C2M_P
AK5	DP1_C2M_N	A23	DP1_C2M_N
-	GND	A24	GND
-	GND	A25	GND
AJ4	DP2_C2M_P	A26	DP2_C2M_P
AJ3	DP2_C2M_N	A27	DP2_C2M_N
-	GND	A28	GND
-	GND	A29	GND
AK2	DP3_C2M_P	A30	DP3_C2M_P
AK1	DP3_C2M_N	A31	DP3_C2M_N
-	GND	A32	GND
-	GND	A33	GND
AH2	DP4_C2M_P	A34	DP4_C2M_P
AH1	DP4_C2M_N	A35	DP4_C2M_N
-	GND	A36	GND
-	GND	A37	GND
AF2	DP5_C2M_P	A38	DP5_C2M_P
AF1	DP5_C2M_N	A39	DP5_C2M_N
-	-	A40	GND
NC	10K PD	B1	RES1
-	GND	B2	GND
-	GND	B3	GND
N/C	N/C	B4	DP9_M2C_P
N/C	N/C	B5	DP9_M2C_N
-	GND	B6	GND
-	GND	B7	GND
N/C	N/C	B8	DP8_M2C_P
N/C	N/C	B9	DP8_M2C_N
-	GND	B10	GND
-	GND	B11	GND
AD6	DP7_M2C_P	B12	DP7_M2C_P
AD5	DP7_M2C_N	B13	DP7_M2C_N

-	GND	B14	GND
-	GND	B15	GND
AF6	DP6_M2C_P	B16	DP6_M2C_P
AF5	DP6_M2C_N	B17	DP6_M2C_N
-	GND	B18	GND
-	GND	B19	GND
AA8	GCLK1_M2C_P	B20	GBTCLK1_M2C_P
AA7	GCLK1_M2C_N	B21	GBTCLK1_M2C_N
-	GND	B22	GND
-	GND	B23	GND
N/C	N/C	B24	DP9_C2M_P
N/C	N/C	B25	DP9_C2M_N
-	GND	B26	GND
-	GND	B27	GND
N/C	N/C	B28	DP8_C2M_P
N/C	N/C	B29	DP8_C2M_N
-	GND	B30	GND
-	GND	B31	GND
AD2	DP7_C2M_P	B32	DP7_C2M_P
AD1	DP7_C2M_N	B33	DP7_C2M_N
-	GND	B34	GND
-	GND	B35	GND
AE4	DP6_C2M_P	B36	DP6_C2M_P
AE3	DP6_C2M_N	B37	DP6_C2M_N
-	GND	B38	GND
-	GND	B39	GND
N/C	N/C	B40	RES0
-	GND	C1	GND
AK10	DP0_C2M_P	C2	DP0_C2M_P
AK9	DP0_C2M_N	C3	DP0_C2M_N
-	GND	C4	GND
-	GND	C5	GND
AH10	DP0_M2C_P	C6	DP0_M2C_P
AH9	DP0_M2C_N	C7	DP0_M2C_N
-	GND	C8	GND
-	GND	C9	GND
AC14	LA06_P	C10	LA06_P
AC13	LA06_N	C11	LA06_N
-	GND	C12	GND
-	GND	C13	GND
AJ16	LA10_P	C14	LA10_P
AK16	LA10_N	C15	LA10_N
-	GND	C16	GND
-	GND	C17	GND

AG12	LA14_P	C18	LA14_P
AH12	LA14_N	C19	LA14_N
-	GND	C20	GND
-	GND	C21	GND
U25	LA18_CC_P	C22	LA18_P_CC
V26	LA18_CC_N	C23	LA18_N_CC
-	GND	C24	GND
-	GND	C25	GND
V27	LA27_P	C26	LA27_P
W28	LA27_N	C27	LA27_N
-	GND	C28	GND
-	GND	C29	GND
I2C SWITCH	I2C_SDA_1	C30	SCL
I2C SWITCH	I2C_SCL_1	C31	SDA
-	GND	C32	GND
-	GND	C33	GND
-	GA0	C34	GA0
-	**12.0V**	C35	**12P0V**
-	-	C36	GND
	12.0V	C37	**12P0V**
-	-	C38	GND
-	**3.3V**	C39	**3P3V**
-	-	C40	GND
-	2.5V	D1	PG_C2M
-	GND	D2	**GND**
-	GND	D3	**GND**
AD10	GCLK0_M2C_P	D4	GBTCLK0_M2C_P
AD9	GCLK0_M2C_N	D5	GBTCLK0_M2C_N
-	GND	D6	**GND**
-	GND	D7	**GND**
AF14	LA01_CC_P	D8	LA01_P_CC
AG14	LA01_CC_N	D9	LA01_N_CC
-	**GND**	D10	**GND**
AD16	LA05_P	D11	LA05_P
AD15	LA05_N	D12	LA05_N
-	**GND**	D13	**GND**
AE16	LA09_P	D14	LA09_P
AE15	LA09_N	D15	LA09_N
-	**GND**	D16	**GND**
AH14	LA13_P	D17	LA13_P
AH13	LA13_N	D18	LA13_N
-	**GND**	D19	**GND**
AF15	LA17_CC_P	D20	LA17_P_CC
AG15	LA17_CC_N	D21	LA17_N_CC

-	**GND**	D22	**GND**
AA15	LA23_P	D23	LA23_P
AA14	LA23_N	D24	LA23_N
-	**GND**	D25	**GND**
W25	LA26_P	D26	LA26_P
W26	LA26_N	D27	LA26_N
-	**GND**	D28	**GND**
Y12	JTAG_TCK	D29	TCK
P10	JTAG_TDI	D30	TDI
-Y10	TDO_0	D31	TDO
-	**3.3V**	D32	**3P3VAUX**
V10	JTAG_TMS	D33	TMS
AD18	TRST_L	D34	TRST_L
-	GA1	D35	GA1
-	**3.3V**	D36	**3P3V**
-	**GND**	D37	GND
-	**3.3V**	D38	**3P3V**
-	GND	D39	GND
-	**3.3V**	D40	**3P3V**
-	**GND**	E1	**GND**
AE22	HA01_CC_P	E2	HA01_P_CC
AF22	HA01_CC_N	E3	HA01_N_CC
-	**GND**	E4	**GND**
-	**GND**	E5	**GND**
Y22	HA05_P	E6	HA05_P
Y23	HA05_N	E7	HA05_N
-	**GND**	E8	**GND**
AA24	HA09_P	E9	HA09_P
AB24	HA09_N	E10	HA09_N
-	**GND**	E11	**GND**
AH23	HA13_P	E12	HA13_P
AH24	HA13_N	E13	HA13_N
-	**GND**	E14	**GND**
AJ20	HA16_P	E15	HA16_P
AK20	HA16_N	E16	HA16_N
-	**GND**	E17	**GND**
AF19	HA20_P	E18	HA20_P
AG19	HA20_N	E19	HA20_N
-	**GND**	E20	**GND**
Y28	HB03_P	E21	HB03_P
AA29	HB03_N	E22	HB03_N
-	**GND**	E23	**GND**
AB29	HB05_P	E24	HB05_P
AB30	HB05_N	E25	HB05_N

-	**GND**	E26	**GND**
AD30	HB09_P	E27	HB09_P
AE30	HB09_N	E28	HB09_N
-	**GND**	E29	**GND**
AF29	HB13_P	E30	HB13_P
AG29	HB13_N	E31	HB13_N
-	**GND**	E32	**GND**
AG26	HB19_P	E33	HB19_P
AG27	HB19_N	E34	HB19_N
-	**GND**	E35	**GND**
AA27	HB21_P	E36	HB21_P
AA28	HB21_N	E37	HB21_N
-	**GND**	E38	**GND**
-	**VADJ**	E39	**VADJ**
-	**GND**	E40	**GND**
-	-	F1	PG_M2C
-	**GND**	F2	**GND**
-	**GND**	F3	**GND**
AD23	HA00_CC_P	F4	HA00_P_CC
AE23	HA00_CC_N	F5	HA00_N_CC
-	**GND**	F6	**GND**
AA22	HA04_P	F7	HA04_P
AA23	HA04_N	F8	HA04_N
-	**GND**	F9	**GND**
AF20	HA08_P	F10	HA08_P
AG20	HA08_N	F11	HA08_N
-	**GND**	F12	**GND**
AK22	HA12_P	F13	HA12_P
AK23	HA12_N	F14	HA12_N
-	**GND**	F15	**GND**
AH19	HA15_P	F16	HA15_P
AJ19	HA15_N	F17	HA15_N
-	**GND**	F18	**GND**
W21	HA19_P	F19	HA19_P
Y21	HA19_N	F20	HA19_N
-	**GND**	F21	**GND**
Y30	HB02_P	F22	HB02_P
AA30	HB02_N	F23	HB02_N
-	**GND**	F24	**GND**
AC29	HB04_P	F25	HB04_P
AD29	HB04_N	F26	HB04_N
-	**GND**	F27	**GND**
AF30	HB08_P	F28	HB08_P
AG30	HB08_N	F29	HB08_N

-	**GND**	F30	**GND**
AK27	HB12_P	F31	HB12_P
AK28	HB12_N	F32	HB12_N
-	**GND**	F33	**GND**
AB25	HB16_P	F34	HB16_P
AB26	HB16_N	F35	HB16_N
-	**GND**	F36	**GND**
Y26	HB20_P	F37	HB20_P
Y27	HB20_N	F38	HB20_N
-	**GND**	F39	**GND**
-	**VADJ**	F40	**VADJ**
-	**GND**	G1	**GND**
U26	CLK1_M2C_P	G2	CLK1_M2C_P
U27	CLK1_M2C_N	G3	CLK1_M2C_N
-	**GND**	G4	**GND**
-	**GND**	G5	**GND**
AE13	LA00_CC_P	G6	LA00_P_CC
AF13	LA00_CC_N	G7	LA00_N_CC
-	**GND**	G8	**GND**
AB17	LA03_P	G9	LA03_P
AB16	LA03_N	G10	LA03_N
-	**GND**	G11	**GND**
AE18	LA08_P	G12	LA08_P
AE17	LA08_N	G13	LA08_N
-	**GND**	G14	**GND**
AH18	LA12_P	G15	LA12_P
AJ18	LA12_N	G16	LA12_N
-	**GND**	G17	**GND**
AD14	LA16_P	G18	LA16_P
AD13	LA16_N	G19	LA16_N
-	**GND**	G20	**GND**
AK13	LA20_P	G21	LA20_P
AK12	LA20_N	G22	LA20_N
-	**GND**	G23	**GND**
AE12	LA22_P	G24	LA22_P
AF12	LA22_N	G25	LA22_N
-	**GND**	G26	**GND**
R28	LA25_P	G27	LA25_P
T28	LA25_N	G28	LA25_N
-	**GND**	G29	**GND**
T30	LA29_P	G30	LA29_P
U30	LA29_N	G31	LA29_N
-	**GND**	G32	**GND**
V28	LA31_P	G33	LA31_P

V29	LA31_N	G34	LA31_N
-	**GND**	G35	**GND**
N29	LA33_P	G36	LA33_P
P29	LA33_N	G37	LA33_N
-	**GND**	G38	**GND**
-	**VADJ**	G39	**VADJ**
-	**GND**	G40	**GND**
-	NC	H1	VREF_A_M2C
AC19	PRSNT_M2C_L	H2	PRSNT_M2C_L
-	**GND**	H3	**GND**
AG17	CLK0_M2C_P	H4	CLK0_M2C_P
AG16	CLK0_M2C_N	H5	CLK0_M2C_N
-	**GND**	H6	**GND**
AB15	LA02_P	H7	LA02_P
AB14	LA02_N	H8	LA02_N
-	**GND**	H9	**GND**
AC17	LA04_P	H10	LA04_P
AC16	LA04_N	H11	LA04_N
-	**GND**	H12	**GND**
AF18	LA07_P	H13	LA07_P
AF17	LA07_N	H14	LA07_N
-	**GND**	H15	**GND**
AH17	LA11_P	H16	LA11_P
AH16	LA11_N	H17	LA11_N
-	**GND**	H18	**GND**
AJ15	LA15_P	H19	LA15_P
AK15	LA15_N	H20	LA15_N
-	**GND**	H21	**GND**
AJ14	LA19_P	H22	LA19_P
AJ13	LA19_N	H23	LA19_N
-	**GND**	H24	**GND**
AB12	LA21_P	H25	LA21_P
AC12	LA21_N	H26	LA21_N
-	**GND**	H27	**GND**
T29	LA24_P	H28	LA24_P
U29	LA24_N	H29	LA24_N
-	**GND**	H30	**GND**
W29	LA28_P	H31	LA28_P
W30	LA28_N	H32	LA28_N
-	**GND**	H33	**GND**
P30	LA30_P	H34	LA30_P
R30	LA30_N	H35	LA30_N
-	**GND**	H36	**GND**
N28	LA32_P	H37	LA32_P

P28	LA32_N	H38	LA32_N
-	**GND**	H39	**GND**
-	**VADJ**	H40	**VADJ**
-	**GND**	J1	**GND**
R25	CLK1_C2M_P	J2	CLK1_C2M_P
R26	CLK1_C2M_N	J3	CLK1_C2M_N
-	**GND**	J4	**GND**
-	**GND**	J5	**GND**
AB21	HA03_P	J6	HA03_P
AB22	HA03_N	J7	HA03_N
-	**GND**	J8	**GND**
AF23	HA07_P	J9	HA07_P
AF24	HA07_N	J10	HA07_N
-	**GND**	J11	**GND**
AJ25	HA11_p	J12	HA11_P
AK25	HA11_N	J13	HA11_N
-	**GND**	J14	**GND**
AJ21	HA14_P	J15	HA14_P
AK21	HA14_N	J16	HA14_N
-	**GND**	J17	**GND**
AK17	HA18_P	J18	HA18_P
AK18	HA18_N	J19	HA18_N
-	**GND**	J20	**GND**
AD21	HA22_P	J21	HA22_P
AE21	HA22_N	J22	HA22_N
-	**GND**	J23	**GND**
AD25	HB01_P	J24	HB01_P
AE26	HB01_N	J25	HB01_N
-	**GND**	J26	**GND**
AE25	HB07_P	J27	HB07_P
AF25	HB07_N	J28	HB07_N
-	**GND**	J29	**GND**
AJ30	HB11_P	J30	HB11_P
AK30	HB11_N	J31	HB11_N
-	**GND**	J32	**GND**
AH28	HB15_P	J33	HB15_P
AH29	HB15_N	J34	HB15_N
-	**GND**	J35	**GND**
AC26	HB18_P	J36	HB18_P
AD26	HB18_N	J37	HB18_N
-	**GND**	J38	**GND**
-	**+VIO_B_M2C**	J39	**VIO_B_M2C**
-	**GND**	J40	**GND**
-	NC	K1	**VREF_B_M2C**

-	**GND**	K2	**GND**
-	**GND**	K3	**GND**
U26	CLK1_M2C_P	K4	CLK1_M2C_P
U27	CLK1_M2C_N	K5	CLK1_M2C_N
-	**GND**	K6	**GND**
AC24	HA02_P	K7	HA02_P
AD24	HA02_N	K8	HA02_N
-	**GND**	K9	**GND**
AG24	HA06_P	K10	HA06_P
AG25	HA06_N	K11	HA06_N
-	**GND**	K12	**GND**
AJ23	HA10_P	K13	HA10_P
AJ24	HA10_N	K14	HA10_N
-	**GND**	K15	**GND**
AG21	HA17_CC_P	K16	HA17_P_CC
AH21	HA17_CC_N	K17	HA17_N_CC
-	**GND**	K18	**GND**
AG22	HA21_P	K19	HA21_P
AH22	HA21_N	K20	HA21_N
-	**GND**	K21	**GND**
AC22	HA23_P	K22	HA23_P
AC23	HA23_N	K23	HA23_N
-	**GND**	K24	**GND**
AB27	HB00_CC_P	K25	HB00_CC_P
AC27	HB00_CC_N	K26	HB00_CC_N
-	**GND**	K27	**GND**
AE28	HB06_CC_P	K28	HB06_CC_P
AF28	HB06_CC_N	K29	HB06_CC_N
-	**GND**	K30	**GND**
AJ28	HB10_P	K31	HB10_P
AJ29	HB10_N	K32	HB10_N
-	**GND**	K33	**GND**
AH26	HB14_P	K34	HB14_P
AH27	HB14_N	K35	HB14_N
-	**GND**	K36	**GND**
AE27	HB17_CC_P	K37	HB17_CC_P
AF27	HB17_CC_N	K38	HB17_CC_N
-	**GND**	K39	**GND**
-	**+VIO_B_M2C**	K40	**VIO_B_M2C**

Table 17 - FMC HPC Connector Pin Locations

2.11 HDMI

The Zynq Mini-ITX Development Kit has an HDMI video interface that supports up to HDMI v1.4 and resolutions up to 1080p. An Analog Devices ADV7511 low power HDMI transmitter is used to drive the interface. The ADV7511 used both 1.8V and 3.3V to power the device with the I/O logic level at 1.8V.

The ADV7511 is a high speed High Definition Multimedia Interface (HDMI) transmitter that is capable of supporting an input data rate up to 165MHz (1080p @ 60Hz, UXGA @ 60Hz) and an output data rate up to 225MHz. Deep Color to 36 bits per pixel is supported to 1080p at 60Hz.

The ADV7511 is clocked at 12MHz from the clock chip U33.

Configuration of the ADV7511 is done over the I2C interface (I2C switch U10 Channel 1).

The HDMI digital interface is 16-bits wide and is connected to bank 35 of the Zynq-7000 AP SoC. The table below shows the connections to the Zynq-7000 AP SoC.

Signal Name	7Z045/7Z100 Pin
HDMI_D8	G17
HDMI_D9	G16
HDMI_D10	H16
HDMI_D11	J16
HDMI_D12	G15
HDMI_D13	F15
HDMI_D14	J15
HDMI_D15	K15
HDMI_D16	F14
HDMI_D17	G14
HDMI_D18	F13
HDMI_D19	G12
HDMI_D20	E13
HDMI_D21	D13
HDMI_D22	F12
HDMI_D23	E12
HDMI_DE	E16
HDMI_ CLK	E15
HDMI_VSYNC	D15
HDMI_HSYNC	D14
HDMI_SPDIF	F17
HDMI_SPDIF_OUT	E17
HDMI_INT	D16

Table 18 – HDMI Pin Assignments

2.12 LVDS Touch Panel Display Port

The Zynq Mini-ITX Development Kit has a port that supports the Avnet ALI3 Touch Panel (PN: AES-ALI2_ZED-G).

The 7-inch Zed Touch Display Kit provides engineers with everything needed to develop products with interactive GUIs and touchscreen capabilities. The kit combines an 800 x 480 WVGA TFT-LCD display with an industrial projective capacitive touch sensor, I2C-based touch controller, LED backlight supply and all the necessary cables.

The touch display connects to the Zynq Mini-ITX Development Kit through a standard DisplayPort cable and adapter cards. The projected capacitive touch overlay provides enhanced touch ruggedness which is suitable for outdoor or industrial environments.

The 7-inch Zed Touch Display Kit is supported by the www.microzed.org community website where users can download kit documentation and reference designs as well as collaborate with other engineers also working on Zynq designs.

The touch panel is configured over the I2C interface (I2C switch U10, Channel 4). The table below shows the connections to the Zynq-7000 AP SoC.

Signal Name	7Z045/7Z100 Pin
D0_P	T24
D0_N	T25
D1_P	U22
D1_N	V22
D2_P	T22
D2_N	T23
D3_P	P25
D3_N	P26
CLK_P	P23
CLK_N	P24
LVDS_IRQ#	AA20

Table 19 – LVDS Pin Assignments

2.13 Audio Codec

The Zynq Mini-ITX Development Kit implements an audio codec circuit to drive the audio jack interface on the I/O back panel.

The **Analog Devices ADAU1761** is a low power, stereo audio codec with integrated digital audio processing that supports stereo 48 kHz record and playback at 14 mW from a 1.8 V analog supply. The stereo audio ADCs and DACs support sample rates from 8 kHz to 96 kHz as well as a digital volume control.

There audio jack interface consists of two Kycon STX4235-3/3-N dual 3.5mm audio jacks J2 (A and B) and J3 (A and B) for a total of four audio jacks.

J2A (top jack) is a headphone output, J2B (bottom jack) is Stereo single-ended output, J3A is configured as a differential input to the codec and J3B is a stereo single-ended input.

The figure below shows what the jacks look like.

Figure 13 – Audio Jacks

The table below shows the signal connections to the Zynq-7000 AP SoC.

Signal Name	7Z045/7Z100 Pin
AUD_GPIO0	C17
AUD_GPIO1	B16
AUD_GPIO2	B17
AUD_GPIO3	A17
AUD_ADR0	C12
AUD_ADR1	B12
AUD_MCLK	C14

Table 20 – Audio Codec Pin Assignments

2.14 LEDs, Push Buttons and Switches

The Zynq Mini-ITX Development Kit has a variety of user GPIO assigned to LEDs, push buttons and switches.

Four momentary closure push buttons is installed on the board and connected to the Zynq-7000 AP SoC I/O. These buttons can be programmed by the user and are ideal for logic reset and similar functions. Pull down resistors hold the signals low until the switch closure pulls them high (active high signals). The push button switches are designated on the board as SW4, SW5, SW6 and SW7. The table below shows the push button pin assignments to the Zynq-7000 AP SoC.

Signal Name	7Z045/7Z100 Pin
PB0	B14
PB1	A14
PB2	A13
PB3	A12

Table 21 – Push Button Pin Assignments

An eight-position dipswitch (SPST) is installed on the board. These switches provide digital inputs to user logic as needed. The signals are pulled low by 4.7K ohm resistors when the switch is open and tied high when closed. The table below shows the dipswitch pin assignments to the Zynq-7000 AP SoC.

Signal Name	7Z045/7Z100 Pin
SW0	C7
SW1	B7
SW2	A7
SW3	B9
SW4	A8
SW5	A9
SW6	B10
SW7	A10

Table 22 – DIP Switch Pin Assignments

Eight discrete user LEDs are installed on the board and can be used to display the status of the Zynq-7000 AP SoC internal logic. These LEDs are attached as shown below and are lit by forcing the associated I/O pin to a logic '1' and are off when the pin is either low (0) or not driven. The table below shows the user LED pin assignments to the Zynq-7000 AP SoC.

Signal Name	7Z045/7Z100 Pin
LED0	C6
LED1	B6
LED2	L9
LED3	L10
LED4	K10
LED5	K11
LED6	L12
LED7	K12

Table 23 – User LED Pin Assignments

2.15 Power

The Zynq Mini-ITX Development Kit power is derived from a +12V input provided by the 24-pin ATX power connector P2. All of the voltage rails used on the board are derived from the 12V source. The 12V source is used to supply the input voltages to a variety of switching regulators that reside on the power module installed on the Mini-ITX board. The Zynq Mini-ITX Development Kit comes installed with the Maxim power module Avnet part number: BD-POM-MXM1-G.

Below is a link that provides more detailed information about the Maxim power module. http://avnet.com/us/design/drc/Pages/Maxim-Power-Module.aspx

The voltage rails produced by the power module are: 1.5V/1.35V (jumper selectable on the power module), 1.8V, 2.0V, 3.3V, 1.0V, 1.0V_MGT, and 1.2V_MGT.

Connectors J8 and J9 are the main power connectors that source the voltage rails to the main board. The voltage assignments are as listed below:

Pin	1	2	3	4	5	6	7	8	9	10
Signal	GND	1.5V/1.35V	GND	1.8V	GND	2V	GND	3.3V	GND	12V

Table 24 – Power Connector J8 Pin Assignments

Pin	1	2	3	4	5	6	7	8
Signal	GND	1V	GND	1V(MGT)	GND	1.2V	GND	2.5V

Table 25 – Power Connector J9 Pin Assignments

The Zynq Mini-ITX Development Kit also implements remote sense feedback to the power module regulators via connector J10. The remote sense feedback nodes are placed strategically at the heaviest loads on the main board and the remote sense signal fed back to the power modules on J10. Implementing remote sense helps insure the voltages are being tightly regulated and kept within the Zynq specification.

Below are the pin assignments for the remote sense connector J10:

Pin	2	4	6	8	10
Signal	2.5Vrm	1Vmgtrm	2Vrm	1.2Vrm	rmGND
Pin	1	3	5	7	9
Signal	3.3Vrm	1.8Vrm	1Vrm	1.5Vrm	rmGND

Table 26 – Remote Sense Connector Pin Assignments

2.15.1 FMC VADJ

VADJ is a selectable voltage used for sending supply voltage to the FMC HPC module connector JX1. The voltage options are 1.8V, 2.5V or 3.3V. VADJ is selected by placing the jumper shunt on JP7 in the correct position. Below is a diagram of JP7.

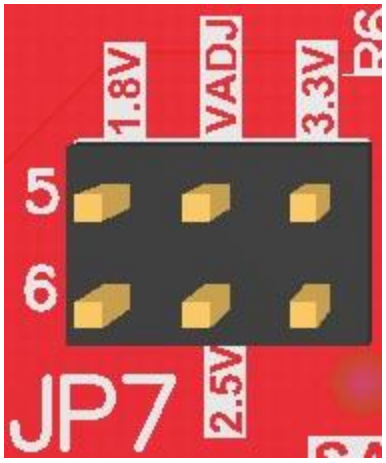

Figure 14 – FMC VADJ Select Jumper

Placing the jumper in the following positions selects the voltages listed:

JP7 Position	VADJ
1-3	3.3V
3-4	2.5V
4-5	1.8V

Table 27 – FMC Voltage Select Jumper

2.15.2 Power Switches

The Zynq Mini-ITX Development Kit as a standalone kit (AES-MINI-ITX-7Zxxx-G and AES-MINI-ITX-7Zxxx-BAS-G) will use SW12 as the main power switch to turn power on and off to the board.

AES-MINI-ITX-7Zxxx-SYS-G kits can use either the main power switch SW12 or the push-button chassis switch located on the front of the chassis. The chassis switch is connected to the main board at J14. Pressing the chassis switch once will toggle power to the main board. The main power switch SW12 can still be used to control power to the main board while in the chassis, but is the chassis switch is intended to exclusively control power to the main board SW12 should remain in the OFF position.

Eight green LEDs on the main board indicate a positive voltage on each of the board's voltage rails. The power LEDs are located just above the power module and are labeled to indicate which voltage rail is turned on. D18-D25 are the board designators for the power LEDs. All of these LEDs should be illuminated when power is turned on to the main board. If any of the LEDs are not illuminated when power is turned on there is a power issue and should be investigated. Secure connection of the power module to the main board should be checked.

2.16 Thermal Management

An active heat sink is used to dissipate heat from the Zynq-7000 AP SoC. A Cool Innovations heat sink (PN: **3-121202UBFA**) and a Sunon 12V fan (PN: **MC30101V1-000U-A99**) are assembled together and shipped with the the Zynq Mini-ITX Development Kit. The active heat sink is powered by connecting the three position connector (TE PN: 173977-3) to the mating connector on the Zynq Mini-ITX Development Kit at J16.

For aggressive applications that utilize large amounts of Zynq-7000 AP SOC PL resources it is recommended that an accurate worst-case power analysis be performed to avoid the pitfalls of overdesigning or under designing your product's power or cooling system, using the Xilinx Power Estimator (XPE).

For chassis applications where the Zynq Mini-ITX Development Kit is installed into an ATX chassis, a 12V chassis fan connector is provided on the main board at J17. This 3-pin keyed connector is .100" pitch and has the 12V conductor pin as pin 2. The chassis fan supplied with the AES-MINI-ITX-7Z045-SYS-G and AES-MINI-ITX-7Z100-SYS-G systems mate correctly to J17.

3 Pre-programmed Memory

This section describes the factory programmed applications that reside on the Zynq Mini-ITX Development Kit upon shipment. Other test and reference designs are posted on The Zynq Mini-ITX Development Kit Zedboard.org site: www.zedboard.org/products/mini-itx

Both the QSPI and the included microSD card included with the Zynq Mini-ITX Development Kit are pre-programed with applications that allow the user to quickly power on the board and utilize some of the board peripherals.

3.1 QSPI – Ethernet Echo Server Demo

The QSPI devices on the Zynq Mini-ITX Development Kit are programmed with Ethernet echo server design. This application configures a MAC internal to the Zynq-7000 AP SoC and allows communication over the Ethernet port.

SW7 should be set to **SW7[1:5] = x0010.** To boot from the QSPI and load the Ethernet design into DDR3 memory.

To exercise the Ethernet port the user must set up a test PC or laptop with an Ethernet patch cable connected between the Zynq Mini-ITX Development Kit and the PC.

Perform the following to run a quick ping test between the Zynq Mini-ITX Development Kit and the PC:

- Configure the IP settings of the PC network adapter to the following:
  - IP Address: 192.168.1.1
  - Subnet Mask: 255.255.255.0
- Turn on power to the Zynq Mini-ITX Development Kit with SW7[1:5]=x0010.
- Wait for the blue DONE LED and for the network adapter to finish negotiating a connection.
- From a command prompt type "ping 192.168.1.10".
- The ping command will respond with successful replies.

Refer to the Getting Started Guide at the following link to get more details on the Ethernet Echo Server demo:

http://www.zedboard.org/sites/default/files/documentations/zynq_mini_itx_getting_started_guide_v1_2.pdf

3.2 MicroSD Card – Embedded Linux LED Demo

The supplied microSD card shipped with the Zynq Mini-ITX Development Kit is pre-programmed with a Linux image that will boot upon power-up when the configuration switch SW7 is set to the proper mode. To configure from the microSD card and boot Linux set **SW7[1:5] = x011x**.

Prior to power-on the user will need to attach a USB cable between the Zynq Mini-ITX Development Kit USB UART connector J7 and a PC or laptop. Open a terminal session and set it for the correct COM port (shown in the device manager as CP210x) with the following settings: 115200-8-N-1.

Once the terminal shell is open turn on power to the system and the user will see Linux booting on the terminal screen. After boot is complete a Linux command line will be present and commands can be entered.

NOTE: The PC or laptop will require the Silicon Labs CP210x driver be installed in order to use the USB UART interface. These drivers can be found at the Silicon Labs website.

Refer to the Getting Started Guide at the following link to get more details on the Embedded Linux LED demo:

http://www.zedboard.org/sites/default/files/documentations/zynq_mini_itx_getting_started_guide_v1_2.pdf

4 Appendix A – Mechanical/Assembly Drawing and Jumper Definitions

This section provides a description of the jumper settings for the Zynq Mini-ITX Development Kit. The board is ready to use out of the box with the default jumper settings. The following assembly drawing of the component side of the board shows the location of the jumpers followed by a brief description of the jumper functions.

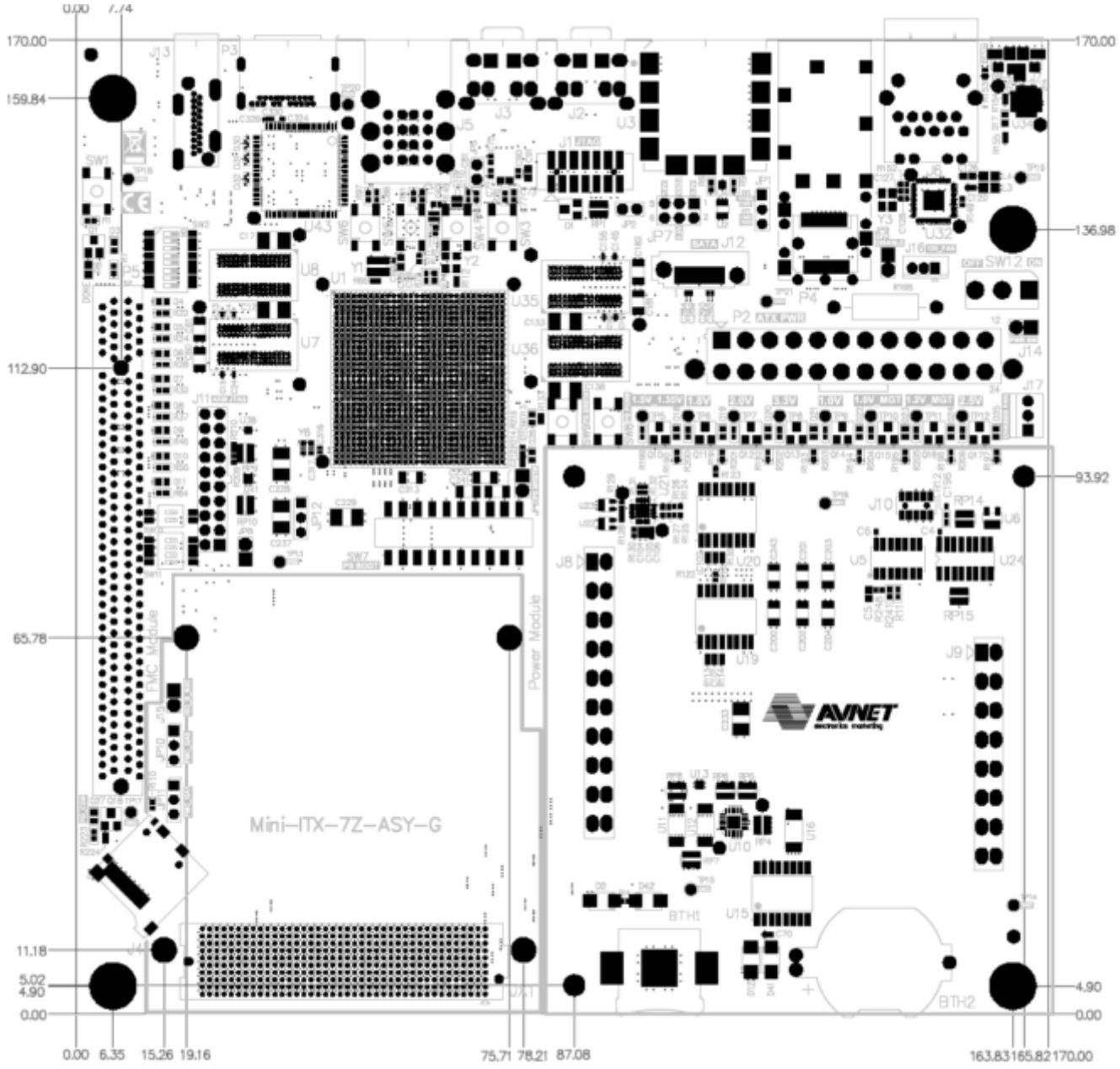

Figure 15 – Assembly and Mechanical Drawing

JP1 – JTAG Chain: Enables the JTAG chain for either the Zynq-7000 AP SoC or the FMC HPC expansion connector.

- JP1: 1-2 = Zynq-7000 AP SoC (Default)
- JP1: 2-3 = FMC HPC

JP2 – JTAG Reset: Placing a jumper shunt on this jumper enable the Xilinx Parallel Cable 4 to reset the Zynq-7000 AP SoC by asserting this signal LOW. Default = Hang

JP6 – Master Reset: Placing a jumper shunt on this jumper will put the Zynq-7000 AP SoC into reset by driving the PS_POR# and PS_SRST# signals low. Default = Hang.

JP7 – FMC VADJ Select: The position of this 3-way jumper determines the voltage applied to the FMC HPC VADJ pins.

- JP7: 1-3 = VADJ = 3.3V
- JP7: 3-4 = VADJ = 2.5V (Default)
- JP7: 3-5 = VADJ = 1.8V

JP9 – SFP Disable: Placing a jumper shunt on this jumper disables the SFP Interface. Default = Hang.

JP10 – FMC GA0: The position of this three position jumper determines the value of the LSB of the FMC HPC connector.

- JP10: 1-2 = GA0 = 0 (Default)
- JP10: 1-2 = GA0 = 1

JP11 – FMC GA1: The position of this three position jumper determines the value of the MSB of the FMC HPC connector.

- JP11: 1-2 = GA1 = 0 (Default)
- JP11: 1-2 = GA1 = 1

JP8 – PJTAG VREF: Placing a jumper shunt on this jumper places a reference voltage of VADJ (determined by position of JP7) on the PJTAG Header Pin 2. Default = Hang.

JP12 – I2C Enable: The position of this three position jumper determines which I2C channel (PS or PL) is enabled.

- JP12: 1-2 = Enable PS I2C.
- JP12: 2-3 = Enable PL I2C.