PicoZed™ SDR Software-Defined Radio Part 1: Board Level Design

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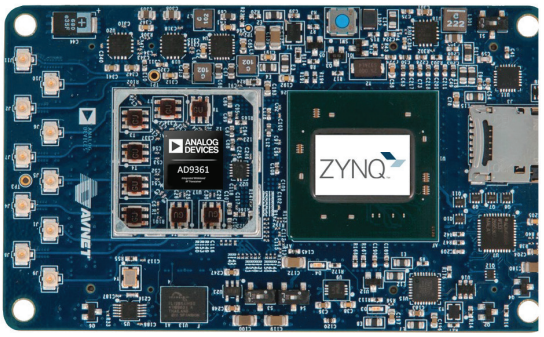
SUMMARY

In the first of this 3-part series, we present the design methodology of Avnet's PicoZed™ SDR family of software-defined radio system-on-modules (SOMs).[i] We highlight best practices to address specific board-level design challenges within tight space constraints, including interconnect between the processor, common embedded system peripherals (such as DDR3L memory, Ethernet, USB) and the RF transceiver. In addition we describe techniques for RF interference mitigation and review the power supply design involving sequencing and fault isolation utilizing a sequencer. Finally, we cover the HDL-based custom IP within the Xilinx® Zynq®-700 All Programmable SoC which controls the system.

Part 2 of this series will explore software design for dual-core ARM® Cortex™-A9 processors within the Zynq-7000 SoC, under bare-metal and Linux environments, peripheral software drivers, and integration with Xilinx SDK.

Part 3 will address practical system-level implementation of end-to-end wireless communications using MATLAB and Simulink for PHY layer and MAC-layer framing of packet-based wireless links.



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OVERVIEW OF PICOZED SDR SOFTWARE-DEFINED RADIO

In the past, IC manufacturers have focused on the features of application-specific products (ASSPs), often leaving the task of system integration to the customer. Today, through a new customer solutions enablement strategy in collaboration with Analog Devices, Avnet offers a portfolio of fully-verified subsystems for software-defined radio. PicoZed SDR is a system-on-module (SOM) for wideband wireless communications supported with open-source HDL and software drivers. In addition, at the system level, it is enhanced to allow modelling, research, and development through Matlab and Simulink tools from MathWorks.

A system-on-module (SOM) provides a pre-engineered subsystem in a production-ready form factor with which companies can build fully customized solutions. Combining an embedded processor, its peripherals and custom interfaces, a SOM saves the effort of a bottom-up design and development of core functionality. When complemented with a custom baseboard, one can quickly release a SOM-based product that is comparable to a fully custom-engineered solution at much lower development costs, with reduced technical risks and faster time to market.

Avnet's PicoZed SDR family of software-defined radio SOMs are small form-factor system-on-modules with various combinations of AD936x integrated RF Agile Transceivers™ from Analog Devices, Inc. and Xilinx Zynq-7000 All Programmable SoCs. The modules also host 1GB of DDR3 memory, USB, Ethernet, UART, SD and 256MB flash memory.

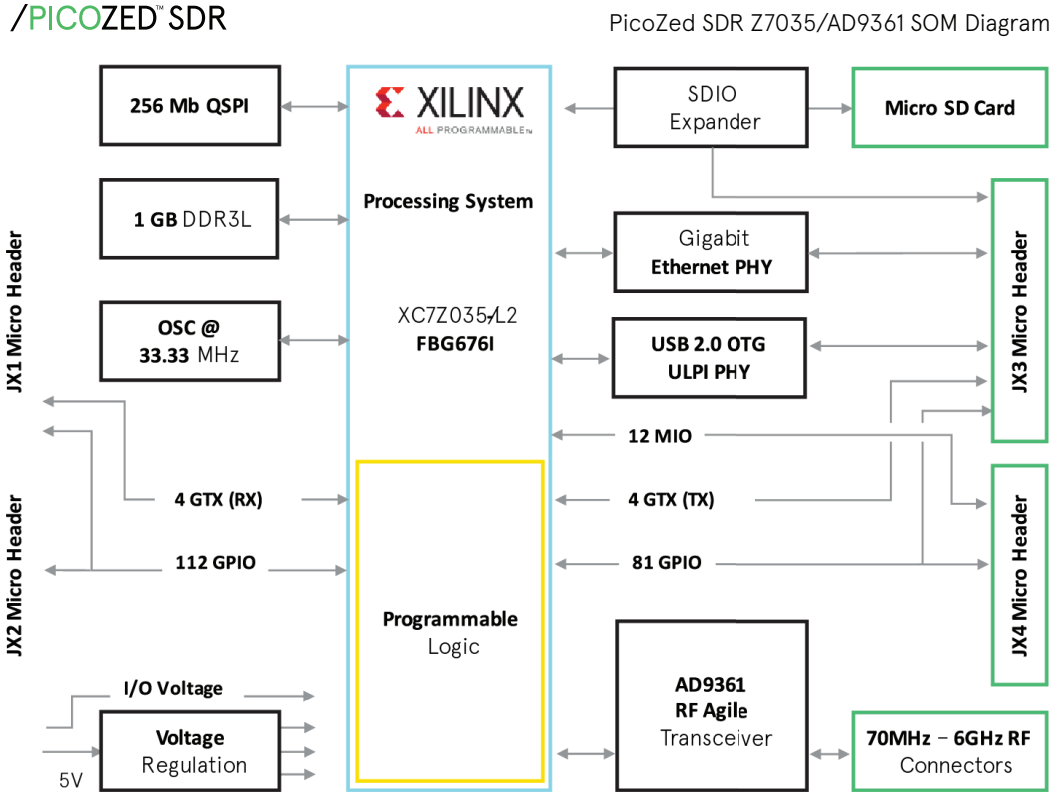

FIGURE 1: PicoZed SDR 2x2 SOM Simplified System Diagram

To accelerate development with PicoZed SDR SOMs, various carrier cards provide a mix of connectivity options including additional Ethernet, SFP, HDMI and audio peripherals with expansion capabilities such as FMC, PMOD and camera connectors.

RF Personality cards specially designed for PicoZed SDR can boost the transmitter output using a power amplifier (PA) and increase the dynamic range of the receiver input with a low-noise amplifier (LNA) or other functionalities such as up/down conversion outside the range of the AD936x.[2]

COMBINING HIGH-SPEED DIGITAL, ANALOG & RF IN SMALL FORM-FACTOR DDR3L MEMORY

The overall performance of an embedded system is highly dependent on the interface to main memory, which must provide sufficient read/write bandwidth to keep up with the flow of data within the system. PicoZed SDR includes two Micron DDR3L low power dynamic memory components creating a 256M x 32-bit interface, totaling 1 GB of random access memory at speeds of up to 1,066 Mb/s. The DDR3L memory is connected to the hard memory controller in the processing system (PS) of the Zynq AP SoC, which includes its own set of dedicated I/Os.

Read data capture from DDR3 memory at high speed requires maintaining the data capture clock within a precise data-valid window, with tight timing margins over changes in voltage and temperature during system operation. A clocking architecture element within the Zynq Z-7035 SoC called the Phaser, when controlled by the calibration logic, provides real-time temperature compensation capability at high data rates.[3]

By design, the layout of PicoZed SDR keeps the DDR3 clock as the longest trace and all address lines within matched shorter distances, configured for fly-by routing topology, as recommended in Xilinx UG933.[4] Specifically, the clocks, address, and control signals are all routed in a daisy-chained fashion through each DDR3 memory component, and terminated at the end of each trace. Propagation delay mismatches inside the Zynq SoC were extracted from the Vivado tools and fed into the constraints manger in Cadence schematic capture. Constraints on the address lines between Zynq SoC pins and the first and second DDR3 components were set to within 20ps and 40 ps respectively. DDR3 layout topology is depicted in figure 2.

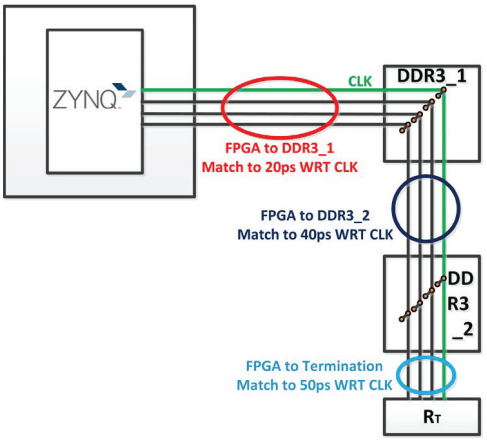

FIGURE 2: Zynq-7000 SoC and DDR3 Address Lines Trace Matching Block Diagram

While the recommended termination on the DDR3 address lines is 40Ω, it was found that termination resistors could be increased to 120Ω and still maintain sufficient signal quality in the data eye if the distance from the Zynq SOC to both DDR3 components is less than 2 inches. This minimizes power consumption and thermal issues within the restricted board space of PicoZed SDR SOM.

FORM FACTOR

As a pre-engineered subsystem, a SOM provides a set of core components in a compact form factor. PicoZed SDR combines the Zynq-7000 SoC, DDR3L memory, USB 2.0, Gigabit Ethernet, RF transceiver and power circuitry in an area of 100mm by 62mm, of which 27mm x 27mm from the top and bottom of

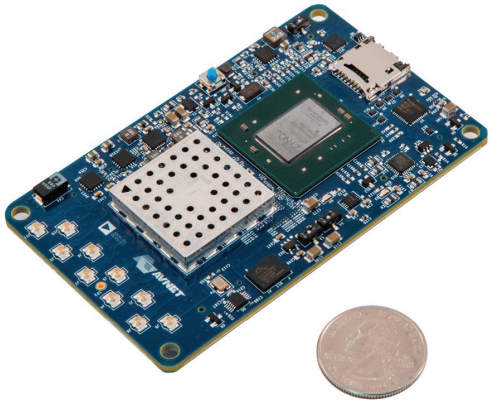

FIGURE 3: PicoZed SDR 2x2 SOM

the board is reserved for the Zynq-7000 package. This was achieved through careful component selection. The smallest 0201 packages of capacitor and resistor were used when possible, gradually increasing towards larger sizes to meet power rating requirements. SOIC and through-hole IC packages were avoided in favour of SC70, SOT23, BGA and LFSCP. Routing over 400 pins of the Zynq-7000 device and more than 12 power rails led to a 20 layer PCB, with 4 layers dedicated to power, 6 to ground and the rest as signal layers. Blind and buried vias were necessary to complete the routing.

REDUCING INTERFERENCE FOR OPTIMAL RF PERFORMANCE

Optimal RF performance in a full-duplex, multi-channel system requires careful attention to inter-channel isolation by minimizing crosstalk. AD9361 has two transmit and two receive channels of complex I&Q, each of which has two or three multiplexed input or output signal paths. PicoZed SDR 2x2 routes two TX outputs and two RX inputs from each of the two channels, requiring a total of 8 RF transformers with isolated traces in a very tight area. Adjacent transformers are rotated in 90 degree formation with respect to each other to minimize magnetic field crosstalk as shown in

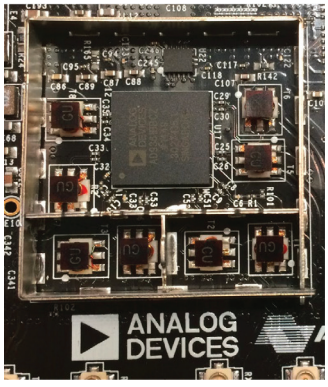

FIGURE 4: Custom Shield Chambers and Transformers orientations

figure 4. In addition, ground stitching was done from both sides for each RF trace all the way to the antenna U.FL connector.

Close proximity of high-speed digital signals from the Zynq-7000 SoC was a potential source of near-field interference for the analog signal paths within the restricted area of PicoZed SDR SOM. Given that a 1-ns pulse edge has an upper bandwidth of approximately 350 MHz, the near-field limit is approximately 5 inches, well within the dimensions of PicoZed SDR SOM.[5] A custom shield mitigates interference by isolating the four analog signal paths to/from AD9361.

POWER SUPPLY SEQUENCING AND FAULT ISOLATION

Robust power supply sequencing is essential to protect key components including the Zynq-7000 SoC, which has specific power-on requirements.[ii] PicoZed SDR 2X2 uses the ADM1166 Super Sequencer® to implement a single-chip supervisory/ sequencing system to ensure all power rails are energized in the required order and to protect the board from overvoltage up to 20V. If the SOM detects any of its voltage rails are outside of normal regulation, it will prevent any damage to the module by disabling all regulators in reverse order until the entire system is powered down.

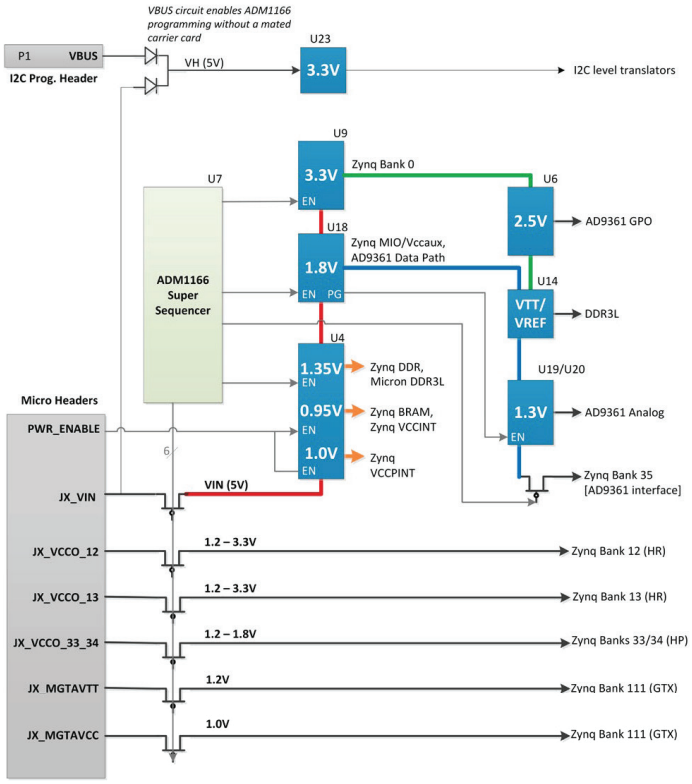

FIGURE 5: PicoZed SDR 2x2 Voltage Regulation

The ADM1166 integrates a 12-bit ADC and six 8-bit voltage output DACs which are used to implement a closed-loop margining system that enables supply adjustment by altering the feedback node of the buck converter using the DAC outputs. The margining loop can be used dynamically to accurately control the supply voltages.

HDL-BASED IP LIBRARIES FOR PICOZED SDR

Avnet offers several PicoZed SDR-compatible carrier cards for rapid prototyping of wireless links, and as starting points for custom-designed carrier hardware. All carrier + SOM combinations are supported by HDL code libraries, Xilinx Vivado projects and software from Analog Devices.[iii] Here we highlight key design features and benefits of an IP-centric design flow for custom software-defined radio systems.

The Zynq-7000 SoC device within each PicoZed SDR SOM includes a processing system (PS) with dual-core ARM Cortex-A9 processors and a fixed set of hard peripherals including DDR memory controller, Ethernet, USB, UART, etc. HDL libraries add custom IP components in Zynq programmable logic (PL) to manage dataflow between the AD936x and the various carrier card devices such as HDMI, audio, etc. HDL-based IP is consistent across the various carriers, except that in actual hardware some of the peripheral and/or devices are disabled and/or not available.

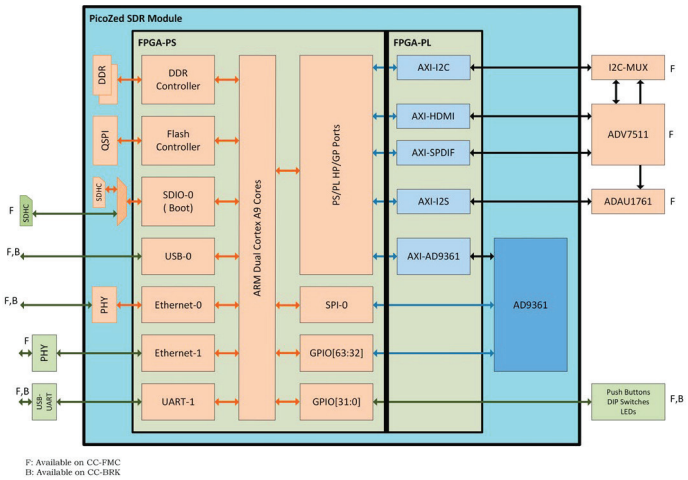

FIGURE 6: HDL Block Diagram

We now turn our attention to the AD9361 interface within Zynq programmable logic, referred to as the AXI-AD9361 core, which handles the data path interface to the ARM Cortex-A9 processors. Using the LVDS/DDR (double data rate) mode of the AD9361 digital interface, up to four full-duplex data channels may be multiplexed to/from the AD9361 for PicoZed SDR 2x2, or two full-duplex data channels to/from the AD9364 for PicoZed SDR 1x1. The SPI programming interface to the internal registers of the AD936x is handled by the PS SPI-0 peripheral, allowing a single SPI core to program most, if not all, of the SPI-addressable peripherals within the system.

AD9361 CORE IO INTERFACE AND CLOCKING

The receive interface operates in LVDS/DDR mode of the AD9361, with 12-bit data samples sent to the Zynq device across two 6-bit lanes on differential pairs, plus a FRAME signal to delineate the four data channels.[iv] From Zynq input pins each data lane is routed through an LVDS IO buffer followed by an adjustable delay element, then clocked into the single-edge clock domain as 2-bits through input DDR registers (IDDR). The design explicitly instantiates Xilinx 7-Series architecture primitives, ensuring direct routing from Zynq device pins to synchronous elements within the I/O logic.[v]

All clock paths within the core are kept synchronous to the incoming clock from the AD9361; the receive clock is simply turned around as transmit clock. The clocking uses a global clock buffer (BUFG) with high fanout that can reach every flip-flop clock, clock enable, and set/reset with low skew across the various clock regions of the Zynq SoC PL. Any delay through the BUFG which might offset the precise timing alignment between incoming clock and data at the pins is easily compensated with the IDELAY element in the I/O logic to a fine resolution of 78 ps.[vi]

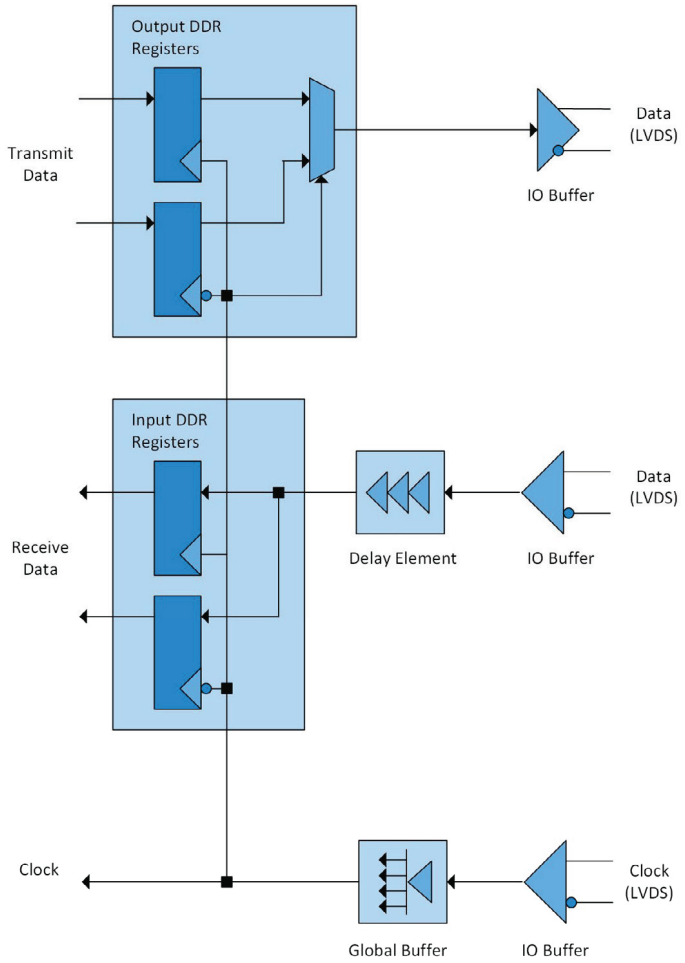

FIGURE 7: Interface Logic to AD9361 in Zynq PL

Although single-domain clocking was chosen for reasons of simplicity, the rest of the logic allows customization by the user to choose their own clocking scheme. This may involve the mixed mode clock managers (MMCM) and Phase-Locked Loops (PLL) to drive the downstream data paths, for example to accommodate multirate digital signal processing.

RECEIVE INTERFACE

The receive interface supports a PRBS monitor that may be enabled to check data integrity. It can be driven at reset time from a standard-compliant PRBS sequence generator within the transmit core in order to calibrate the receiver IDELAY elements and to set the optimum point of data sampling at the DDR registers.

The receive interface also supports DC offset and IQ correction (phase & gain) per channel. Any residual DC offset can be removed either by the hardware (using an IIR filter) or by software using a programmable register. The register may be set to the average DC offset observed initially without any correction with the desired settings for a short period of time.

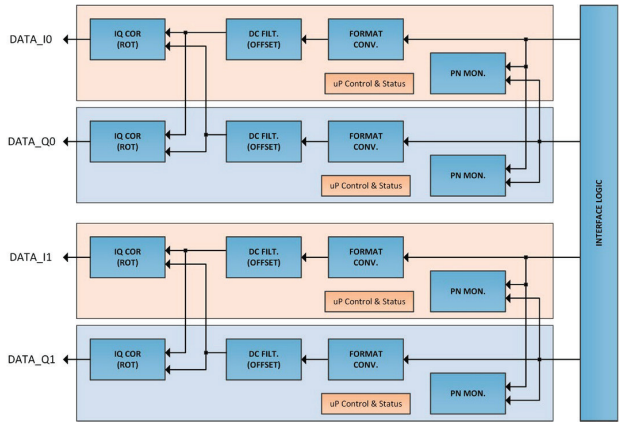

FIGURE 8: Receiver Interface

The IQ correction is implemented as a 2x2 matrix multiplier with software-programmable coefficients. The correction is implemented across each pair of IQ channels. It is NOT possible to correct the signals across the pairs. It is best to use the builtin IQ correction in the AD9361 across all the channels. The core may then be used to correct phase (rotation) or gain within each IQ pair. The core accepts either offset-binary or 2's complement data formats, which are then output as 16-bit data by either sign extension or setting the most significant nibble as 0x0.

By default the receive data is passed via DMA directly to the Zynq processing system, where it may be processed in software such as Analog Devices IIO Oscilloscopevii or streamed via Ethernet, PCI Express or USB to Matlab and Simulink at the PC.[6] In productionready SDR applications, further digital signal processing must be implemented in the programmable logic to sustain throughput and bandwidth requirements.

The transmit interface closely resembles the receive data path in reverse. Data destined for the DAC arrives on four channels at the device clock. The core assumes a simple FIFO-like interface at the user side. It indicates a data request on the channels via a read signal. The data may either be 2's complement or offset binary and aligned to the MSB of the 16-bit data signal.

The data is then passed to IQ correction logic on each of the pairs and finally to the interface logic towards LVDS outputs, with the FRAME signal marking the four channels.

The core also supports an optional data pattern generator for test purposes. This includes a DDS that generates two sinusoidal waveforms that are scaled and added together. It also includes a constant data pattern programmable by the software as well as a PRBS sequence generator.

CONCLUSION:

In the first of this 3-part series, we presented the design methodology for Avnet's PicoZed SDR family of software-defined radio system-on-modules (SOMs). We highlighted best practices to address specific board-level design challenges within tight space constraints, including interconnect between the processor, common embedded system peripherals and the RF transceiver. In addition we described techniques for RF interference mitigation and reviewed the power supply design. Finally, we covered the HDL-based custom IP for PicoZed SDR within the Xilinx Zynq-7000 SoC.

Subsequent articles within this series will explore software design and practical system-level implementation of end-to-end wireless communications using MATLAB and Simulink.

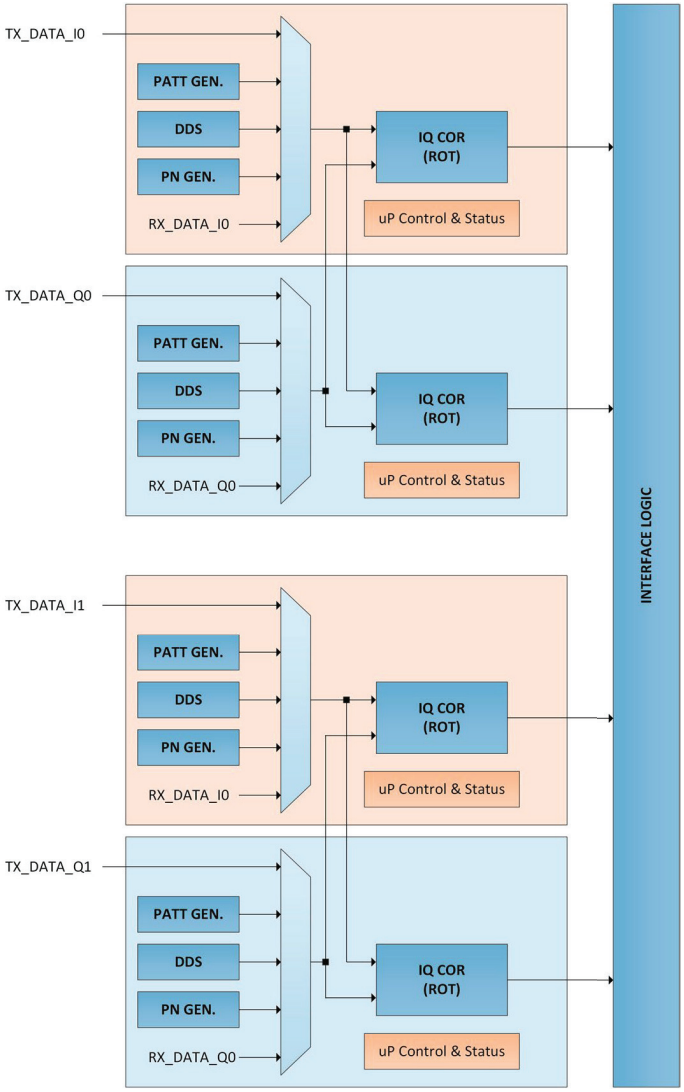

FIGURE 9: Transmitter Interface

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[vi] 7 Series FPGAs Clocking Resources http://www.xilinx.com/support/documentation/user_guides/ug472_7Series_Clocking.pdf

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