AVNET®

PCB BOARD NAME	PBA-US2CAR.PcbDoc
PCB Thickness	62.7mils
Document Number	UltraZed-EG PCIe Carrier Card
Date	1/20/2017
Time	1:55:50 PM
Board Rev	1
Project Engineer	PL
PCB Designer	N/A

IMPEDANCE REQUIREMENTS

PLEASE REFER TO PROJECT IMPEDANCE STACKUP FOR LINE WIDTH DIMENSIONS!
SEE T14040_Impedance_stackup.pdf

LAYER USAGE

Top Mechanical | Keep-Out Layer | 3D Objects | Courtyard | GM15 | Bottom Mechanical
Top Overlay | Bottom Overlay
Component Side | Inner Layer 1 | Breakaway
Inner Layer 2 | Solder Side | Mech_PCIE
Multi-Layer | Dimensions GM3 | Board Outline | Fabrication Drawing | Mech_IF

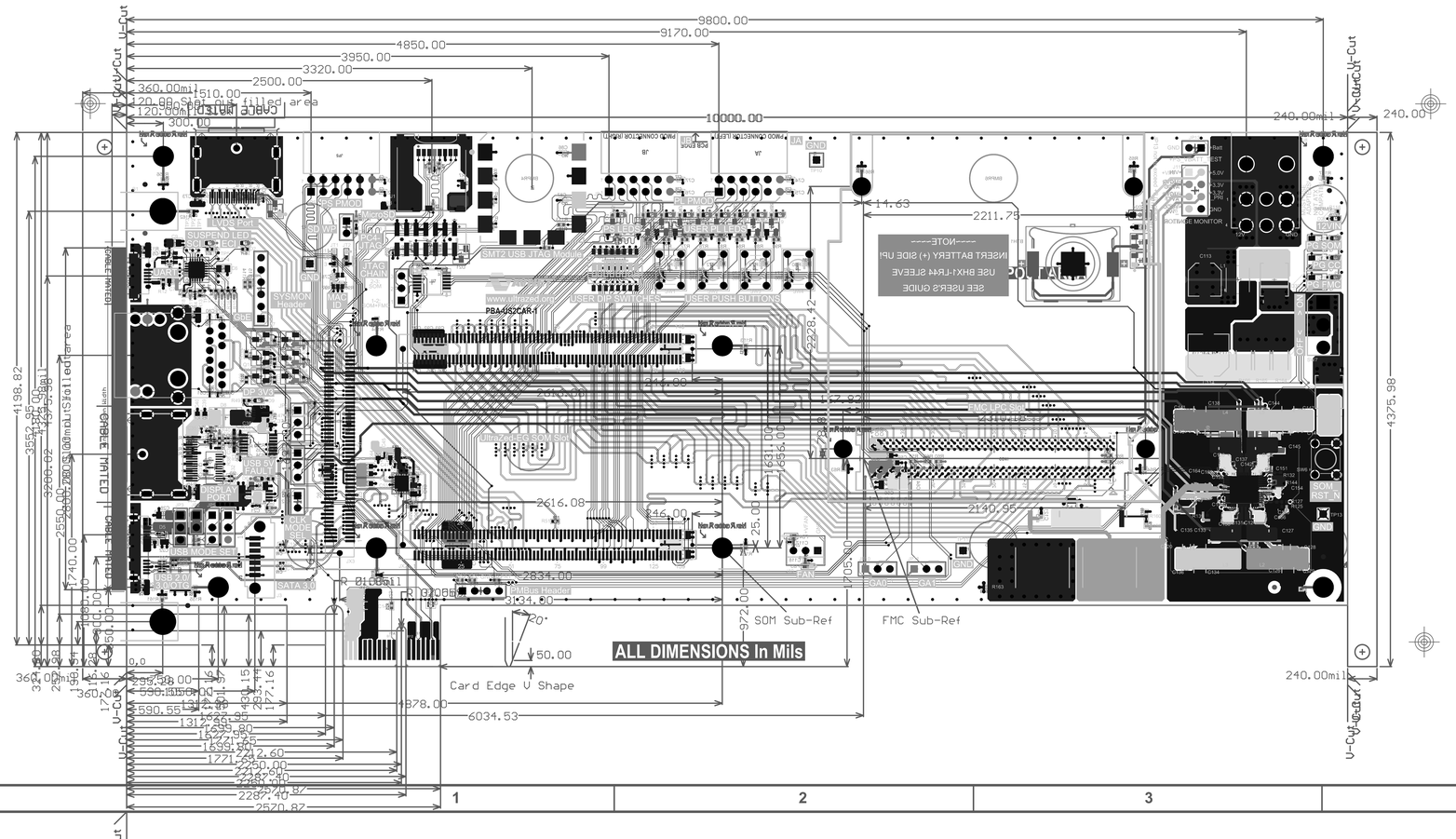
INTENTIONAL NETLIST SHORTS

1. All Signals NT*

BUILD INFO

PAD COUNT — 2003
HOLE COUNT — 1764
VIA COUNT — 1590
COMPONENTS — 515
NET COUNT — 455

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.40mil		
4	Dielectric 1	FR-4	2.80mil	4.2	
5	Ground Plane (GND1)	Copper	1.40mil		
6	Dielectric 2	FR-4	2.80mil	4.2	
7	Inner Layer 1	Copper	1.40mil		
8	Dielectric 3	FR-4	2.80mil	4.2	
9	Internal Plane (PWR1)	Copper	1.40mil		
10	Dielectric 6		31.50mil	4.2	
11	Internal Plane (PWR2)	Copper	1.40mil		
12	Dielectric 7		2.80mil	4.2	
13	Inner Layer 2	Copper	1.40mil		
14	Dielectric 4	FR-4	2.80mil	4.2	
15	Ground Plane (GND2)	Copper	1.40mil		
16	Dielectric 5	FR-4	2.80mil	4.2	
17	Solder Side	Copper	1.40mil		
18	Bottom Solder	Solder Resist	0.40mil	3.5	
19	Bottom Overlay				



DESIGN INFORMATION

FILE NAME: PBA-US2CAR.PcbDoc FILE TYPE: GERBER SET
SURFACE MOUNT: [ ] 1 SIDE [X] 2 SIDES Number of Layers : 8 ARTWORK: [X] CAD
CIRCUIT TYPE: [ ] SS [X] DS [X] PTH MULTILAYER
LAYER CONSTRUCTION PER: LAMINATION SEQUENCE [X] AS SHOWN

MATERIAL PER IPC-4101A/24/26/29/99
COPPER CLAD, HIGH TEMPERATURE FR4 CLASS EPOXY GLASS RATED UL94V-0
MUST SURVIVE A LEAD-FREE ASSEMBLY MAX REFLOW OF 260 DEG C (6 PASSES)
Td RATING: > 340 DEG C , Z AXIS CTE < 3.5% , Tg > 170 DEG C (MIN)

THICKNESS: [X] +/-10% [ ] OTHER _____
TOLERANCE: [X] IN A/W ANSI IPC-6012 TYPE 2 CLASS 2 [ ] OTHER +/- _____
BOW & TWIST: [X] IN A/W ANSI IPC-6012 TYPE 2 CLASS 2 [ ] AS SHOWN

COPPER THICKNESS (FINISHED)

OUTER:	[ ] 18um (1/2oz)	[X] 35um (1oz)	[ ] 70um (2oz)
INNER SIGNAL:	[ ] 18um (1/2oz)	[X] 35um (1oz)	[ ] 70um (2oz)
INNER PWR:	[ ] 18um (1/2oz)	[X] 35um (1oz)	[ ] 70um (2oz)

VIAS: [X] THRU [ ] BLIND [ ] BURIED

STRUCTURE [X] AS SHOWN IN LAYER TABLE [X] FINISHED BOARD THICKNESS = 0.063 +/- 0.007

DRILLING VIEWED FROM: [X] COMPONENT SIDE [ ] SOLDER SIDE
REFERENCE: [X] AS SHOWN [ ] PATTERN MASTER LIST [X] NC_ DRILL FILES
ALL HOLE SIZES ARE AFTER PLATING

NPTH [ ] TENTED [ ] PADS REMOVED [ ] REMOVE PADS
[ ] 2nd DRILL [ ] BOTH [X] AS SHOWN [ ] NONE

PTH MINIMUM COPPER THICKNESS: [X] 20um [ ] OTHER _____

LEGEND / SCREEN PRINT COLOUR (RoHS COMPLIANT INK): [X] WHITE [ ] YELLOW
CLIP SILK SCREEN ON PADS, PLATED THROUGH HOLES, AND NON-TENTED VIAS

SOLDER MASK [X] LPI (RoHS Compliant) [X] SMOBC PER IPC-SM-840C, CLASS T
COLOR: [ ] GREEN [ ] BLUE [X] RED [ ] BLACK [ ] VIAS TENTED ON TOP SIDE
[X] GLOSS [ ] MATTE **ALL TEST POINTS SHALL BE FREE OF SOLDERMASK**

BOARD FINISH: [X] 2-8 Micro Inches IMMERSION GOLD [ ] Pb Free HASL (HOT AIR SOLDER LEVEL)
[ ] IMMERSION SILVER

EDGE FINGERS: [X] HARD GOLD PLATE FINISH (150-250 MICRO INCHES NICKEL, MINIMUM OF 30 MICRO INCHES OF HARD GOLD)

PROFILING
[X] CUT AND TRIM ACCORDING TO LAYER MECHANICAL 7 (BOARD OUTLINE)
[ ] REFER PCB BLANK DWG No. _____
[ ] USE PROFILE/ ROUTE TAPE SUPPLIED (REFER PATTERN MASTER LIST)
[ ] SQUARE CUT [X] N.C. ROUTE [ ] V. SCORE

TESTING/QUALITY CONTROL
[X] ELECTRICAL TEST
[X] IMPEDANCE REPORT
[X] MICROSECTION [X] TDR TEST COUPON
MATERIALS AND WORKMANSHIP FOR ALL PRINTED WIRING BOARDS TO MEET OR EXCEED THE REQUIREMENTS OF: IPC-6011 AND IPC-6012 [X] CLASS [ ] 1 [X] 2 [ ] 3
[X] SOLDERABILITY-(CATEGORY 2 OF J-STD-003)

MANUFACTURER PRODUCT ID MARKINGS

DO NOT PLACE ANY FOIL ITEMS IN KEEPOUT AREA(S)
MANUFACTURER'S ACCREDITATION (i.e. ISO9001): [X] LEGEND [ ] FOIL
ID/LOGO: [X] LEGEND [ ] FOIL DATE CODE: [X] LEGEND [ ] FOIL TEST STAMP: [X] LEGEND [ ] FOIL
DATE CODE FORMAT-WWYY WHERE WW=WEEK AND YY=YEAR

VENDOR MODIFICATIONS

COPPER THEVING	-VENDOR MAY ADD COPPER THIEVING AS NEEDED TO IMPROVE MANUFACTURABILITY, THIEVING TO BE 0.030 ROUND PADS AT 0.050 SPACING. THIEVING WILL HAVE A MINIMUM OF 0.100 CLEARANCE FROM SPACING. THIEVING WILL HAVE A MINIMUM OF 0.100 CLEARANCE FROM EXISTING COPPER AND SHOULD NOT BE PLACED UNDER SURFACE MOUNT DEVICES.
CONTROLLED IMPEDANCE	-VENDOR MAY MODIFY DIELECTRIC THICKNESS BY 10% WITHOUT WRITTEN CONSENT. ANY GREATER THAN 10% REQUIRES WRITTEN CONSENT FROM AVNET ENGINEERING
NON-FUNCTIONAL PADS	-VENDOR SHALL REMOVE NON-FUNCTIONAL PADS
TEAR DROPS	-VENDOR MAY USE TEAR DROPS TO IMPROVE ANNULAR RINGS AS LONG AS DRC RULES ARE FOLLOWED
TIE-BARS	-TIE BARS ON THERMAL PADS SHOULD BE 15 MILS MINIMUM WIDTH

ADDITIONAL REQUIREMENTS

ROHS CERTIFICATION	-PCBAs MUST BE RoHS COMPLIANT (VENDOR SHALL PROVIDE CERTIFICATION).
CLEANING	-ALL CLEANING PROCESSES MUST BE LEAD FREE AND FOLLOW RoHS PROCEDURES.
SOLDERING	-ALL SOLDERING PROCESSES MUST BE LEAD FREE AND FOLLOW RoHS PROCEDURES.
SERIALIZE	-PCBAs MUST BE SERIALIZED.
OVERALL QUALITY	-FINISHED BOARDS SHALL NOT HAVE NICKS, SCRATCHES, VOIDS, EXPOSED COPPER, POOR PLATING, MISDRILLED HOLES, AND MUST BE FREE OF ANY RESIDUES.