ISM Networking FMC User Guide

AES-FMC-ISMNET2-G

V1.0

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Contents

1 Introduction

This manual describes the functionality and contents of the **AES-FMC-ISMNET2-G** module. This document includes descriptions of the hardware features and instructions for operating the board.

FMC-ISMNET2 is the 2nd evolution of the ISM Networking FMC Module. It is pin compatible with designs that use the previous version (AES-FMC-ISMNET-G). Two new jumpers, as detailed below, select between FMC-ISMNET1 and FMC-ISMNET2 mode of operation.

1.1 Description

The FMC-ISMNET2 enables a variety of digital communication interfaces common to industrial applications, including Industrial Ethernet. The module is designed to operate with any Avnet or Xilinx base board that is FMC enabled. The module uses an FMC Low Pin Count (LPC) connector to interface to the carrier board.

1.2 Features

Communication

- Dual IEEE 1588 Compatible 10/100 Ethernet Interfaces.
- Support for Industrial Ethernet protocols include EtherCAT®, EtherNet/IP, Modbus TCP, Powerlink, and Profinet®
- Dual CAN Interfaces
- Legacy RS-232 and RS-485 interfaces

Memory

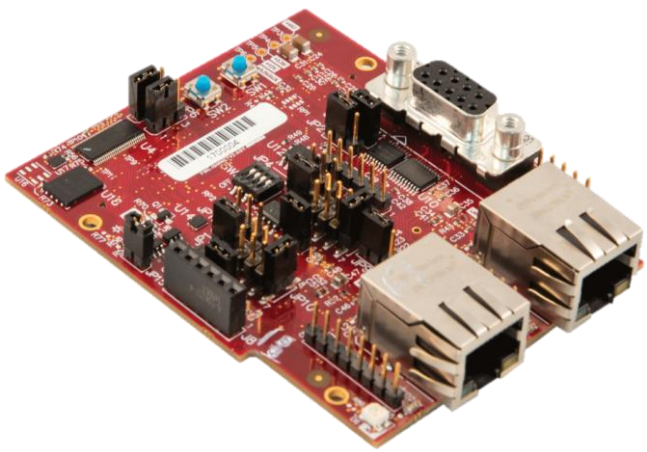
- EEPROM #1: used as module Identification for FMC compliance
- EEPROM #2: used for EtherCAT configuration storage
- SHA-1 secure EEPROM
- 256Mb SPI Flash

Board I/O Connectors

- FMC LPC Connector
- (2) 8 pin GPIO Headers (one per PHY)
- 9 pin female DB9 for RS-232 communications
- RJ-45 connectors for Ethernet communications

Miscellaneous I/O

- 4 Position user selectable DIP switch
- 6 pin Digilent header
- 6 pin PHY JTAG header
- 8 user LEDs



2 Functional Description

2.1 Overview

The diagram below summarizes the features and interfaces of the FMC-ISMNET2 module. Notice the multiplexer that selects between FMC-ISMNET1 pin compatible mode and new FMC-ISMNET2 features. See section 2.2 for details on configuring these modes of operation.

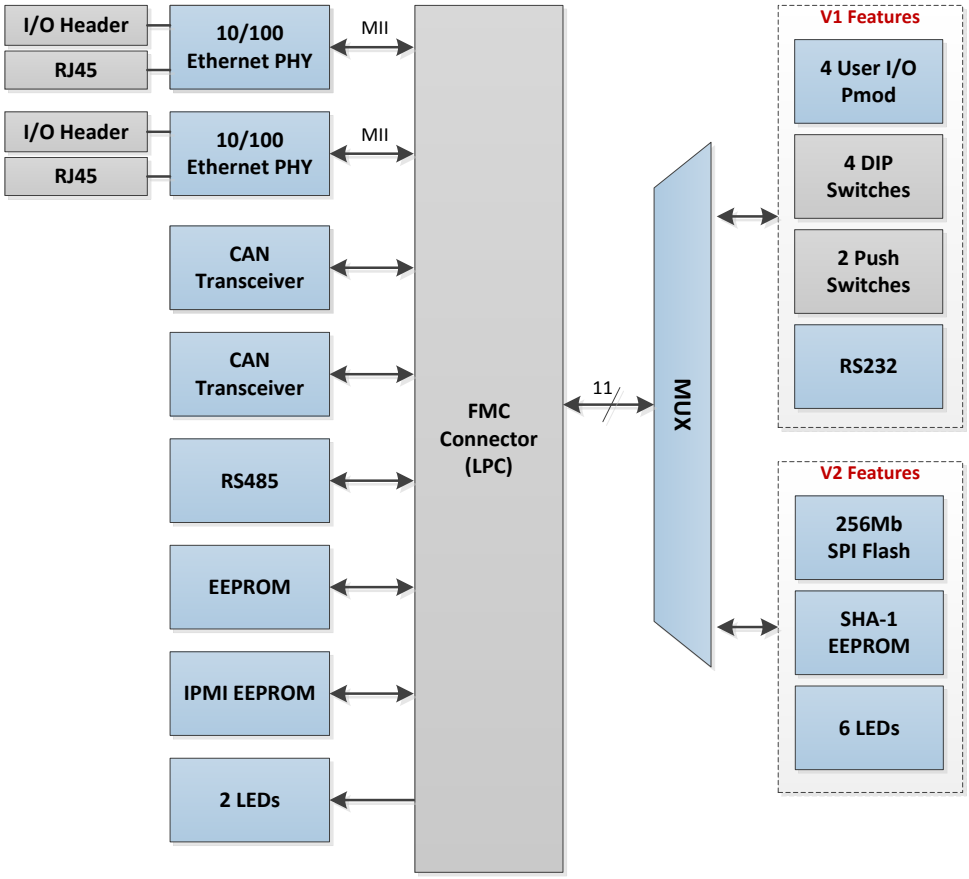
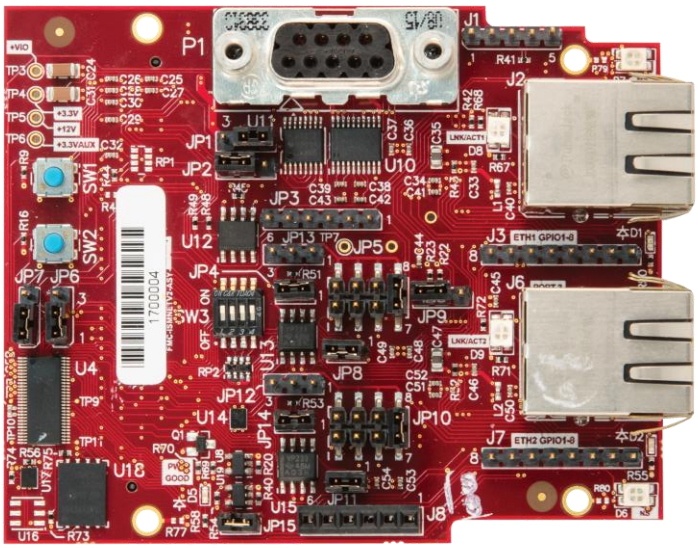


Figure 1 – Simplified Module Block Diagram



2.2 Mode Configuration

FMC-ISMNET2 is the 2nd evolution of the ISM Networking FMC Module. It is pin compatible with designs that use the previous version (AES-FMC-ISMNET-G). Two new jumpers, as detailed below, select between FMC-ISMNET1 and FMC-ISMNET2 mode of operation.

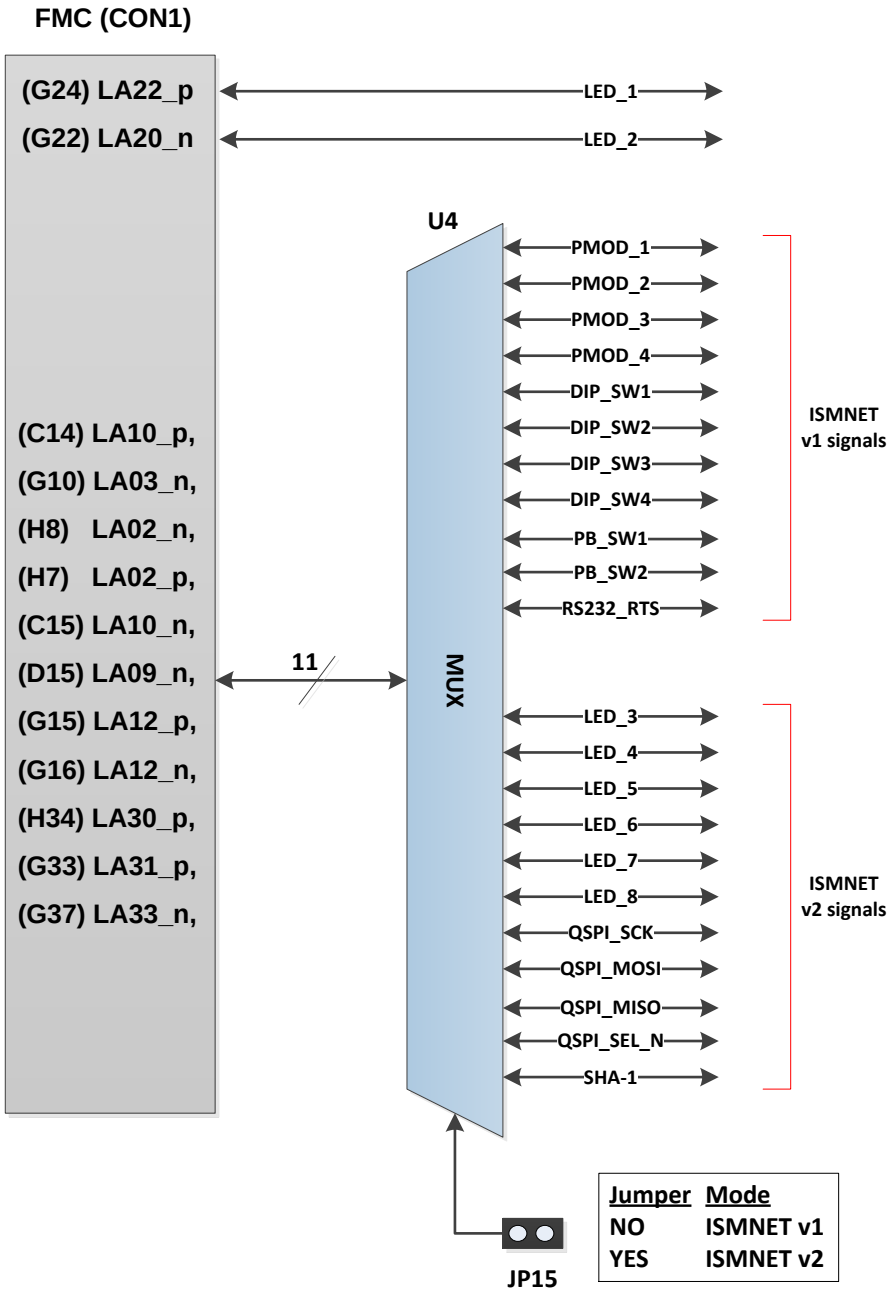


Figure 2 – Mode Selection Multiplexor

2.3 I/O Voltage Selection

The FMC-ISMNET2 module supports I/O voltages of 2.5V or 3.3V. The carrier card provides the Vio voltage on the FMC pins labelled VADJ. The module provides all required voltage translation between the carrier and its on-board devices.

Important! *This FMC module does not support 1.8V I/O signalling.*

2.4 Ethernet

The ISM Networking FMC module provides dual IEEE 1588 compatible 10/100 Ethernet interfaces by using 2 separate Texas Instruments DP83640TVV PHY devices. Figure 3 shows the 10/100 Ethernet Interface block diagram. This represents one of two identical PHY interfaces on the board.

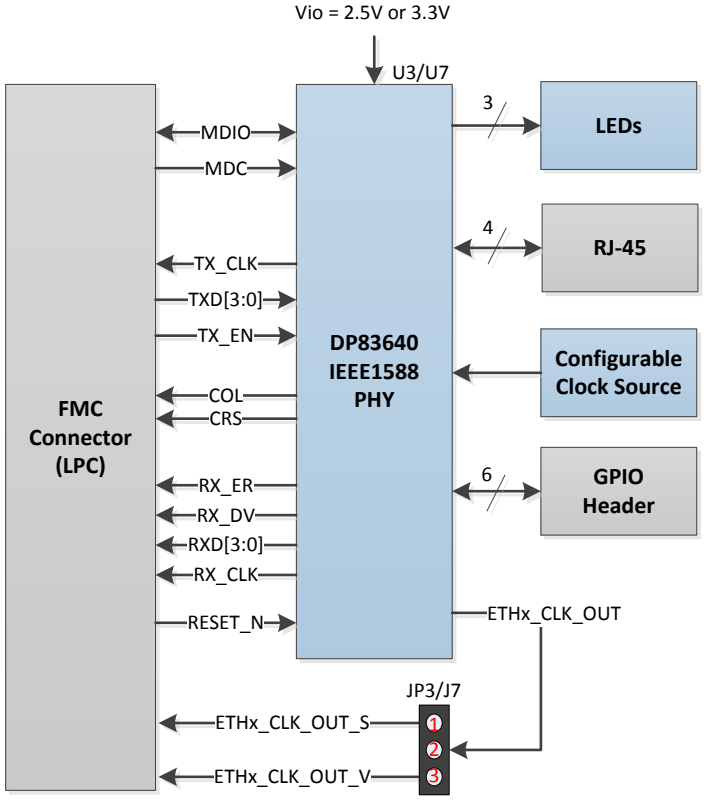


Figure 3 - Ethernet PHY Interface

2.4.1 User I/O

Each DP83640 has a 1x8 header (J3 / J7) connected to its GPIO port to provide user access to status indicators or other flags generated by the device. Pin 1 of J3 and J7 is attached to the Vio voltage source and pin 8 on each header is attached to ground. Header J3 is connected to U3, and J7 is connected to U7.

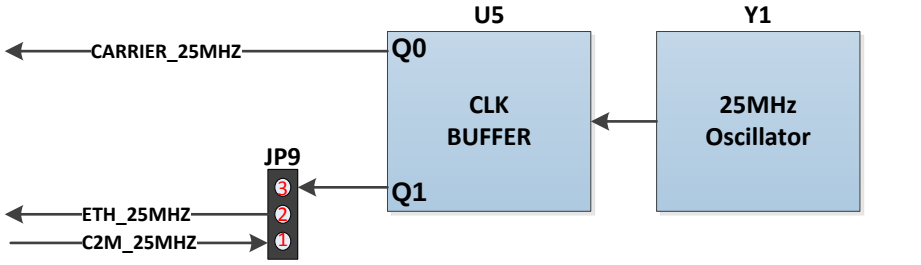
For status the PHY drives 2 LEDs on the RJ45 jack (ACTIVITY & LINK) and 1 LED on the board (LINK_SPEED).

2.4.2 Clock Configuration

The PHY CLK_OUT signal can be connected to 1 of 2 FMC pins. The choice is made with jumper JP3 for U3 and JP7 for U7 (see Figure 3). Your selection will depend upon the pin location of dedicated clock inputs of the FPGA/SoC device used on the carrier card.

The Ethernet PHYs may be clocked by the on-board 25MHz oscillator (Y1), or from a clock sourced from the carrier card FPGA/SoC through the FMC connector. For backwards

compatibility with version1 of this FMC module, configure for ISMNETv1 mode (JP9 2-3 shorted). In the diagram below, the abbreviation C2M stands for Carrier-to-Module to indicate the source.



Jumper	Mode	Description
2-3	ISMNET v1	FMC supplies Eth PHY ref. clock
1-2	ISMNET v2	Carrier supplies Eth PHY ref. clock

Figure 4 - Ethernet Reference Clock Configuration

2.5 CAN Transceivers

2.5.1 Overview

The FMC-ISMNET2 module includes two CAN transceivers. The block diagram is shown below.

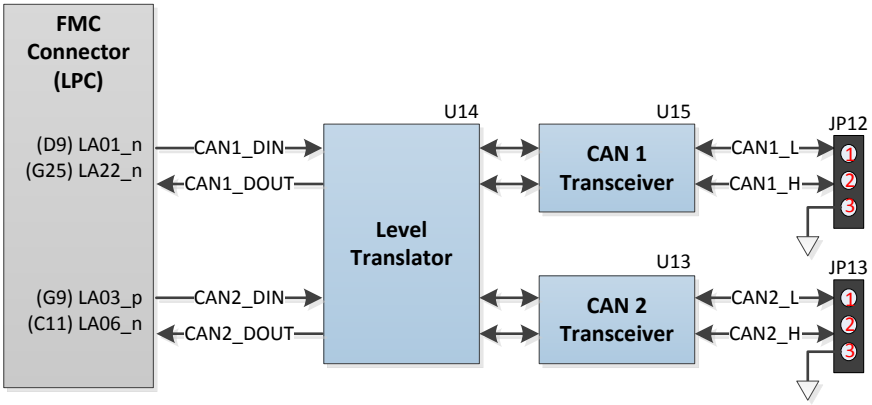


Figure 5 – CAN Transceiver Block Diagram

The Texas Instruments SN65HVD233 used in this application employs the controller area network (CAN) serial communication physical layer in accordance with the ISO 11898 standard. As a CAN transceiver, each provides transmit and receive capability between the differential CAN bus and a CAN controller, with signaling rates up to 1 Mbps.

2.5.2 Mode Configuration

Four modes of operation are supported – a high-speed mode, two intermediate modes, and a low-power standby mode. These modes are selected by shorting the appropriate pins on jumpers JP10 for CAN1 (U15), and JP5 for CAN2 (U13). See Table 1 for details on configuring these modes. The high-speed mode of operation allows the driver output transistors to switch on and off as fast as possible. The intermediate modes limit the driver slew rate.

JP5 and JP10 Pins	Mode of Operation
1:2	CAN Standby

3:4	CAN Slew Rate 15 V/uS
5:6	CAN Slew Rate 2 V/uS
7:8	CAN High Speed

Table 1- CAN Transceiver Jumper Settings

The diagnostic loopback or internal loopback function of the SN65HVD233 transceiver is enabled by shorting JP11 for CAN1 and JP8 for CAN2. This mode disables the driver output while keeping the bus pins biased to the recessive state. This mode also redirects the D data input (TX data) through logic to the received data pin, thus creating an internal loopback of the transmit to receive data path. This mode allows the host protocol controller to input and read back a bit sequence or CAN message to perform diagnostic routines without disturbing the CAN bus.

A 120-ohm termination resistor can be placed across the bus signals of the transceiver by installing a jumper across JP14 for CAN1 (U15) and JP4 for CAN2 (U13).

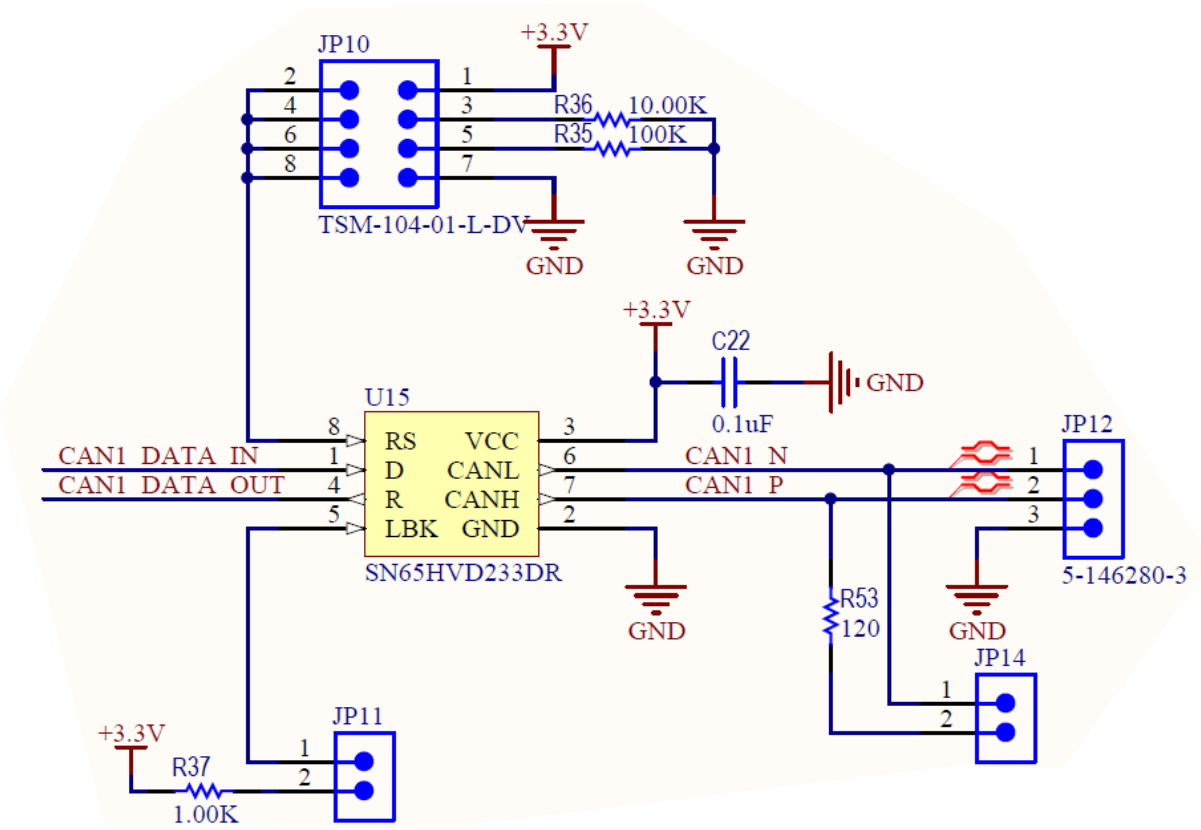


Figure 6 – CAN Transceiver Schematic Diagram

2.6 RS-485 Transceiver

RS-485 communication is achieved using the Maxim MAX13433EESD+ and operates in full duplex mode. Figure 7 shows a graphic of the data flow through the device. The input / output pins of this device are located at the 5 pin header J1.

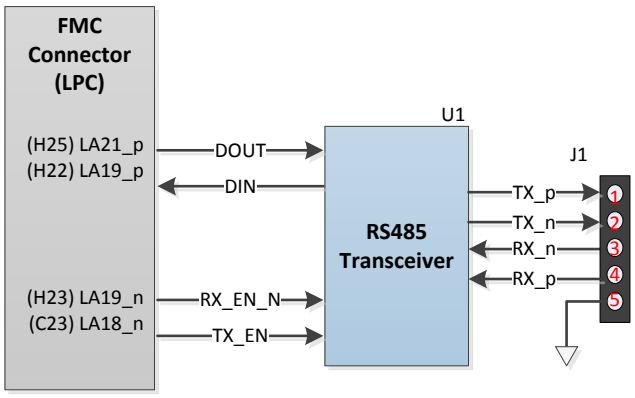


Figure 7 – RS-485 Diagram

2.7 RS232 Transceiver

The ISM Networking FMC Module provides a standard female DB9 RS232 compatible interface that can be configured through jumpers to be either DCE or DTE by setting jumper JP1 to the desired position. Table 2 shows the settings required for either DCE or DTE operation.

JP1 Pins	Mode of Operation
1-2	DCE
2-3	DTE

Table 2 – RS232 Operation Modes

The integrated circuit used for serial communications is the Maxim MAX13234EEUP+ which is a +3V to +5.5V powered EIA/TIA-232 and V.28/V.24 communications interface with high data-rate capabilities (up to 3Mbps), a flexible logic voltage interface, with enhanced electrostatic discharge (ESD) protection.

____ shown below shows the pin connections of the DB9 connector P1.

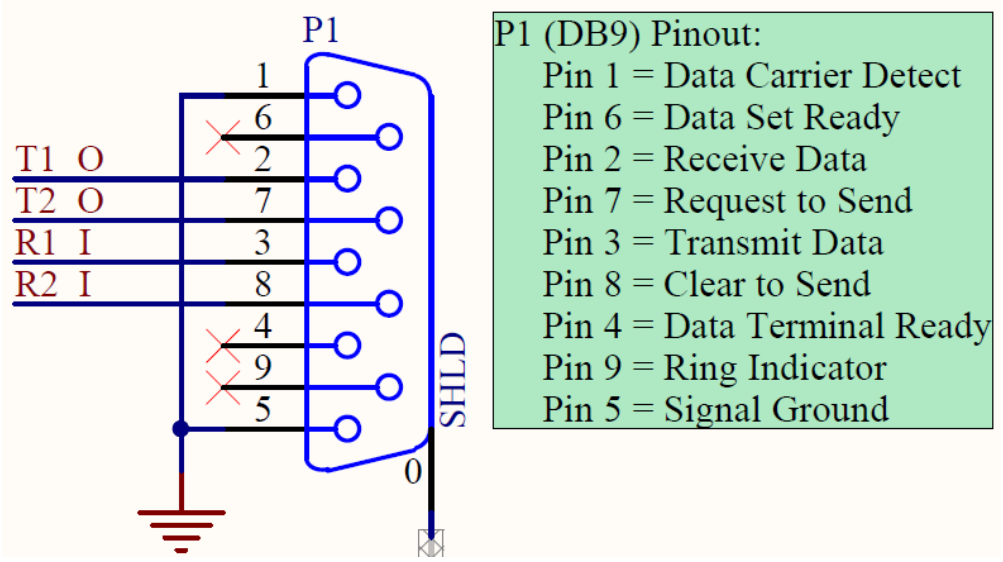


Figure 8 – RS232 Connector Pin Diagram

2.8 Memory Devices

The FMC-ISMENT2 module includes four unique memory devices, each for a different purpose as described the follow sections.

2.8.1 IPMI EEPROM

The Intelligent Platform Management Interface (IPMI) EEPROM (U12) Atmel AT24C02D-SSHM-T, provides module characterization information to the carrier board for proper voltage settings. The carrier detects the presence of an FMC module by verifying that PRSTN_M2C_L is asserted low. It then queries the I2C EEPROM to discover which voltage is requested by the module for VADJ. The requirement and protocol are detailed in the VITA-57 specification.

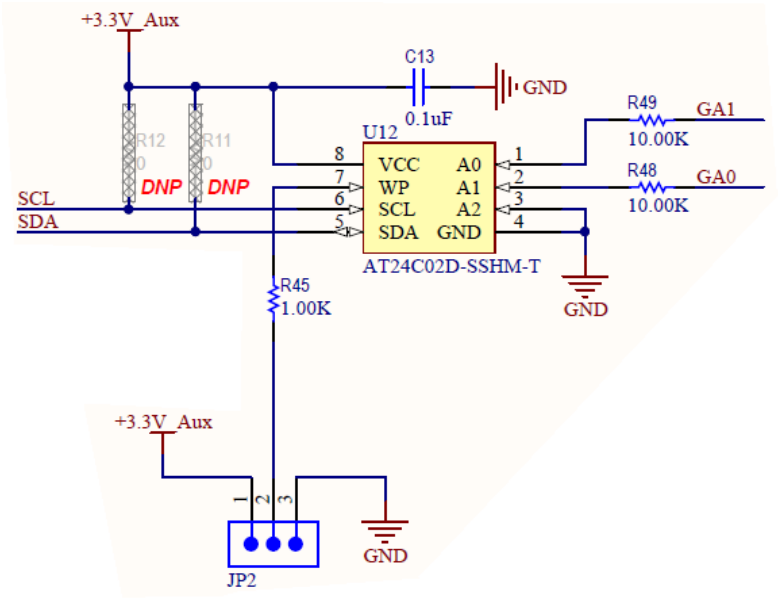


Figure 9 – IPMI EEPROM Circuit

The IPMI EEPROM address is partially derived from the FMC connector's GA0 and GA1 pins. The configuration of these signals on the carrier board will determine the complete I2C address of the EEPROM. The IPMI EEPROM I2C address is composed as follows:

- Write Address = 10100 [GA0] [GA1] 0
- Read Address = 10100 [GA0] [GA1] 1

The EEPROM may be write protected by shorting pins 1-2 on JP2.

2.8.2 Ethernet ID EEPROM

The Ethernet ID EEPROM (U2) is an On Semiconductor® CAT24C32WI-GT3. This EEPROM is provided to store configuration information for networking applications like EtherCAT. Communication with this device is accomplished via an I2C bus. The bus voltage is either 3.3V or 2.5V as determined by the carrier VADJ voltage.

The Ethernet ID EEPROM does not share the dedicated I2C bus used by the IPMI EEPROM described in section 2.8.1, which are dedicated pins mandated by the VITA-57 FMC specification. Therefore the Ethernet ID EEPROM has a hard-wired I2C address as follows:

- Write Address = 0xA0
- Read Address = 0xA1

2.8.3 Security EEPROM

The Security EEPROM (U16) is not populated, however the PCB includes landing pads for a Maxim DS28E35P+. This device provides a highly secure solution for the carrier host controller to authenticate peripherals based on the industry standard (FIPS 186) public-key based Elliptic Curve Digital Signature Algorithm (ECDSA).

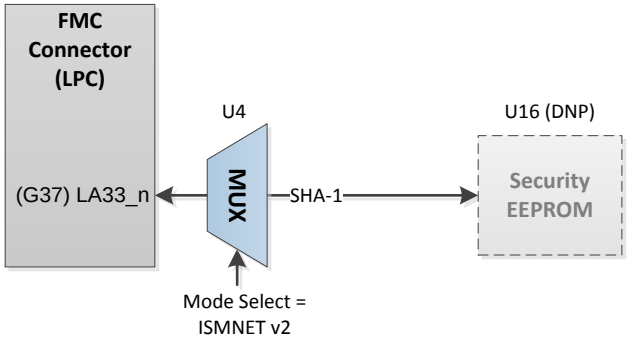


Figure 10 – Security EEPROM Diagram

The Security EEPROM can be used as a convenient method for 3rd party IP providers to implement licensing provisions for software/firmware running on the carrier FPGA/SoC.

2.8.4 Flash

The purpose of this memory device is to store persistent network information. It is implemented with the Micron N25Q256A13EF840E (U18), a 256Mb SPI Flash device with max clock rate of 108MHz. See section 2.2 for details on configuring the Mode Select multiplexor.

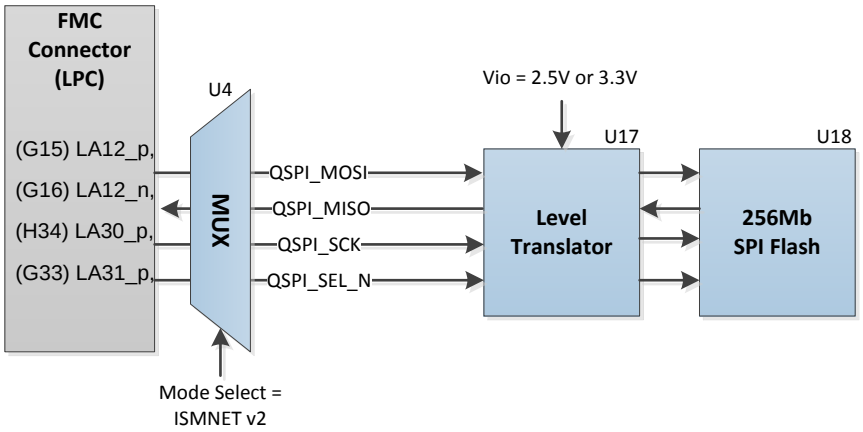


Figure 11 – Flash Memory Diagram

2.9 Expansion I/O (Pmod)

Figure 12 shows a block diagram of the GPIO PMOD interface. The ISM Networking FMC module provides a 1x6-pin I/O header receptacle, J8, compatible with the Digilent® 1x6-pin Peripheral Module (Pmod™) standard. This standard specifies four user I/O plus 3.3V and ground. A bi-directional voltage translator is used to convert the FPGA's Vio voltage to the 3.3V format required at the PMOD connector. The level shifter, U9, is a Texas Instruments TXB0104ZXUR.

See section 2.2 for details on configuring the Mode Select multiplexor.

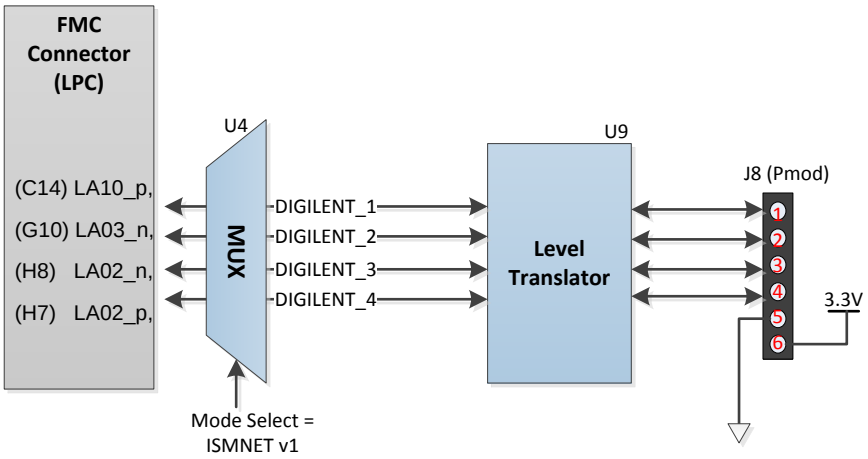


Figure 12 – Pmod Diagram

2.10 User LEDs

In addition to the three LEDs connected to each Ethernet PHY to indicate link status, the FMC-ISMNET2 module includes a total of eight user LEDs. See section 2.2 for details on configuring the Mode Select multiplexor to use these LEDs.

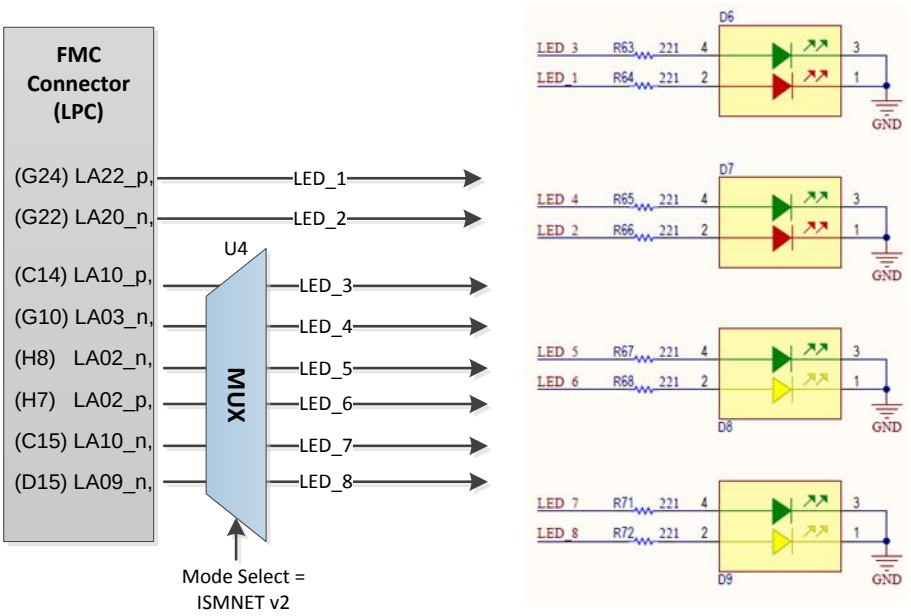


Figure 13 – User LED Diagram

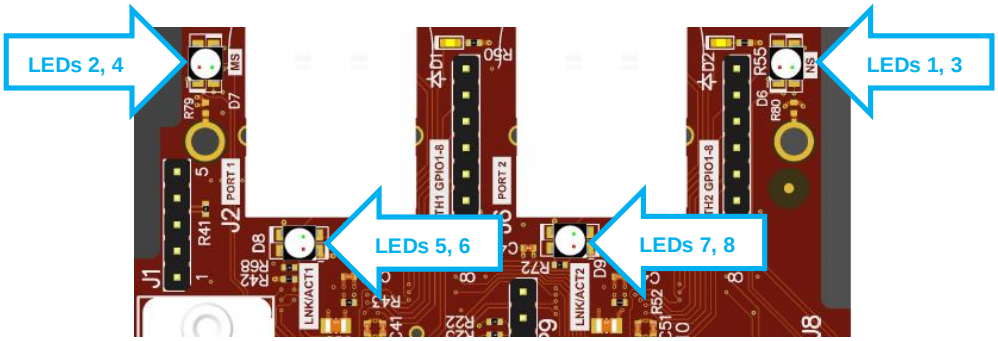


Figure 14 – User LED Locations

3 User I/O and Jumper Configurations

The tables in this section summarize the location and configuration of all user I/O connections and jumper configurations for the FMC module.

3.1 User Interfaces

Designator	Function
SW1	User Defined Push-Button Switch
SW2	User Defined Push-Button Switch
SW3	User Defined 4-position DIP Switch
RS-485	
J1-1	RS485 TX P output from U1 MAX13433EESD+ (U1)
J1-2	RS485 TX N output from U1 MAX13433EESD+ (U1)
J1-3	RS485 RX N output from U1 MAX13433EESD+ (U1)
J1-4	RS485 RX P output from U1 MAX13433EESD+ (U1)
J1-5	GND
Ethernet Jacks	
J2	Ethernet RJ-45 Jack (PHY1)
J6	Ethernet RJ-45 Jack (PHY2)
Ethernet PHY	
J3-1	Vio
J3-2:7	6 GPIO Header for PHY1
J3-8	GND
J7-1	Vio
J7-2:7	6 GPIO Header for PHY2
J7-8	GND
JP3	FMC/PHY JTAG Configuration Header
CAN	
JP12-1	CAN1_N output from SN65HVD233D (U15)
JP12-2	CAN1_P output from SN65HVD233D (U15)
JP12-3	GND
JP13-1	CAN2_N output from SN65HVD233D (U13)

JP13-2	CAN2_P output from SN65HVD233D (U13)
JP13-3	GND
Pmod	
J8	PMOD Header

Table 3 – User I/O Connections

3.2 Jumper Configurations

Jumper ID Setting	Jumper Effect
RS232	
JP1 1-2	RS232 operates as DCE
JP1 2-3	RS232 operates as DTE
IPMI EEPROM	
JP2 1-2	Allows data writes to IPMI EEPROM (U12)
JP2 2-3	Write protects IPMI EEPROM (U12)
CAN2	
JP4 1-2	Places 120 ohm termination resistor across CAN transceiver #2 differential signals
JP5 1-2	Places CAN transceiver #2 in standby mode
JP5 3-4	Sets slew rate for CAN transceiver #2 to 15 V/uS
JP5 5-6	Sets slew rate for CAN transceiver #2 to 2 V/uS
JP5 7-8	Sets slew rate for CAN transceiver #2 to high speed
JP8 1-2	Places CAN transceiver #2 in loopback mode
Ethernet CARRIER_25MHZ	
JP6 1-2	Forwards CARRIER_25MHZ signal to Spartan-6 Clock Capable pin
JP6 2-3	Forwards CARRIER_25MHZ signal to Virtex-6 Clock Capable pin
Ethernet CLK_OUT	
JP7 1-2	Forwards ETH1_CLK_OUT signal to Spartan-6 Clock Capable pin
JP7 2-3	Forwards ETH1_CLK_OUT signal to Virtex-6 Clock Capable pin
Ethernet Ref Clock	

JP9 1-2	Ethernet PHY reference clock ETH_25MHz sourced from the carrier C2M_25MHz signal
JP9 2-3	Ethernet PHY reference clock ETH_25MHz sourced from the on-board 25MHz oscillator.
CAN1	
JP10 1-2	Places CAN transceiver #1 in standby mode
JP10 3-4	Sets slew rate for CAN transceiver #1 to 15 V/uS
JP10 5-6	Sets slew rate for CAN transceiver #1 to 2 V/uS
JP10 7-8	Sets slew rate for CAN transceiver #1 to high speed
JP11 1-2	Places CAN transceiver #1 in loopback mode
JP14 1-2	Places 120 ohm termination resistor across CAN transceiver #1 differential signals
Mode Configuration	
JP15 open	Mode Configuration: selects FMC-ISMNET v1 compatibility
JP15 1-2	Mode Configuration: selects FMC-ISMNET v2 mode See section 2.2 Mode Configuration

Table 4 – Jumper Settings

4 FMC Connector Pin Assignments

The table below lists all of the VITA-57 FMC Low Pin Count (LPC) signal assignments. The FMC specification defines the LPC interface to be a 160-pin connector arranged in a 4x40 array. Below is a table that shows the FMC LPC signal names.

	H	G	D	C
1	VREF_A_M2C	GND	PG_C2M	GND
2	PRSNT_M2C_L	CLK1_M2C_P	GND	DP0_C2M_P
3	GND	CLK1_M2C_N	GND	DP0_C2M_N
4	CLK0_M2C_P	GND	GBTCLK0_M2C_P	GND
5	CLK0_M2C_N	GND	GBTCLK0_M2C_N	GND
6	GND	LA00_P_CC	GND	DP0_M2C_P
7	LA02_P	LA00_N_CC	GND	DP0_M2C_N
8	LA02_N	GND	LA01_P_CC	GND
9	GND	LA03_P	LA01_N_CC	GND
10	LA04_P	LA03_N	GND	LA06_P
11	LA04_N	GND	LA05_P	LA06_N
12	GND	LA08_P	LA05_N	GND
13	LA07_P	LA08_N	GND	GND
14	LA07_N	GND	LA09_P	LA10_P
15	GND	LA12_P	LA09_N	LA10_N
16	LA11_P	LA12_N	GND	GND
17	LA11_N	GND	LA13_P	GND
18	GND	LA16_P	LA13_N	LA14_P
19	LA15_P	LA16_N	GND	LA14_N
20	LA15_N	GND	LA17_P_CC	GND
21	GND	LA20_P	LA17_N_CC	GND
22	LA19_P	LA20_N	GND	LA18_P_CC
23	LA19_N	GND	LA23_P	LA18_N_CC
24	GND	LA22_P	LA23_N	GND
25	LA21_P	LA22_N	GND	GND
26	LA21_N	GND	LA26_P	LA27_P
27	GND	LA25_P	LA26_N	LA27_N
28	LA24_P	LA25_N	GND	GND
29	LA24_N	GND	TCK	GND
30	GND	LA29_P	TDI	SCL
31	LA28_P	LA29_N	TDO	SDA
32	LA28_N	GND	3P3VAUX	GND
33	GND	LA31_P	TMS	GND
34	LA30_P	LA31_N	TRST_L	GA0
35	LA30_N	GND	GA1	12P0V
36	GND	LA33_P	3P3V	GND
37	LA32_P	LA33_N	GND	12P0V
38	LA32_N	GND	3P3V	GND
39	GND	VADJ	GND	3P3V
40	VADJ	GND	3P3V	GND
	LPC Connector	LPC Connector	LPC Connector	LPC Connector

Table 5 – VITA-57 FMC LPC Connector Pinout

Note: For the FMC LPC, the connector columns K, J, F, E, B, and A are not used and not shown in the above table.

The SAMTEC connector receptacle (MC-LPC-10 part number: ASP-134604-01) on the module mates with the SAMTEC low pin count plug (CC-LPC-10 part number: ASP-134603-01) that resides on the carrier boards.

The table below shows the pin and signal assignments on the FMC LPC connector as it is implemented on the FMC-ISMNET2 module.

Schematic Net Name	FMC Connector Pin Location (CON1)	FMC Connector Symbol Name
GND	C1	GND
-	**C2**	**DP0_C2M_P**
-	**C3**	**DP0_C2M_N**
GND	C4	GND
GND	C5	GND
-	**C6**	**DP0_M2C_P**
-	**C7**	**DP0_M2C_N**
GND	C8	GND
GND	C9	GND
ETH2_RESETn	**C10**	**LA06_P**
CAN2_DOUT	**C11**	**LA06_N**
GND	C12	GND
GND	C13	GND
MUXED_D1	**C14**	**LA10_P**
MUXED_D5	**C15**	**LA10_N**
GND	C16	GND
GND	C17	GND
ETH1_CRS	**C18**	**LA14_P**
ETH1_RX_ER	**C19**	**LA14_N**
GND	C20	GND
GND	C21	GND
ETH1_CLK_OUT_V	**C22**	**LA18_P_CC**
RS485_TX_EN	**C23**	**LA18_N_CC**
GND	C24	GND
GND	C25	GND
ETH1_RX_D2	**C26**	**LA27_P**
ETH2_TX_EN	**C27**	**LA27_N**

GND	C28	GND
GND	C29	GND
SCL	**C30**	**SCL**
SDA	**C31**	**SDA**
GND	C32	GND
GND	C33	GND
GA0	**C34**	**GA0**
+12V	C35	12P0V
GND	C36	GND
+12V	C37	12P0V
GND	C38	GND
+3.3V	C39	3P3V
GND	C40	GND
PG_C2M	**D1**	**PG_C2M**
GND	D2	GND
GND	D3	GND
-	**D4**	**GBTCLK0_M2C_P**
-	**D5**	**GBTCLK0_M2C_N**
GND	D6	GND
GND	D7	GND
CARRIER_25MHZ_V	**D8**	**LA01_P_CC**
CAN1_DIN	**D9**	**LA01_N_CC**
GND	D10	GND
ETH2_MDIO	**D11**	**LA05_P**
ETH2_CRS	**D12**	**LA05_N**
GND	D13	GND
ETH2_RX_D1	**D14**	**LA09_P**
MUXED_D6	**D15**	**LA09_N**
GND	D16	GND
ETH1_LINK	**D17**	**LA13_P**

ETH1_RX_DV	**D18**	**LA13_N**
GND	D19	GND
ETH2_TX_CLK	**D20**	**LA17_P_CC**
ETH1_PWRDN_INTn	**D21**	**LA17_N_CC**
GND	D22	GND
ETH2_TX_D0	**D23**	**LA23_P**
ETH2_TX_D1	**D24**	**LA23_N**
GND	D25	GND
ETH2_TX_D2	**D26**	**LA26_P**
ETH2_TX_D3	**D27**	**LA26_N**
GND	D28	GND
JTAG_TCK	**D29**	**TCK**
JTAG_TDI	**D30**	**TDI**
JTAG_TDO	**D31**	**TDO**
+3.3V_AUX	D32	3P3VAUX
JTAG_TMS	**D33**	**TMS**
JTAG_TRSTn	**D34**	**TRST_L**
GA1	**D35**	**GA1**
+3.3V	D36	3P3V
GND	D37	GND
+3.3V	D38	3P3V
GND	D39	GND
+3.3V	D40	3P3V
GND	G1	GND
ETH1_TX_CLK	**G2**	**CLK1_M2C_P**
ETH1_CLK_OUT_S	**G3**	**CLK1_M2C_N**
GND	G4	GND
GND	G5	GND
ETH2_RX_CLK	**G6**	**LA00_P_CC**
ETH2_CLK_OUT	**G7**	**LA00_N_CC**

GND	G8	GND
CAN2_DIN	**G9**	**LA03_P**
MUXED_D2	**G10**	**LA03_N**
GND	G11	GND
ETH2_RX_ER	**G12**	**LA08_P**
ETH2_COL	**G13**	**LA08_N**
GND	G14	GND
MUXED_D7	**G15**	**LA12_P**
MUXED_D8	**G16**	**LA12_N**
GND	G17	GND
ETH1_MDIO	**G18**	**LA16_P**
ETH1_MDC	**G19**	**LA16_N**
GND	G20	GND
ETH2_LINK	**G21**	**LA20_P**
LED_2	**G22**	**LA20_N**
GND	G23	GND
LED_1	**G24**	**LA22_P**
CAN1_DOUT	**G25**	**LA22_N**
GND	G26	GND
ETH1_RX_D1	**G27**	**LA25_P**
ETH1_TX_D3	**G28**	**LA25_N**
GND	G29	GND
C2M_25MHZ	**G30**	**LA29_P**
ETH1_TX_D0	**G31**	**LA29_N**
GND	G32	GND
MUXED_D10	**G33**	**LA31_P**
IO_SDA	**G34**	**LA31_N**
GND	G35	GND
RS232_TX	**G36**	**LA33_P**
MUXED_D11	**G37**	**LA33_N**

GND	G38	GND
+VIO	G39	VADJ
GND	G40	GND
-	H1	VREF_A_M2C
GND	**H2**	**PRSNT_M2C_L**
GND	H3	GND
ETH1_RX_CLK	**H4**	**CLK0_M2C_P**
CARRIER_25MHZ_S	**H5**	**CLK0_M2C_N**
GND	H6	GND
MUXED_D4	**H7**	**LA02_P**
MUXED_D3	**H8**	**LA02_N**
GND	H9	GND
ETH2_MDC	**H10**	**LA04_P**
ETH2_RX_DV	**H11**	**LA04_N**
GND	H12	GND
ETH2_RX_D3	**H13**	**LA07_P**
ETH2_RX_D2	**H14**	**LA07_N**
GND	H15	GND
ETH2_RX_D0	**H16**	**LA11_P**
ETH2_PWRDN_INT	**H17**	**LA11_N**
GND	H18	GND
ETH1_RESETn	**H19**	**LA15_P**
ETH1_COL	**H20**	**LA15_N**
GND	H21	GND
RS485_DIN	**H22**	**LA19_P**
RS485_RX_EN#	**H23**	**LA19_N**
GND	H24	GND
RS485_DOUT	**H25**	**LA21_P**
ETH1_RX_D3	**H26**	**LA21_N**
GND	H27	GND

ETH1_RX_D0	**H28**	**LA24_P**
ETH1_TX_D2	**H29**	**LA24_N**
GND	H30	GND
ETH1_TX_D1	**H31**	**LA28_P**
ETH1_TX_EN	**H32**	**LA28_N**
GND	H33	GND
MUXED_D9	**H34**	**LA30_P**
RS232_RX	**H35**	**LA30_N**
GND	H36	GND
IO_SCL	**H37**	**LA32_P**
RS232_CTS	**H38**	**LA32_N**
GND	H39	GND
+VIO	H40	VADJ