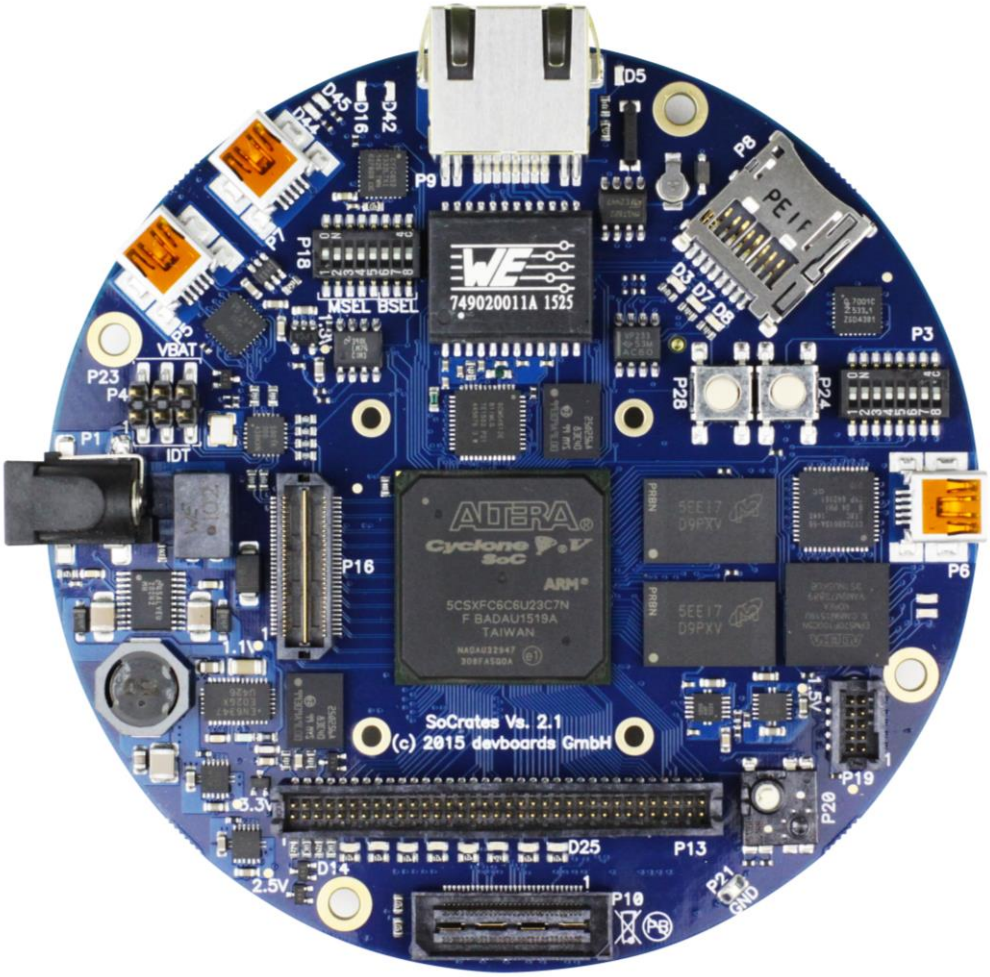
Datasheet

SoCrates II

Cyclone V-SoC Evaluation Board



www.devboards.de

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Revisions

Revision	Remark	Date
1.00	Initial Version	15.03.2015
1.10	Added new hardware features	28.09.2015
1.11	Added Description of TFT Ref Design	15.10.2015

Hardware Revisions

Revision	Remark	Date
2.0	Initial Version	15.02.2015
2.1	Add a NXP Security Chip modify the print for VBAT - IDT	15.06.2015

Ordering Information

SoCrates II

- SoCrates II Evaluation Board
- 90 - 240V wall power Supply
- Two Mini-USB Cables
- µSDCard with Linux Image

Introduction

SoCrates II is the second edition of the SoCrates SoC Evaluation boards. Based on the first version, some minor changes improve the feature set and functionality of the board. The base design is kept: Altera SoC FPGA with 110KLE, 1Gbyte DDR3 memory, SD-Card Interface, two QSPI flashs for FPGA Configuration and HPS booting. The memory was converted from one 32bit memory into two 16 bit devices, due to obsolescence reasons. The QPSI flashes were changed from SOIC footprint to BGA packages. On the peripheral side the Gigabit Ethernet Phy was changed to the Broadcom Phy, the USB / UART device was changed into a chip from Cypress. Most of the pinheaders are kept identically. The FPGA device was changed from a non transceiver device into a transceiver device with six 3.125Gbit/s transceiver. The transceiver channels are available on a new added high speed connector.

The onboard crypto security chip demonstrates ways for adding typical security functions to an embedded system like: Anti-Cloning, Network Security and Signing Transactions. This includes features like a secured key storage, TLS handling, different symmetric and asymmetric calculations, HASH values and a true random number generator in Hardware.

- 5CSXFC6C6U23C7N
- 256Mbit configuration flash
- 256Mbit boot flash
- 1GByte x32 DDR3 Memory
- BCM54612 Gigabit Ethernet Phy
- USB 2.0 OTG Phy
- UART / USB Converter
- CAN Driver
- NXP security chip
- LM74 I²C temperature sensor
- RTC with Goldcap
- 16 GPIO 3.3V (HPS)
- 3 User LEDs
- 8-DIP-Switch

- 30 GPIO 3.3V
- 32 GPIO 2.5 / 3.3V

- LVDS Interface on High-Speed Connector
- LVDS TFT Interface (4.Lanes)+ four 3.3V GPIOs
- 8x User LEDs
- Navigation key
- JTAG interface
- Embedded ΣΔ-ADC /DAC
- 6 3.125Gbit/s transceiver

- Embedded USB-Blaster II

- on board 5V, 3.3V, 2.5V, 1.5V and 1.1V power supply

- dimension : 100mm diameter

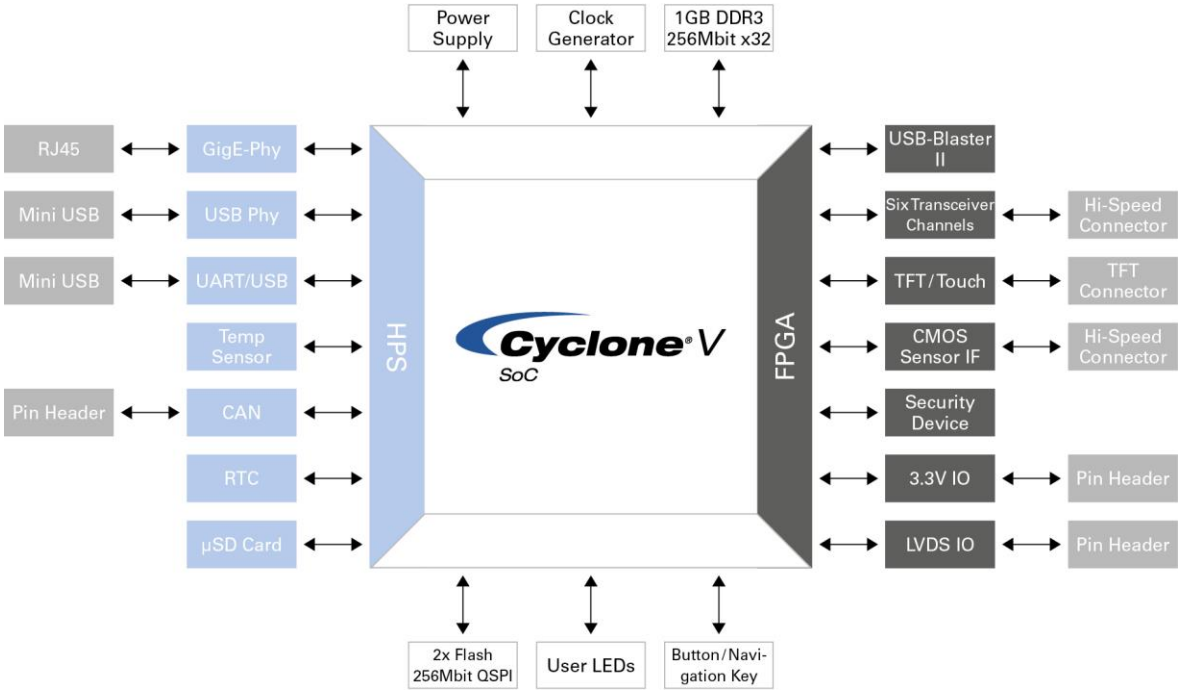

Power Supply
Clock Generator
1GB DDR3 256Mbit x32
RJ45
GigE-Phy
Mini USB
USB Phy
Mini USB
UART/USB
Temp Sensor
Pin Header
CAN
RTC
µSD Card
HPS
Cyclone V SoC
FPGA
USB-Blaster II
Six Transceiver Channels
Hi-Speed Connector
TFT/Touch
TFT Connector
CMOS Sensor IF
Hi-Speed Connector
Security Device
3.3V IO
Pin Header
LVDS IO
Pin Header
2x Flash 256Mbit QSPI
User LEDs
Button/Navi-gation Key

Figure 1

Header locations

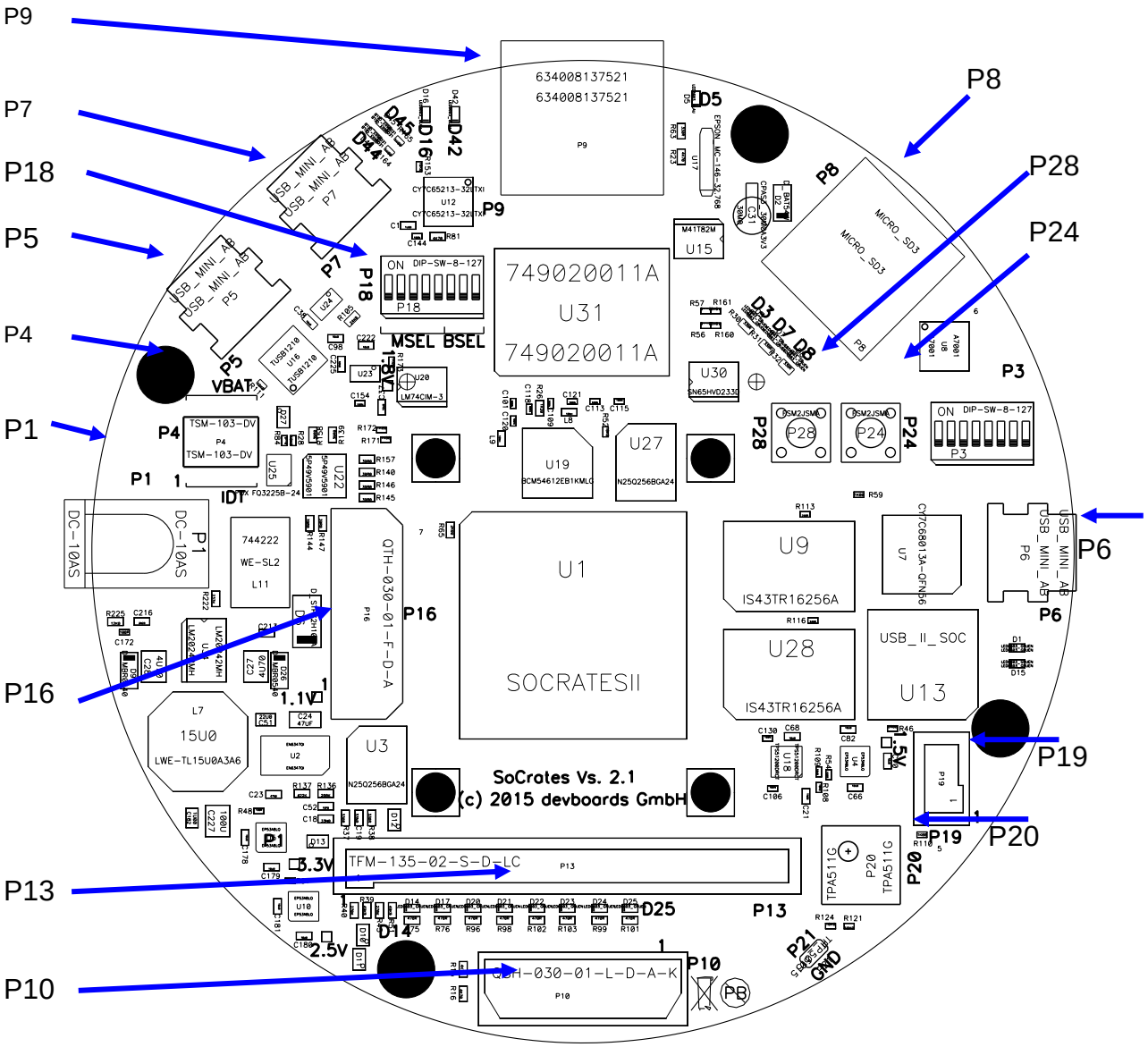


Figure 2

Pin-Header Locations (bottom side)

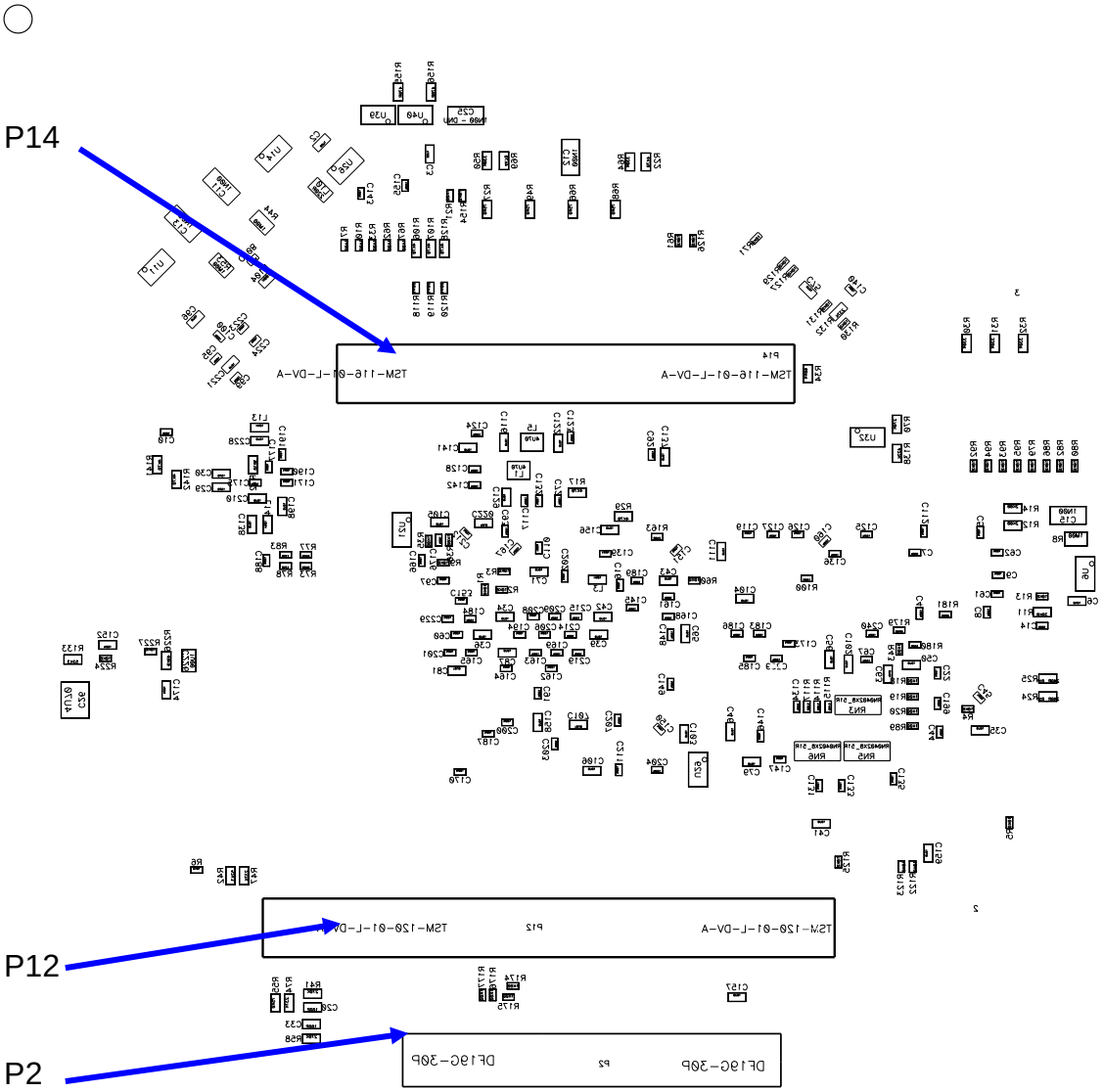


Figure 3

Installation

For installing the documentation, applications and reference designs please download the SoCrates_II_setup.exe file from www.devboards.de/download. After starting the setup program you can install the Reference and documentation on your computer.
The reference designs are built with Quartus Version 15.0. You can download the respective Altera Design Software and the SoC EDS Software Tool from www.altera.com.

Please install the applications in the following sequence:

- install the Quartus® 15.0 Full Edition or Web Edition
- install the Embedded Software 15.0
- install the SoCrates II reference designs.

The Linux software is already installed on the SDCard delivered with the board. Linux Kernel Files can be downloaded from:

Getting started

Documentation

The complete documentation of the board, the reference designs, IP functions and the on-board devices are stored in the documentation directory of the Altera® directory e.g. C:\Altera\15.0\kits\SoCratesII\documents

Setting up the board for Linux

1) Check the jumper of the board. For default setting the jumper P4 should connect Pin 2 and 4.
2) Set the Dip Switch (1.27mm Grid) P18 to
   ON OFF OFF ON ON ON OFF ON
   This selects FPGA boot mode Fast Passive Parallel and SDCard as boot source for the HPS.
3) Insert the SDCard with a Linux Image into the SDCard slot.
4) Connect the UART with a mini-USB Cable between connector (P7) and your PC.
5) Power up the board
6) Check that the USB/UART device driver is loaded and the respective UART is available.
7) Open a terminal program for the respective UART, setup the baudrate to 115200 and press the reset button on the board. (P24)
8) Your terminal should display the Linux Boot-Sequence now.

Setting up the board for JTAG

1) Check the jumper of the board. For default setting the jumper P4 should connect Pin 2 and 4.
2) Set the Dip Switch (1.27mm Grid) P18 to
   OFF OFF ON ON OFF ON OFF ON
   This selects FPGA boot mode Active Serial and SDCard as boot source for the HPS.
1) Connect the USB cable between the USB-Blaster II (P6) and your PC.
2) Power up the board.
3) The USB-Blaster II should be recognized as JTAG-Cable in the "Device Manager".
4) Now you can start Quartus II and work with the board

Reference designs

- Linux
- SD-Card
- DDR3 access from NIOS II
- TFT

Linux

Reference Design

SD-Card:

The design can be found in C:/altera/15.0/kits/SoCrates_II/designs under the folder name “SoCrates_II_reference”.

The design contains a Hard Processor System (HPS) with the following peripherals:

- 1 EMAC (RGMII)
- 1 QSPI Flash controller
- 1 SD/MMC controller
- 1 USB controller
- 2 SPI controllers
- 2 I^2C controllers
- 1 CAN controller

There is no NIOS processor in the design and the clock and reset are provided from the HPS output clock and reset. There is also one JTAG to Avalon Master Bridge in the design and a 64k On-Chip memory. All the IOs are connected to the HPS lightweight bridge and the JTAG to Avalon Master Bridge. There is also an 8 Channel PWM to run the 8 LEDs on the board.

As the design isn’t set to boot from the FPGA it should be mounted on the SD card before running. To have a design running from the FPGA some changes should be made to the HPS settings.

DDR3 access from NIOS:

The design can be found in C:/altera/15.0/kits/SoCrates_II/designs under the folder name “SoCrates_II_NIOS”.

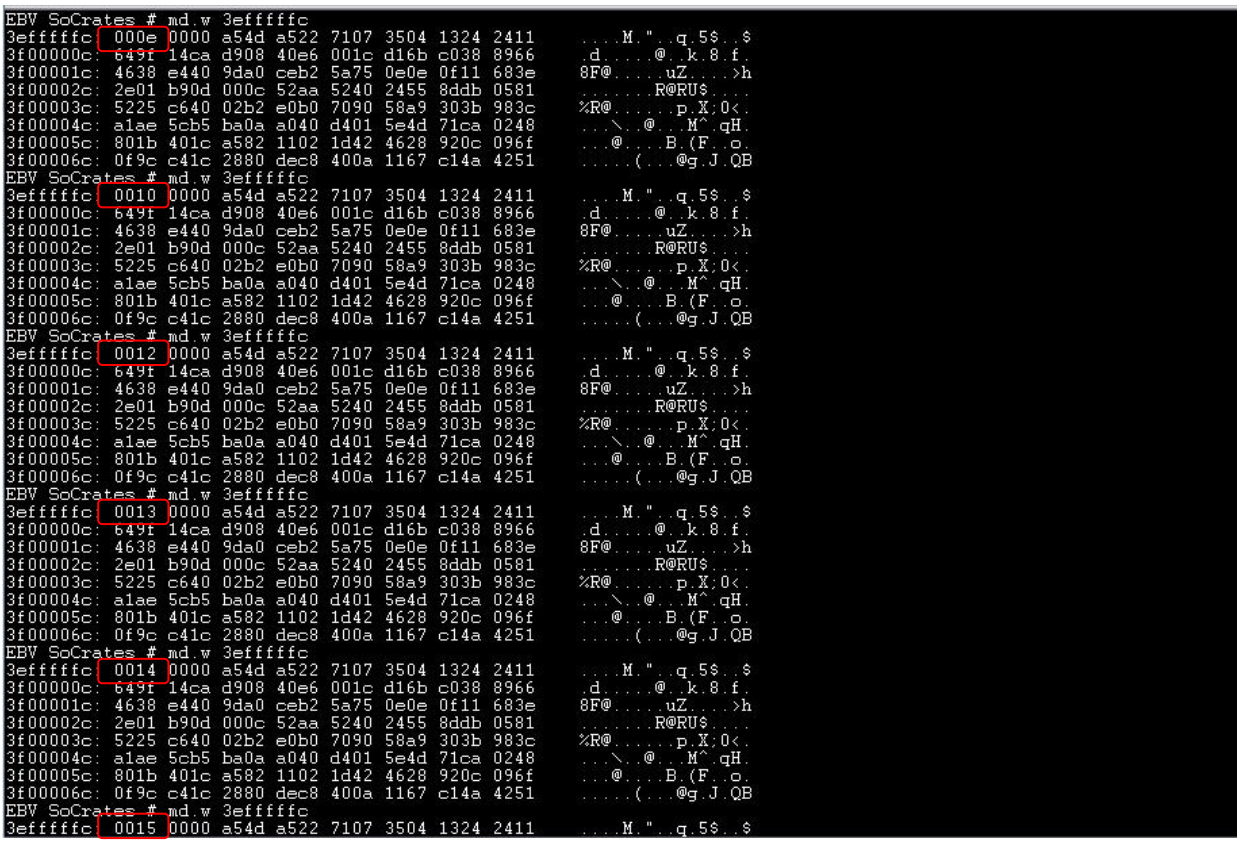
As the NIOS has to access peripherals / memory out of the HPS area, the HPS has to initialize the peripherals, Memory and the bridge between the FPGA and the HPS. Therefore the HPS has to execute the preloader, which is generated by Qsys / Quartus. To keep the system as easy as possible the preloader is located in a

38Kbyte On-Chip memory inside the FPGA and the BSEL Signals are set to “Boot from FPGA” (0x1).

Once the Preloader begins, make sure to stop it at u-boot. Now, open the NIOS II Software Build Tools and import the example software located in C:/altera/15.0/kits/SoCrates_II/designs/SoCrates_II_NIOS/software under the name “SoCrates_II_NIOS_helloworld”. Run the software and switch to the COM terminal. Enter the following u-boot command there:

```
md.w 3effffc
```

The NIOS software basically accesses the DDR3 memory writing some data on a certain address. The data is written in a form of a counter with the interval of 1 second, so if you keep executing the above command you will be able to see a count on the location as shown in the figure below:



TFT

The design can be found in C:/altera/15.0/kits/SoCrates_II/designs under the folder name “SoCrates_II_TFT”.

This design is an example design to operate a 800x480 pixel TFT via the SoCrates II board. The design contains a Hard Processor System (HPS) and the IFI graphic controller in the FPGA. There are two possibilities for this; either boot from the FPGA or load the design on an SD-Card and from there. The SD-card files can be found on the RocketBoards.org webpage:

http://www.rocketboards.org

The design contains an “ifi_socgraphic” component which can be requested from “**I**ngenieurbüro **F**ür **I**C-Technologie” (IFI).

The programming file has to be converted into a .rbf file and copied on to the SD-Card in the /boot folder. The default rbf file name is fpga_image.rbf. This rbf file is loaded in u-boot before starting the linux kernel.

Once the design is ready and mounted on the SD-Card you can insert the SD-Card. before powering up the board you have to set the MSEL settings to Fast Passive Parallel 32 (FPP32). The MSEL pins are set to Active Serial by default but to change to FPP32 change the DIP Switch (P18) settings to the following:

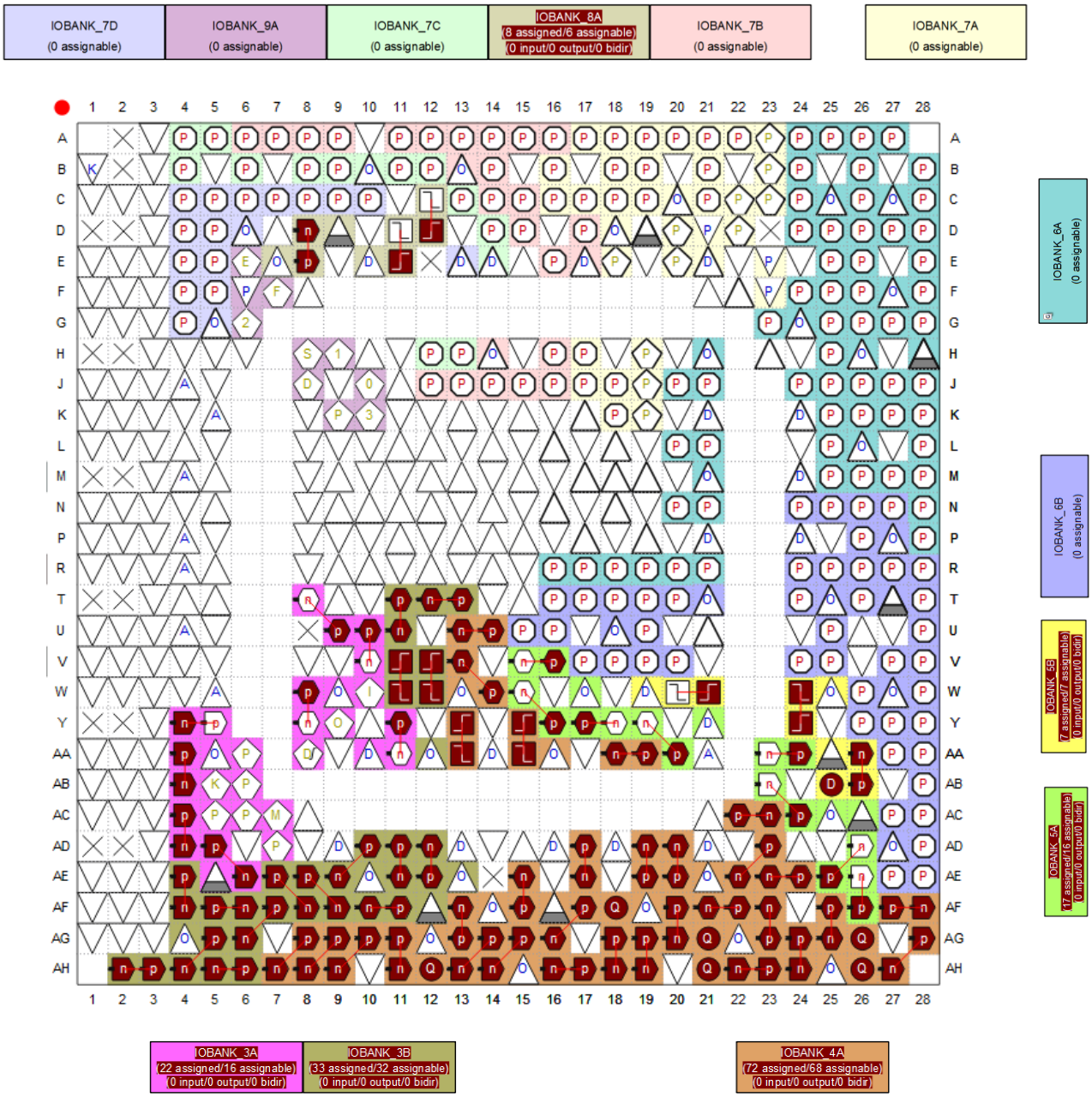
ON OFF OFF ON ON ON OFF ON

Once all the settings are complete, the board can be powered on and the design can be tested with a TFT connected with the TFT port P2.

A complete TFT with Touch Kit for the SoCrates II Kit can be ordered from LNT Automation. Ordering Code: EVK 2 TI1

Board Description

FPGA IO-Banks



IO-Bank	Voltage	VCCPD	VREF
3A	2.5V	2.5V	
3B	3.3V	3.3V	
4A	3.3V	3.3V	
5A	2.5V	2.5V	
5B	2.5V	2.5V	
6A	1.35V	2.5V	0.675V
6B	1.35V	2.5V	0.675V
7A	3.3V	3.3V	
7B	3.3V	3.3V	
7C	3.3V	3.3V	
7D	1.8V	2.5V	
8A	2.5V	2.5V	

Table 1

FPGA Configuration

The SoCrates II provides an embedded USB-Blaster II and a QSPI Flash to configure the FPGA. The QSPI Flash can be programmed using the jtag indirect configuration (.jic) files. The .jic file can be generated in the Quartus®II file / convert programming files menu. The according dialog can be found in the Quartus II menu: File / Convert Programming Files.

HPS Boot Configuration select BSEL (P18)

The BSEL pins are used to specify the boot device for the HPS System. The BSEL pins are connected to the DIP-Switch P18. Table 2 shows the location of the BSEL signals on the DIP-Switch P18. Table 3 shows the BSEL settings. More information on BSEL is available in the Cyclone V datasheet.

BSEL	P18	Default
0	6	ON
1	7	OFF
2	8	ON

Table 2

BSEL	Boot device
001	FPGA
101	SD/MMC
111	QSPI Flash

Table 3

FPGA Configuration select with MSEL (P18)

The MSEL pins are connected to the DIP-Switch P18. These signals are used to select the configuration scheme of the FPGA. SoCrates II supports configuration via the QSPI Flash or the HPS processor system. The default setting is the configuration from EPCQ device using the Active Serial Standard Configuration Scheme. (ON = ‘0’ / OFF = ‘1’)

MSEL	P18	AS-Standard	FPP(32)
0	1	OFF	ON
1	2	OFF	OFF
2	3	ON	OFF
3	4	ON	ON
4	5	OFF	ON

Table 4

Clocking

The SoCrates II Evaluation Board Clock Scheme is build around an IDT VersaClock 5 programmable Clock Generator. The 5P49V5901 has two clock sources and 9 programmable outputs. Input one is connected to a 24MHz Cristal. The device is programmed for the board requirements. Table 5 shows the outputs of the Clock driver.

IO-pin	Clock	Voltage
24 / Out0	CLK24 – USB-Blaster	3.3V
20 / Out1	CLK26 – USB	3.3V
17 / Out2	CLK25 – HPS	3.3V
16 / Out2b	CLK25 – PHY	3.3V
14 / Out3	CLK50 – FPGA	3.3V
13 / Out3b	CLK50 / FPGA	3.3V
11 / Out4	CLK100 – Transceiver	LVPCL
10 / Out4b	CLK100 - Transceiver	LVPCL

Table 5

FPGA Clock Sources

Function	FPGA Pin	FPGA Signal
50MHz	Y13	Clk50a
50MHz	Y15	Clk50a
50MHz	V11	Clk50b
50MHz	V12	Clk50b
25Mhz	E20	HPS-Clock1

Table 6

IDT Clock Buffer I²C Interface (P4)

Function	Pin	Pin	Function
GND	1	2	2.5V
IDT-SDA	3	4	VCCBAT
IDT-SCL	5	6	GND

Table 7

Power Supply

The SoCrates II Evaluation Board allows supplying the board from a 7.5V up to 36V unregulated center-positive input power supply (P1) A TI LM20242 switching regulator generates a 5V rail which is used to generate all other power rails with Enpirion Power SoC modules. A four Ampere module is used to generate the Core voltage, while one Ampere modules are used to generate the 3.3V, 2.5V and 1.5V rails. For the 1.8V USB supply a LDO is used. A TPS51200 is used to generate the DDR reference voltage and the DDR termination voltage.
Power sequencing is implemented to power up the Core Voltages (1.1V) first, then the I/O Voltages.

A "Power Good" signal is generated to signal that all voltages are in the valid ranges.

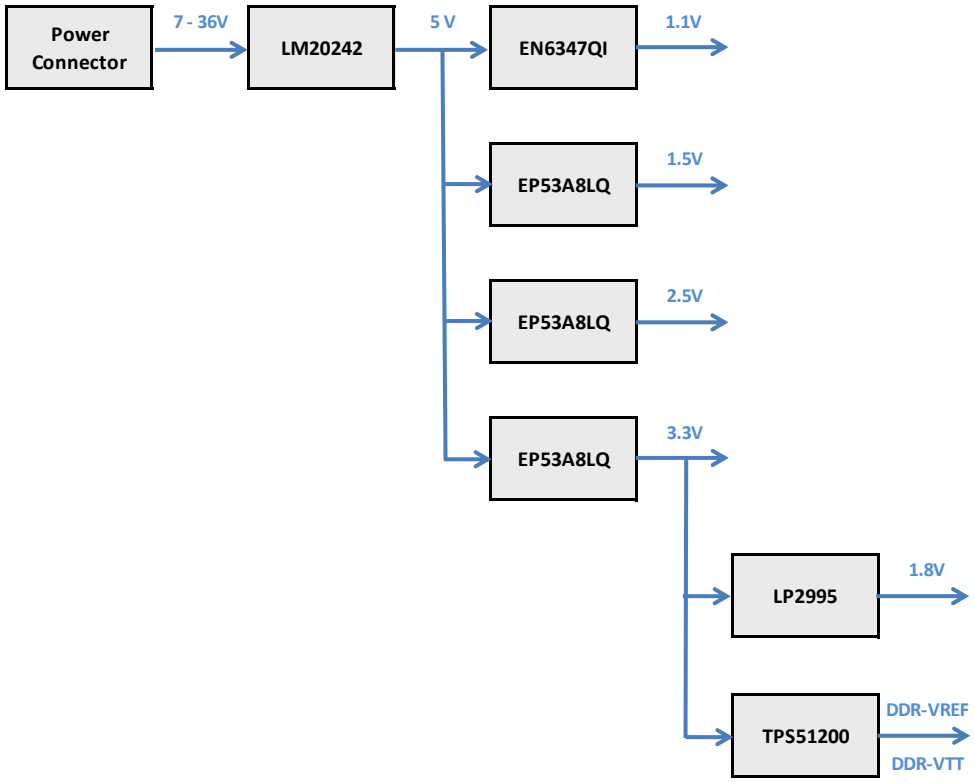


Figure 4

Reset Signal

Function	Pin	Signal Name
Power Good	H19	HPS-NPOR
Power Good	AB25	RSTn

Table 8

VBAT

Power supply for the battery backup of the FPGA can be connected to Pin P4. The VBAT Signal must be powered to start the FPGA. If no external battery backup is required insert a Jumper between pin 2 and 4. This connects 2.5V to the VBAT Signal. If you would like to power the VBAT with an external voltage use Pin 4 for the voltage and pin 6 as a GND Reference Pin.

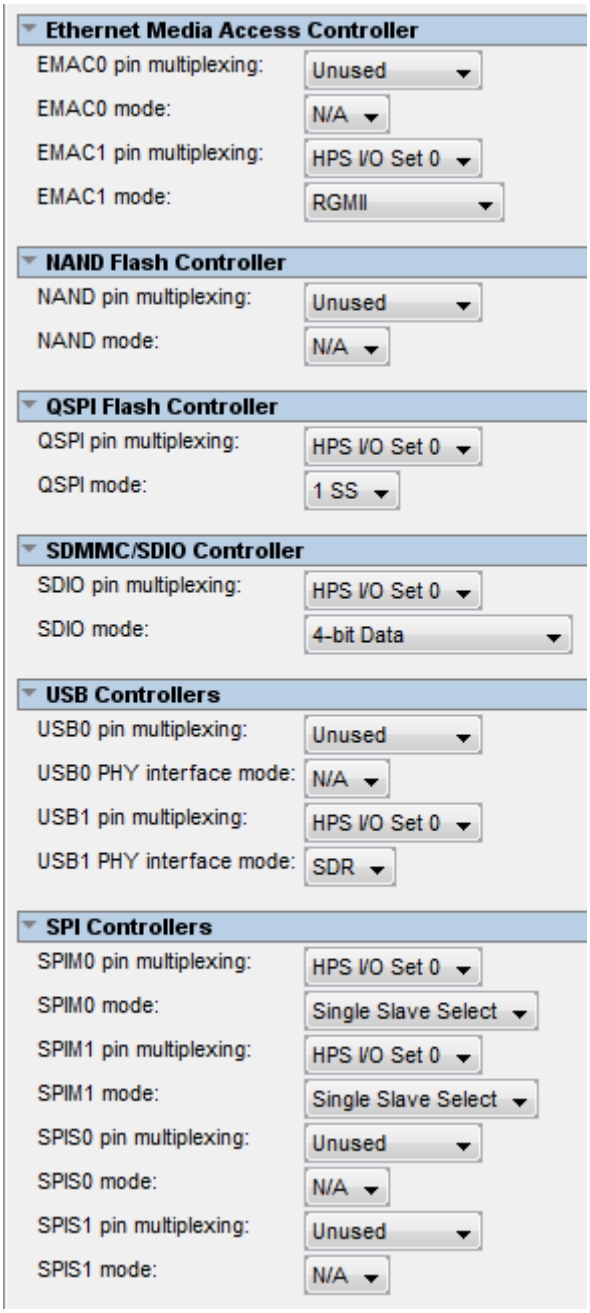
If VBAT is not connected to any voltage, the FPGA will not be accessable!!!

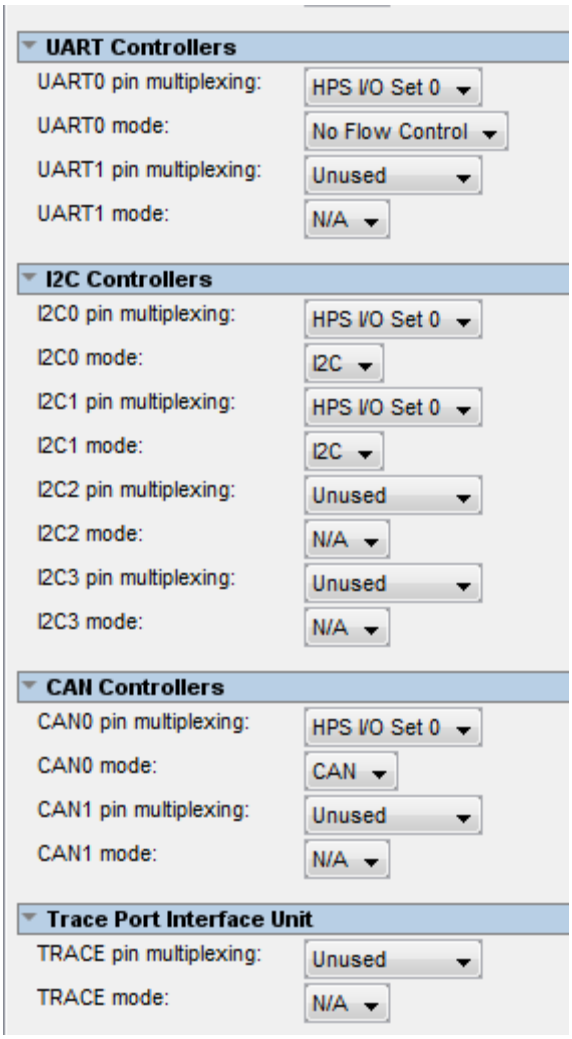
Function	Pin	Pin	Function
GND	1	2	2.5V
IDT-SDA	3	4	VCCBAT
IDT-SCL	5	6	GND

Table 9

HPS Subsystem

The figure below shows the HPS Peripheral Pin multiplexing for the SoCrates II Board.





DDR3 Memory

SoCrates II is equipped with 1Gbyte DDR3 memory based on two 4Gbit x16 DDR3 devices. The memory interface is clocked up to 400MHz using the 1.5V DDR3 standard. Figure 5 shows the memory settings in Qsys. A Preset is available for all the memory settings for the SoCrates II board called “SoCrates_II_memory.qprs” located in C:/altera/15.0/kits/SoCrates_II/designs/SoCrates_II_reference.

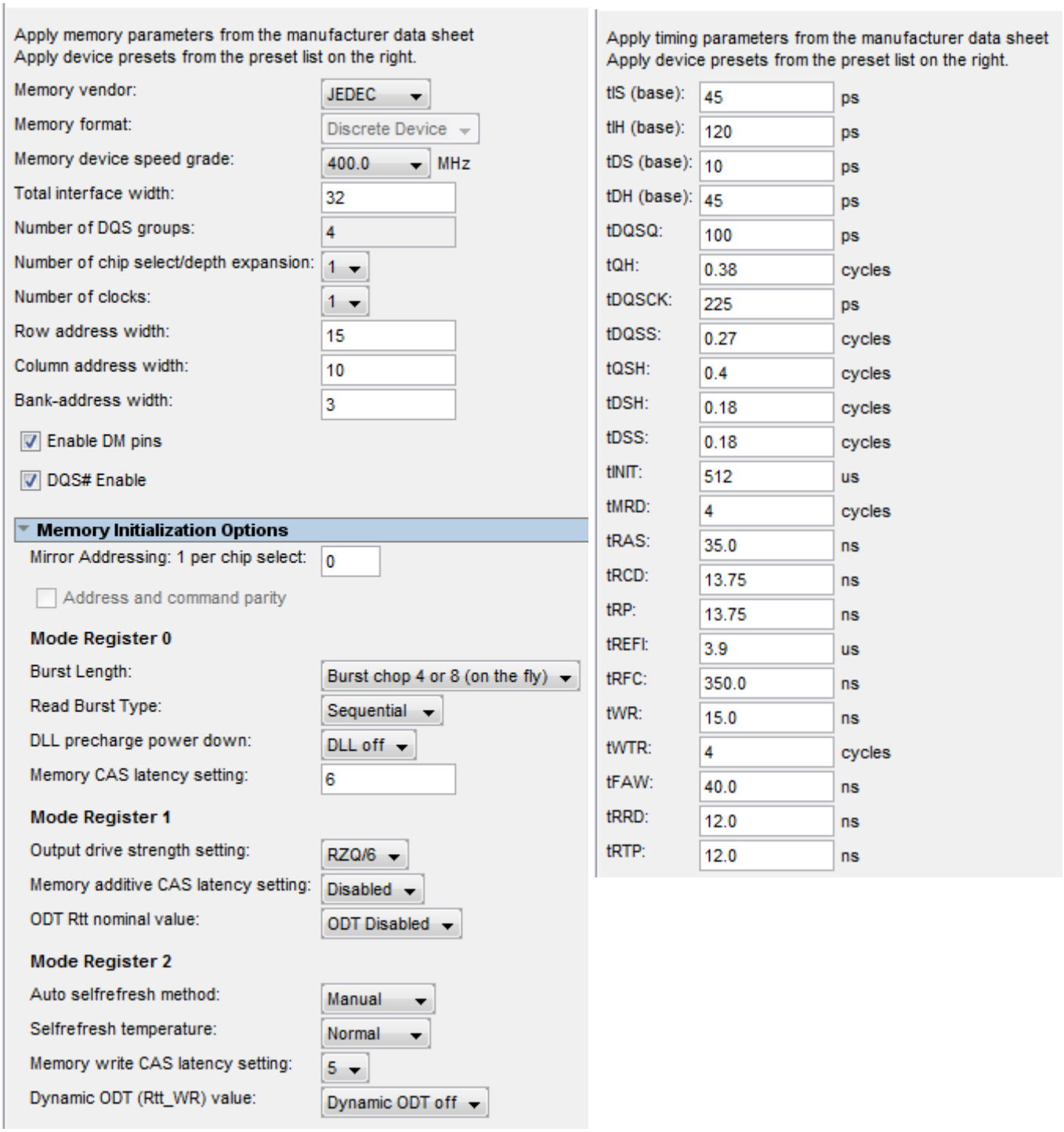


Figure 5

SDCard Interface

The SDCard interface is connected to the HPS System. The SDCard is connected in a 4 bit interface mode. The “Write Protect” Switch is connected to GPIO00.

SDCard (P8) FPGA Connection

Function	Pin	FPGA Pin
HPS-SDIO-CLK		B8
HPS-SDIO-CMD		D14
HPS-SDIO-D0		C13
HPS-SDIO-D1		B6
HPS-SDIO-D2		B11
HPS-SDIO-D3		B9
Protect Switch	GPIO00	E4

Table 10

QSPI Flash

A 256Mbit QSPI Flash device can be used for booting the HPS System. The QSPI Flash is connected to the QSPI Port of the HPS.

QSPI (U27) FPGA Connection

Function	Pin	FPGA Pin
HPS-QSPI-CS	C2	A6
HPS-QSPI-CLK	B2	C14
HPS-QSPI-D0	D3	A8
HPS-QSPI-D1	D2	H16
HPS-QSPI-D2	C4	A7
HPS-QSPI-D3	D4	J16

Table 11

USB Phy

A Texas Instruments TUSB1210 USB Phy is used on SoCrates II. It is connected to the SoC Device with an eight bit parallel interface on a 1.8V standard.

USB Phy (U16) FPGA Connection

Function	Pin	FPGA Pin
USB-D0	3	C10
USB-D1	4	F5
USB-D2	5	C9
USB-D3	6	C4
USB-D4	7	C8
USB-D5	9	D4
USB-D6	10	C7
USB-D7	13	F4
USB-CLK	26	G4
USB-NXT	2	D5

USB-DIR	31	E5
USB-STP	29	C5

Table 12

Ethernet Phy

For Ethernet Connectivity a Broadcom BCM54612 Gigabit Ethernet Phy is used. The Phy is connected to the MAC in RGMII Mode. The RJ45 connector P9 provides the Ethernet connectivity. Two LEDs are available in the RJ45 connector showing activity and 100Mbit Link, a third LED is available on the Board (D5) signalling the Gigabit Link

Ethernet Phy (U14) FPGA Connection

Function	Pin	FPGA Pin
MDC	48	E16
MDIO	47	A13
TX_CLK	40	J15
TXD0	39	A16
TXD1	38	J14
TXD2	37	A15
TXD3	36	D17
TX_CTL	35	Â12
RX_CLK	33	J12
RX_CTL	26	J13
RXD0	32	A14
RXD1	31	A11
RXD2	28	C15
RXD3	27	A9
RSTNn	46	
Interrupt	GPIO35	B14

Table 13

UART

The HPS UART is available in 3.3V Logic on Pin Header P14 and is converted into USB for direct connection with a PC.

UART on P14

These Signals are SoC Pins – no signal conditioning is implemented. If you would like to connect these signals to a standard RS232 UART, Please add a respective Level Shifter!! These signals are connected in parallel to the UART / USB converter. If these signals should be used directly, make sure to disable / remove the UART / USB converter.

Function	Pin	FPGA Pin
HPS-UART-RX	P14.32	A22
HPS-UART-TX	P14.30	B21

Table 14

UART to USB Converter

A Cypres CY7C65213 USB / serial converter is used to provide the UART Signals on a standard USB Header for direct connection to PCs. The device is powered via USB connector. The UART signals are available on the mini USB connecter P7.

Function	Pin	FPGA Pin
HPS-UART-RX	2	A22
HPS-UART-TX	30	B21

Table 15

CAN Phy

One SoC CAN module is connected to a TI SN65HVD233D CAN transceiver device. The CAN signals are available on Connector P14 – together with the termination resistor.

CAN Phy (U30) FPGA Connection

Function	Pin	FPGA Pin
HPS-CAN-RX	4	A17
HPS-CAN-TX	1	H17

Table 16

CAN Connector (P14)

Function	Pin	Pin	Function
60R4	1	2	60R4
CANH	3	4	CANL
GND	5	6	GND

Table 17

DIP Switch

SoCrates II is equipped with a DIP Switch with 8 Switches. The Switch has pull-down resistors and switch to high level in “ON” State. The DIP Switch is connected to the General Purpose Inputs signals of the HPS, located in the DDR3 Memory Bank.

Dip-Switch (P3) FPGA Connection

Function	Pin	FPGA Pin
Switch 1	GPI0	M25
Switch 2	GPI4	R28
Switch 3	GPI8	Y28
Switch 4	GPI13	V24
Switch 5	GPI5	P26
Switch 6	GPI3	R21
Switch 7	GPI9	Y26
Switch 8	GPI12	AC27

Table 18

Navigation Key

SoCrates II is equipped with a 5 Button Navigation Key. The Switch has pull-down resistors and switch to high Level in “ON” State. The Navigation Key is connected to the HPS General Purpose Input signals located in the DDR3 memory bank.

Navigation Key (P20) FPGA Connection

Function	Pin	FPGA Pin
Switch Up	GPI6	T17
Switch Down	GPI7	T16
Switch Left	GPI11	U16
Switch Right	GPI10	U15
Switch Button	GPI2	R20

Table 19

User LEDs

3 Used LEDs are available. A Logic Zero will drive the LED on. The User LEDs are connected to the HPS GPIOs.

User LEDs

Function	Pin	FPGA Pin
LED 0	GPIO28	D15
LED 1	GPIO48	C21
LED 2	GPIO54	J18

Table 20

RTC

A STM M41T82M RTC Circuit is implemented on the SoCrates with I²C Interface. The RTC is backuped with a GoldCap with 33mF. This will keep the RTC running for about 24 hours – without any Power Supply.

RTC (U15) FPGA Connection

Function	Pin	FPGA Pin
RSTn	GPI1	K27
HPS-I²C0_SCL		C18
HPS-I²C0_SDA		A19

Table 21

GPIO

All Spare IO Pins of the HPS System are connected to P14.

GPIO P14 FPGA connection

Function	Pin	Pin	Function
60R4	1	2	60R4
CANH	3	4	CANL
GND	5	6	GND
HPS_GPIO09	7	8	HPS_SPIM0_SS0
HPS_GPIO28	9	10	HPS_SPIM0_CLK
HPS_GPIO37	11	12	HPS_SPIM0_MISO
HPS_GPIO40	13	14	HPS_SPIM0_MOSI
HPS_GPIO41	15	16	HPS_GPIO54
HPS_GPIO42	17	18	HPS_GPIO63
GND	19	20	GND
HPS_GPIO43	21	22	HPS_GPI64
HPS_GPIO44	23	24	HPS_GPIO65
HPS_GPIO48	25	26	HPS_GPIO66
HPS_GPIO51	27	28	GND
HPS_GPI52	29	30	HPS_UART_TX
HPS_GPIO53	21	32	HPS_UART_RX

Table 22

Reset Buttons

The SoCrates II Board provides a Hard Reset Button (power good) and a HPS warm Reset button.

Function	Pin	FPGA Pin
RST Button P28	RSTn	
HPS-Warm Reset P24	HPS_RSTn	A23

Table 23

NXP Security device (U8)

A NXP Secuity device is connected to the I²C interface if the HPS.

Function	Pin	FPGA Pin
HPS_GPIO63 / SDA	5	C19
HPS_GPIO64 / SCL	7	B16

Table 24

FPGA Connections

IOBANK 3B

The Signals of IOBANK3 are connected to Pinheader P12. P12 is a 2.54mm Pinheader on the Bottom Side of the Board. The IOBank is supplied with 3.3V

Function	FPGA	Pin	Pin	FPGA	Function
		1	2		
GND		3	4		VCC33
IOB3B0	T12	5	6	T13	IOB3B1
IOB3B2	W11	7	8	W12	IOB3B3
IOB3B4	T11	9	10	U11	IOB3B5
IOB3B6	AE12	11	12	AD12	IOB3B7
IOB3B8	AE11	13	14	AD11	IOB3B9
IOB3B10	AD10	15	16	AF11	IOB3B11
IOB3B12	AE9	17	18	AF10	IOB3B13
IOB3B14	AF9	19	20	AF8	IOB3B15
GND		21	22		VCC33
GND		23	24		VCC33
IOB3B16	AE8	25	26	AE7	IOB3B17
IOB3B18	AF6	27	28	AF5	IOB3B19
IOB3B20	AF7	29	30	AH6	IOB3B21
IOB3B22	AG6	31	32	AH5	IOB3B23
IOB3B24	AG5	33	34	AH4	IOB3B25
IOB3B26	AF4	35	36	AH3	IOB3B27
IOB3B28	AH2	37	38	AE4	IOB3B29
GND		39	40		VCC33

Table 25

IOBANK 4A

The signals of IOBANK4 are connected to Pinheader P13. P13 is a 1.27mm Pinheader on the Top Side of the Board.
4 Signals of this IOBank are used for the ΣΔ-ADC/DAC Subsystem. This IOBank is supplied with 3.3V.Eight I/O Pins are connected to LEDs in Parallel.

Function	FPGA	Pin	Pin	FPGA	Function
AIN1		1	2		AOUT2
GND		3	4		GND
AIN2		5	6		AOUT2
GND		7	8		VCC33
IOB4A0	V13	9	10	AH7	IOB4A1
IOB4A2	W14	11	12	AG8	IOB4A3
IOB4A4	AF15	13	14	AH8	IOB4A5
IOB4A6	AE15	15	16	AG9	IOB4A7
GND		17	18		VCC33
IOB4A8	AA15	19	20	AH9	IOB4A9
IOB4A10	U13	21	22	AG10	IOB4A11
IOB4A12	AE17	23	24	AG11	IOB4A13
IOB4A14	AF18	25	26	AH11	IOB4A15
GND		27	28		VCC33
IOB4A16	AD17	29	30	AH12	IOB4A17
IOB4A18	AE19	31	32	AG13	IOB4A19
IOB4A20	AF20	33	34	AH13	IOB4A21
IOB4A22	AG14	35	36	AH14	IOB4A23
GND		37	38		VCC33
IOB4A24	AG15	39	40	AG16	IOB4A25
IOB4A26	AH16	41	42	AF17	IOB4A27
IOB4A28	AH17	43	44	AG18	IOB4A29
IOB4A30	AH18	45	46	AG19	IOB4A31
GND		47	48		GND
IOB4A32	AH19	49	59	AG20	IOB4A33
IOB4A34	AG21	51	52	AH21	IOB4A35
IOB4A36	AF21	53	54	AH22	IOB4A37
IOB4A38	AG23	55	56	AH23	IOB4A39
GND		57	58		VCC33
IOB4A40	AG24	59	60	AH24	IOB4A41
IOB4A42	AG25	61	62	AF25	IOB4A43
IOB4A44	AH26	63	64	AH27	IOB4A45
IOB4A46	AG26	65	66	AG28	IOB4A47
GND		67	68		VCC33
IOB4A48	AF27	69	70	AF28	IOB4A49

Table 26

User LEDs

Eight User LEDs are connected to Signals of IOBANK4A. These signals are connected to P13 in parallel.

User LED FPGA Connection

Function	Pin	FPGA Pin
LED0	IOB4A0	V13
LED1	IOB4A4	AF15
LED2	IOB4A8	AA15
LED3	IOB4A12	AE17
LED4	IOB4A16	AD17
LED5	IOB4A20	AF20
LED6	IOB4A24	AG15
LED7	IOB4A28	AH17

Table 27

ΣΔ-ADC / DAC Subsystem

Missing Link Electronics provides an IP-Core for ΣΔ-ADC / DAC technology using LVDS Input Signals and 3.3V IO. SoCrates II implements two ADC Channels and two DAC channels. The DAC Subsystem uses two IO Signals from IOBANK4A with a RC Low pass. The ADC requires two LVDS Inputs and two Ref outputs from IOBANK4A.

FPGA Connection (IOBANK4A)

Function	Pin	FPGA Pin
SD_Out0		AA13
SD_Out1		AF13
SD_REF0		AD19
SD_REF1		AE20

Table 28

FPGA Connection (IOBANK8A)

Function		FPGA Pin
LVDS_IN_SD0N		D11
LVDS_IN_SD0P	1.65V	E11
LVDS_IN_SD1N		C12
LVDS_IN_SD1P	1.65V	D12

Table 29

CMOS Sensor Connector (P10)

The EBV Observer CMOS Sensor Development Platform provides several CMOS Sensor boards with a standardized Pin Header. These Modules can be used on SoCrates II too. The Header provides several LVDS Channels and additional 3.3V GPIO Signals. SoCrates II is assembled with a Samtec QSH-030-01-L-A-K connector.

Function	FPGA	Pin	Pin	FPGA	Function
VCC5		1	2		VCC33
VCC5		3	4		VCC33
VCC5		5	6		VCC33
VCC5		7	8		VCC33
GND		9	10		GND
IO0	AE22	11	12	U14	IO1
IO2	AA19	13	14	AA18	IO3
IO4	AD23	15	16	AC23	IO5
GND		17	18		GND
ID0	AD4	19	20	Y24	LVDS_CLK_INP
ID1	AC4	21	22	W24	LVDS_CLKINN
GND		23	24		GND
LVDS_IN2P	Y17	25	26	W21	LVDS_IN0P
LVDS_IN2N	Y18	27	28	W20	LVDS_IN0N
LVDS_IN3P	Y16	29	30	AA20	LVDS_IN1P
LVDS_IN3N	W15	31	32	Y19	LVDS_IN1N
GND		33	34		GND
		35	36		
		37	38		
LVDS_IN4P	U10	39	40	V16	LVDS_IN6P
LVDS_IN4N	V10	41	42	V15	LVDS_IN6N
GND		43	44		GND
LVDS_IN5P	Y11	45	46	U8	LVDS_IN7P
LVDS_IN5N	AA11	47	48	T8	LVDS_IN7N
LVDS_CLK_OUTP	AB26	49	50	W8	LVDS_IN8P
LVDS_CLK_OUTN	AA26	51	52	Y8	LVDS_IN8N
GND		53	54		GND
IO6	AF23	55	56	AC22	IO7
IO8	AD20	57	58	AE23	IO9
IO10	AF22	59	60	AE24	IO11

Table 30

FPGA Connection Temperature Sensor

For the temperature sensor the National Semiconductor LM74 Temperature Sensor with a SPI / Microwire compatible interface is used. The LM74 has a 12bit resolution.

FPGA Connection

Function	Device	FPGA Pin
TS/O		D8
TSCL		E8
TCSn		Y4

Table 31

LVDS TFT Interface (P2)

SoCrates II provides a header to connect LVDS based TFT Displays directly. The Interface provides one differential Clock signal and 3 differential Data signals.

Additionally four 3.3V GPIO Signals are available for Touch controller interface or Dimming of the backlight.

FPGA Connection

Function	Pin	FPGA Pin
VCC33	1	
VCC33	2	
GND	3	
GND	4	
LVDS_TFT0N	5	AB23
LVDS_TFT0P	6	AC24
GND	7	
LVDS_TFT1N	8	AE26
LVDS_TFT1P	9	AF26
GND	10	
LVDS_TFT2N	11	AD26
LVDS_TFT2P	12	AE25
GND	13	
LVDS_CLKN	14	AA23
LVDS_CLKP	15	AA24
GND	16	
	17	
	18	
GND	19	
GND	20	
VCC33	21	
TC3	22	AE6
TC2	23	AD5
TC1	24	AB4
TC0	25	AA4
GND	26	
VCC99	27	
VCC99	28	
GND	29	
GND	30	

Table 32

Transceiver connector (P16)

All the six transceiver channels, the reference clock inputs and a 100MHz clock is connected to the high-speed samtec connector P16. SoCrates II is equipped with a Samtec QTH-030-01-F-C-A connector.

Function	FPGA	Pin	Pin	FPGA	Function
GND		1	2		GND
GXB_RX_L0p	AF2	3	4	AB2	GXB_RX_L1p
GXB_RX_L0n	AF1	5	6	AB1	GXB_RX_L1n
GND		7	8		GND
GXB_TX_L0p	AD2	9	10	Y2	GXB_TX_L1p
GXB_TX_L0n	AD1	11	12	Y1	GXB_TX_L1n
GND		13	14		GND
		15	16	V2	GXB_RX_L2p
		17	18	V1	GXB_RX_L2n
GND		19	20		GND
		21	22	T2	GXB_TX_L2p
		23	24	T1	GXB_TX_L2n
GND		25	26		GND
REFCLK0Lp	V5	27	28	P2	GXB_RX_L3p
REFCLK0Ln	V4	29	30	P1	GXB_RX_L3n
GND		31	32		GND
REFCLK1Lp	P8	33	34	M2	GXB_TX_L3p
REFCLK1Ln	N8	35	36	M1	GXB_TX_L3n
GND		37	38		GND
		39	40	K2	GXB_RX_L4p
		41	42	K1	GXB_RX_L4n
GND		43	44		GND
		45	46	H2	GXB_TX_L4p
		47	48	H1	GXB_TX_L4n
GND		49	50		GND
		51	52	F2	GXB_RX_L5p
		53	54	F1	GXB_RX_L5n
GND		55	56		GND
Clk100p		57	58	D2	GXB_TX_L5p
Clk100n		59	60	D1	GXB_TX_L5n

Table 33

Bill of Material

Part Number	Amount	Package	Reference
CY7C68013A-56LTXC	1	QFN56	U7
M41T82ZM6F	1	SOIC8	U15
CY7C65213-32LTXI	1	QFN-32	U12
5P49V5901A000NLGI	1	VFQFPN-24	U22
BCM54612EB1IMLG	1	MLP-48	U19
EPM570F100C5N	1	FPGA-100	U13
EN6347QI	1	QFN-38	U2
EP53A8LQI	3	QFN-16	U4 U5 U10
5CSXFC6C6U23C7N	1	BGA 672	U1
SN65HVD233D	1	SO8	U30
TPS3103K33DBVTG	1	SOT23-5	U32
SN65220DBVTG4	3	SO8	U6 U11 U14
SN74AVCH1T45DCKT	1	SC706	U29
REF3033AIDBZTG4	1	SOT-23	U21
TPS51200DRCT	1	SON10	U18
TPS2553DBV	1	SOT-23	U24
TUSB1210BRHBT	1	QFN	U16
TPS76933DBVT	1	SOT-23	U26
LM74	1	SO8	U20
LM20242MH	1	TSSOP20	U34
LP2992AIM5-1.8	1	SOT-23	U23
MT41K256M16HA-125:E	2	96-FBGA	U9 U28
N25Q256A83E1240F	2	24-TBGA	U3 U27
A7001AGHN1/HVQFN32	1	HVQFN32	U8
MBR0540	2	SOD123	D9 D26
D_STPS2H100A	1	SMA	D6
LED 0603_Blau	3	603	D5 D16 D42
LED 0603_yellow	2	SMD	D44 D45
LED 0603_GREEN 5mA	13	SMD	D1 D3 D7 D8 D14 D15 D17 D20 D21 D22 D23 D24 D25
BAT54SWT1G	5	SOT323	D10 D11 D12 D13 D27
BAT54H,115 (SOD123)	1	SOD123	D2
BC850B	2	SOT23	U39 U40
Quarz Oscillator Epson MC-146 32.768KHz	1		U17
OSC24.00 MHz Commercial Temperaturbereich	1	4-SMD	U25
R0603_2K00A1%0	3	R0603	R12 R14 R65
R0603_12K0A1%0	1	R0603	R225
R0603_20K0A1%0	1	R0603	R11
R0603_60R4A1%0	1	R0603	R34
R0603_100KA1%0	1	R0603	R104
R0603_330RA1%0	8	R0603	R30 R31 R32 R37 R38 R50 R63 R64
R0603_470RA1%0	10	R0603	R75 R76 R96 R98 R99 R101 R102 R103 R155 R156

R0603_4K70A1%0	13	R0603	R15 R16 R17 R22 R23 R29 R69 R81 R106 R107 R128 R141 R142
R0603_24K0A1%0	1	R0603	R105
R0603_75RA1%0	4	R0603	R27 R49 R66 R68
R0603_49K9	3	R0603	R39 R51 R226
R0603_75K0A1%0	1	R0603	R55
R0603_270KA1%0	5	R0603	R40 R41 R45 R58 R70
R0603_1K20A1%0	1	R0603	R26
R0603_52K3A1%0	2	603	R42 R133
R0603_3R30A1%0	1	603	R72
R0603_200KA1%0	1	603	R136
R0603_240RA1%0	2	603	R24 R25
R0603_39R0A1%0	8	R0603	R139 R140 R144 R145 R146 R147 R157 R158
R0603_422KA1%0	2	603	R137 R138
R0603_237KA1%0	4	603	R47 R74 R132 R222
R0805_1M00A1%0	3	R0805	R8 R44 R53
R0402_0R00A1%0	4	S0402AR	R46 R112 R179 R181
R0402_100RA1%0	5	402	R48 R54 R97 R100 R180
R0402_10K0A1%0	44	402	R1 R2 R3 R4 R5 R6 R9 R13 R28 R52 R60 R61 R71 R79 R80 R82 R86 R87 R88 R90 R91 R92 R93 R94 R95 R108 R109 R111 R121 R122 R123 R124 R125 R126 R127 R129 R130 R131 R153 R154 R160 R161 R224 R227
R0402_51R0A1%0	3	402	R114 R115 R117
R0402_240R0A1%0	3	402	R113 R116 R163
R0402_1K0A1%0	28	402	R7 R10 R18 R19 R20 R21 R33 R35 R36 R43 R59 R62 R67 R85 R89 R110 R118 R119 R120 R164 R165 R171 R172 R173 R174 R175 R176 R177
R0402_84R50A1%0	2	402	R73 R77
R0402_127RA1%0	2	402	R78 R83
RN0402x8_51R	3	RN0402x8	RN3 RN5 RN6
C0603_10N0A50V	2	C0603	C6 C225
C0603_100NA50V	3	C0603	C152 C174 C213
C0603_47N0A50V	1	C0603	C23
C0603_33N0A50V	2	C0603	C18 C19
C0603_15P0A50V	1	C0603	C52
C0603_2N20A50V	1	C0603	C216
C0603_10U0A6V3	44	C0603	C34 C35 C36 C37 C38 C39 C41 C42 C43 C46 C50 C56 C63 C65 C66 C68 C70 C79 C81 C82 C87 C96 C98 C102 C103 C104 C105 C111 C116 C122 C129 C138 C141 C158 C178 C179 C180 C181 C198 C210 C220 C221 C222 C228
C0603_1U00A10V	3	C0603	C1 C2 C3
C0603_1N00A100V	1	C0603	C21
C0603_24PA50V	2	603	C29 C30
C0805_1U00A10V	2	C0805	C182 C226
C0805_22U0A6V3	1	C0805	C51
C1206_1N00A2KV	4	1206	C11 C12 C13 C15
C1206_47UFA6V3	1	1206	C24
C1210_100UA6V3	1	C1210	C227

C1210_4U70A50V	3	1210	C26 C27 C28
C0402_100NA25V	117	C0402	C4 C5 C7 C8 C9 C10 C14 C16 C22 C44 C45 C47 C60 C61 C62 C67 C69 C71 C72 C73 C74 C75 C91 C92 C93 C95 C97 C99 C100 C101 C106 C107 C108 C109 C110 C112 C113 C115 C117 C118 C119 C120 C121 C123 C124 C125 C126 C128 C130 C131 C132 C133 C134 C135 C136 C139 C140 C142 C143 C144 C145 C146 C147 C148 C149 C150 C151 C153 C154 C155 C157 C160 C161 C162 C163 C164 C165 C166 C167 C168 C169 C170 C171 C173 C175 C176 C177 C183 C184 C185 C186 C187 C188 C189 C190 C191 C194 C199 C200 C201 C202 C203 C204 C206 C207 C208 C209 C211 C212 C214 C215 C219 C223 C224 C229 C239 C240
C0402_100PA50V	3	C0402	C20 C33 C172
CPAS3_30M0A3V3	1	PAS	C31
L0603_10NHA0A4	5	S0603BR	L3 L8 L9 L13 L14
LWE-TL15U0A3A6	1	WE-TPC	L7
744222	1	WE-SL2	L11
L0806_4U70A0A2	2	806	L1 L5
749020011A	1	WE-LAN	U31
L0805_220RA2A0	1	805	L10
USB_MINI_AB	3	MOLEX	P5 P6 P7
TSM-120-01-L-DV-A	1	RM2,54	P12
TSM-116-01-L-DV-A	1	RM2,54	P14
TFC-105-02-L-D-LC-K	1		P19
DF19G-30P-1H	1	DF19G-30P-1H	P2
QTH-030-01-L-D-A-K	1		P16
QSH-030-01-L-D-A-K	1	RM0,197	P10
DC-10AS	1	SMD	P1
TSM-103-01-L-DV-A	1	RM2,54	P4
Micro SDCard Buchse	1		P8
TFC-135-02-L-D-LC-P	1	RM1,27	P13
634008137521	1	WR-MJ	P9
TPA511G	1	TPA511G	P20
FSM2JSMA	2	FSM/SMD	P24 P28
DIP-SW-8-127	2		P3 P18
LP SoCrates 2.1 ML8 Durchmesser 100mm	1		
Testpoint SMD	1		P21

Schematics

If you need better quality of the Schematic, please download the Schematic and Silk Information in PCAD-2006 Format from www.devboards.de/download

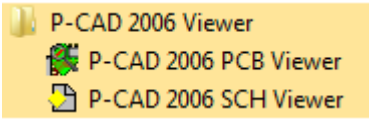
A respective Viewer can be downloaded from:

http://www.altium.com/community/downloads/legacy_p-cad.cfm

P-CAD Viewer

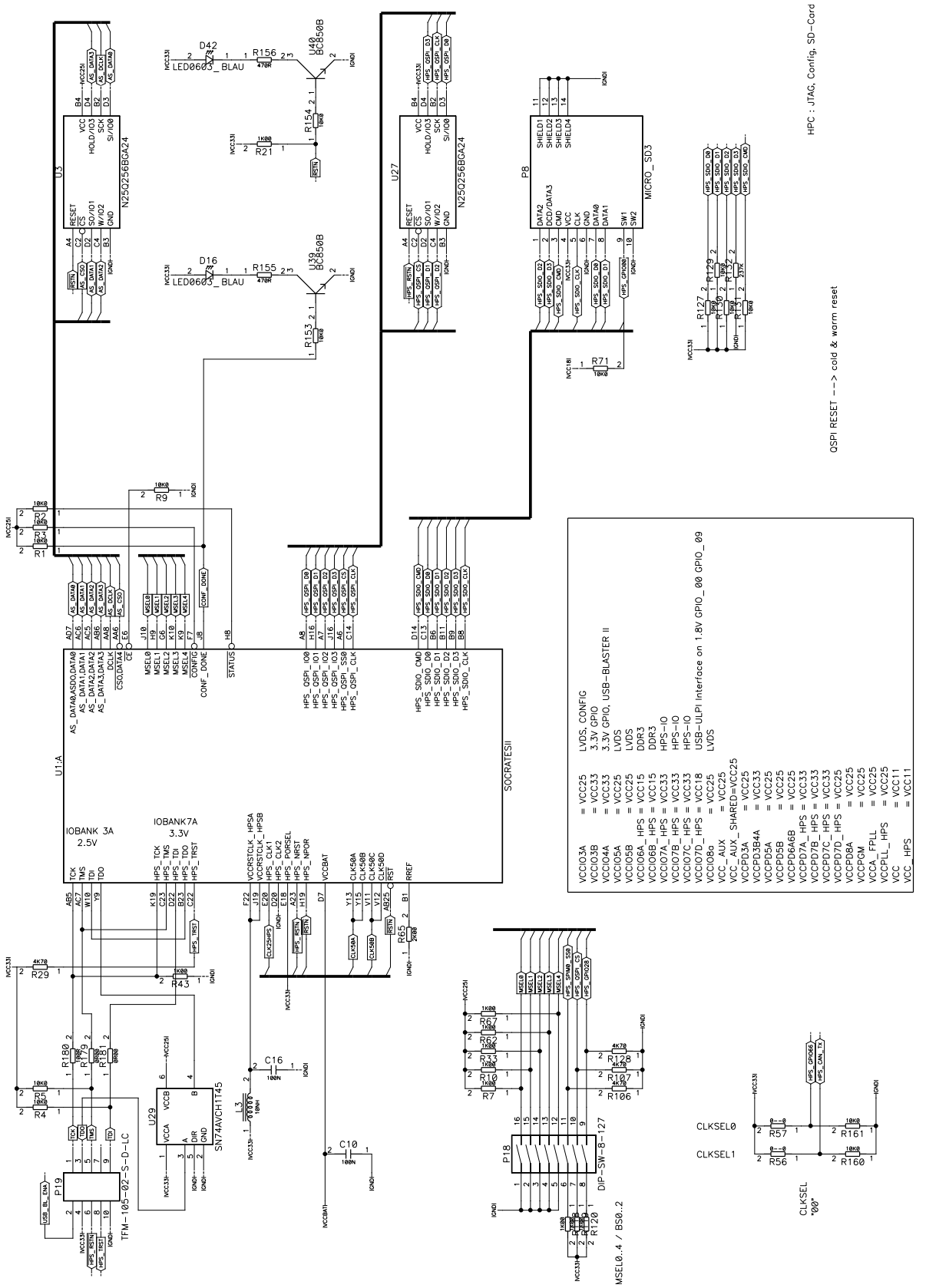
P-CAD 2006 Viewer (9,908 KB)
The P-CAD 2006 freeware* Viewer works with P-CAD 2006 (including Service Pack 1 and 2), P-CAD 2004, P-CAD 2002, P-CAD 2001 and P-CAD 2000 schematic & PCB files, as well as ACCEL EDA V15 schematic & PCB files.

After installing you can find the Schematic and Layout Viewer in your Start Menu :

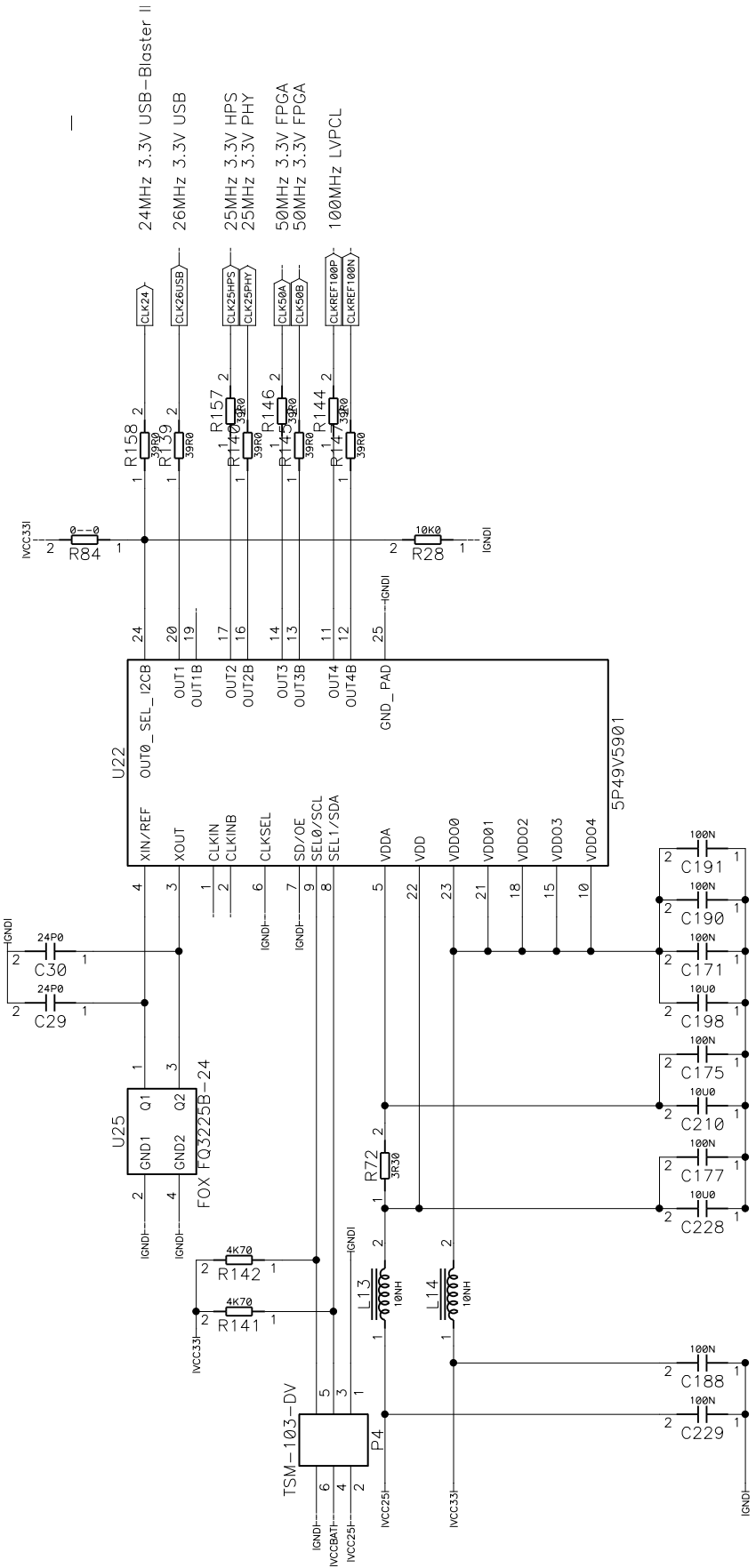


Use PCAD 2006 SCH Viewer to open the SoCrates.SCH file. PCAD 2006 PCB Viewer allows to open the Layout file SoCrates-Silk.PCB. Only the Silk information is provided. Complete Layout is available on request.

HPS, JTAG, Config, SDCard



Clocking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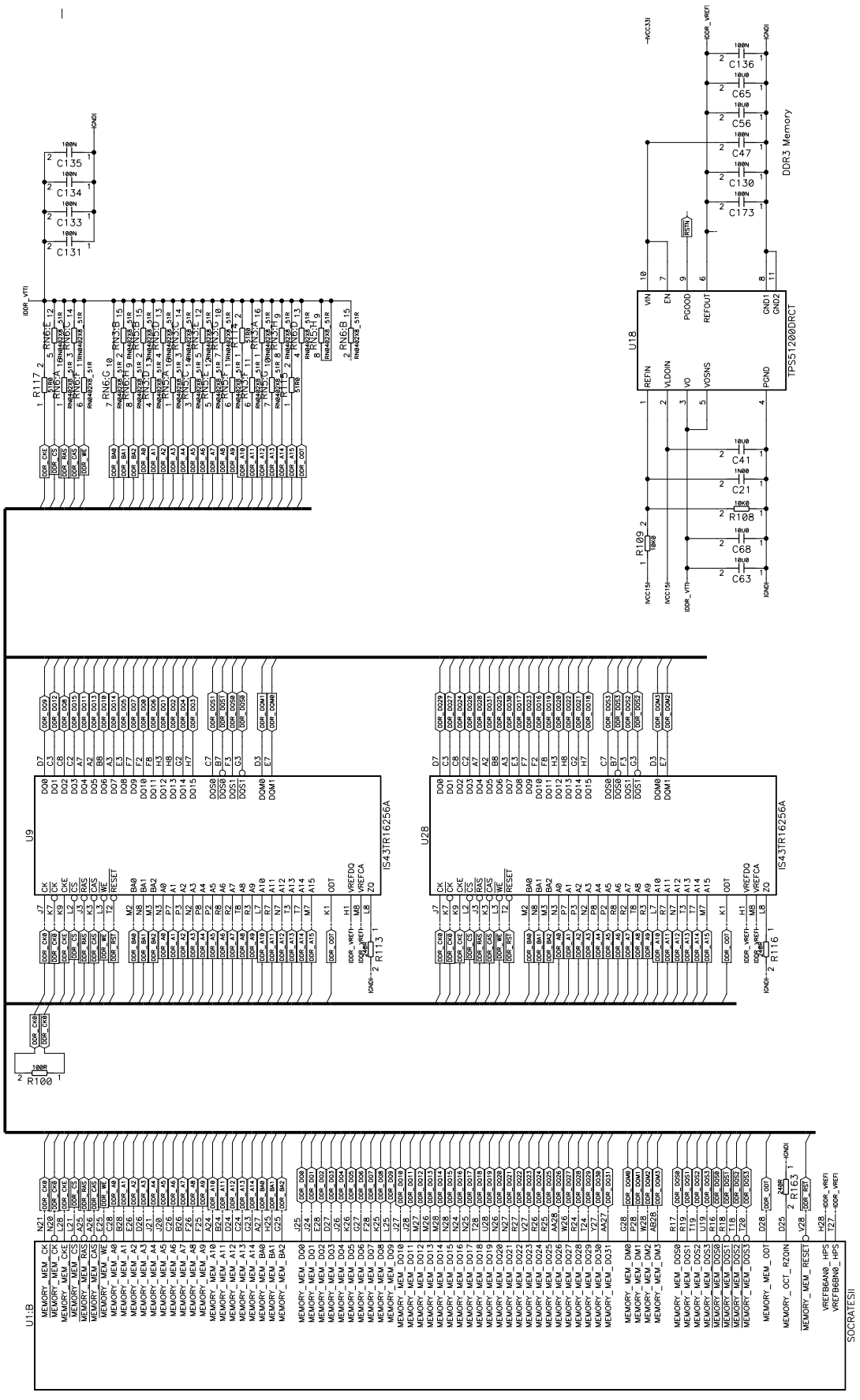
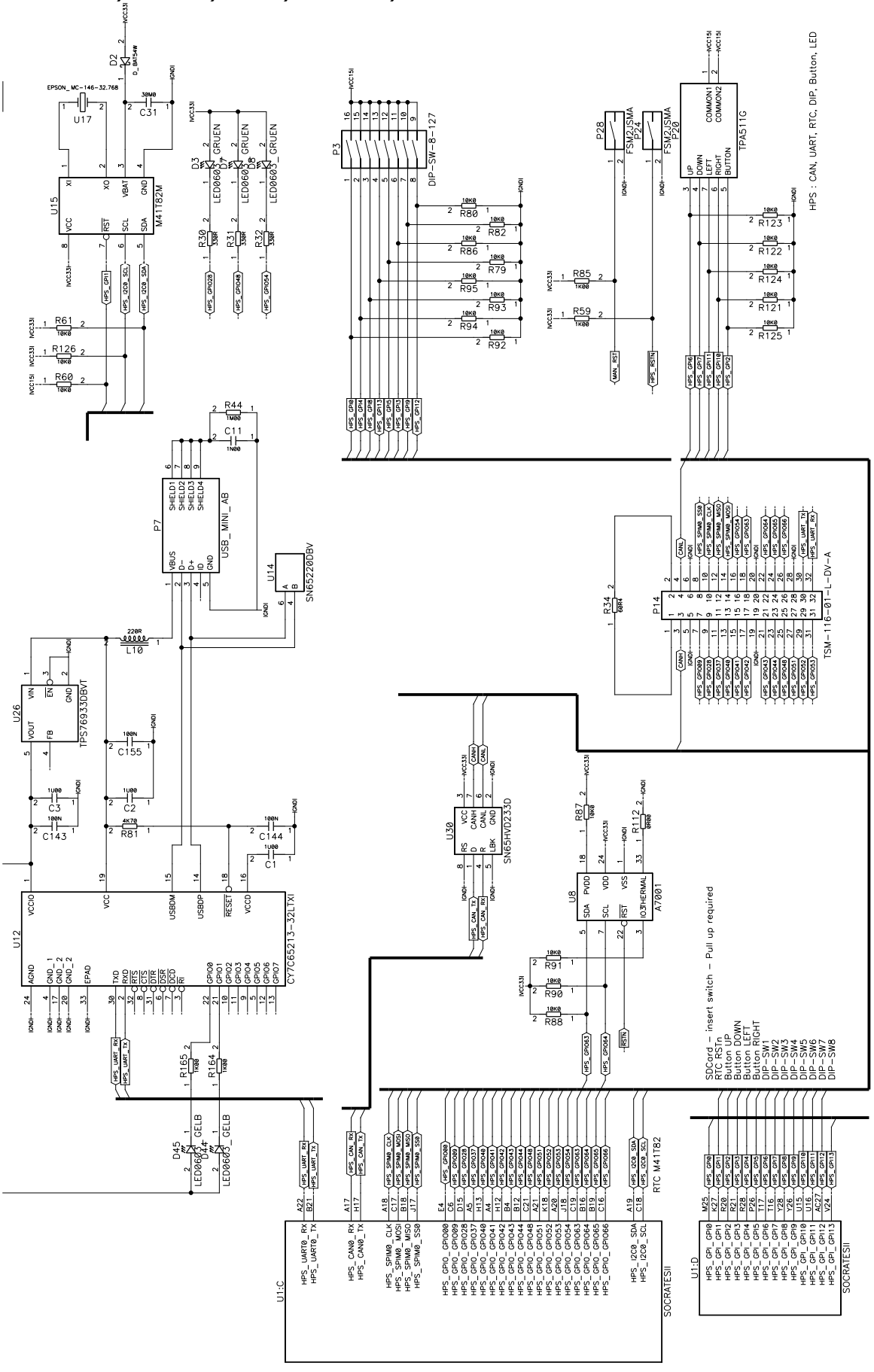
26MHz 3.3V USB
25MHz 3.3V HPS
25MHz 3.3V PHY
50MHz 3.3V FPGA
50MHz 3.3V FPGA
100MHz LVPCL
CLK24
CLK26USB
CLK25HPS
CLK25PHY
CLK50A
CLK50B
CLKREF100P
CLKREF100N
R158
R139
R157
R140
R146
R145
R144
R147
39R0
R84
0R
10K0
R28
IVCC33I
IGNDI
U22
5P49V5901
OUT0_SEL_I2CB
OUT1
OUT1B
OUT2
OUT2B
OUT3
OUT3B
OUT4
OUT4B
GND_PAD
XIN/REF
XOUT
CLKIN
CLKINB
CLKSEL
SD/OE
SEL0/SCL
SEL1/SDA
VDDA
VDD
VDDO0
VDDO1
VDDO2
VDDO3
VDDO4
C30
C29
24P0
C191
C190
C171
C198
C175
C210
C177
C228
C188
C229
100N
10U0
U25
FOX FQ3225B-24
GND1
GND2
Q1
Q2
R72
3R30
R142
R141
4K70
L13
L14
10NH
IVCC33I
TSM-103-DV
P4
IVCC25I
IVCCBATI

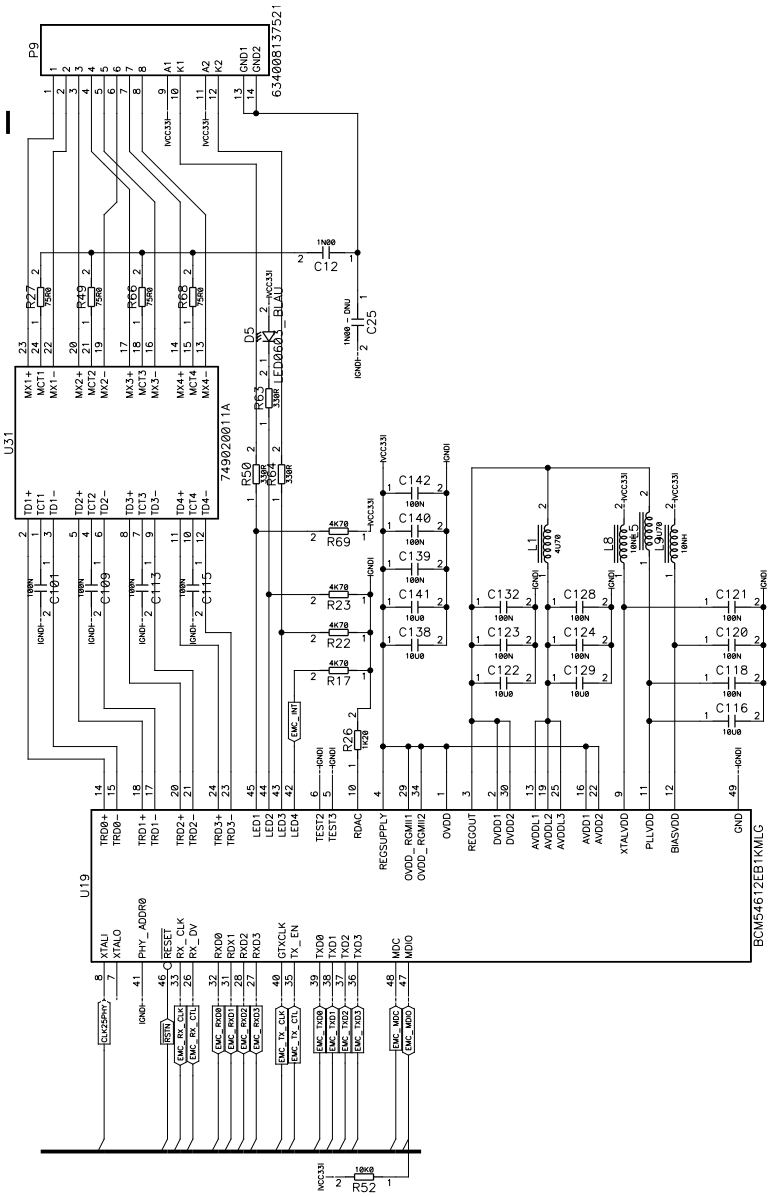
HPS: DDR3 Memory

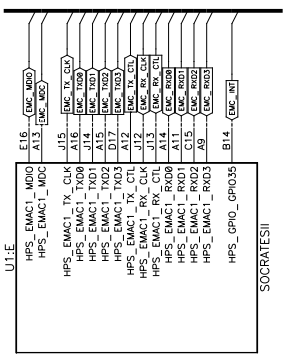


HPS: CAN, UART, RTC, Button, LEDs

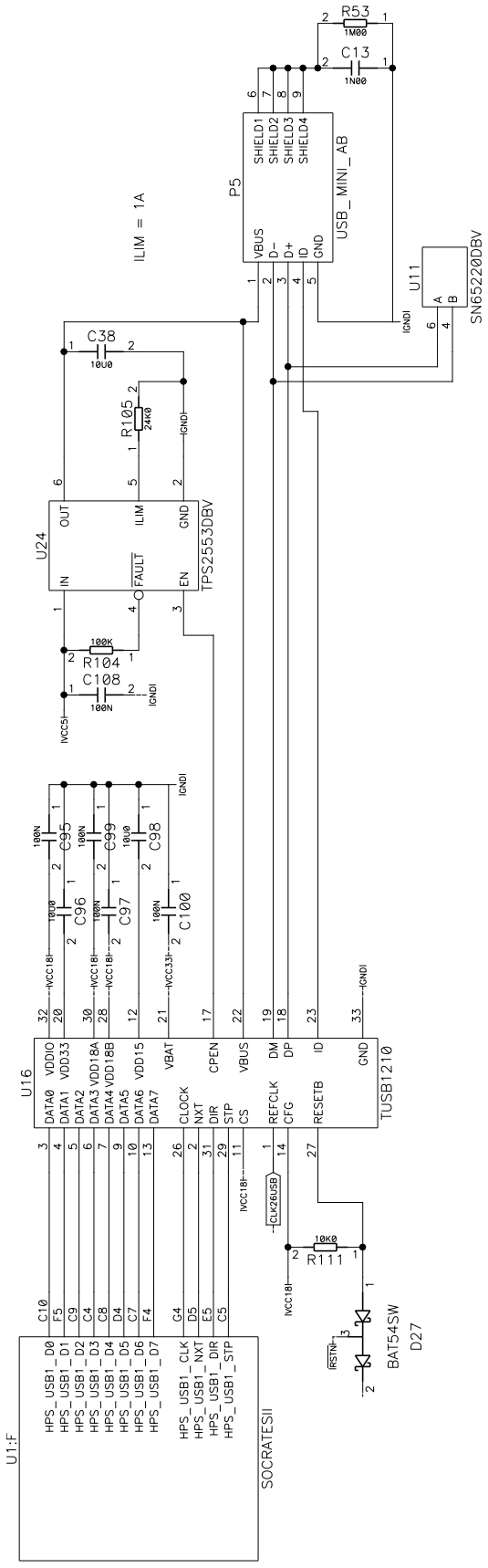


HPS: Gigabit Ethernet Phy

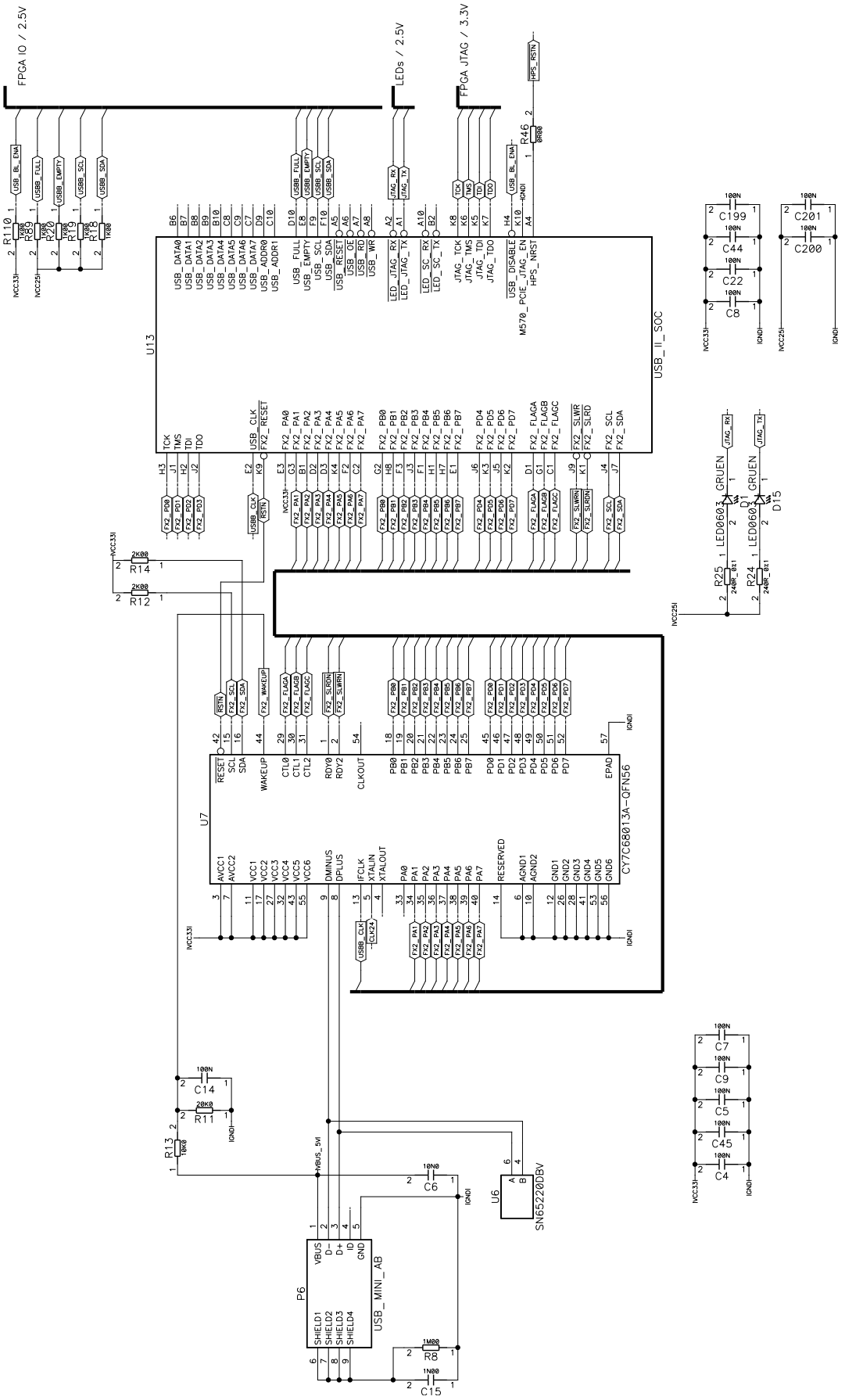




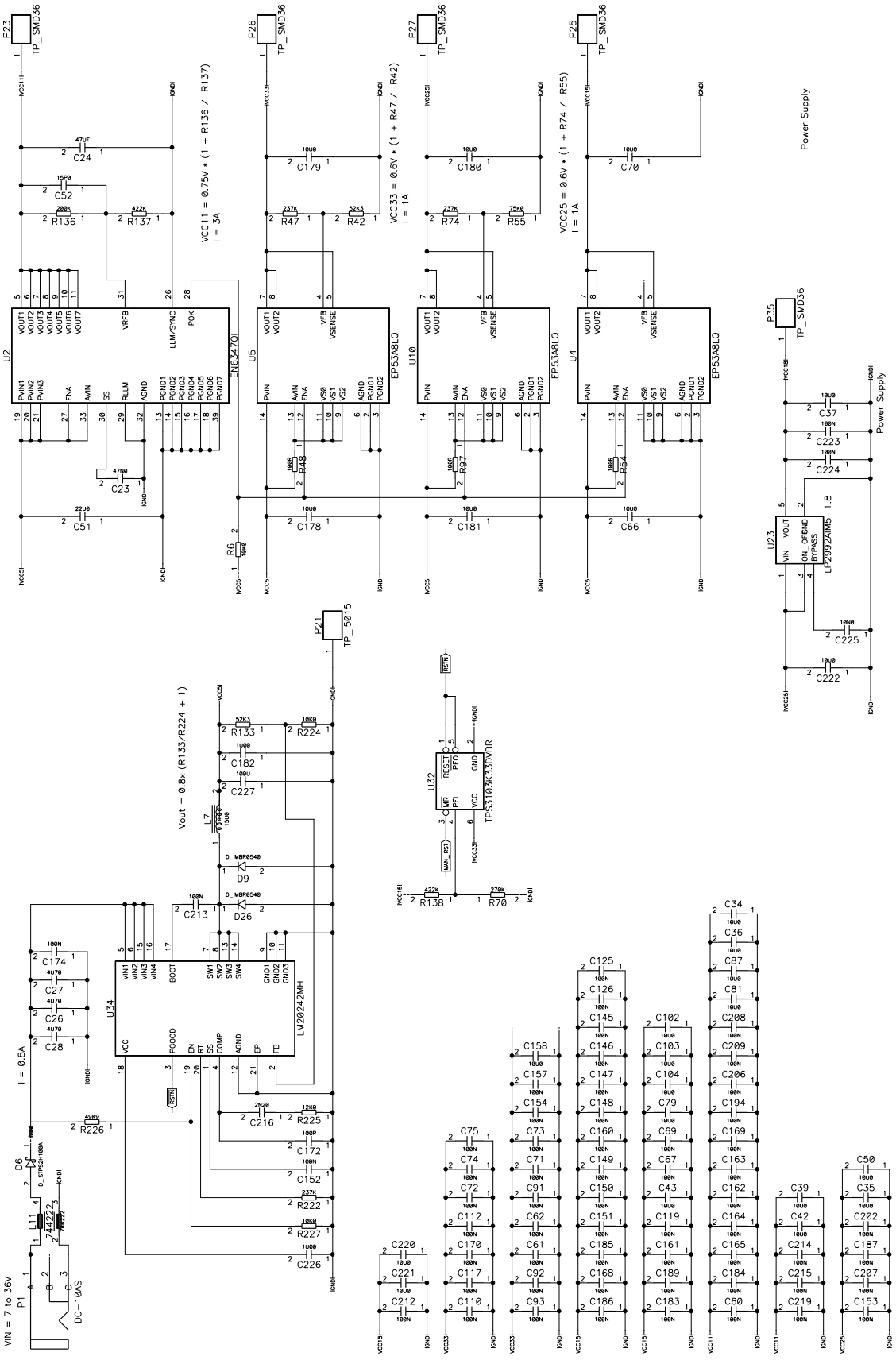
HPS: USB


R53
1M00
C13
1N00
P5
USB_MINI_AB
SHIELD1
SHIELD2
SHIELD3
SHIELD4
VBUS
D-
D+
ID
GND
ILIM = 1A
U11
SN65220DBV
C38
10U0
R105
24K0
U24
TPS2553DBV
OUT
ILIM
GND
IN
FAULT
EN
R104
100K
C108
100N
U16
TUSB1210
C95
C96
C99
C97
C98
C100
U1:F
SOCRATESII
CLK26USB
R111
10K0
BAT54SW
D27

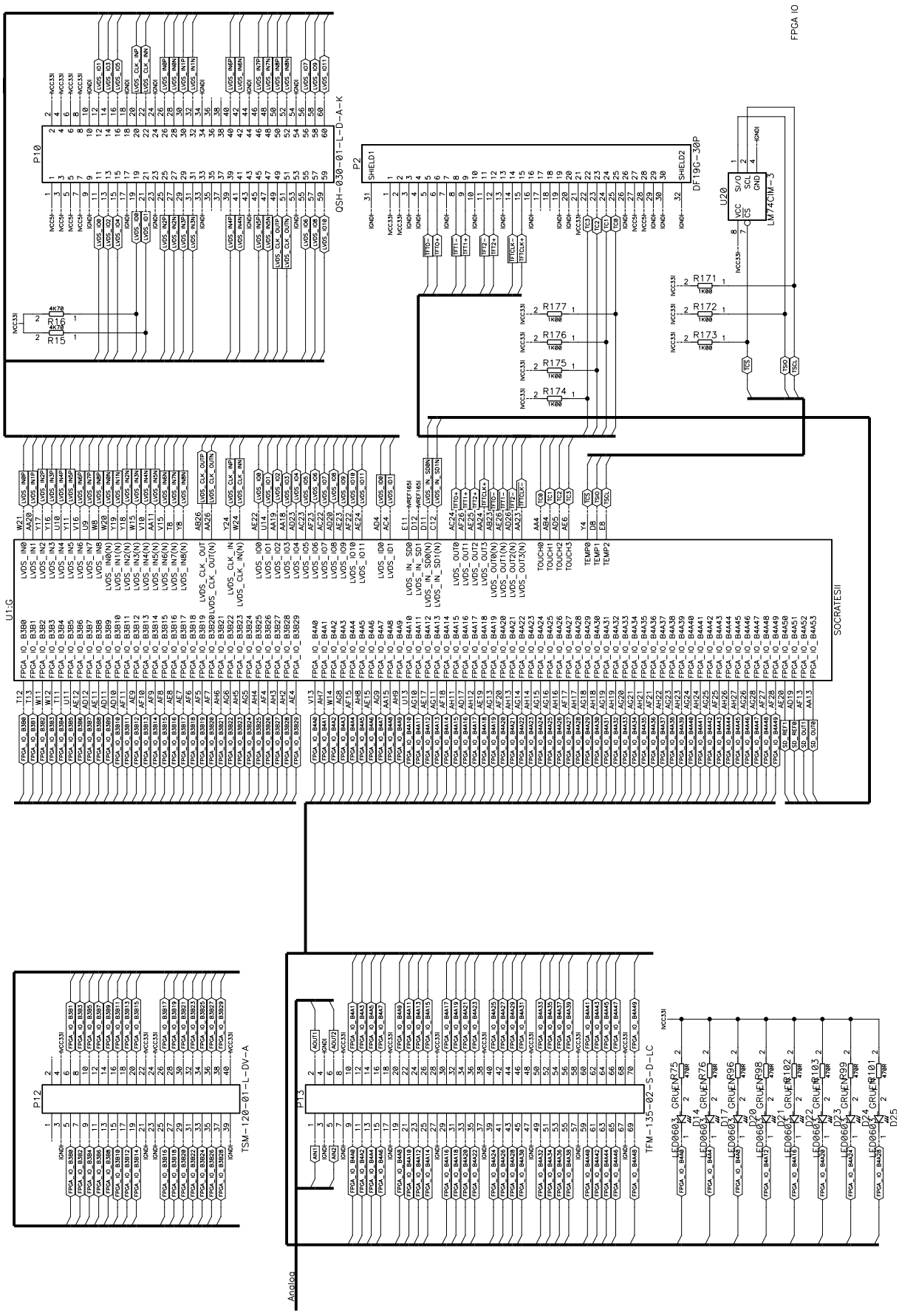
Embedded USB-Blaster II



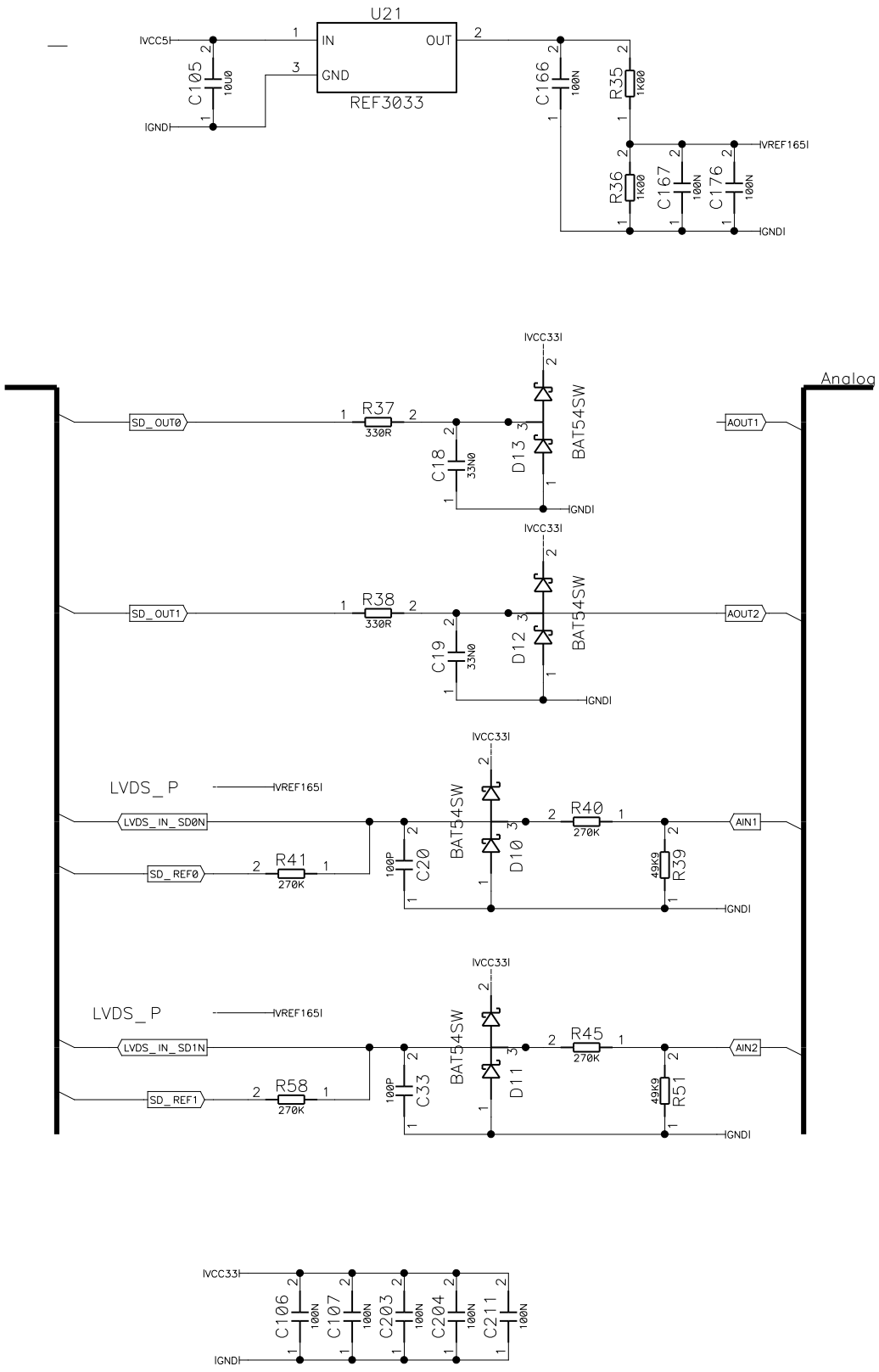
Power Supply



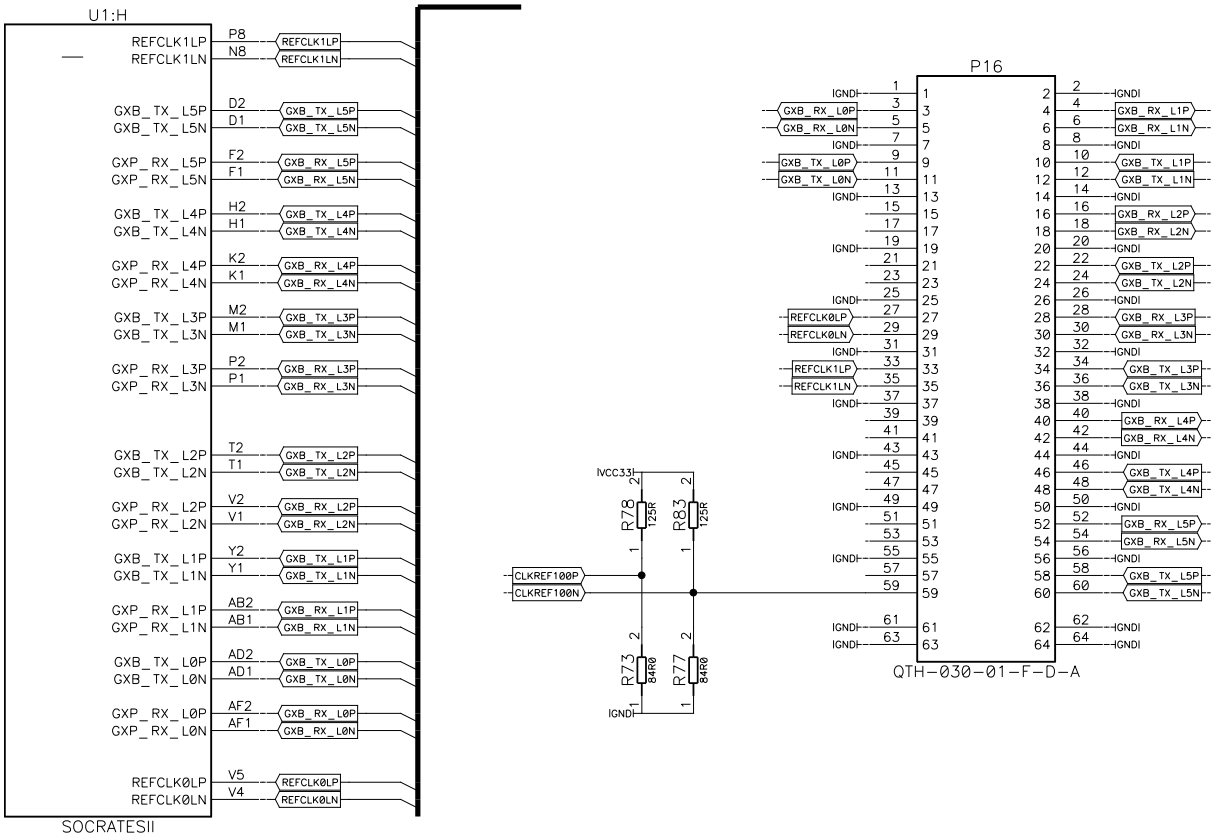
FPGA IO


FPGA IO
P10
QSH-030-01-L-D-A-K
P2
DF19G-30P
U20
LM74CIM-3
R171
R172
R173
R174
R175
R176
R177
U1:G
SOCRATESII
P12
TSM-120-01-L-DV-A
P13
TFM-135-02-S-D-LC
Analog

ΣΔ-ADC / DAC Subsystem



Transceiver



Hidden Supply Pins

Power Table								
Ref Des	Device(Type)	Package	GND	VCC33	VCC18	VCC11	VCC15	VCC25
U1	SOCRATESII	BGA0672C	AH20,AH10,AG27,AG17, AG7,AG3,AG2,AG1,AF24, AF16,AF12,AF3,AE18, AE16,AE5,AE3,AE2,AE1, AD25,AD22,AD14,AD8, AD6,AD3,AC26,AC3,AC2, AC1,AB27,AB24,AB3, AA25,AA17,AA9,AA3, AA2,AA1,Y25,Y20,Y14, Y12,Y3,W18,W16,W4,W3, W2,W1,V26,V21,V14,V9, V8,V3,U27,U24,U20, U17,U12,U5,U3,U2,U1, T14,T10,T3,R15,R13, R11,R8,R3,R2,R1,P25, P20,P18,P16,P12,P10, P9,P5,P3,N19,N17,N15, N13,N4,N3,N2,N1,M20, M16,M14,M11,M10,M8, M3,L27,L24,L19,L17, L15,L13,L10,L9,L8,L5, L3,L2,L1,K20,K16,K14, K12,K11,K8,K4,K3,J9, J5,J3,J2,J1,H27,H24, H20,H18,H15,H11,H6, H5,H4,H3,G3,G2,G1, F23,F6,F3,E27,E24, E23,E22,E19,E9,E3,E2, E1,D21,D19,D16,D13, D10,D9,D3,C11,C3,C2, C1,B27,B25,B22,B20, B17,B15,B7,B5,B3,A10, A3	AH25,AH15,AG22,AG12, AG4,AF19,AF14,AE21, AE13,AE10,AD21,AD18, AD16,AD13,AD9,AA16, AA14,AA12,W13,H14, E21,E17,E14,D18,C20, B13,B10	G5,D6	U26,U21,T15,T9,T5,T4, R14,R12,R10,R9,R5, P19,P17,P15,P14,P13, P11,N18,N16,N14,N12, N11,N10,N9,N5,M19, M18,M17,M15,M13,M12, M9,M5,L18,L16,L14, L12,L11,L4,K17,K15, K13,J11	AD27,W27,U18,T25,T21, P27,M21,L26,H26,H21, G24,F27,C27,C25	AD24,AD15,AC25,AC21, AC8,AA21,AA10,AA5, Y21,Y10,W25,W19,W17, W9,W5,U4,R4,P24,P21, P4,M24,M4,K24,K21,K5, J4,H23,H10,F21,F8, E15,E13,E10,E7
U6	SN65220DBV	SOT23-6	5,2					
U9	IS43TR16256A	BGA0096A	T9,T1,P9,P1,M9,M1,J8, J2,G9,G8,G1,F9,E8,E2, E1,D8,D1,B9,B3,B1,A9				R9,R1,N9,N1,K8,K2,H9, H2,G7,F1,E9,D9,D2,C9, C1,B2,A8,A1	
U11	SN65220DBV	SOT23-6	5,2					
U13	USB_II_SOC	BGA0100A	H5,G7,G5,F6,F5,E6,E5, D7,D5,C5	H6,G6,G4,F4,E7,E4,C6				F7,D6,D4
U14	SN65220DBV	SOT23-6	5,2					
U28	IS43TR16256A	BGA0096A	T9,T1,P9,P1,M9,M1,J8, J2,G9,G8,G1,F9,E8,E2, E1,D8,D1,B9,B3,B1,A9				R9,R1,N9,N1,K8,K2,H9, H2,G7,F1,E9,D9,D2,C9, C1,B2,A8,A1	

Board Top View

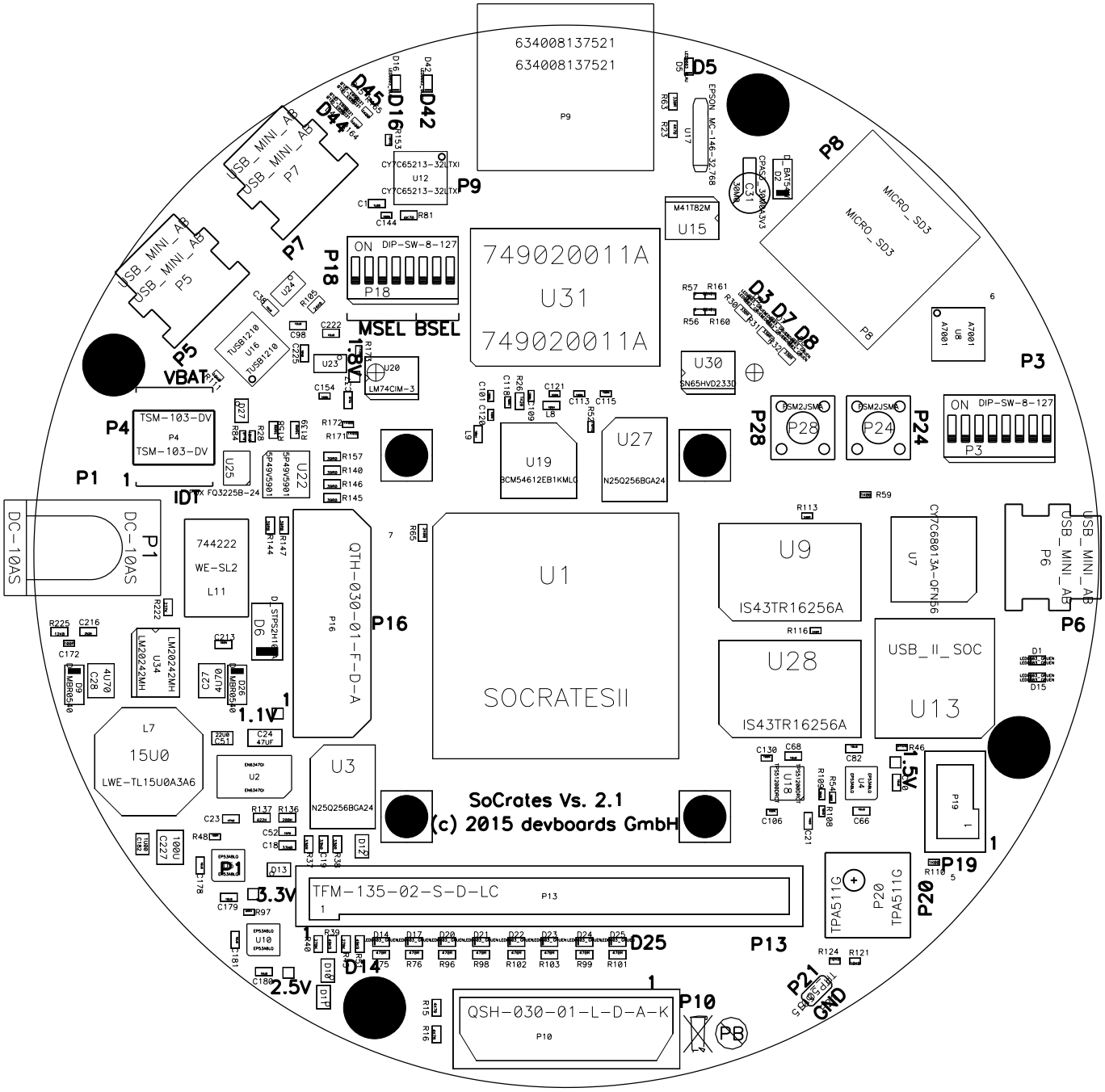


Figure 6

Board Bottom View

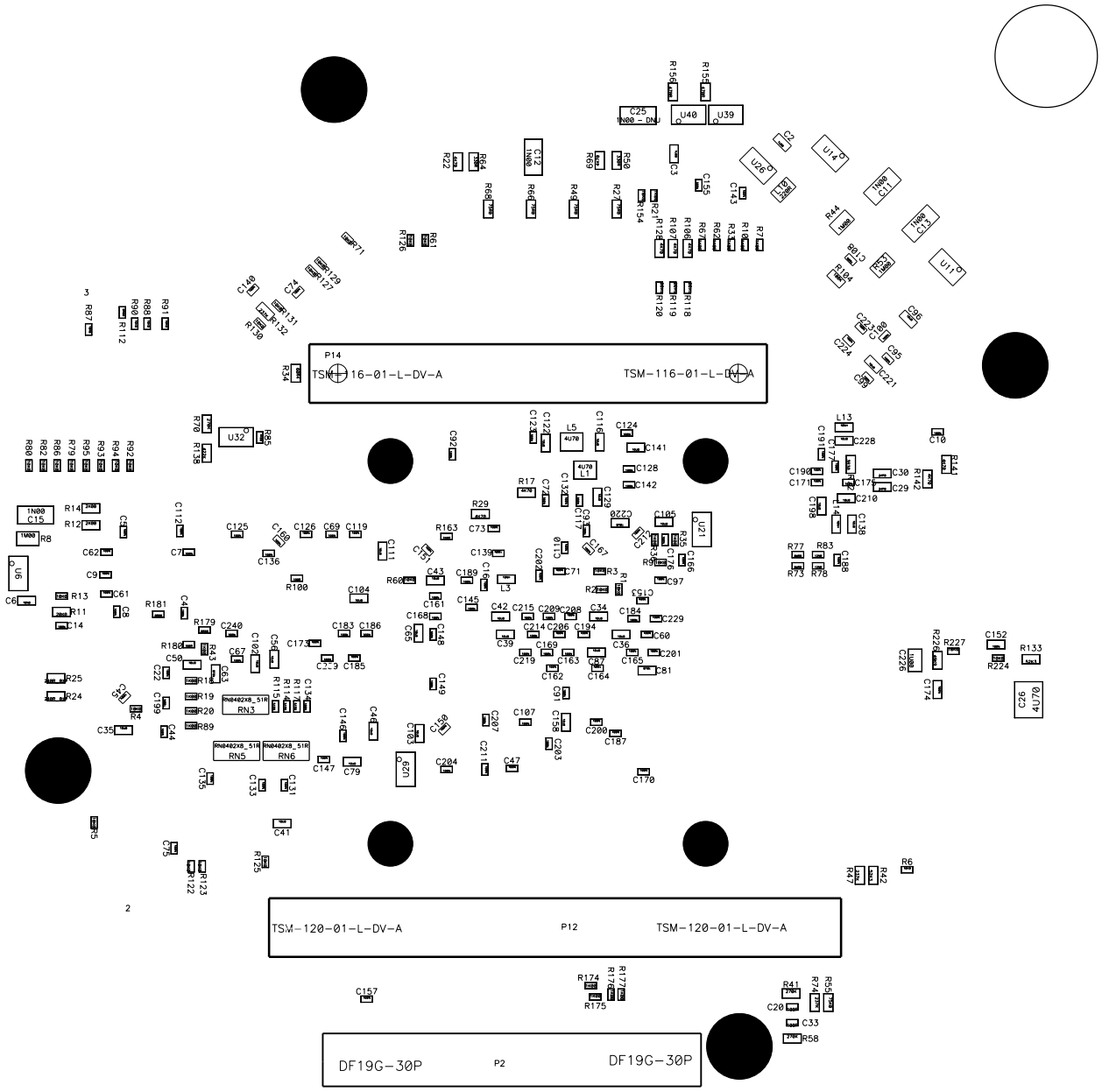


Figure 7